

# 74LVC132APW-Q100J Datasheet

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DiGi Electronics Part Number	74LVC132APW-Q100J-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	74LVC132APW-Q100J
Description	IC GATE NAND 4CH 2-INP 14TSSOP
Detailed Description	NAND Gate IC 4 Channel Schmitt Trigger 14-TSSOP



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## Purchase and inquiry

Manufacturer Product Number:

74LVC132APW-Q100J

Series:

74LVC

Logic Type:

NAND Gate

Number of Inputs:

2

Voltage - Supply:

1.2V ~ 3.6V

Current - Output High, Low:

24mA, 24mA

Input Logic Level - High:

1V ~ 2V

Operating Temperature:

-40°C ~ 125°C

Qualification:

AEC-Q100

Supplier Device Package:

14-TSSOP

Base Product Number:

74LVC132

Manufacturer:

Nexperia USA Inc.

Product Status:

Active

Number of Circuits:

4

Features:

Schmitt Trigger

Current - Quiescent (Max):

40 µA

Input Logic Level - Low:

0.12V ~ 0.8V

Max Propagation Delay @ V, Max CL:

6.4ns @ 3.3V, 50pF

Grade:

Automotive

Mounting Type:

Surface Mount

Package / Case:

14-TSSOP (0.173", 4.40mm Width)

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

# 74LVC132A-Q100

## Quad 2-input NAND Schmitt trigger

Rev. 4 — 12 February 2024

Product data sheet

### 1. General description

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The 74LVC132A-Q100 provides four 2-input NAND gates with Schmitt trigger inputs. It can transform slowly changing input signals into sharply defined, jitter-free output signals.

The inputs switch at different points for positive and negative-going signals. The difference between the positive voltage  $V_{T+}$  and the negative voltage  $V_{T-}$  is defined as the input hysteresis voltage  $V_H$ .

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environment.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

### 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.2 V to 3.6 V
- 5 V tolerant inputs for interfacing with 5 V logic
- CMOS low-power consumption
- Direct interface with TTL levels
- Unlimited input rise and fall times
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

### 3. Applications

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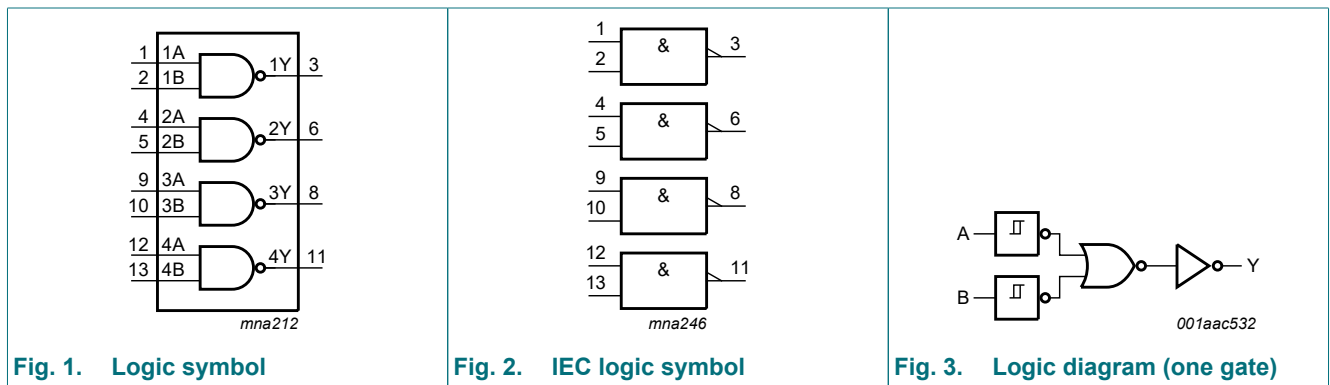
- Wave and pulse shapers for highly noisy environments
- Astable multivibrator
- Monostable multivibrator.

## 4. Ordering information

Table 1. Ordering information

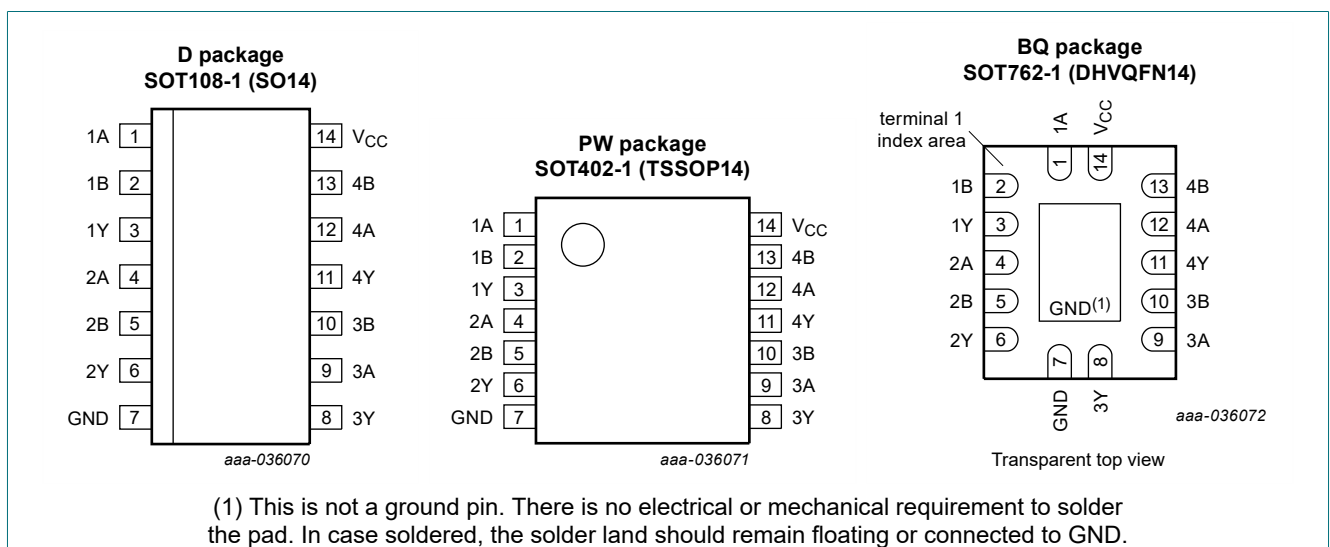
Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74LVC132AD-Q100</a>	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<a href="#">SOT108-1</a>
<a href="#">74LVC132APW-Q100</a>	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<a href="#">SOT402-1</a>
<a href="#">74LVC132ABQ-Q100</a>	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	<a href="#">SOT762-1</a>

## 5. Functional diagram



## 6. Pinning information

### 6.1. Pinning



## 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
V <sub>I</sub>	input voltage		[1] -0.5	+6.5	V
V <sub>O</sub>	output voltage		[2] -0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT108-1 (SO14) package: P<sub>tot</sub> derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P<sub>tot</sub> derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P<sub>tot</sub> derates linearly with 9.6 mW/K above 98 °C.

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C

## 10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	V <sub>CC</sub> - 0.45	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.6	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	4.0	-	pF

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.3	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	V <sub>CC</sub> - 0.6	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.75	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	-	5	mA

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see Fig. 4 [2]						
		V <sub>CC</sub> = 1.2 V	-	18.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	7.2	12.8	2.0	16.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	4.0	7.6	1.5	9.6	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.8	7.6	1.5	9.6	ns
t <sub>sk(o)</sub>	output skew time		-	-	1.0	-	1.5	ns
		[3]						
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub> [4]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	10.5	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	10.8	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	11.4	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW). P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz;

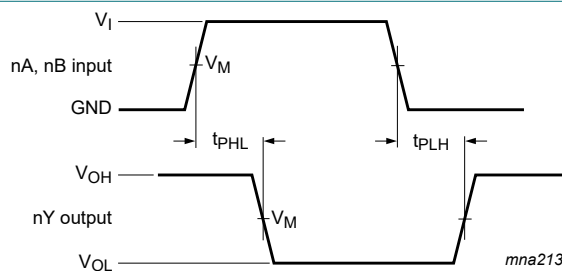
N = number of inputs switching;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

## 11.1. Waveforms and test circuit

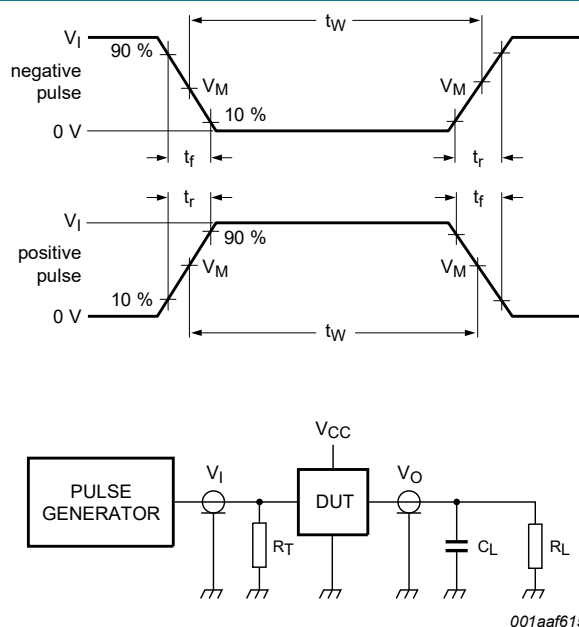


$V_M = 1.5 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ .

$V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$ .

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 4. The input (nA, nB) to output (nY) propagation delays



Test data is given in [Table 8](#). Definitions for test circuit:

$R_L$  = Load resistance

$C_L$  = Load capacitance including jig and probe capacitance

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig. 5. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load	
	$V_I$	$t_r, t_f$	$C_L$	$R_L$
1.2 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	1 k $\Omega$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	1 k $\Omega$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	500 $\Omega$
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$



## 12. Transfer characteristics

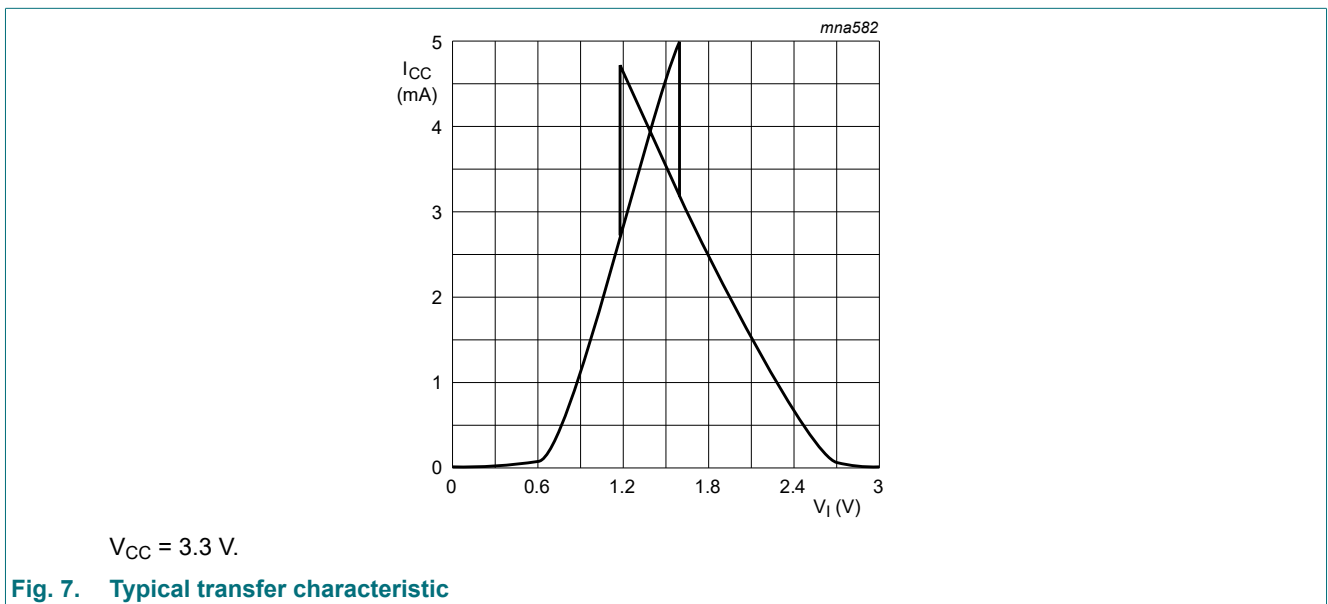
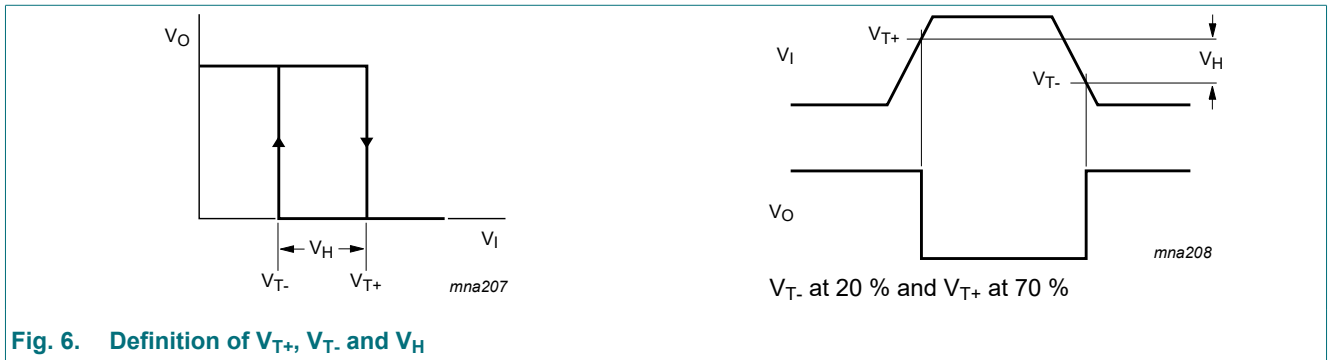
**Table 9. Transfer characteristics**

Voltages are referenced to GND (ground = 0 V); see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>T+</sub>	positive-going threshold voltage	V <sub>CC</sub> = 1.2 V	0.2	1.0	0.2	1.0	V
		V <sub>CC</sub> = 1.65 V	0.4	1.3	0.4	1.3	V
		V <sub>CC</sub> = 1.95 V	0.6	1.5	0.6	1.5	V
		V <sub>CC</sub> = 2.3 V	0.8	1.7	0.8	1.7	V
		V <sub>CC</sub> = 2.5 V	0.9	1.7	0.9	1.7	V
		V <sub>CC</sub> = 2.7 V	1.1	2	1.1	2	V
		V <sub>CC</sub> = 3 V	1.2	2	1.2	2	V
		V <sub>CC</sub> = 3.6 V	1.2	2	1.2	2	V
V <sub>T-</sub>	negative-going threshold voltage	V <sub>CC</sub> = 1.2 V	0.12	0.75	0.12	0.75	V
		V <sub>CC</sub> = 1.65 V	0.15	0.85	0.15	0.85	V
		V <sub>CC</sub> = 1.95 V	0.25	0.95	0.25	0.95	V
		V <sub>CC</sub> = 2.3 V	0.4	1.1	0.4	1.1	V
		V <sub>CC</sub> = 2.5 V	0.4	1.2	0.4	1.2	V
		V <sub>CC</sub> = 2.7 V	0.8	1.4	0.8	1.4	V
		V <sub>CC</sub> = 3 V	0.8	1.5	0.8	1.5	V
		V <sub>CC</sub> = 3.6 V	0.8	1.5	0.8	1.5	V
V <sub>H</sub>	hysteresis voltage (V <sub>T+</sub> - V <sub>T-</sub> )	V <sub>CC</sub> = 1.2 V	0.1	1.0	0.1	1.0	V
		V <sub>CC</sub> = 1.65 V	0.2	1.15	0.2	1.15	V
		V <sub>CC</sub> = 1.95 V	0.2	1.25	0.2	1.25	V
		V <sub>CC</sub> = 2.3 V	0.3	1.3	0.3	1.3	V
		V <sub>CC</sub> = 2.5 V	0.3	1.3	0.3	1.3	V
		V <sub>CC</sub> = 2.7 V	0.3	1.1	0.3	1.1	V
		V <sub>CC</sub> = 3 V	0.3	1.2	0.3	1.2	V
		V <sub>CC</sub> = 3.6 V	[1]	0.3	1.2	0.3	1.2

[1] Typical transfer characteristic is displayed in Fig. 7.

## 12.1. Waveforms transfer characteristics



## 13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

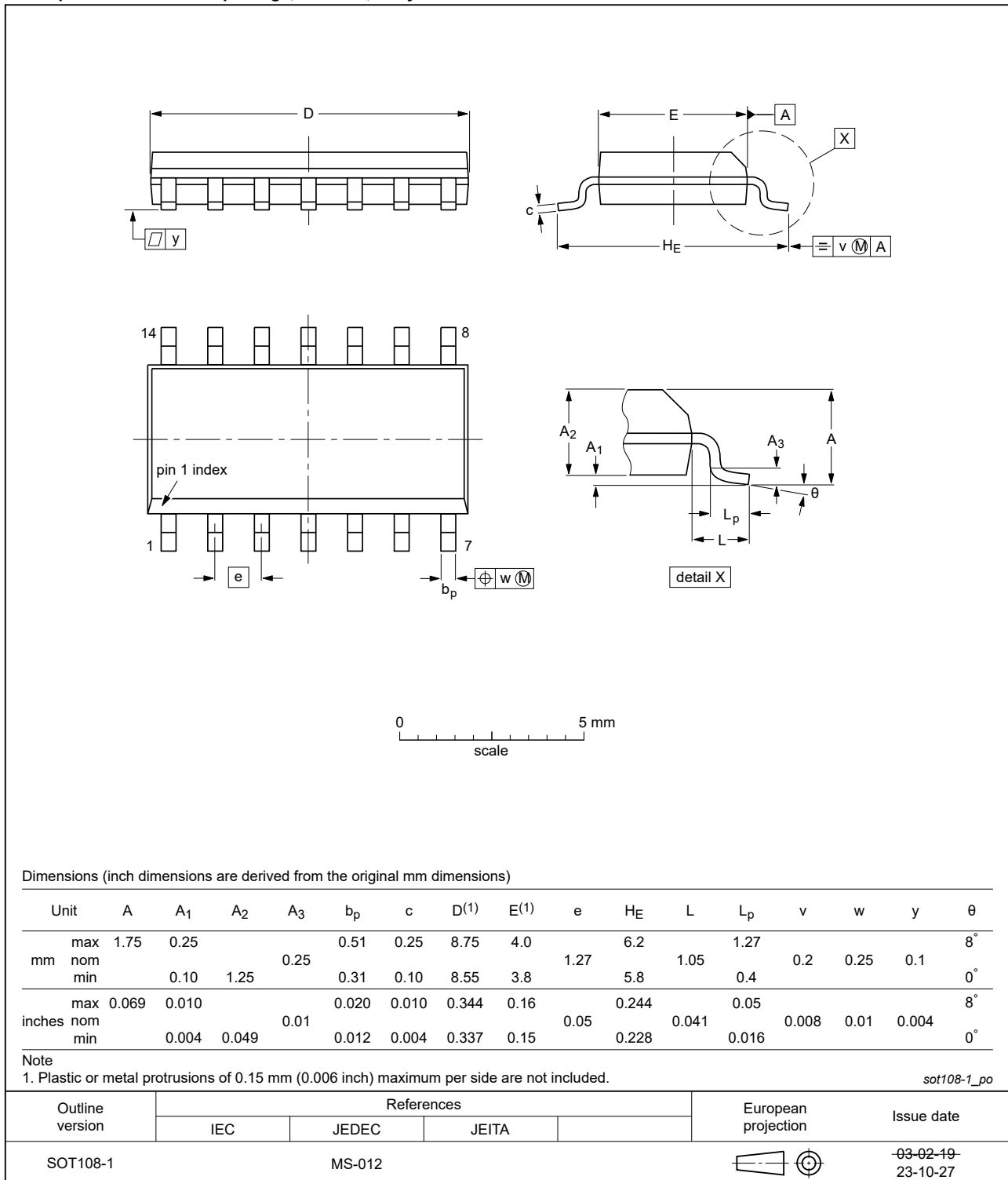


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

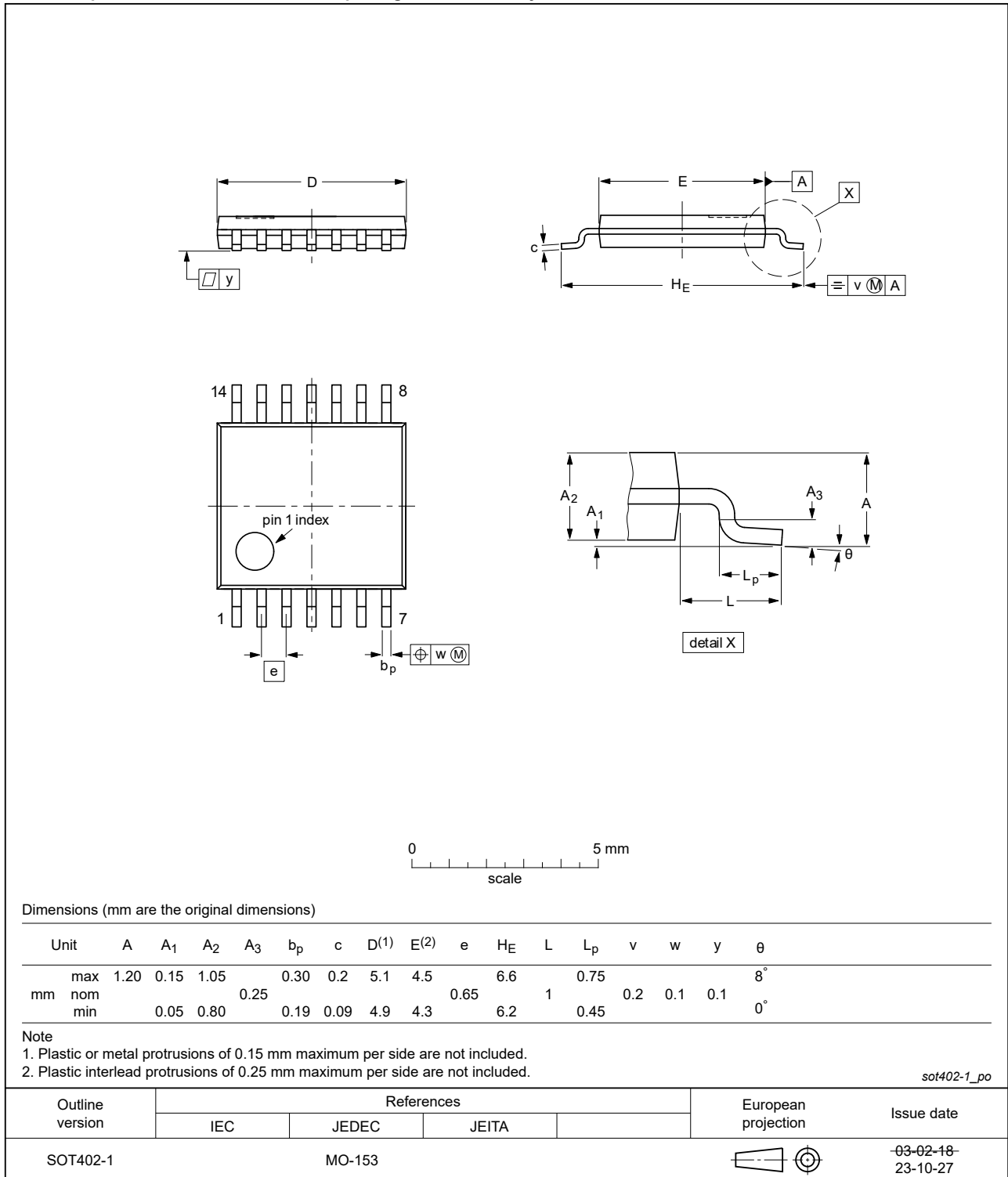


Fig. 9. Package outline SOT402-1 (TSSOP14)



## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC132A_Q100 v.4	20240212	Product data sheet	-	74LVC132A_Q100 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Fig. 8</a>, <a href="#">Fig. 9</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> </ul>			
74LVC132A_Q100 v.3	20230803	Product data sheet	-	74LVC132A_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74LVC132A_Q100 v.2	20200706	Product data sheet	-	74LVC132A_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Fig. 10</a>: Package outline drawing SOT762-1 (DHVQFN14) updated.</li> </ul>			
74LVC132A_Q100 v.1	20130404	Product data sheet	-	-

## 16. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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