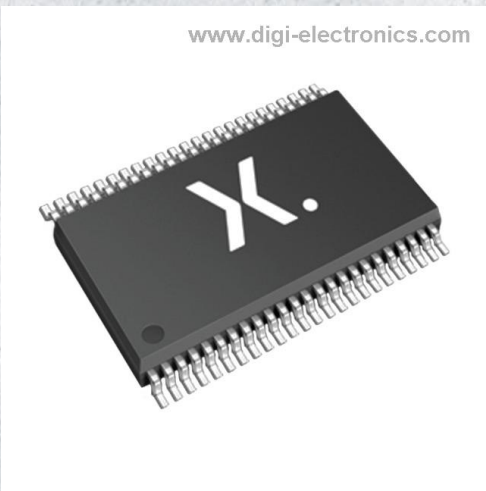
# 74LVC16241ADGG,112 Datasheet




https://www.DiGi-Electronics.com

| | |
|---|---|
| DiGi Electronics Part Number | 74LVC16241ADGG,112-DG |
| Manufacturer | Nexperia USA Inc. |
| Manufacturer Product Number | 74LVC16241ADGG,112 |
| Description | IC BUF NON-INVERT 3.6V 48TSSOP |
| Detailed Description | Buffer, Non-Inverting 4 Element 4 Bit per Element 3 -State Output 48-TSSOP |

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| 74LVC16241ADGG,112 | Nexperia USA Inc. |
| Series: | Product Status: |
| 74LVC | Obsolete |
| Logic Type: | Number of Elements: |
| Buffer, Non-Inverting | 4 |
| Number of Bits per Element: | Input Type: |
| 4 | - |
| Output Type: | Current - Output High, Low: |
| 3-State | 24mA, 24mA |
| Voltage - Supply: | Operating Temperature: |
| 1.2V ~ 3.6V | -40°C ~ 125°C (TA) |
| Mounting Type: | Package / Case: |
| Surface Mount | 48-TFSOP (0.240", 6.10mm Width) |
| Supplier Device Package: | Base Product Number: |
| 48-TSSOP | 74LVC16241 |

## Environmental & Export classification

| RoHS Status: | Moisture Sensitivity Level (MSL): |
| --- | --- |
| ROHS3 Compliant | 1 (Unlimited) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8542.39.0001 | |


# 74LVC16241A

## 16-bit buffer/line driver with 5 V tolerant inputs/outputs; 3-state

Rev. 7 — 22 April 2024 Product data sheet

## 1. General description

The 74LVC16241A is a 16-bit non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs (1$\overline{OE}$, 2OE, 3OE and 4$\overline{OE}$). Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

## 2. Features and benefits

- 5 V tolerant inputs and outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance outputs when $V_{CC}$ = 0 V
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC16241ADGG | -40 °C to +125 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |

## 4. Functional diagram

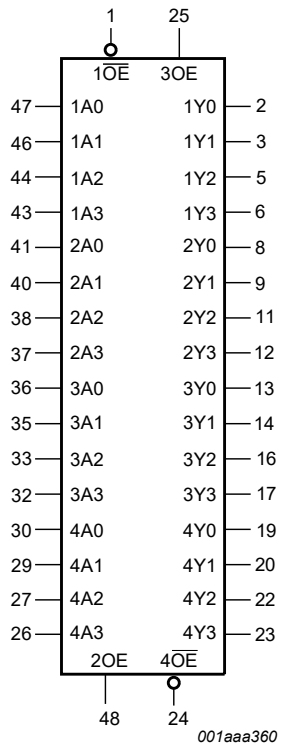



Fig. 1. Logic symbol

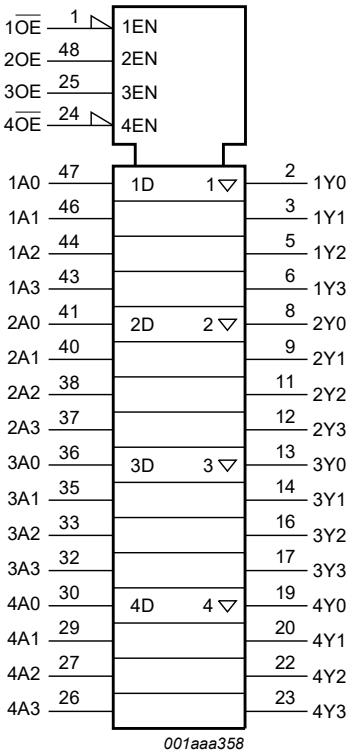



Fig. 2. IEC logic symbol

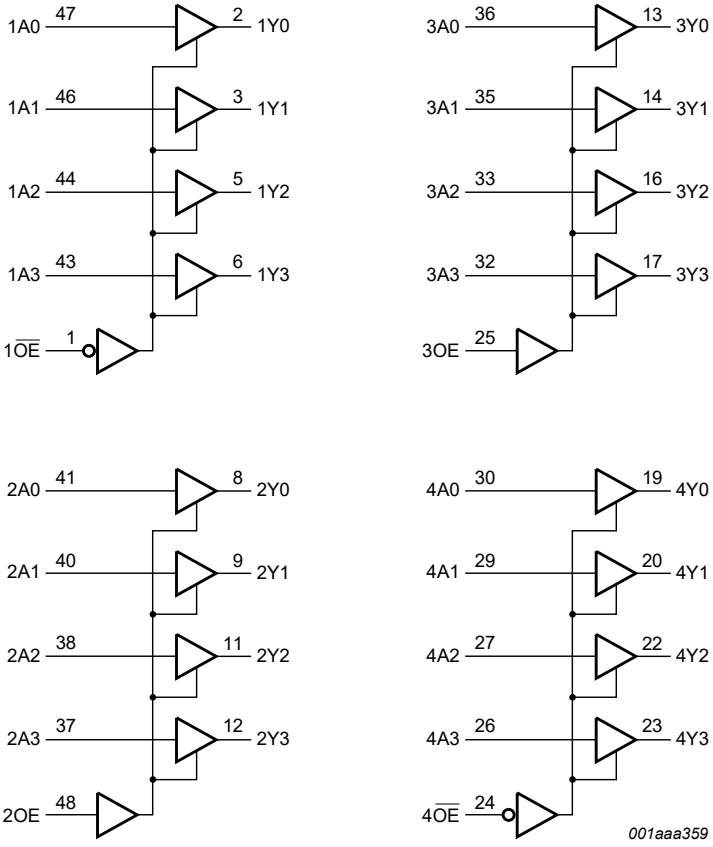
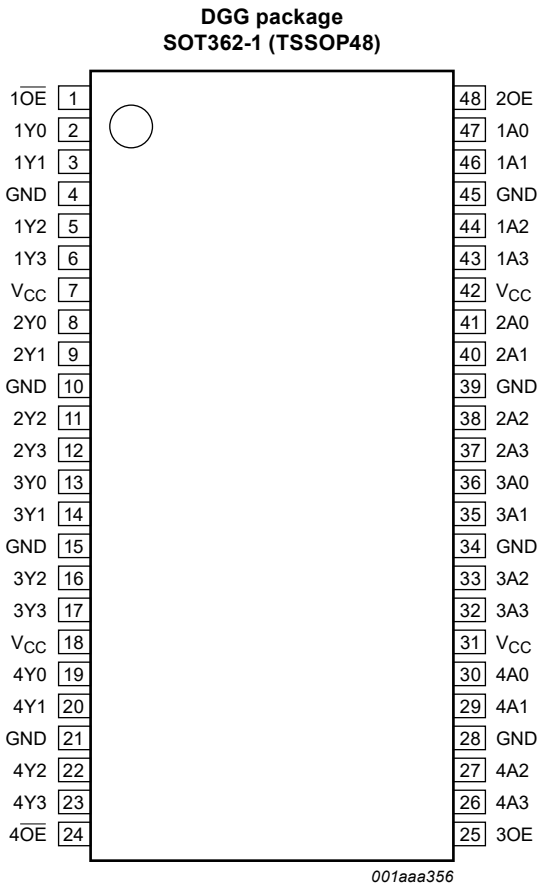



Fig. 3. Logic diagram

# 5. Pinning information

## 5.1. Pinning




## 5.2. Pin description

**Table 2. Pin description**

| Name | Pin | Description |
|---|---|---|
| $1\overline{OE}$; $4\overline{OE}$ | 1, 24 | output enable input (active LOW) |
| 2OE; 3OE | 48, 25 | output enable input (active HIGH) |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| $V_{CC}$ | 7, 18, 31, 42 | supply voltage |
| 1Y0, 1Y1, 1Y2, 1Y3 | 2, 3, 5, 6 | data output |
| 2Y0, 2Y1, 2Y2, 2Y3 | 8, 9, 11, 12 | data output |
| 3Y0, 3Y1, 3Y2, 3Y3 | 13, 14, 16, 17 | data output |
| 4Y0, 4Y1, 4Y2, 4Y3 | 19, 20, 22, 23 | data output |
| 1A0, 1A1, 1A2, 1A3 | 47, 46, 44, 43 | data input |
| 2A0, 2A1, 2A2, 2A3 | 41, 40, 38, 37 | data input |
| 3A0, 3A1, 3A2, 3A3 | 36, 35, 33, 32 | data input |
| 4A0, 4A1, 4A2, 4A3 | 30, 29, 27, 26 | data input |

# 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state*

| Input | | | Output |
|---|---|---|---|
| **nAn** | **$n\overline{OE}$** | **nOE** | **nYn** |
| H | L | - | H |
| | - | H | H |
| L | L | - | L |
| | - | H | L |
| X | H | - | Z |
| | - | L | Z |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | -0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | -50 | - | mA |
| $V_I$ | input voltage | | [1] | -0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | | - | ±50 | mA |
| $V_O$ | output voltage | HIGH or LOW state | [2] | -0.5 | $V_{CC}$ + 0.5 | V |
| | | 3-state | [2] | -0.5 | +6.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | -100 | - | mA |
| $T_{stg}$ | storage temperature | | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C | [3] | - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT362-1 (TSSOP48) packages: $P_{tot}$ derates linearly with 12.2 mW/K above 109 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | - | 3.6 | V |
| | | functional | 1.2 | - | - | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | HIGH or LOW state | 0 | - | $V_{CC}$ | V |
| | | 3-state | 0 | - | 5.5 | V |
| $T_{amb}$ | ambient temperature | in free air | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CC}$ = 1.65 V to 2.7 V | 0 | - | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | - | 10 | ns/V |

# 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.2 V | 1.08 | - | - | 1.08 | - | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | $0.65V_{CC}$ | - | - | $0.65V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.2 V | - | - | 0.12 | - | 0.12 | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | - | $0.35V_{CC}$ | - | $0.35V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = -100 µA; $V_{CC}$ = 1.65 V to 3.6 V | $V_{CC}$ - 0.2 | - | - | $V_{CC}$ - 0.3 | - | V |
| | | $I_O$ = -4 mA; $V_{CC}$ = 1.65 V | 1.2 | - | - | 1.05 | - | V |
| | | $I_O$ = -8 mA; $V_{CC}$ = 2.3 V | 1.8 | - | - | 1.65 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | $I_O$ = -18 mA; $V_{CC}$ = 3.0 V | 2.4 | - | - | 2.25 | - | V |
| | | $I_O$ = -24 mA; $V_{CC}$ = 3.0 V | 2.2 | - | - | 2.0 | - | V |
| $V_{OL}$ | LOW-level outpu voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 1.65 V | - | - | 0.45 | - | 0.65 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 2.3 V | - | - | 0.6 | - | 0.8 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 3.6 V; $V_I$ = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 3.6 V; $V_O$ = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 5.5 V | - | ±0.1 | ±10 | - | ±20 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I = V_{CC}$ or GND; $I_O$ = 0 A | - | 0.1 | 20 | - | 80 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 2.7 V to 3.6 V; $V_I = V_{CC}$ - 0.6 V; $I_O$ = 0 A | - | 5 | 500 | - | 5000 | µA |
| $C_I$ | input capacitance | $V_{CC}$ = 0 V to 3.6 V; $V_I$ = GND to $V_{CC}$ | - | 5.0 | - | - | - | pF |

[1] All typical values are measured at $V_{CC}$ = 3.3 V (unless stated otherwise) and $T_{amb}$ = 25 °C.

# 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.*

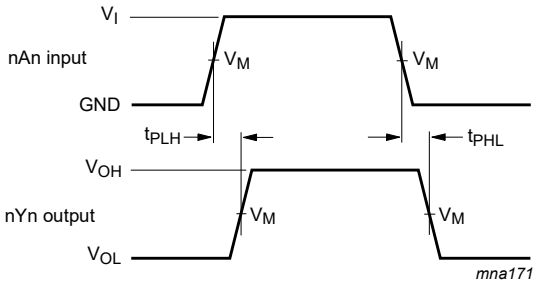
| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | nAn to nYn; see Fig. 4 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 13 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.7 | 4.8 | 10.1 | 1.7 | 11.7 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.5 | 2.6 | 5.3 | 1.5 | 6.1 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 2.6 | 5.0 | 1.0 | 6.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.2 | 4.4 | 1.0 | 5.5 | ns |
| $t_{en}$ | enable time | $n\overline{OE}$ to nYn; see Fig. 5 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 17 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.0 | 5.2 | 12.5 | 1.0 | 13.2 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 3.0 | 6.9 | 1.0 | 7.3 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 3.2 | 6.0 | 1.0 | 7.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.4 | 5.5 | 1.0 | 7.0 | ns |
| | | nOE to nYn; see Fig. 6 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 19 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.5 | 6.9 | 14.2 | 2.5 | 15.0 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 2.1 | 3.9 | 7.5 | 2.1 | 8.3 | ns |
| | | $V_{CC}$ = 2.7 V | 1.5 | 3.3 | 6.0 | 1.5 | 7.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | 3.1 | 5.5 | 1.5 | 7.0 | ns |
| $t_{dis}$ | disable time | $n\overline{OE}$ to nYn; see Fig. 5 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 9.0 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.4 | 4.3 | 8.3 | 2.4 | 9.2 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 2.4 | 4.7 | 1.0 | 5.2 | ns |
| | | $V_{CC}$ = 2.7 V | 1.5 | 3.2 | 5.5 | 1.5 | 7.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | 3.0 | 5.0 | 1.5 | 6.5 | ns |
| | | nOE to nYn; see Fig. 6 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 8.0 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.5 | 3.5 | 8.4 | 1.5 | 9.6 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0.5 | 1.9 | 4.8 | 0.5 | 5.5 | ns |
| | | $V_{CC}$ = 2.7 V | 1.5 | 3.5 | 5.5 | 1.5 | 7.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.6 | 5.0 | 1.0 | 6.5 | ns |
| $C_{PD}$ | power dissipation capacitance | per input; $V_I$ = GND to $V_{CC}$ [3] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | 8.4 | - | - | - | pF |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | 11.9 | - | - | - | pF |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | 15.0 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF; $V_{CC}$ = supply voltage in Volts;
N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

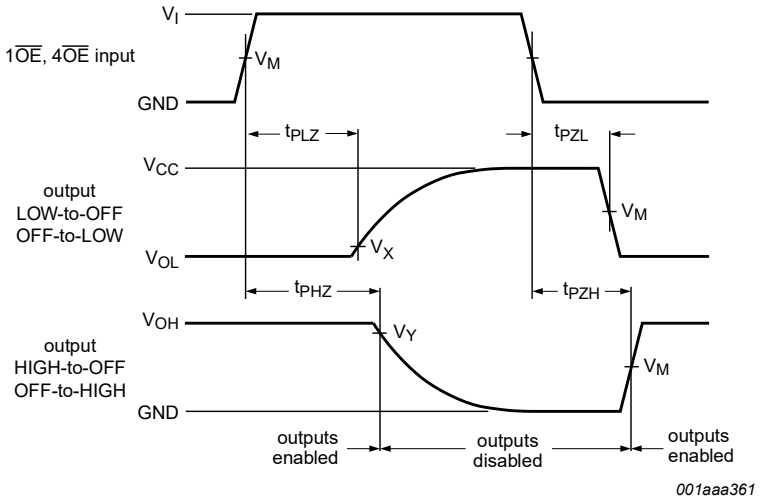
## 10.1. Waveforms and test circuit




Measurements points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

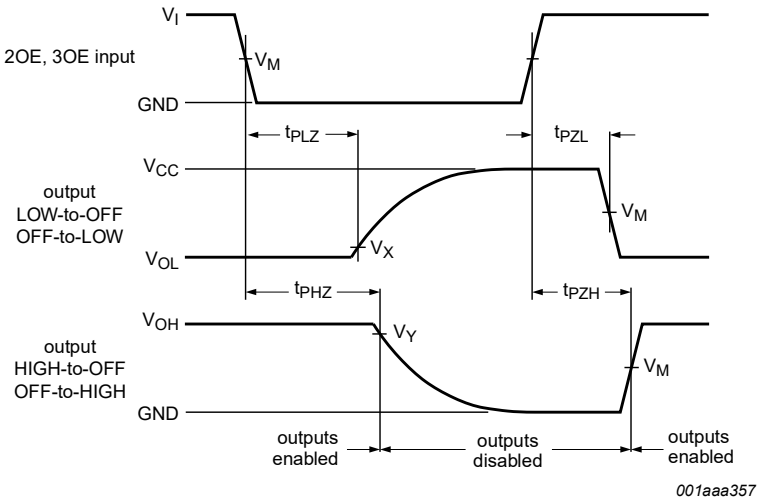
**Fig. 4. Input nAn to output nYn propagation delays**




Measurements points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 5. 3-state enable and disable times for inputs 1$\overline{OE}$ and 4$\overline{OE}$**



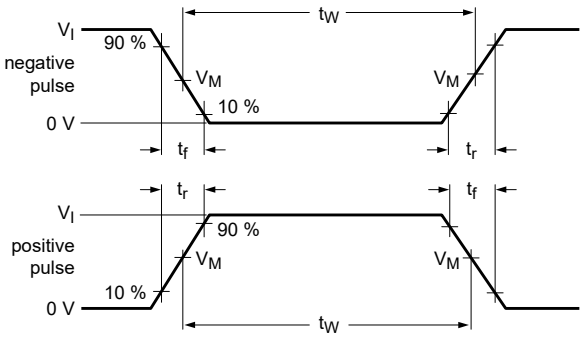

Measurements points are given in Table 8.

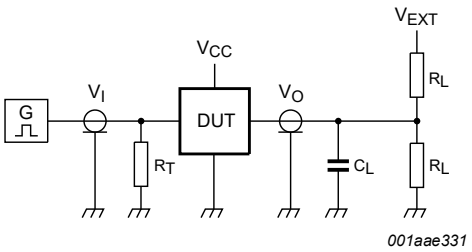
$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 6. 3-state enable and disable times for inputs 2OE and 3OE**

**Table 8. Measurement points**

| Supply voltage | Input | Output | | |
|---|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.2 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 1.65 V to 1.95 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 2.3 V to 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |




Test data is given in Table 9.

Definitions for test circuit:

$R_L$ = Load resistance;

$C_L$ = Load capacitance including jig and probe capacitance;

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator;

$V_{EXT}$ = External voltage for measuring switching times.

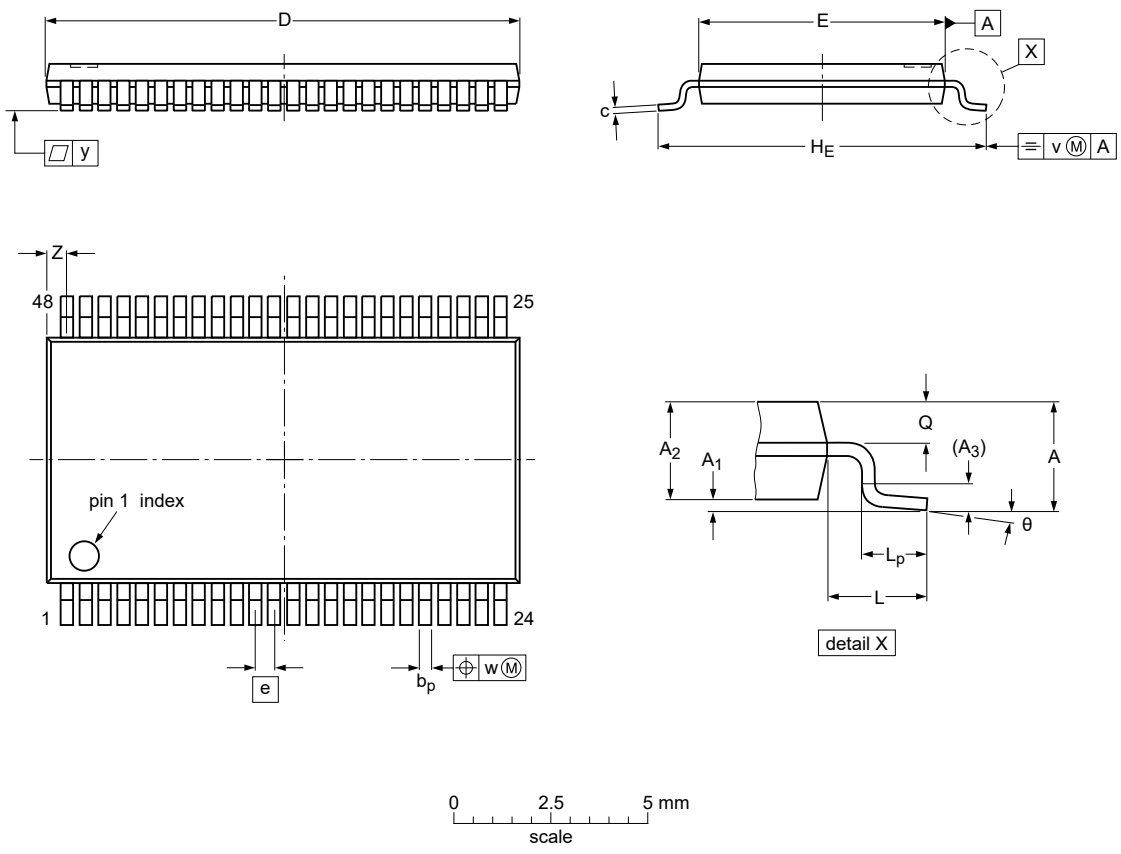
**Fig. 7. Test circuit for measuring switching times**

**Table 9. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 1.2 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ | open | $2V_{CC}$ | GND |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ | open | $2V_{CC}$ | GND |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 500 Ω | open | $2V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2V_{CC}$ | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2V_{CC}$ | GND |

# 11. Package outline

**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm** **SOT362-1**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.2 | 0.15 | 1.05 | | 0.28 | 0.2 | 12.6 | 6.2 | | 8.3 | | 0.8 | 0.50 | | | | 0.8 | 8° |
| | nom | | | | 0.25 | | | | | 0.5 | | 1 | | | 0.25 | 0.08 | 0.1 | | |
| | min | | 0.05 | 0.85 | | 0.17 | 0.1 | 12.4 | 6.0 | | 7.9 | | 0.4 | 0.35 | | | | 0.4 | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

*sot362-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT362-1 | | MO-153 | | | | ~~13-08-05~~ 24-01-05 |

**Fig. 8. Package outline SOT362-1 (TSSOP48)**

## 12. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

## 13. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC16241A v.7 | 20240422 | Product data sheet | - | 74LVC16241A v.6 |
| Modifications: | • Fig. 8: Updated package outline drawing SOT362-1 (TSSOP48). | | | |
| 74LVC16241A v.6 | 20230804 | Product data sheet | - | 74LVC16241A v.5 |
| Modifications: | • Section 2: ESD specification updated according to the latest JEDEC standard.<br>• Section 7: Derating values for $P_{tot}$ total power dissipation updated. | | | |
| 74LVC16241A v.5 | 20190426 | Product data sheet | - | 74LVC16241A v.4 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Type number 74LVC16241ADL (SOT370-1) removed.<br>• Package outline drawing SOT362-1 (TSSOP48) updated. | | | |
| 74LVC16241A v.4 | 20111026 | Product data sheet | - | 74LVC16241A v.3 |
| Modifications: | • The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Table 4, Table 5, Table 6, Table 7, and Table 9: values added for lower voltage ranges. | | | |
| 74LVC16241A v.3 | 20040305 | Product specification | - | 74LVC16241A v.2 |
| 74LVC16241A v.2 | 19970729 | Product specification | - | 74LVC16241A v.1 |
| 74LVC16241A v.1 | 19951226 | Product specification | - | - |

# 14. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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