

# 74LVC1G08GM,132 Datasheet



DiGi Electronics Part Number	74LVC1G08GM,132-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	74LVC1G08GM,132
Description	IC GATE AND 1CH 2-INP 6XSON
Detailed Description	AND Gate IC 1 Channel 6-XSON, SOT886 (1.45x1)



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## Purchase and inquiry

**Manufacturer Product Number:**

74LVC1G08GM,132

**Series:**

74LVC

**Logic Type:**

AND Gate

**Number of Inputs:**

2

**Voltage - Supply:**

1.65V ~ 5.5V

**Current - Output High, Low:**

32mA, 32mA

**Input Logic Level - High:**

1.7V ~ 2V

**Operating Temperature:**

-40°C ~ 125°C (TA)

**Supplier Device Package:**

6-XSON, SOT886 (1.45x1)

**Base Product Number:**

74LVC1G08

**Manufacturer:**

Nexperia USA Inc.

**Product Status:**

Active

**Number of Circuits:**

1

**Features:**

-

**Current - Quiescent (Max):**4  $\mu$ A**Input Logic Level - Low:**

0.7V ~ 0.8V

**Max Propagation Delay @ V, Max CL:**

4ns @ 5V, 50pF

**Mounting Type:**

Surface Mount

**Package / Case:**

6-XFDN

## Environmental & Export classification

**RoHS Status:**

ROHS3 Compliant

**REACH Status:**

REACH Unaffected

**HTSUS:**

8542.39.0001

**Moisture Sensitivity Level (MSL):**

1 (Unlimited)

**ECCN:**

EAR99



# 74LVC1G08

Single 2-input AND gate

Rev. 16.1 — 3 September 2024

Product data sheet

## 1. General description

The 74LVC1G08 is a single 2-input AND gate. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall time.

This device is fully specified for partial power-down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power dissipation
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up performance  $\leq 250$  mA
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74LVC1G08GW</a>	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	<a href="#">SOT353-1</a>
<a href="#">74LVC1G08GV</a>	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	<a href="#">SOT753</a>
<a href="#">74LVC1G08GM</a>	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	<a href="#">SOT886</a>
<a href="#">74LVC1G08GN</a>	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	<a href="#">SOT1115</a>
<a href="#">74LVC1G08GS</a>	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	<a href="#">SOT1202</a>
<a href="#">74LVC1G08GX</a>	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	<a href="#">SOT1226-3</a>
<a href="#">74LVC1G08GZ</a>	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	<a href="#">SOT8065-1</a>

### 4. Marking

Table 2. Marking

Type number	Marking code [1]
74LVC1G08GW	VE
74LVC1G08GV	V08
74LVC1G08GM	VE
74LVC1G08GN	VE
74LVC1G08GS	VE
74LVC1G08GX	VE
74LVC1G08GZ	VE

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram

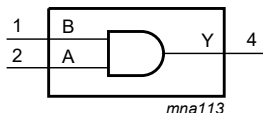


Fig. 1. Logic symbol



Fig. 2. IEC logic symbol

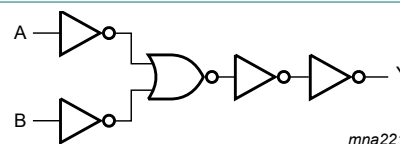
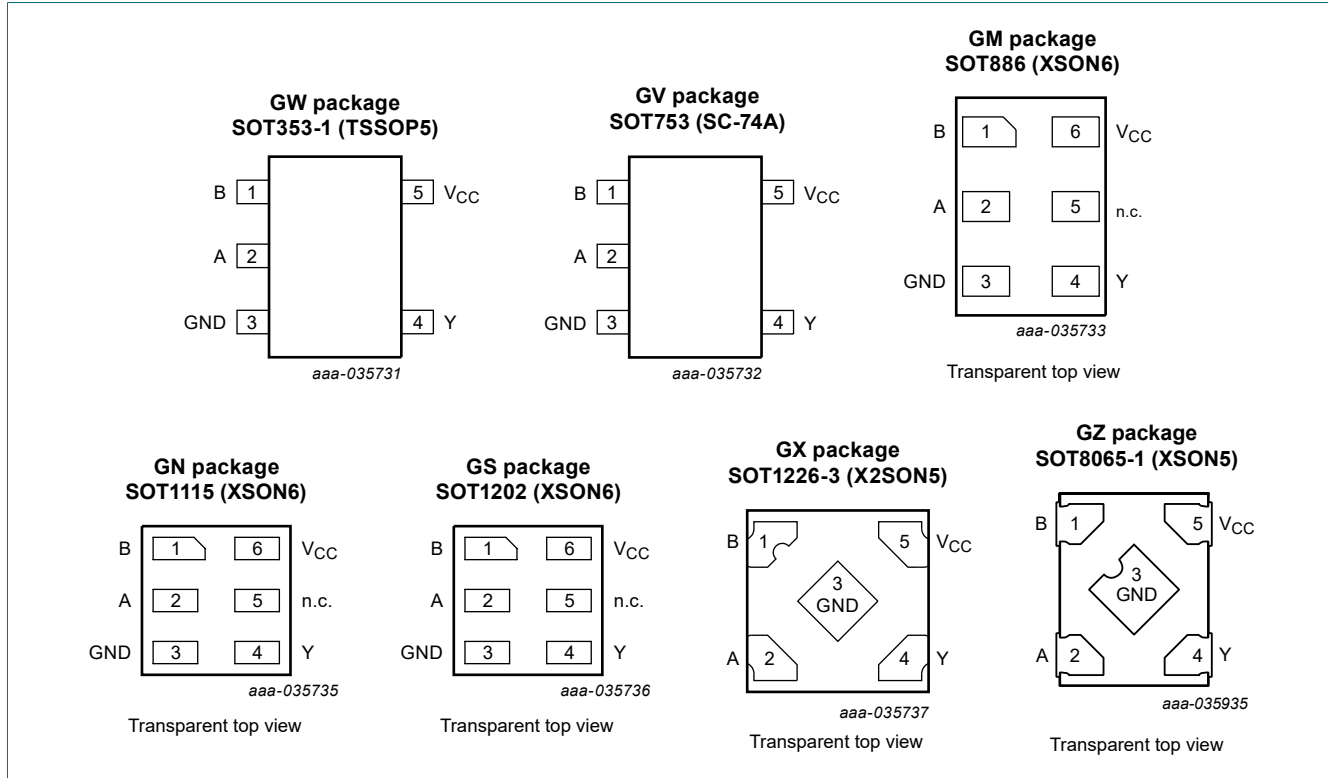


Fig. 3. Logic diagram

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5, SC-74A, XSON5 and X2SON5	XSON6	
B	1	1	data input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V <sub>CC</sub>		6	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level.*

Input		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	Active mode	[1] -0.5	$V_{CC} + 0.5$	V
		Power-down mode; $V_{CC} = 0$ V	[1] -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	250	mW
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package:  $P_{tot}$  derates linearly with 3.8 mW/K above 85 °C.

For SOT886 (XSON6) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.

For SOT1115 (XSON6) package:  $P_{tot}$  derates linearly with 3.2 mW/K above 71 °C.

For SOT1202 (XSON6) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.

For SOT1226-3 (X2SON5) package:  $P_{tot}$  derates linearly with 3.0 mW/K above 67 °C.

For SOT8065-1 (XSON5) package:  $P_{tot}$  derates linearly with 3.2 mW/K above 72 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	Active mode	0	-	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	-	5.5	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	-	10	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	-	0.3V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V <sub>CC</sub> - 0.1	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	0.95	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.9	-	-	1.7	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	1.9	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.3	-	-	2.0	-	V
		I <sub>O</sub> = -32 mA; V <sub>CC</sub> = 4.5 V	3.8	-	-	3.4	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.10	-	0.10	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.70	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.30	-	0.45	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.40	-	0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.80	V
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V	-	-	0.55	-	0.80	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	±0.1	±1	-	±1	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	±0.1	±2	-	±2	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 1.65 V to 5.5 V	-	0.1	4	-	4	µA
ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>CC</sub> = 2.3 V to 5.5 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	500	µA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5	-	-	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{pd}$	propagation delay	A, B to Y; see Fig. 4 [2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	3.4	8.0	1.0	10.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.5	2.2	5.5	0.5	7.0	ns
		$V_{CC} = 2.7 \text{ V}$	0.5	2.5	5.5	0.5	7.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.5	2.1	4.5	0.5	6.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.5	1.7	4.0	0.5	5.5	ns
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC}; V_{CC} = 3.3 \text{ V}$ [3]	-	16	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25 \text{ °C}$  and  $V_{CC} = 1.8 \text{ V}, 2.5 \text{ V}, 2.7 \text{ V}, 3.3 \text{ V}$  and  $5.0 \text{ V}$  respectively.

[2]  $t_{pd}$  is the same as  $t_{PLZ}$  and  $t_{PZL}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

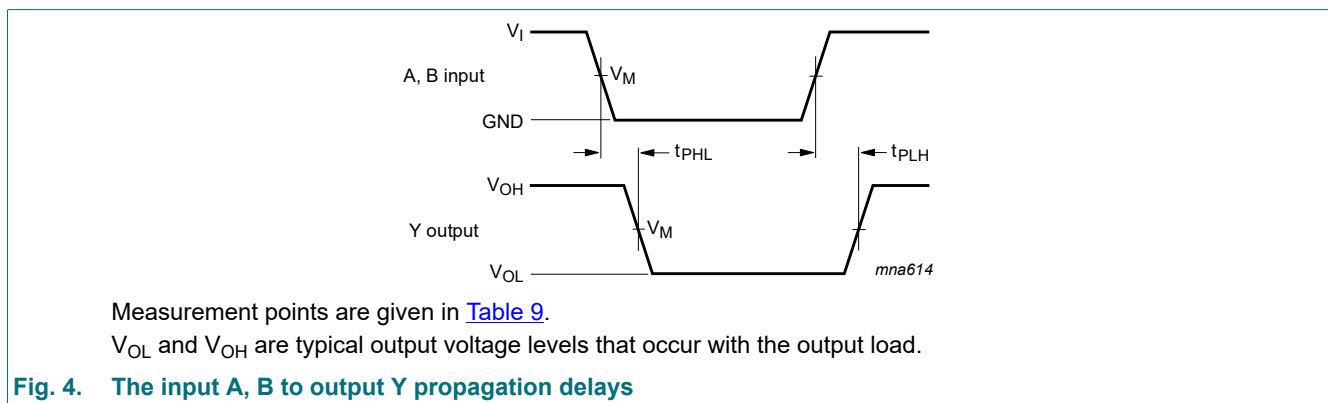
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

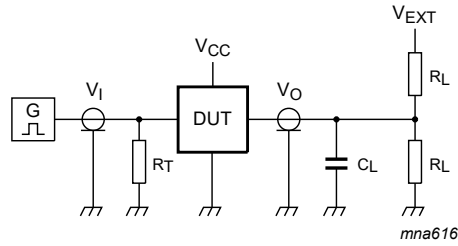
$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 11.1. Waveforms and test circuit


**Fig. 4. The input A, B to output Y propagation delays**
**Table 9. Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$





Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 5. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$
$V_{CC}$	$V_I$	$t_r = t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open

## 12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

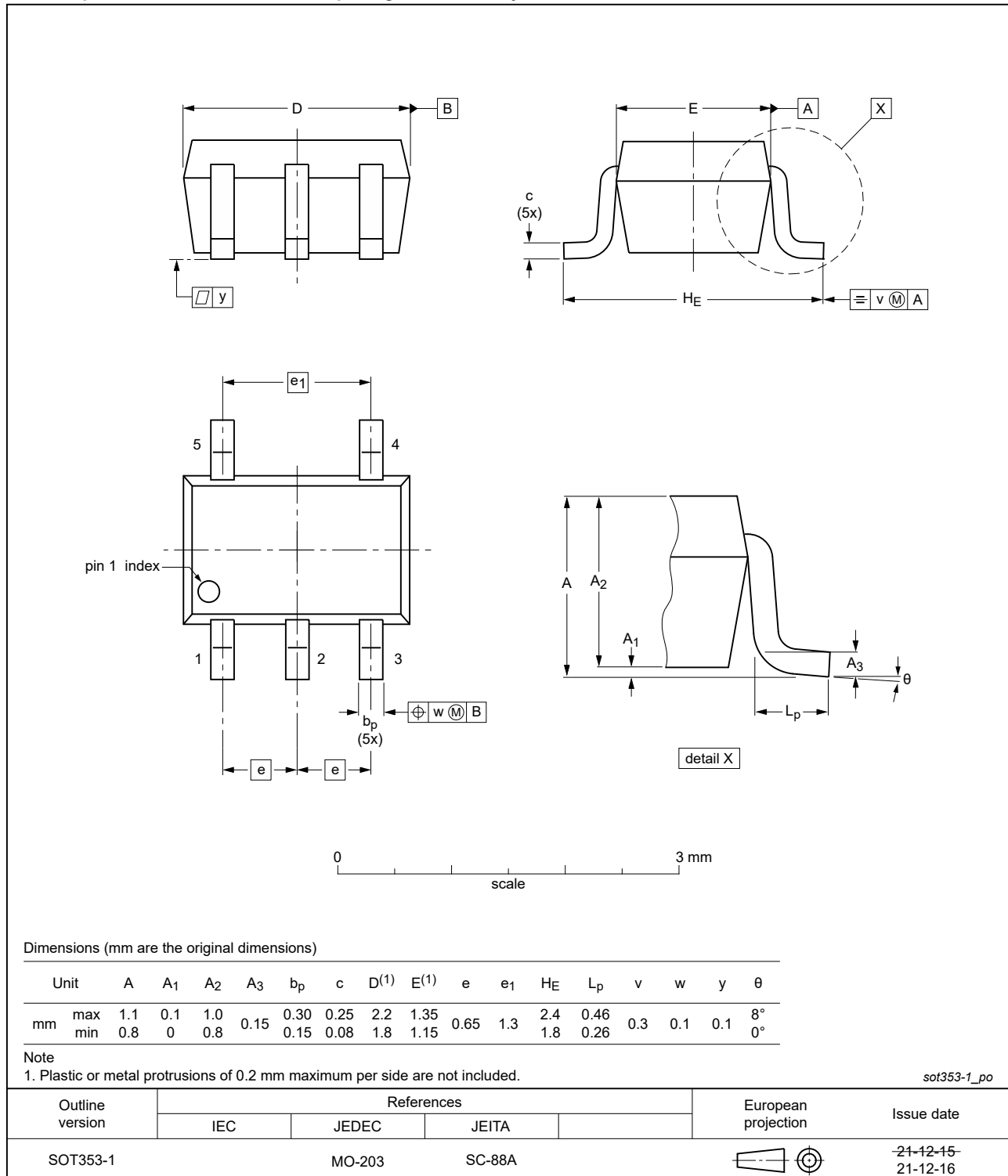


Fig. 6. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

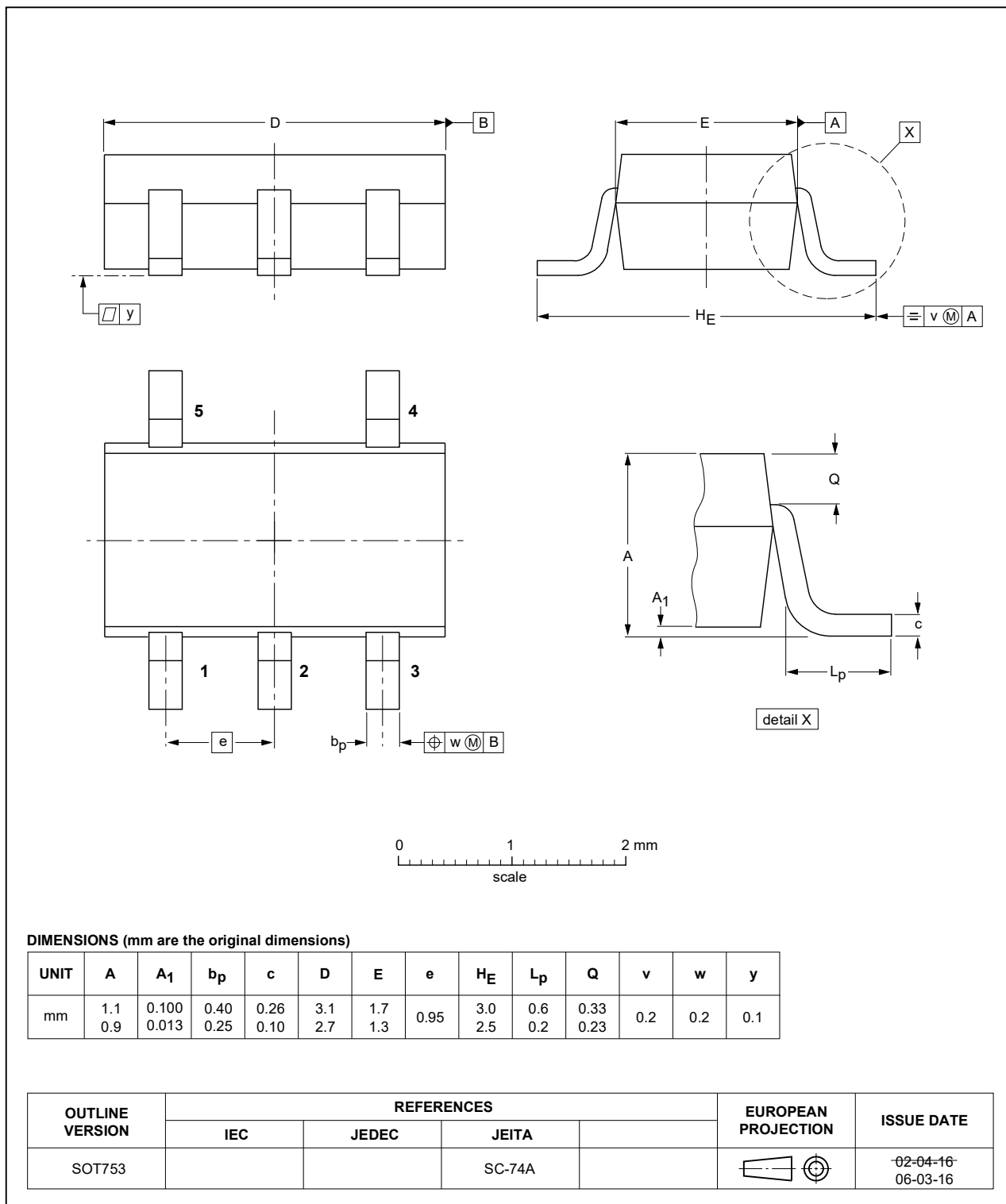


Fig. 7. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

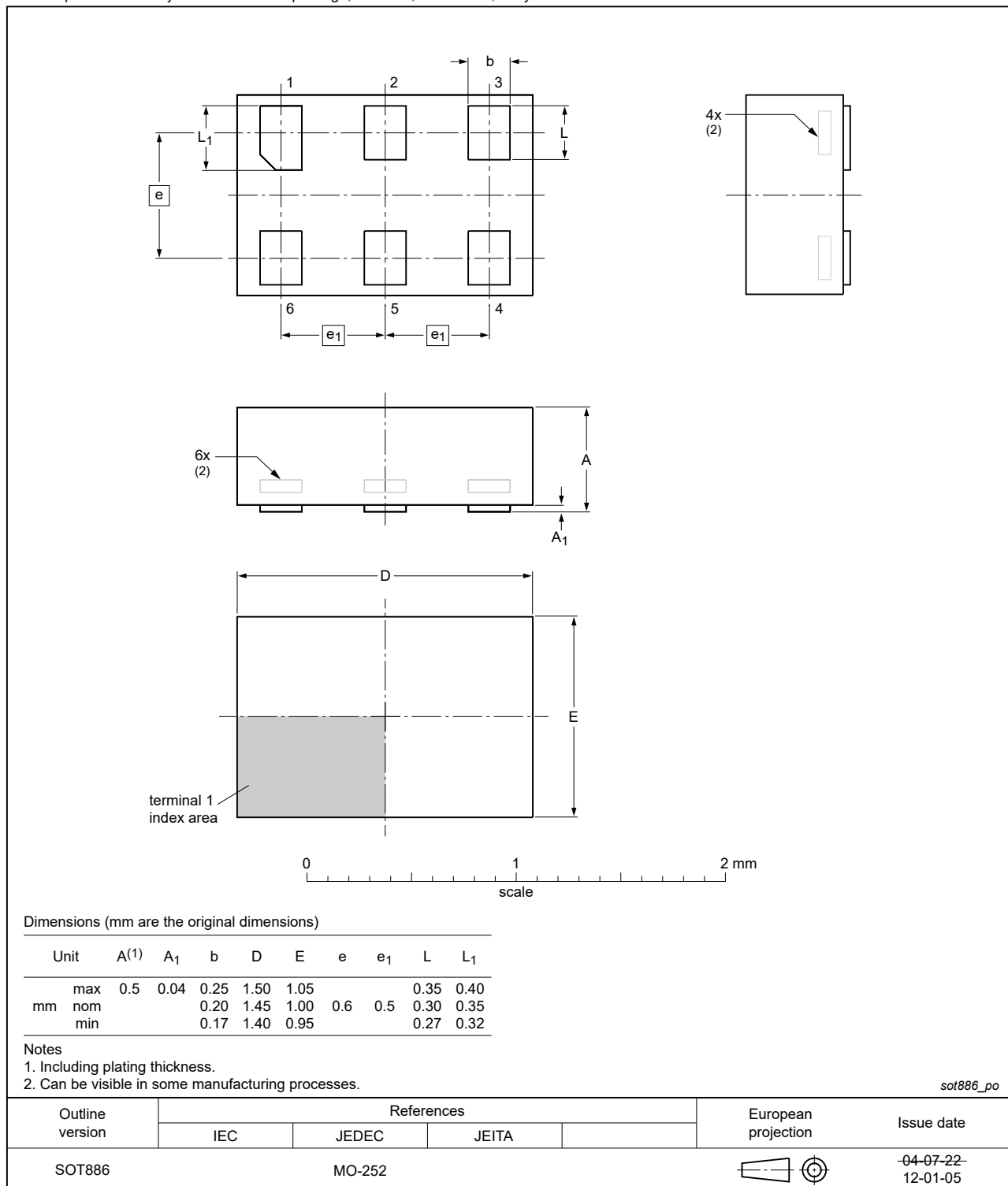
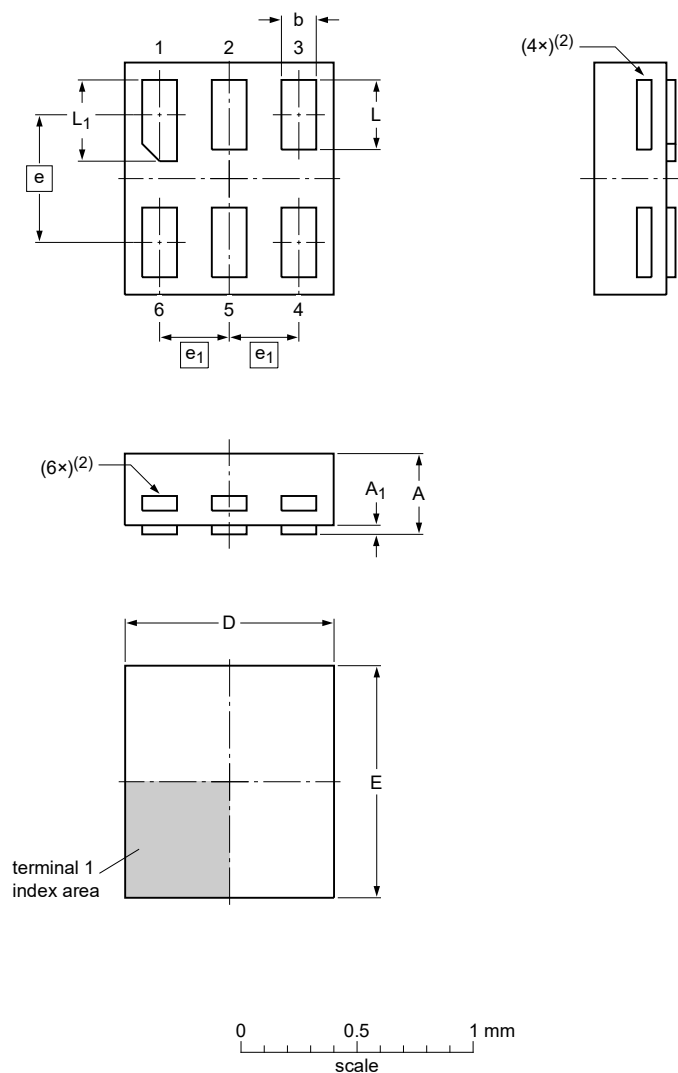


Fig. 8. Package outline SOT886 (XSON6)

**XSON6: extremely thin small outline package; no leads;  
6 terminals; body 0.9 x 1.0 x 0.35 mm**

SOT1115




## Dimensions

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	max 0.35	0.04	0.20	0.95	1.05			0.35	0.40
	nom		0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min		0.12	0.85	0.95			0.27	0.32

## Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

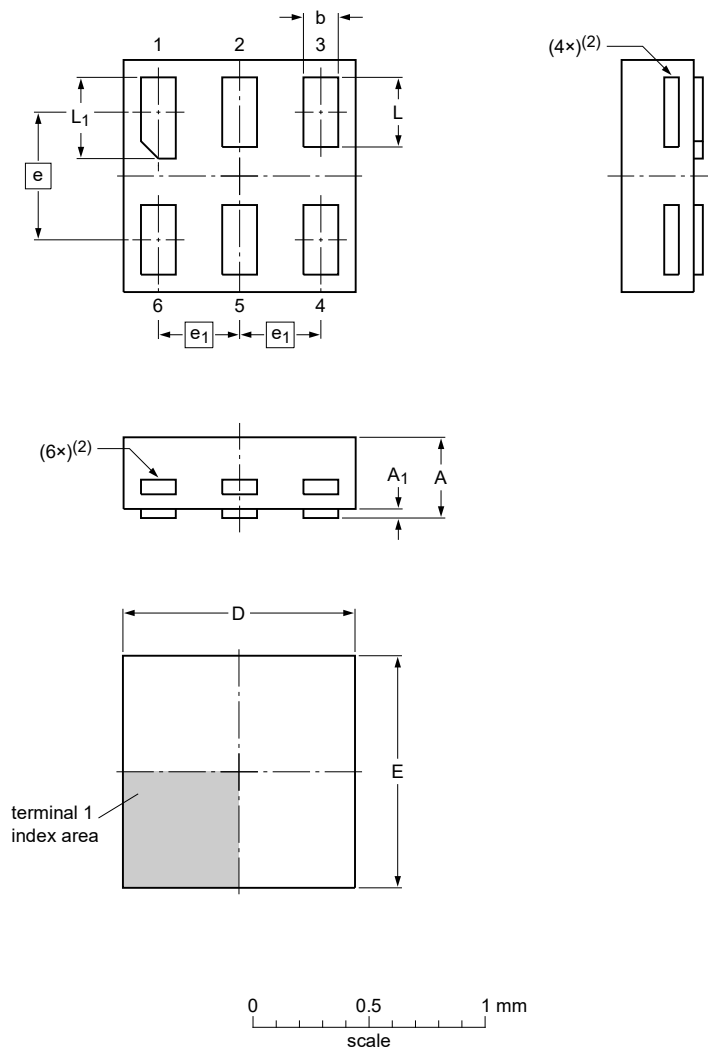
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Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						<del>10-04-02</del> 10-04-07

**Fig. 9. Package outline SOT1115 (XSON6)**

**XSON6: extremely thin small outline package; no leads;  
6 terminals; body 1.0 x 1.0 x 0.35 mm**

SOT1202




## Dimensions

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	max 0.35	0.04	0.20	1.05	1.05			0.35	0.40
	nom		0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min		0.12	0.95	0.95			0.27	0.32

## Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

sot1202\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						<del>10-04-02</del> 10-04-06

**Fig. 10. Package outline SOT1202 (XSON6)**

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.32 mm

SOT1226-3

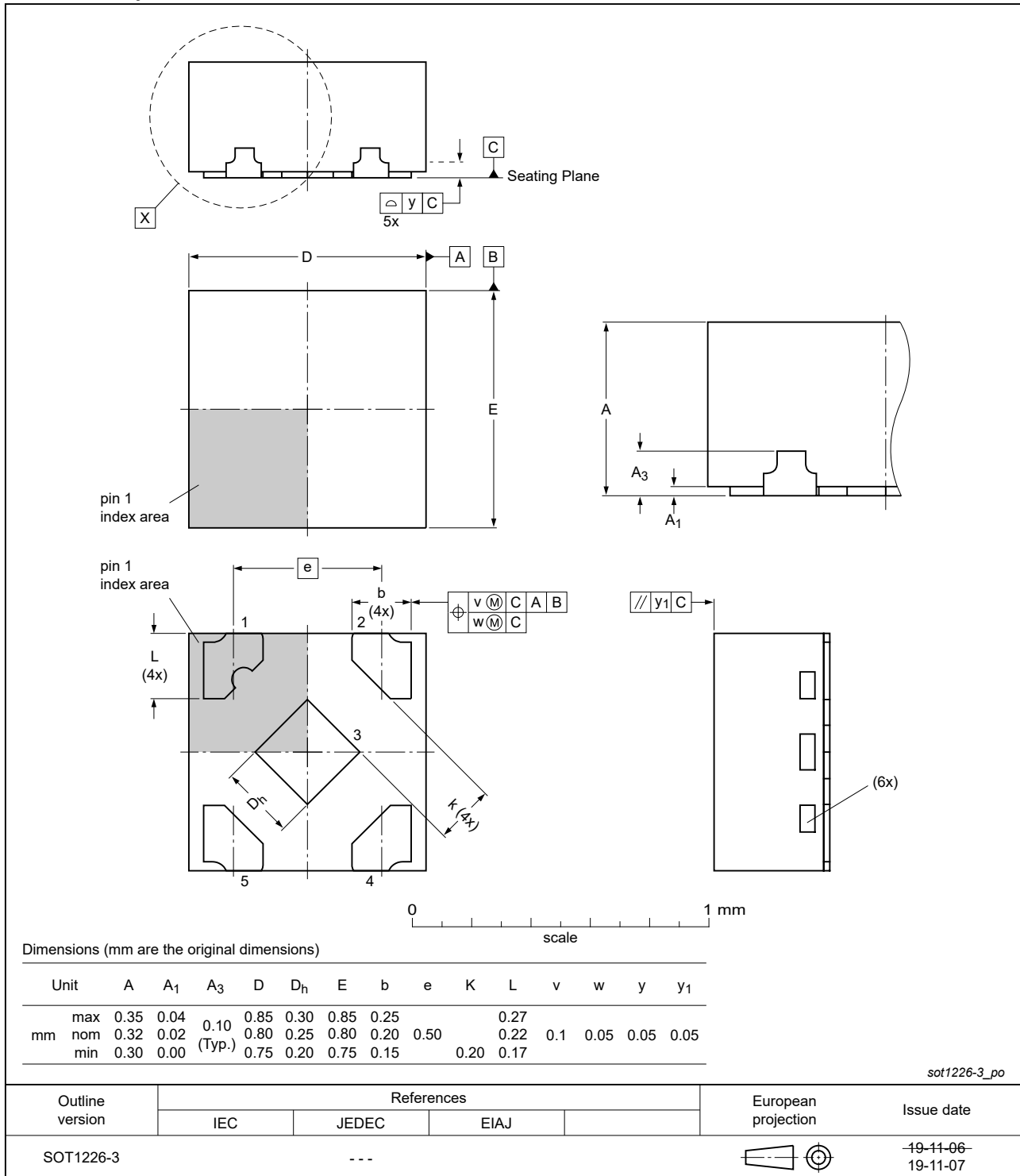


Fig. 11. Package outline SOT1226-3 (X2SON5)

**XSON5:** Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm

SOT8065-1

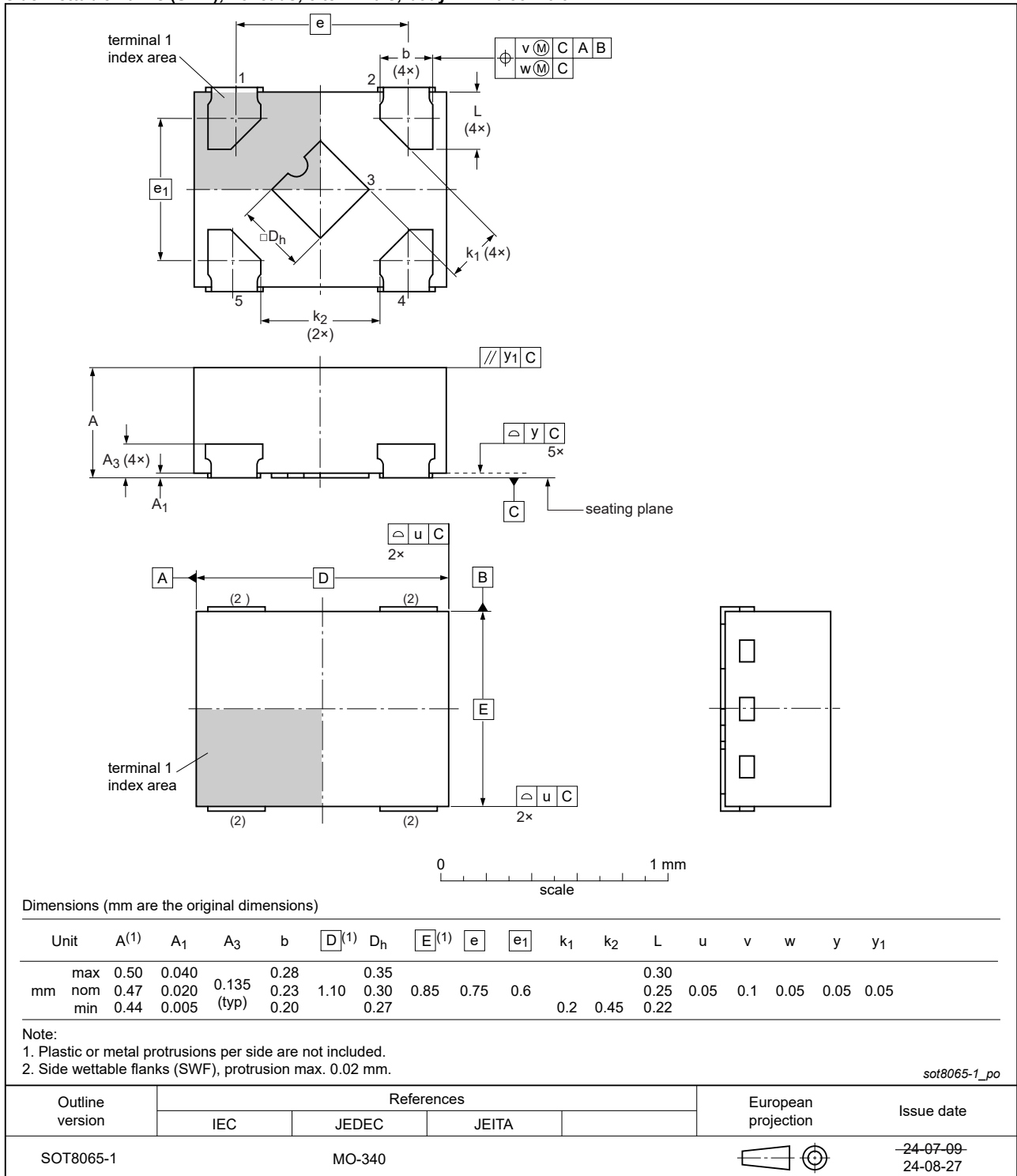


Fig. 12. Package outline SOT8065-1 (XSON5)



## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G08 v.16.1	20240903	Product data sheet	-	74LVC1G08 v.16
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Fig. 12</a>: Added JEDEC reference MO-340 to SOT8065-1 package outline drawing.</li> </ul>			
74LVC1G08 v.16	20240711	Product data sheet	-	74LVC1G08 v.15
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVC1G08GZ (SOT8065-1/XSON5) added.</li> <li>Type number 74LVC1G08GF (SOT891/XSON6) removed.</li> </ul>			
74LVC1G08 v.15	20230804	Product data sheet	-	74LVC1G08 v.14
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74LVC1G08 v.14	20220224	Product data sheet	-	74LVC1G08 v.13
Modifications:	<ul style="list-style-type: none"> <li>Package SOT1226 (X2SON5) changed to SOT1226-3 (X2SON5).</li> </ul>			
74LVC1G08 v.13	20220209	Product data sheet	-	74LVC1G08 v.12
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Table 5</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Fig. 6</a>: Package outline drawing for SOT353-1 (TSSOP5) has changed.</li> </ul>			
74LVC1G08 v.12	20180116	Product data sheet	-	74LVC1G08 v.11
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Pin configuration drawing of SOT1226 modified.</li> </ul>			
74LVC1G08 v.11	20161128	Product data sheet	-	74LVC1G08 v.10
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7</a>: The maximum limits for leakage current and supply current have changed.</li> </ul>			
74LVC1G08 v.10	20120629	Product data sheet	-	74LVC1G08 v.9
Modifications:	<ul style="list-style-type: none"> <li>Added type number 74LVC1G08GX (SOT1226)</li> <li>Package outline drawing of SOT886 (<a href="#">Fig. 8</a>) modified.</li> </ul>			
74LVC1G08 v.9	20111209	Product data sheet	-	74LVC1G08 v.8
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74LVC1G08 v.8	20101019	Product data sheet	-	74LVC1G08 v.7

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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