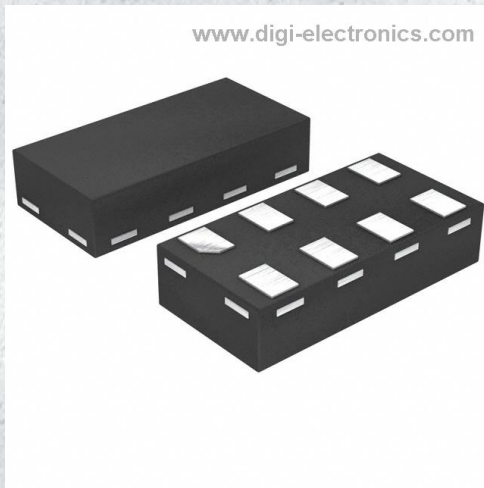# 74LVC3G06GS,115 Datasheet

www.digi-electronics.com

DiGi Electronics Part Number	74LVC3G06GS,115-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74LVC3G06GS,115
Description	IC INVERTER 3CH 3-INP 8XSON
Detailed Description	Inverter IC 3 Channel Open Drain 8-XSON (1.35x1)

https://www.DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	**Manufacturer:**
74LVC3G06GS,115	Nexperia USA Inc.
Series:	**Product Status:**
74LVC	Active
Logic Type:	**Number of Circuits:**
Inverter	3
Number of Inputs:	**Features:**
3	Open Drain
Voltage - Supply:	**Current - Quiescent (Max):**
1.65V ~ 5.5V	4 µA
Current - Output High, Low:	**Input Logic Level - Low:**
-, 32mA	0.7V ~ 0.8V
Input Logic Level - High:	**Max Propagation Delay @ V, Max CL:**
1.7V ~ 2V	2.9ns @ 5V, 50pF
Operating Temperature:	**Mounting Type:**
-40℃ ~ 125℃	Surface Mount
Supplier Device Package:	**Package / Case:**
8-XSON (1.35x1)	8-XFDFN
Base Product Number:	
74LVC3G06	

Environmental & Export classification

RoHS Status:	**Moisture Sensitivity Level (MSL):**
ROHS3 Compliant	1 (Unlimited)
REACH Status:	**ECCN:**
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

74LVC3G06

Triple inverter with open-drain output

Rev. 16 — 28 August 2023   **Product data sheet**

1. General description

The 74LVC3G06 is a triple inverter with open-drain outputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- -24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

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74LVC3G06

Triple inverter with open-drain output

3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74LVC3G06DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm		SOT505-2
74LVC3G06DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm		SOT765-1
74LVC3G06GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm		SOT833-1
74LVC3G06GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm		SOT1116
74LVC3G06GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm		SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code [1]
74LVC3G06DP	V06
74LVC3G06DC	V06
74LVC3G06GT	V06
74LVC3G06GN	V6
74LVC3G06GS	V6

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.
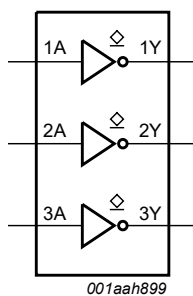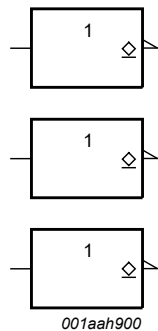
5. Functional diagram

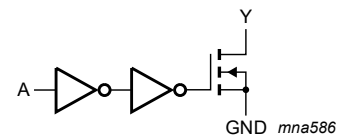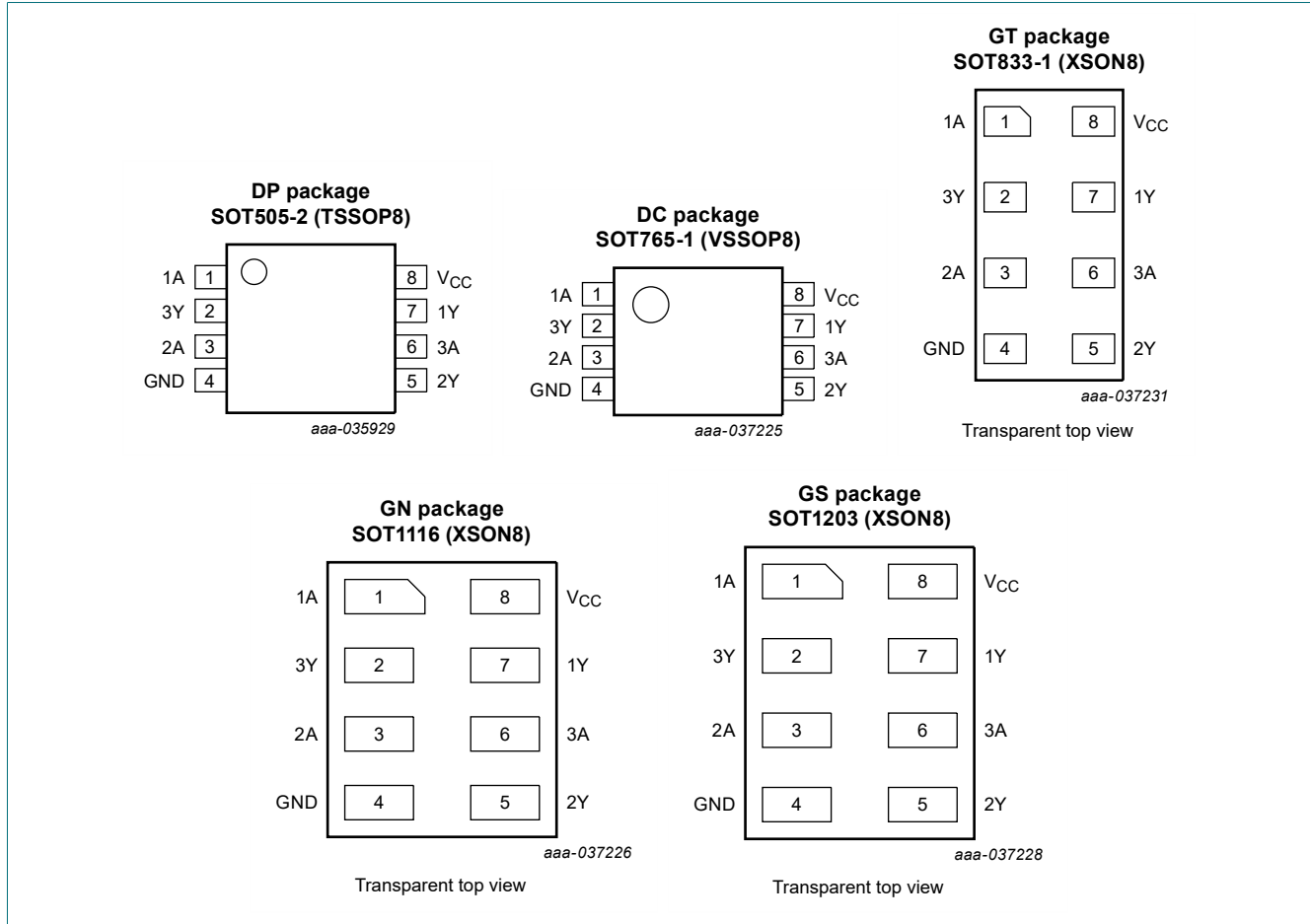**Fig. 1. Logic symbol**

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram (one inverter)

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74LVC3G06

Triple inverter with open-drain output

6. Pinning information

6.1. Pinning

DP package
SOT505-2 (TSSOP8)

aaa-035929

DC package
SOT765-1 (VSSOP8)

aaa-037225

GT package
SOT833-1 (XSON8)

aaa-037231

Transparent top view

GN package
SOT1116 (XSON8)

aaa-037226

Transparent top view

GS package
SOT1203 (XSON8)

aaa-037228

Transparent top view

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
1Y, 2Y, 3Y	7, 5, 2	data output
GND	4	ground (0 V)
V_{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input nA	Output nY
L	Z
H	L

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74LVC3G06

Triple inverter with open-drain output

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O < 0$ V		-50	-	mA
V_O	output voltage	Active mode	[1]	-0.5	+6.5	V
		Power-down mode; $V_{CC} = 0$ V	[1]	-0.5	+6.5	V
I_O	output current	$V_O = 0$ V to 6.5 V		-	50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
   For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.
   For SOT833-1 (XSON8) package: P_{tot} derates linearly with 3.1 mW/K above 68 °C.
   For SOT1116 (XSON8) package: P_{tot} derates linearly with 4.2 mW/K above 90 °C.
   For SOT1203 (XSON8) package: P_{tot} derates linearly with 3.6 mW/K above 81 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	5.5	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T$_{amb}$ = -40 °C to +85 °C						
V$_{IH}$	HIGH-level input voltage	V$_{CC}$ = 1.65 V to 1.95 V	0.65V$_{CC}$	-	-	V
		V$_{CC}$ = 2.3 V to 2.7 V	1.7	-	-	V
		V$_{CC}$ = 2.7 V to 3.6 V	2.0	-	-	V
		V$_{CC}$ = 4.5 V to 5.5 V	0.7V$_{CC}$	-	-	V
V$_{IL}$	LOW-level input voltage	V$_{CC}$ = 1.65 V to 1.95 V	-	-	0.35V$_{CC}$	V
		V$_{CC}$ = 2.3 V to 2.7 V	-	-	0.7	V
		V$_{CC}$ = 2.7 V to 3.6 V	-	-	0.8	V
		V$_{CC}$ = 4.5 V to 5.5 V	-	-	0.3V$_{CC}$	V
V$_{OL}$	LOW-level output voltage	V$_I$ = V$_{IH}$ or V$_{IL}$				
		I$_O$ = 100 µA; V$_{CC}$ = 1.65 V to 5.5 V	-	-	0.10	V
		I$_O$ = 4 mA; V$_{CC}$ = 1.65 V	-	-	0.45	V
		I$_O$ = 8 mA; V$_{CC}$ = 2.3 V	-	-	0.30	V
		I$_O$ = 12 mA; V$_{CC}$ = 2.7 V	-	-	0.40	V
		I$_O$ = 24 mA; V$_{CC}$ = 3.0 V	-	-	0.55	V
		I$_O$ = 32 mA; V$_{CC}$ = 4.5 V	-	-	0.55	V
I$_I$	input leakage current	V$_I$ = 5.5 V or GND; V$_{CC}$ = 0 V to 5.5 V [2]	-	±0.1	±1	µA
I$_{OZ}$	OFF-state output current	V$_I$ = V$_{IH}$ or V$_{IL}$; V$_O$ = V$_{CC}$ or GND; V$_{CC}$ = 5.5 V	-	±0.1	±2	µA
I$_{OFF}$	power-off leakage current	V$_I$ or V$_O$ = 5.5 V; V$_{CC}$ = 0 V	-	±0.1	±2	µA
I$_{CC}$	supply current	V$_I$ = 5.5 V or GND; I$_O$ = 0 A; V$_{CC}$ = 1.65 V to 5.5 V	-	0.1	4	µA
ΔI$_{CC}$	additional supply current	per pin; V$_I$ = V$_{CC}$ - 0.6 V; I$_O$ = 0 A; [2] V$_{CC}$ = 2.3 V to 5.5 V	-	5	500	µA
C$_I$	input capacitance		-	2.5	-	pF
T$_{amb}$ = -40 °C to +125 °C						
V$_{IH}$	HIGH-level input voltage	V$_{CC}$ = 1.65 V to 1.95 V	0.65V$_{CC}$	-	-	V
		V$_{CC}$ = 2.3 V to 2.7 V	1.7	-	-	V
		V$_{CC}$ = 2.7 V to 3.6 V	2.0	-	-	V
		V$_{CC}$ = 4.5 V to 5.5 V	0.7V$_{CC}$	-	-	V
V$_{IL}$	LOW-level input voltage	V$_{CC}$ = 1.65 V to 1.95 V	-	-	0.35V$_{CC}$	V
		V$_{CC}$ = 2.3 V to 2.7 V	-	-	0.7	V
		V$_{CC}$ = 2.7 V to 3.6 V	-	-	0.8	V
		V$_{CC}$ = 4.5 V to 5.5 V	-	-	0.3V$_{CC}$	V

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100$ µA; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.10	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	-	0.70	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	-	0.45	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	-	0.60	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	-	0.80	V
		$I_O = 32$ mA; $V_{CC} = 4.5$ V	-	-	0.80	V
I_I	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	-	±1	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±2	µA
I_{OFF}	power-off leakage current	V_I or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	-	±2	µA
I_{CC}	supply current	$V_I = 5.5$ V or GND; $I_O = 0$ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	4	µA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V	-	-	500	µA

[1] All typical values are measured at $T_{amb} = 25$ °C.
[2] These typical values are measured at $V_{CC} = 3.3$ V.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Fig. 4 [2]						
		$V_{CC} = 1.65$ V to 1.95 V	1.0	2.6	6.5	1.0	8.2	ns
		$V_{CC} = 2.3$ V to 2.7 V	0.5	1.6	3.9	0.5	4.9	ns
		$V_{CC} = 2.7$ V	1.0	2.2	4.2	1.0	5.3	ns
		$V_{CC} = 3.0$ V to 3.6 V	0.5	2.0	3.4	0.5	4.3	ns
		$V_{CC} = 4.5$ V to 5.5 V	0.5	1.4	2.9	0.5	3.7	ns
C_{PD}	power dissipation capacitance	$V_I = $ GND to V_{CC}; $V_{CC} = 3.3$ V [3]	-	5.9	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25$ °C and $V_{CC} = 1.8$ V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
[2] t_{pd} is the same as t_{PLZ} and t_{PZL}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;
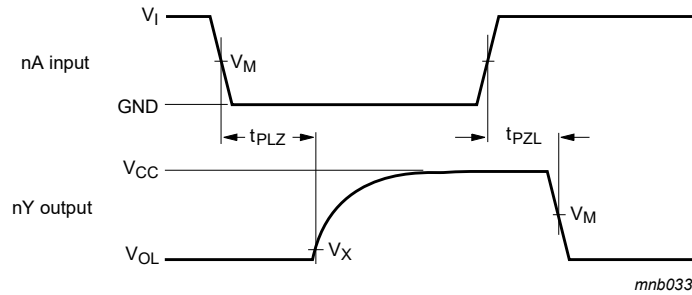
V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit

Measurement points are given in Table 9.

V_{OL} is the typical output voltage level that occurs with the output load.

Fig. 4. **The input (nA) to output (nY) propagation delays**

Table 9. Measurement points

Supply voltage	Input	Output	
V_{CC}	V_M	V_M	V_X
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.3 V
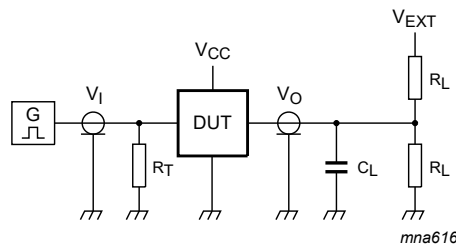
Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 5. **Test circuit for measuring switching times**

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	$2 \times V_{CC}$

Triple inverter with open-drain output

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm   **SOT505-2**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A1	A2	A3	b_p	c	D[1]	E[1]	e	H_E	L	L_p	v	w	y	Z[1]	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16
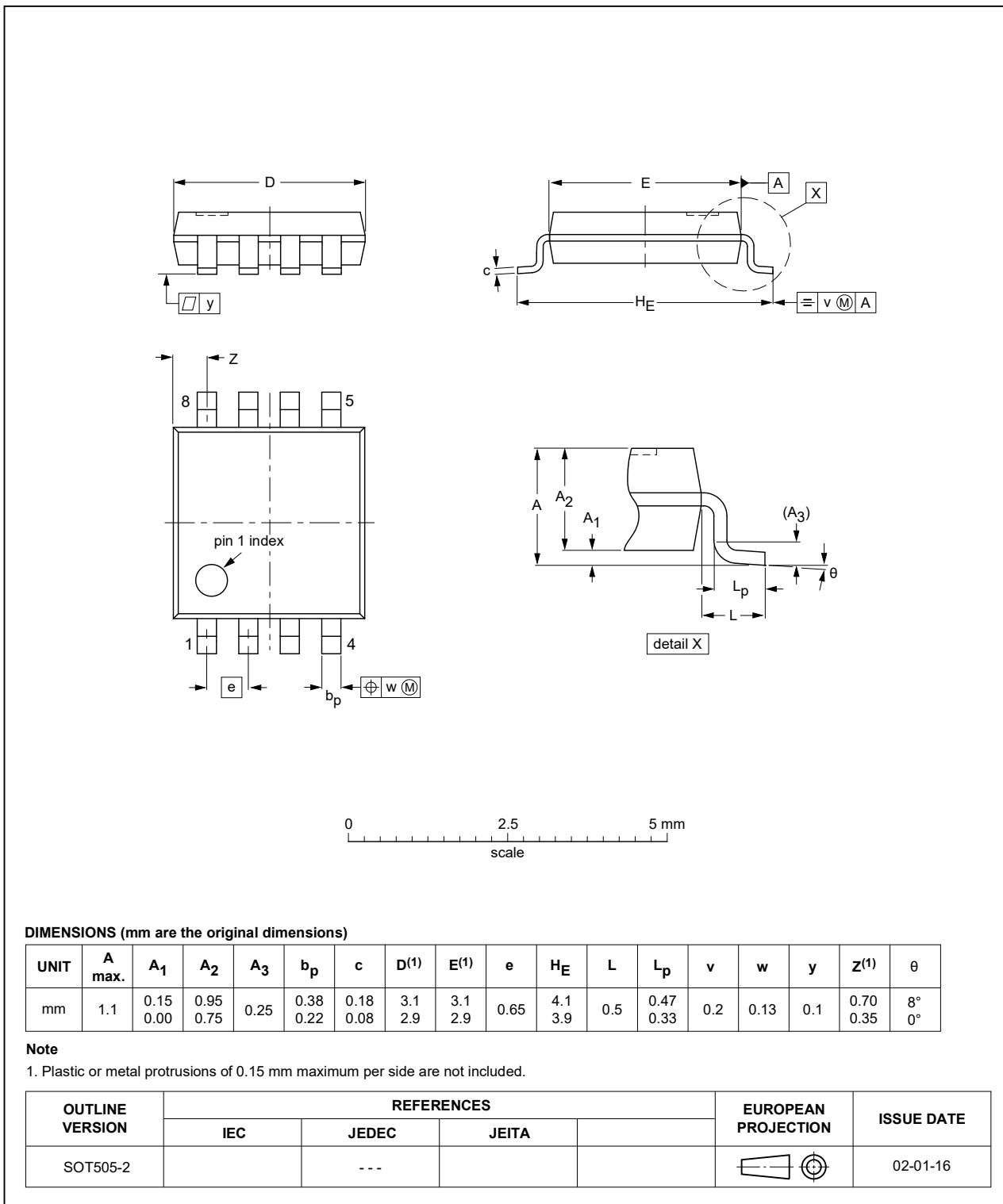
Fig. 6.   Package outline SOT505-2 (TSSOP8)

Triple inverter with open-drain output

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm　　　　**SOT765-1**

Dimensions (mm are the original dimensions)

Unit	A max.	A1	A2	A3	bp	c	D(1)	E(2)	e	HE	L	Lp	Q	v	w	y	Z(1)	θ
mm max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
nom	1			0.12					0.5		0.4			0.2	0.08	0.1		
min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19					0.1	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 7.　Package outline SOT765-1 (VSSOP8)

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XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm   SOT833-1

DIMENSIONS (mm are the original dimensions)

UNIT	A[1] max	A$_1$ max	b	D	E	e	e$_1$	L	L$_1$
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			07-11-14 07-12-07
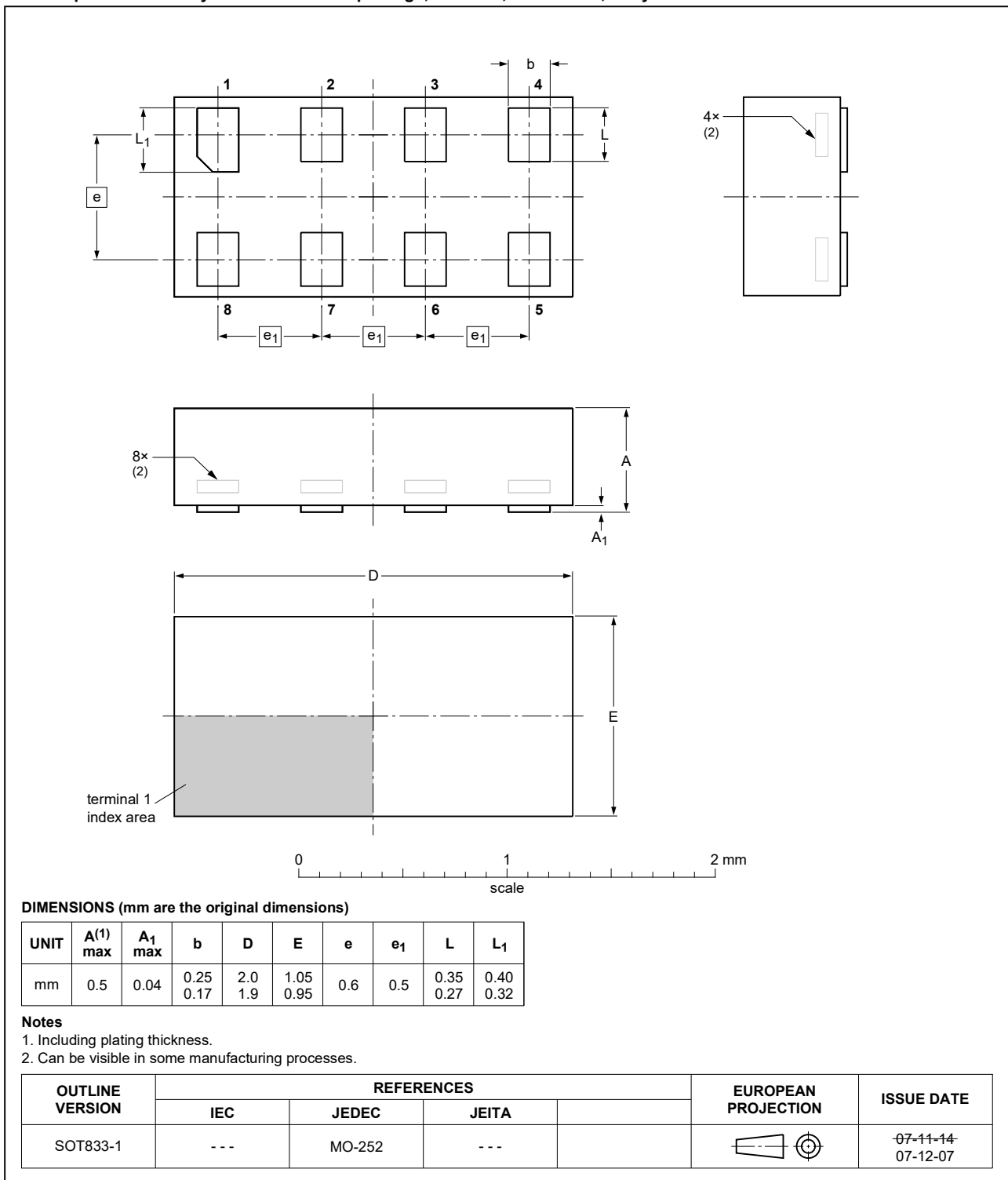
Fig. 8.   Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
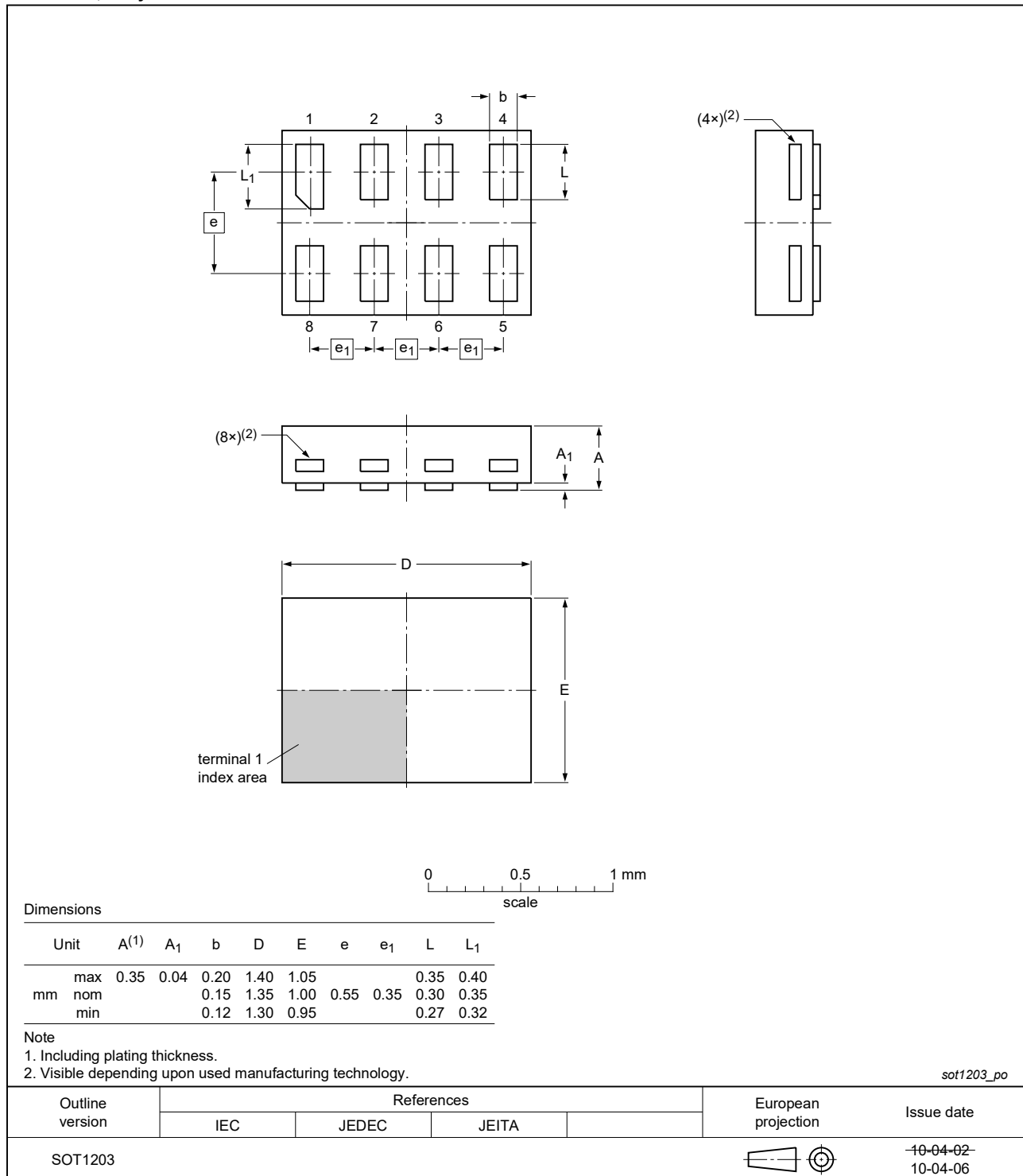**8 terminals; body 1.2 x 1.0 x 0.35 mm**

SOT1116

Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.25	1.05			0.35	0.40
	nom			0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min			0.12	1.15	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1116_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						~~10-04-02~~ 10-04-07
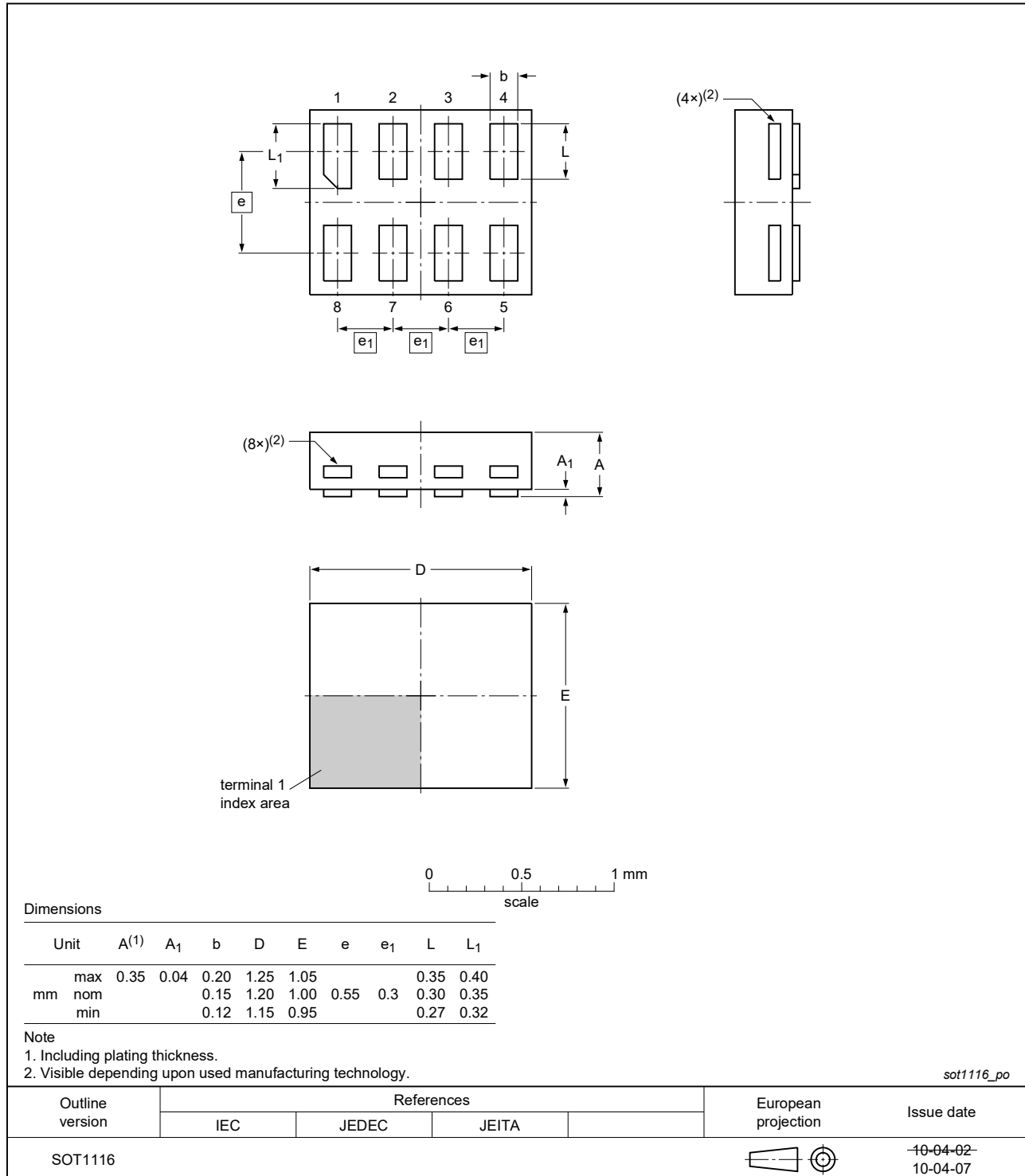
Fig. 9. Package outline SOT1116 (XSON8)

Triple inverter with open-drain output

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

Dimensions										
Unit	$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1	
mm max	0.35	0.04	0.20	1.40	1.05			0.35	0.40	
nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35	
min			0.12	1.30	0.95			0.27	0.32	

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						~~10-04-02~~ 10-04-06

Fig. 10. Package outline SOT1203 (XSON8)

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74LVC3G06

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC3G06 v.16	20230828	Product data sheet	-	74LVC3G06 v.15
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC3G06 v.15	20210420	Product data sheet	-	74LVC3G06 v.14
Modifications:	• Section 1 and Section 2 updated. • Type number 74LVC3G06GF (SOT1089 / XSON8) removed.			
74LVC3G06 v.14	20190731	Product data sheet	-	74LVC3G06 v.13
Modifications:	• Type number 74LVC3G06GM (SOT902-2) removed. • Table 5: Derating values for P_{tot} total power dissipation updated.			
74LVC3G06 v.13	20190206	Product data sheet	-	74LVC3G06 v.12
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74LVC3G06GD (SOT996-2) removed.			
74LVC3G06 v.12	20161215	Product data sheet	-	74LVC3G06 v.11
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC3G06 v.11	20130328	Product data sheet	-	74LVC3G06 v.10
Modifications:	• For type number 74LVC3G06GD XSON8U has changed to XSON8.			
74LVC3G06 v.10	20120627	Product data sheet	-	74LVC3G06 v.9
Modifications:	• For type number 74LVC3G06GM the SOT code has changed to SOT902-2.			
74LVC3G06 v.9	20111123	Product data sheet	-	74LVC3G06 v.8
Modifications:	• Legal pages updated.			
74LVC3G06 v.8	20100809	Product data sheet	-	74LVC3G06 v.7
74LVC3G06 v.7	20090312	Product data sheet	-	74LVC3G06 v.6
74LVC3G06 v.6	20080403	Product data sheet	-	74LVC3G06 v.5
74LVC3G06 v.5	20070521	Product data sheet	-	74LVC3G06 v.4
74LVC3G06 v.4	20060302	Product data sheet	-	74LVC3G06 v.3
74LVC3G06 v.3	20050201	Product data sheet	-	74LVC3G06 v.2
74LVC3G06 v.2	20041021	Product data sheet	-	74LVC3G06 v.1
74LVC3G06 v.1	20040607	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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