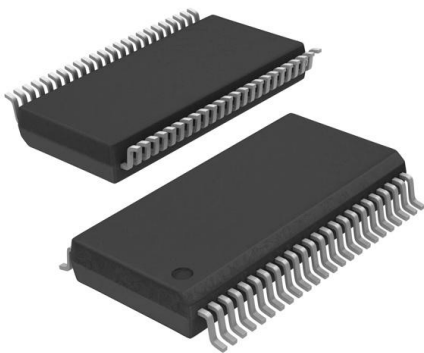


# 74LVT162240ADL,112 Datasheet

[www.digi-electronics.com](http://www.digi-electronics.com)



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	74LVT162240ADL,112-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	74LVT162240ADL,112
Description	IC BUFFER INVERT 3.6V 48SSOP
Detailed Description	Buffer, Inverting 4 Element 4 Bit per Element 3-Stat e Output 48-SSOP



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.

## Purchase and inquiry

Manufacturer Product Number:

74LVT162240ADL,112

Series:

74LVT

Logic Type:

Buffer, Inverting

Number of Bits per Element:

4

Output Type:

3-State

Voltage - Supply:

2.7V ~ 3.6V

Mounting Type:

Surface Mount

Supplier Device Package:

48-SSOP

Manufacturer:

Nexperia USA Inc.

Product Status:

Not For New Designs

Number of Elements:

4

Input Type:

-

Current - Output High, Low:

12mA, 12mA

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

48-BSSOP (0.295", 7.50mm Width)

Base Product Number:

74LVT162240

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



# 74LVT162240A

3.3 V 16-bit inverting buffer/driver with 30  $\Omega$  termination resistors; 3-state

Rev. 6 — 8 July 2024

Product data sheet

## 1. General description

The 74LVT162240A is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four output enable pins (1OE, 2OE, 3OE, 4OE), each controlling four of the 3-state outputs.

The 74LVT162240A is designed with 30  $\Omega$  series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

## 2. Features and benefits

- 16-bit bus interface
- 3-state buffers
- Output capability: +12 mA/–12 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30  $\Omega$  making external termination resistors unnecessary
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - JESD17: exceeds 500 mA
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74LVT162240ADGG</a>	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	<a href="#">SOT362-1</a>

## 4. Functional diagram

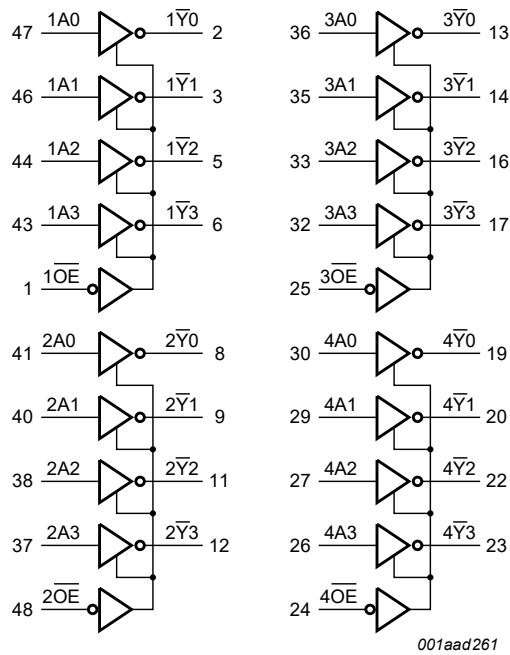


Fig. 1. Logic symbol

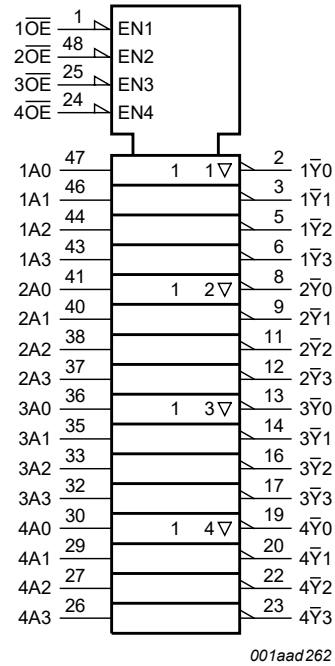


Fig. 2. IEC logic symbol

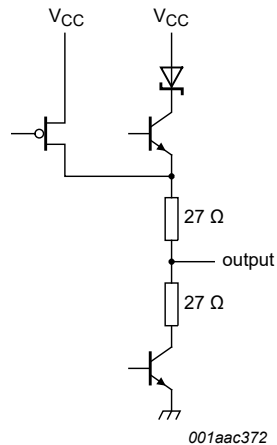
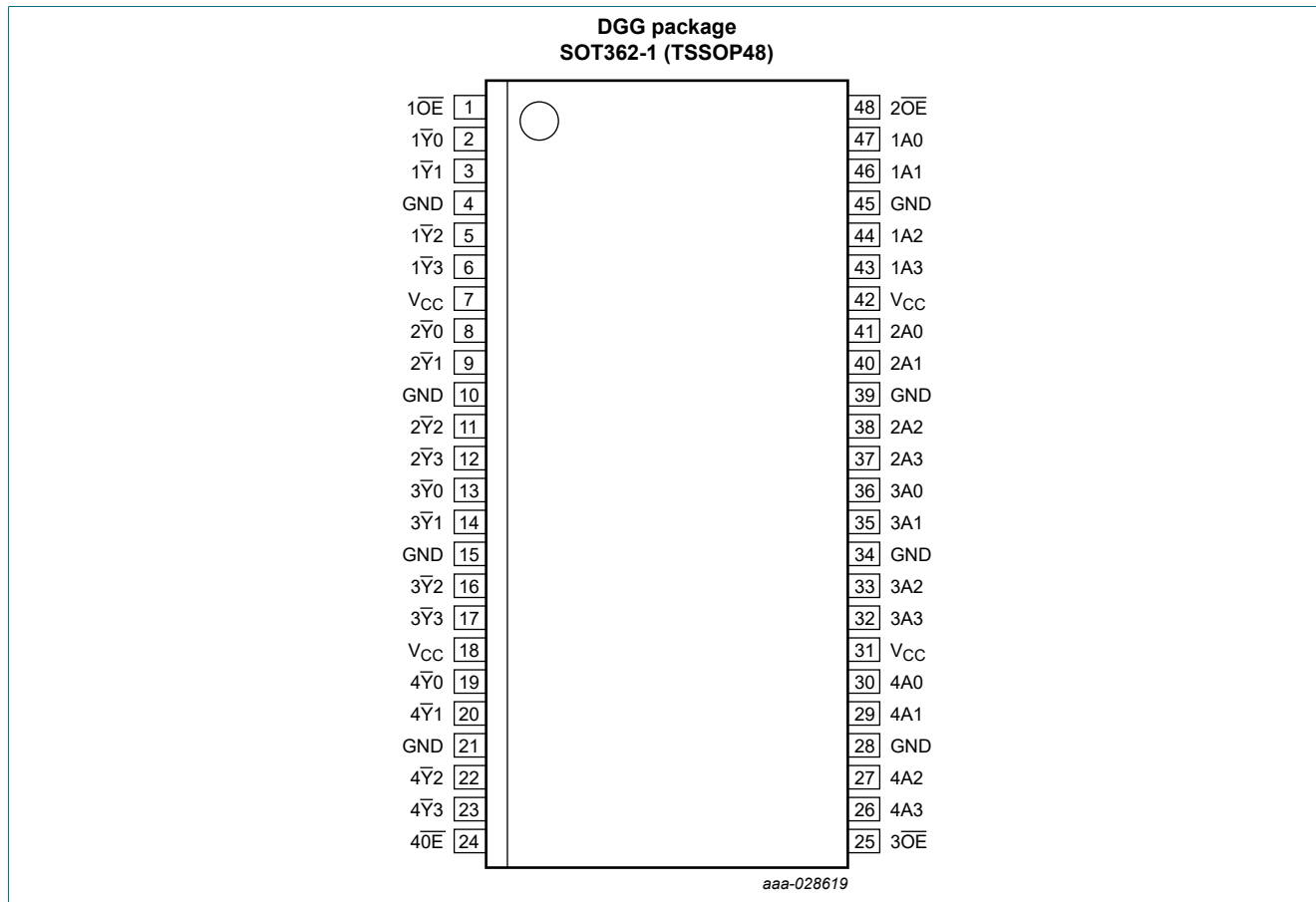


Fig. 3. Schematic of one output

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

**Table 2. Pin description**

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 48, 25, 24	output enable inputs (active LOW)
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data inputs
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data inputs
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data inputs
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data inputs
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data outputs
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data outputs
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data outputs
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Input		Output
nOE	nAn	nYn
L	L	H
L	H	L
H	X	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage		[1] -0.5	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
$T_{stg}$	storage temperature		-65	+150	$^{\circ}$ C
$T_j$	junction temperature		[2] -	+150	$^{\circ}$ C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.7	-	3.6	V
$V_I$	input voltage		0	-	5.5	V
$I_{OH}$	HIGH-level output current		-	-	-12	mA
$I_{OL}$	LOW-level output current		-	-	12	mA
$T_{amb}$	ambient temperature	in free air	-40	-	+85	$^{\circ}$ C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{IK}$	input clamping voltage	$V_{CC} = 2.7 \text{ V}$ ; $I_{IK} = -18 \text{ mA}$	-	-0.85	-1.2	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 3.0 \text{ V}$ ; $I_{OH} = -12 \text{ mA}$	2.0	-	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 3.0 \text{ V}$ ; $I_{OL} = 12 \text{ mA}$	-	-	0.8	V
$I_I$	input leakage current	all input pins				
		$V_{CC} = 0 \text{ V}$ or $3.6 \text{ V}$ ; $V_I = 5.5 \text{ V}$	-	0.4	10	$\mu\text{A}$
		control pins				
		$V_{CC} = 3.6 \text{ V}$ ; $V_I = V_{CC}$ or GND	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		data pins				
		$V_{CC} = 3.6 \text{ V}$ ; $V_I = V_{CC}$ [2]	-	0.1	1	$\mu\text{A}$
		$V_{CC} = 3.6 \text{ V}$ ; $V_I = 0 \text{ V}$ [2]	-	-0.4	-5	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0 \text{ V}$ ; $V_I$ or $V_O = 0 \text{ V}$ to $4.5 \text{ V}$	-	0.1	$\pm 100$	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	nAn input; $V_{CC} = 3 \text{ V}$ ; $V_I = 0.8 \text{ V}$	75	135	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	nAn input; $V_{CC} = 3 \text{ V}$ ; $V_I = 2.0 \text{ V}$	-75	-135	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	nAn input; $V_{CC} = 3.6 \text{ V}$ ; $V_I = 0 \text{ V}$ to $3.6 \text{ V}$ [3]	500	-	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	nAn input; $V_{CC} = 3.6 \text{ V}$ ; $V_I = 0 \text{ V}$ to $3.6 \text{ V}$ [3]	-	-	-500	$\mu\text{A}$
$I_{EX}$	external current	output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5 \text{ V}$ ; $V_{CC} = 3.0 \text{ V}$	-	50	125	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2 \text{ V}$ ; $V_O = 0.5 \text{ V}$ to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; n $\overline{\text{OE}}$ = don't care [4]	-	1	$\pm 100$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_{CC} = 3.6 \text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$				
		output HIGH: $V_O = 3.0 \text{ V}$	-	0.5	5	$\mu\text{A}$
		output LOW: $V_O = 0.5 \text{ V}$	-	0.5	-5	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 3.6 \text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $I_O = 0 \text{ A}$				
		outputs HIGH	-	0.07	0.12	mA
		outputs LOW	-	4.0	6	mA
		outputs disabled [5]	-	0.07	0.12	mA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 3 \text{ V}$ to $3.6 \text{ V}$ ; one input at $V_{CC} - 0.6 \text{ V}$ and other inputs at $V_{CC}$ or GND [6]	-	0.1	0.2	mA
$C_I$	input capacitance	n $\overline{\text{OE}}$ ; $V_I = 0 \text{ V}$ or $3 \text{ V}$	-	3	-	pF
$C_O$	output capacitance	$V_O = 0 \text{ V}$ or $3.0 \text{ V}$	-	9	-	pF

[1] All typical values are at  $V_{CC} = 3.3 \text{ V}$  (unless stated otherwise) and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

[2] Unused pins at  $V_{CC}$  or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2 \text{ V}$  to  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  a transition time of 100  $\mu\text{s}$  is permitted. This parameter is valid for  $T_{amb} = 25 \text{ }^\circ\text{C}$  only.

[5] Measured with outputs pulled up to  $V_{CC}$  or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 10. Dynamic characteristics

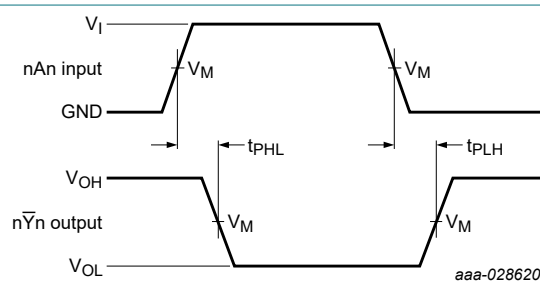
**Table 7. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$t_{PLH}$	LOW to HIGH propagation delay	$nAn$ to $n\bar{Y}n$ ; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	5.0	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.5	2.6	4.2	ns
$t_{PHL}$	HIGH to LOW propagation delay	$nAn$ to $n\bar{Y}n$ ; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	5.0	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.5	2.6	4.2	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	$n\bar{OE}$ to $n\bar{Y}n$ ; see Fig. 5				
		$V_{CC} = 2.7\text{ V}$	-	-	6.5	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.3	5.5	ns
$t_{PZL}$	OFF-state to LOW propagation delay	$n\bar{OE}$ to $n\bar{Y}n$ ; see Fig. 5				
		$V_{CC} = 2.7\text{ V}$	-	-	5.5	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.0	5.0	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	$n\bar{OE}$ to $n\bar{Y}n$ ; see Fig. 5				
		$V_{CC} = 2.7\text{ V}$	-	-	5.5	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.5	5.0	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	$n\bar{OE}$ to $n\bar{Y}n$ ; see Fig. 5				
		$V_{CC} = 2.7\text{ V}$	-	-	4.5	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.2	4.5	ns

[1] Typical values are at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

### 10.1. Waveforms and test circuit



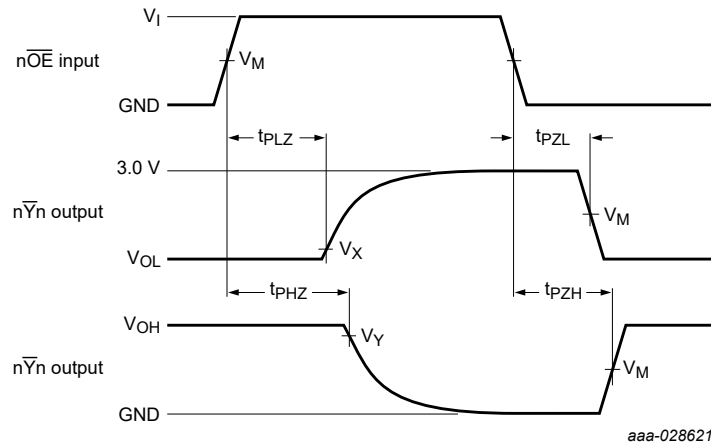
Measurement points are given in Table 8.

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 4. Input ( $nAn$ ) to output ( $n\bar{Y}n$ ) propagation delay**



## 3.3 V 16-bit inverting buffer/driver with 30 Ω termination resistors; 3-state



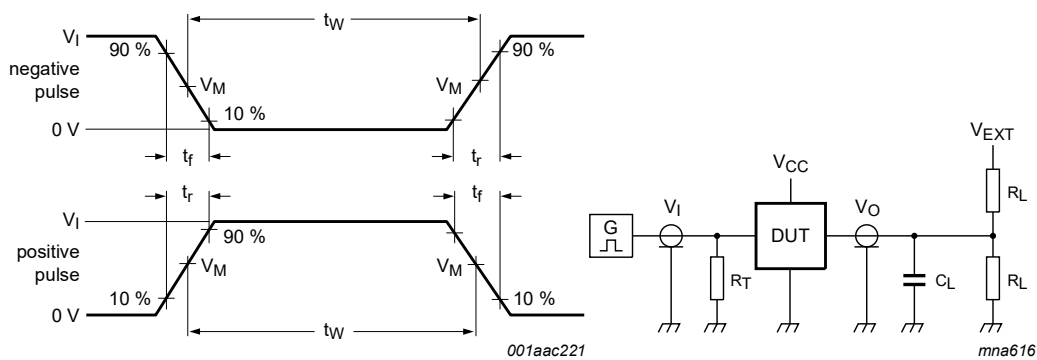
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 5. Enable and disable times of 3-state outputs**

**Table 8. Measurement points**

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = Test voltage for switching times.

**Fig. 6. Test circuit for measuring switching times**

**Table 9. Test data**

Input				Load		$V_{EXT}$		
$V_i$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 Ω	GND	6 V	open

## 11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

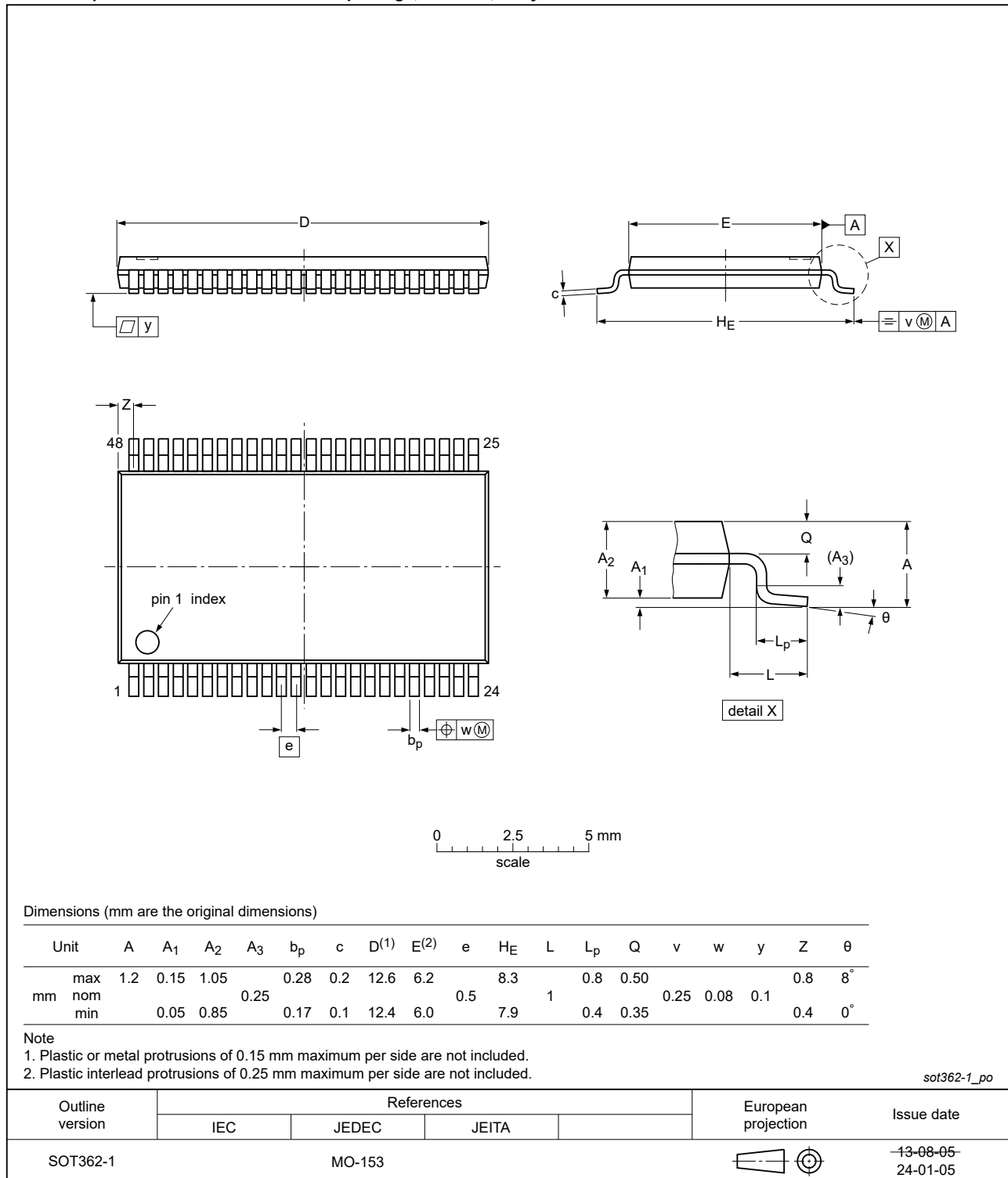


Fig. 7. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT162240A v.6	20240708	Product data sheet	-	74LVT162240A v.5
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74LVT162240A v.5	20240201	Product data sheet	-	74LVT162240A v.4
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Fig. 7</a>: Updated package outline drawing SOT362-1 (TSSOP48).</li> </ul>			
74LVT162240A v.4	20180604	Product data sheet	-	74LVT162240A v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74LVT162240ADL (SSOP48 / SOT370-1) removed.</li> </ul>			
74LVT162240A v.3	20030221	Product data sheet	ECN 853-1777 29438	74LVT162240A v.2
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 1</a> corrected: removed 'North America' column.</li> <li><a href="#">Fig. 2</a> modified to correct pin names</li> </ul>			
74LVT162240A v.2	19980219	Product specification	ECN 853-1777 18990	74LVT162240A v.1
74LVT162240A v.1	19950822	Product specification	-	-

3.3 V 16-bit inverting buffer/driver with 30  $\Omega$  termination resistors; 3-state

## 14. Legal information

## Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

## Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

**Right to make changes** — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## Contents

---

<b>1. General description</b> .....	<b>1</b>
<b>2. Features and benefits</b> .....	<b>1</b>
<b>3. Ordering information</b> .....	<b>1</b>
<b>4. Functional diagram</b> .....	<b>2</b>
<b>5. Pinning information</b> .....	<b>3</b>
5.1. Pinning.....	3
5.2. Pin description.....	3
<b>6. Functional description</b> .....	<b>4</b>
<b>7. Limiting values</b> .....	<b>4</b>
<b>8. Recommended operating conditions</b> .....	<b>4</b>
<b>9. Static characteristics</b> .....	<b>5</b>
<b>10. Dynamic characteristics</b> .....	<b>6</b>
10.1. Waveforms and test circuit.....	6
<b>11. Package outline</b> .....	<b>8</b>
<b>12. Abbreviations</b> .....	<b>9</b>
<b>13. Revision history</b> .....	<b>9</b>
<b>14. Legal information</b> .....	<b>10</b>

---

© Nexperia B.V. 2024. All rights reserved

For more information, please visit: <http://www.nexperia.com>  
 For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)  
 Date of release: 8 July 2024

---

## OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we stricly control the quality of products and services. Welcome your RFQ to

Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.