

# BSH203,215 Datasheet



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DiGi Electronics Part Number	BSH203,215-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	BSH203,215
Description	MOSFET P-CH 30V 470MA TO236AB
Detailed Description	P-Channel 30 V 470mA (Ta) 417mW (Ta) Surface Mount TO-236AB



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

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## Purchase and inquiry

**Manufacturer Product Number:**

BSH203,215

**Series:**

-

**FET Type:**

P-Channel

**Drain to Source Voltage (Vdss):**

30 V

**Drive Voltage (Max Rds On, Min Rds On):**

1.8V, 4.5V

**Vgs(th) (Max) @ Id:**

680mV @ 1mA (Typ)

**Vgs (Max):**

±8V

**FET Feature:**

-

**Operating Temperature:**

-55°C ~ 150°C (Tj)

**Supplier Device Package:**

TO-236AB

**Base Product Number:**

BSH203

**Manufacturer:**

Nexperia USA Inc.

**Product Status:**

Not For New Designs

**Technology:**

MOSFET (Metal Oxide)

**Current - Continuous Drain (Id) @ 25°C:**

470mA (Ta)

**Rds On (Max) @ Id, Vgs:**

900mOhm @ 280mA, 4.5V

**Gate Charge (Qg) (Max) @ Vgs:**

2.2 nC @ 4.5 V

**Input Capacitance (Ciss) (Max) @ Vds:**

110 pF @ 24 V

**Power Dissipation (Max):**

417mW (Ta)

**Mounting Type:**

Surface Mount

**Package / Case:**

TO-236-3, SC-59, SOT-23-3

## Environmental & Export classification

**RoHS Status:**

ROHS3 Compliant

**REACH Status:**

REACH Unaffected

**HTSUS:**

8541.21.0095

**Moisture Sensitivity Level (MSL):**

1 (Unlimited)

**ECCN:**

EAR99

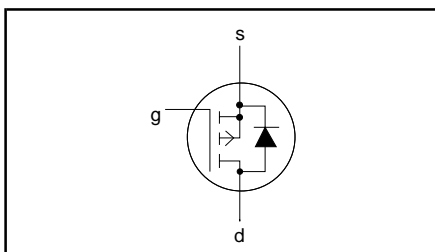
**P-channel enhancement mode  
MOS transistor**

**BSH203**

**FEATURES**

- Very low threshold voltage
- Fast switching
- Logic level compatible
- Subminiature surface mount package

**SYMBOL**



**QUICK REFERENCE DATA**

$V_{DS} = -30\text{ V}$
$I_D = -0.47\text{ A}$
$R_{DS(ON)} \leq 1.1\ \Omega (V_{GS} = -2.5\text{ V})$
$V_{GS(TO)} \geq 0.4\text{ V}$

**GENERAL DESCRIPTION**

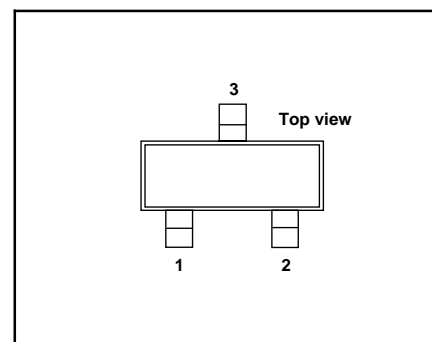
P-channel, enhancement mode, logic level, field-effect power transistor. This device has low threshold voltage and extremely fast switching making it ideal for battery powered applications and high speed digital interfacing.

The BSH203 is supplied in the SOT23 subminiature surface mounting package.

**PINNING**

PIN	DESCRIPTION
1	gate
2	source
3	drain

**SOT23**



**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage		-	-30	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	-30	V
$V_{GS}$	Gate-source voltage		-	$\pm 8$	V
$I_D$	Drain current (DC)	$T_a = 25\text{ }^\circ\text{C}$	-	-0.47	A
		$T_a = 100\text{ }^\circ\text{C}$	-	-0.3	A
$I_{DM}$	Drain current (pulse peak value)	$T_a = 25\text{ }^\circ\text{C}$	-	-1.9	A
$P_{tot}$	Total power dissipation	$T_a = 25\text{ }^\circ\text{C}$	-	0.417	W
		$T_a = 100\text{ }^\circ\text{C}$	-	0.17	W
$T_{stg}, T_j$	Storage & operating temperature		- 55	150	$^\circ\text{C}$

**THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint	300	-	K/W

## P-channel enhancement mode MOS transistor

BSH203

### ELECTRICAL CHARACTERISTICS

T<sub>j</sub> = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = -10 μA	-30	-	-	V	
V <sub>GS(TO)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = -1 mA	-0.4	-0.68	-	V	
R <sub>DS(ON)</sub>	Drain-source on-state resistance	T <sub>j</sub> = 150 °C	V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -280 mA	-0.1	-	-	V
			V <sub>GS</sub> = -2.5 V; I <sub>D</sub> = -280 mA	-	0.66	0.9	Ω
			V <sub>GS</sub> = -1.8 V; I <sub>D</sub> = -140 mA	-	0.92	1.1	Ω
			V <sub>GS</sub> = -2.5 V; I <sub>D</sub> = -280 mA; T <sub>j</sub> = 150 °C	-	1.1	1.2	Ω
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = -24 V; I <sub>D</sub> = -280 mA	-	1.4	1.65	Ω	
I <sub>GSS</sub>	Gate source leakage current	V <sub>GS</sub> = ±8 V; V <sub>DS</sub> = 0 V	0.3	1.0	-	S	
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>DS</sub> = -24 V; V <sub>GS</sub> = 0 V;	-	±10	±100	nA	
		T <sub>j</sub> = 150 °C	-	-50	-100	nA	
			-	-1.3	-10	μA	
Q <sub>g(tot)</sub>	Total gate charge	I <sub>D</sub> = -0.5 A; V <sub>DD</sub> = -10 V; V <sub>GS</sub> = -4.5 V	-	2.2	-	nC	
Q <sub>gs</sub>	Gate-source charge		-	0.4	-	nC	
Q <sub>gd</sub>	Gate-drain (Miller) charge		-	0.25	-	nC	
t <sub>d on</sub>	Turn-on delay time	V <sub>DD</sub> = -10 V; I <sub>D</sub> = -0.5 A;	-	2	-	ns	
t <sub>r</sub>	Turn-on rise time	V <sub>GS</sub> = -8 V; R <sub>G</sub> = 6 Ω	-	4.5	-	ns	
t <sub>d off</sub>	Turn-off delay time	Resistive load	-	45	-	ns	
t <sub>f</sub>	Turn-off fall time		-	20	-	ns	
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = -24 V; f = 1 MHz	-	110	-	pF	
C <sub>oss</sub>	Output capacitance		-	27	-	pF	
C <sub>rss</sub>	Feedback capacitance		-	7	-	pF	

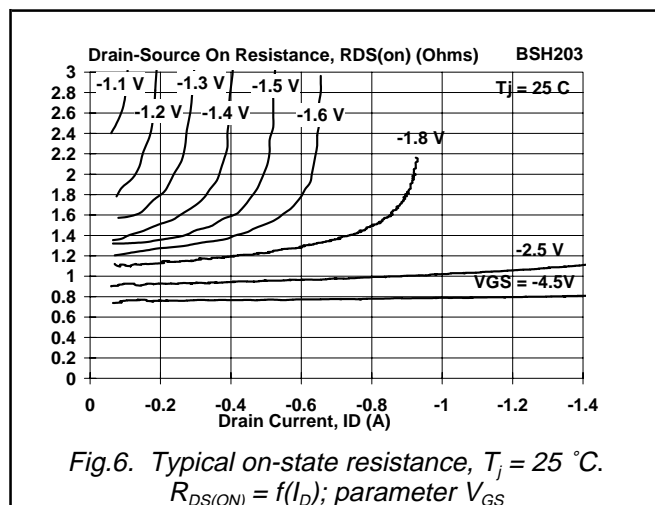
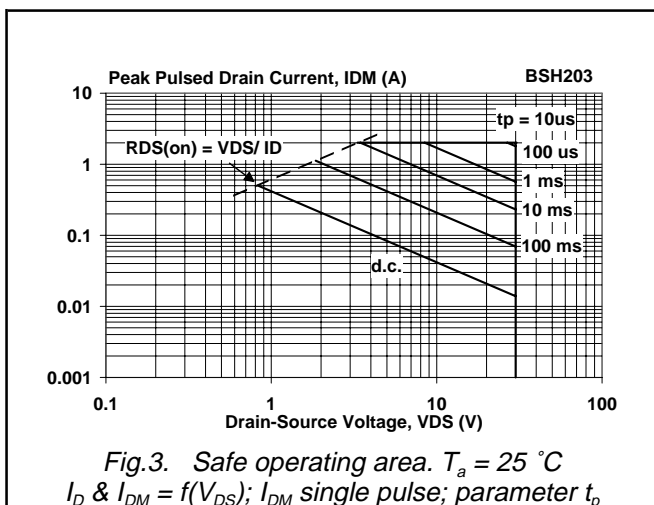
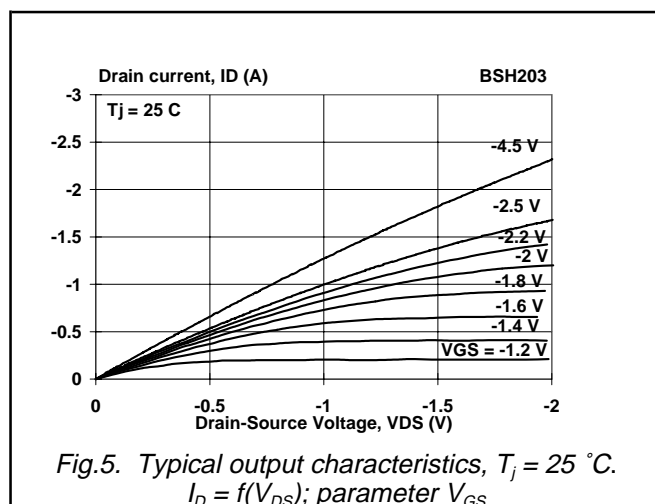
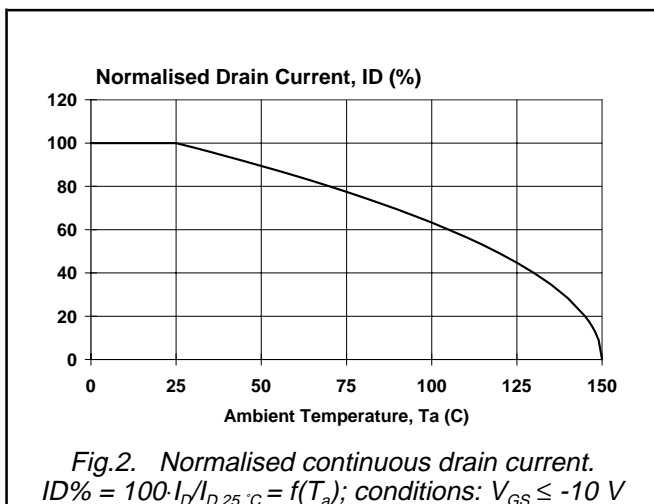
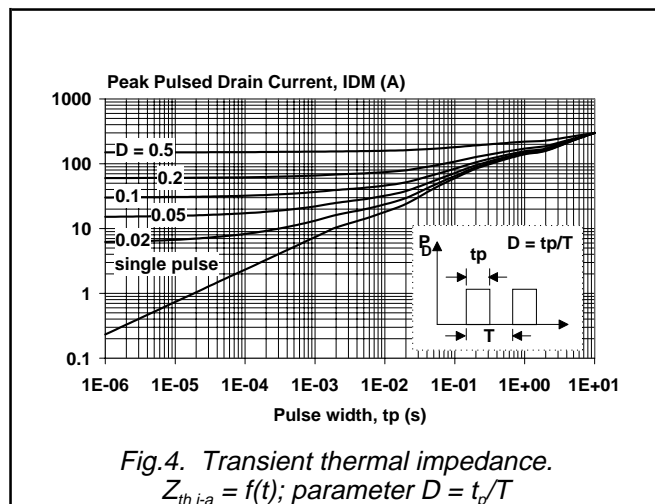
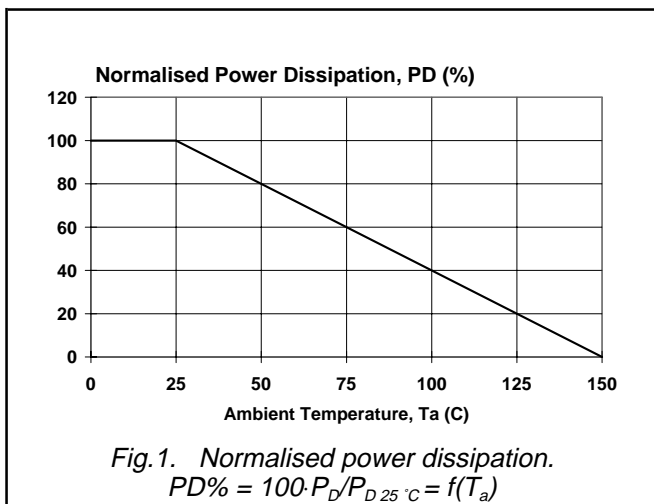
### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T<sub>j</sub> = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>DR</sub>	Continuous reverse drain current	T <sub>a</sub> = 25 °C	-	-	-0.47	A
I <sub>DRM</sub>	Pulsed reverse drain current		-	-	-1.9	A
V <sub>SD</sub>	Diode forward voltage	I <sub>F</sub> = -0.38 A; V <sub>GS</sub> = 0 V	-	-0.87	-1.3	V
t <sub>rr</sub>	Reverse recovery time	I <sub>F</sub> = -0.5 A; -dI <sub>F</sub> /dt = 100 A/μs;	-	27	-	ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>GS</sub> = 0 V; V <sub>R</sub> = -24 V	-	28	-	nC

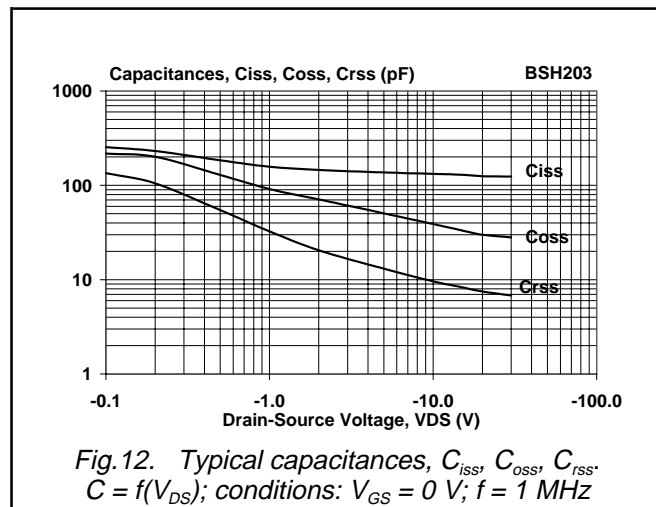
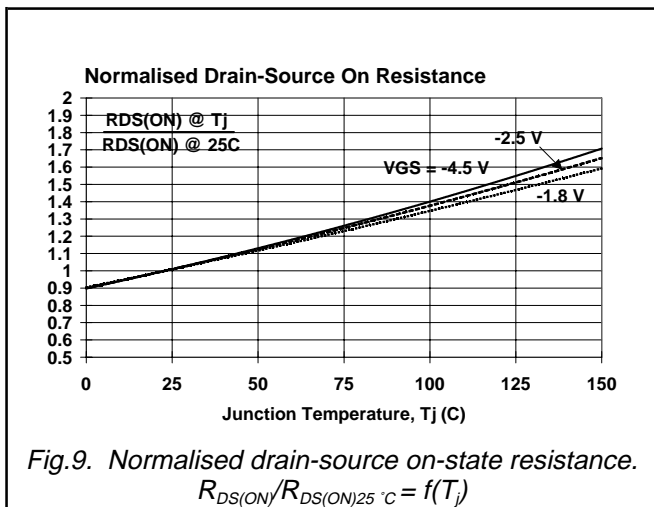
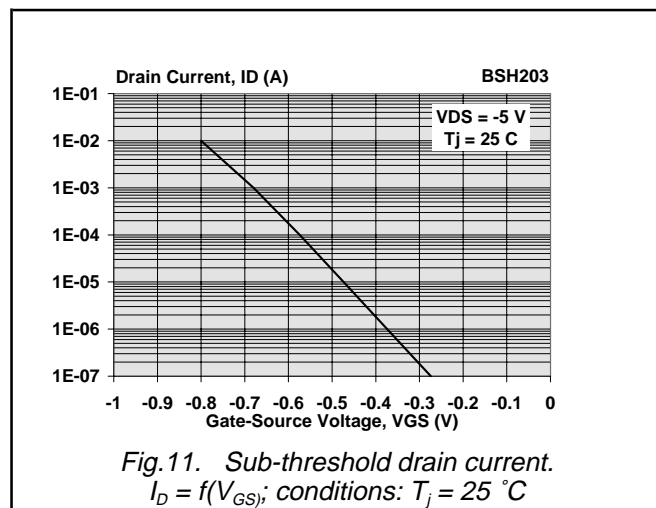
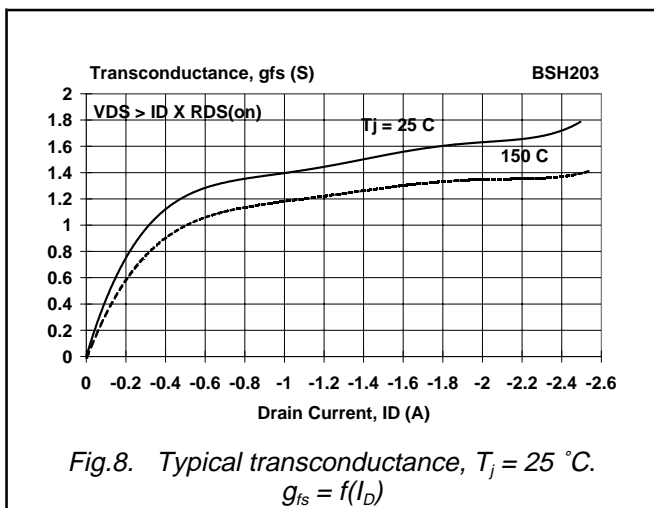
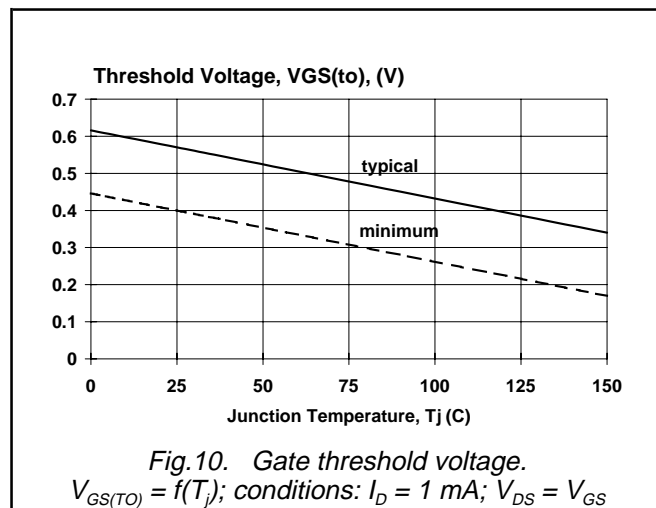
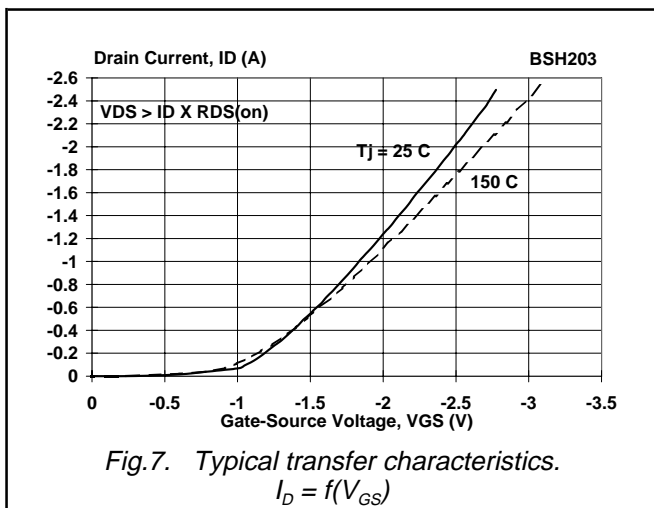
P-channel enhancement mode MOS transistor

BSH203



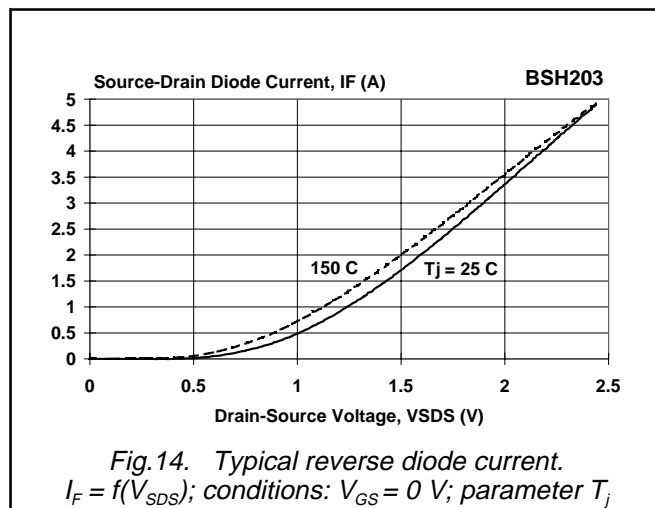
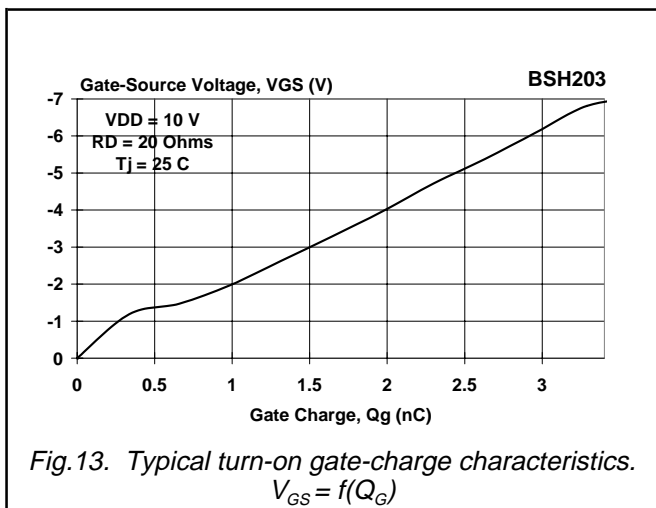
P-channel enhancement mode MOS transistor

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P-channel enhancement mode  
MOS transistor

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P-channel enhancement mode  
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MECHANICAL DATA

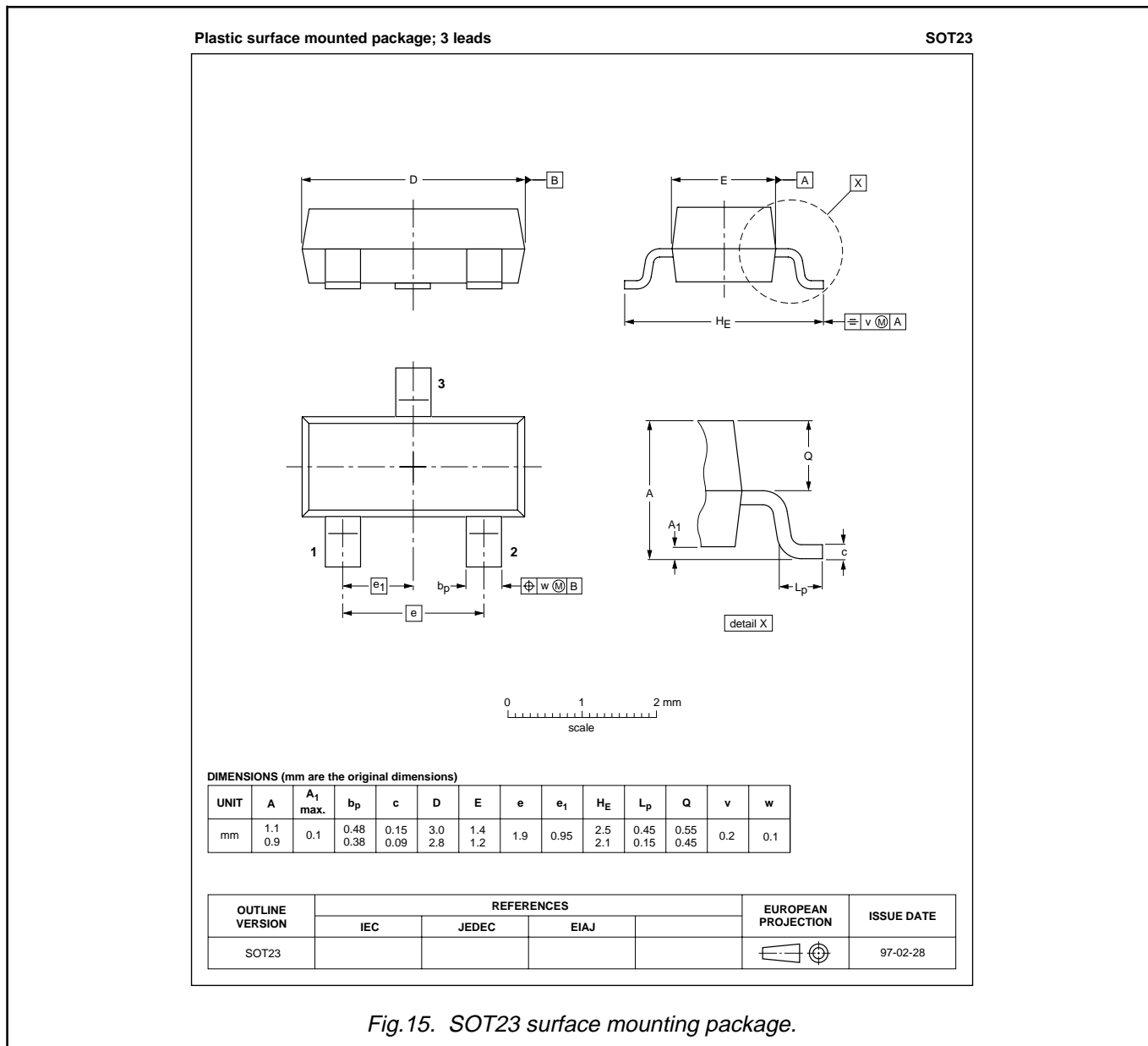


Fig.15. SOT23 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".



## P-channel enhancement mode MOS transistor

BSH203

### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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