BSS84AKW-BX Datasheet

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DiGi Electronics Part Number	BSS84AKW-BX-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	BSS84AKW-BX
Description	MOSFET P-CHANNEL 50V 150MA SC70
Detailed Description	P-Channel 50 V 150mA (Ta) 830mW (Tc) Surface Mount SOT-323

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
BSS84AKW-BX	Nexperia USA Inc.
Series:	Product Status:
-	Obsolete
FET Type:	Technology:
P-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
50 V	150mA (Ta)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
5V, 10V	7.5Ohm @ 100mA, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
2.1V @ 250µA	0.35 nC @ 5 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	36 pF @ 25 V
FET Feature:	Power Dissipation (Max):
-	830mW (Tc)
Operating Temperature:	Grade:
-55°C ~ 150°C (TJ)	Automotive
Qualification:	Mounting Type:
AEC-Q101	Surface Mount
Supplier Device Package:	Package / Case:
SOT-323	SC-70, SOT-323

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.21.0095	

BSS84AKW

50 V, 150 mA P-channel Trench MOSFET

Rev. 1 — 23 May 2011 Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 1 kV
- AEC-Q101 qualified

1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

1.4 Quick reference data

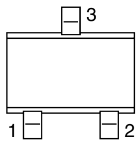
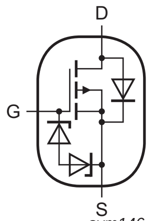
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C	-	-	-50	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	V_{GS} = -10 V; T_{amb} = 25 °C [1]	-	-	-150	mA
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -100 mA; T_j = 25 °C	-	4.5	7.5	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT323 (SC-70)	
2	S	source		
3	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BSS84AKW	SC-70	plastic surface-mounted package; 3 leads	SOT323

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
BSS84AKW	%VT

[1] % = placeholder for manufacturing site code

5. Limiting values

Table 5. Limiting values

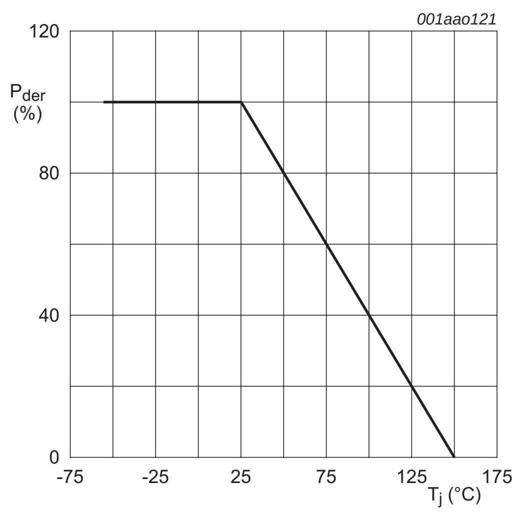
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-50	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = -10 V; T_{amb} = 25 °C	[1]	-	-150	mA
		V_{GS} = -10 V; T_{amb} = 100 °C	[1]	-	-95	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	260	mW
			[1]	-	310	mW
		T_{sp} = 25 °C		-	830	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-150	mA
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	1000	V

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

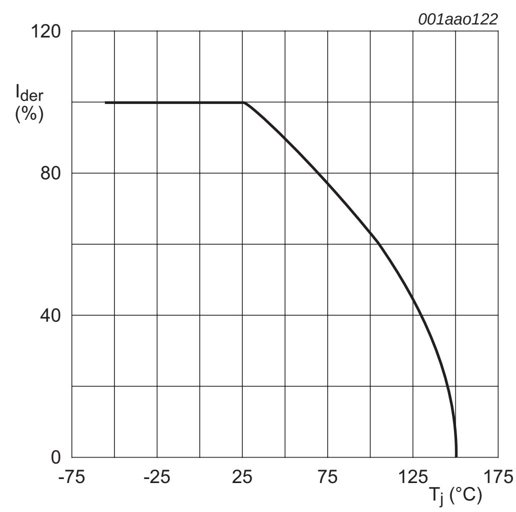
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



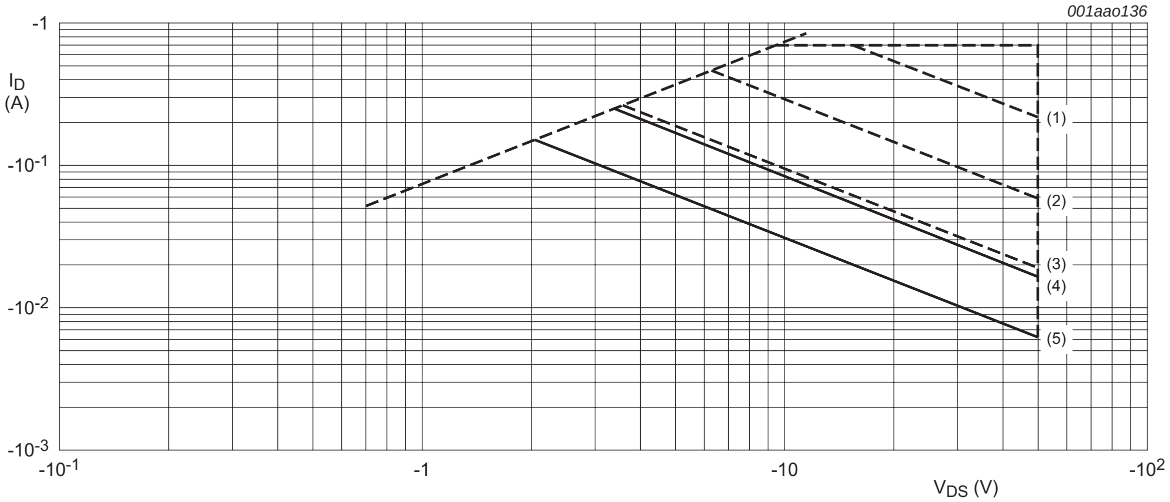
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} is single pulse

(1) t_p = 1 ms

(2) t_p = 10 ms

(3) t_p = 100 ms

(4) DC; T_{sp} = 25 °C

(5) DC; T_{amb} = 25 °C; drain mounting pad 1 cm^2

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

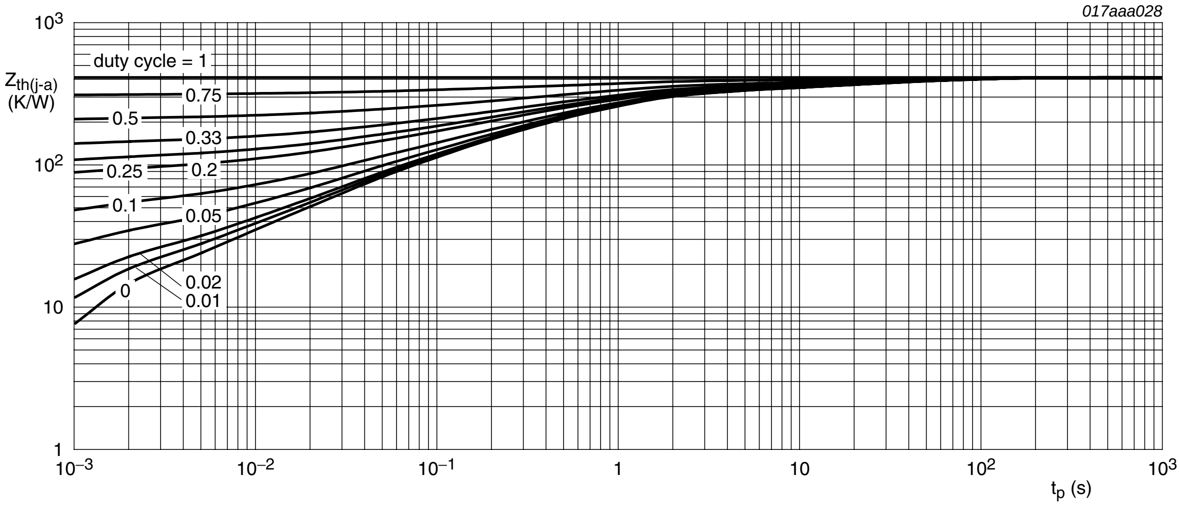
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	415	480	K/W
			[2]	-	350	400	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	150	K/W

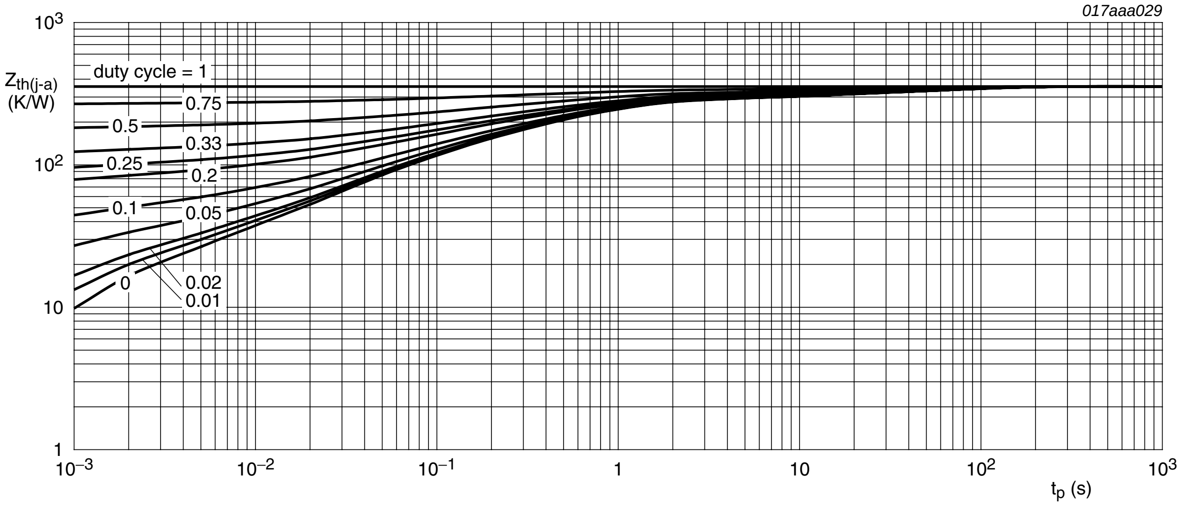
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2.



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



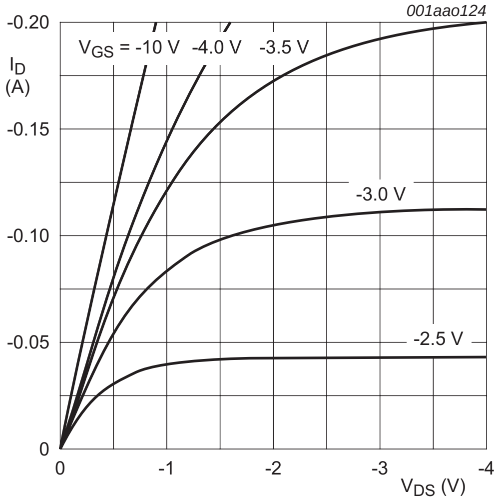
FR4 PCB, mounting pad for drain 1 cm^2

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

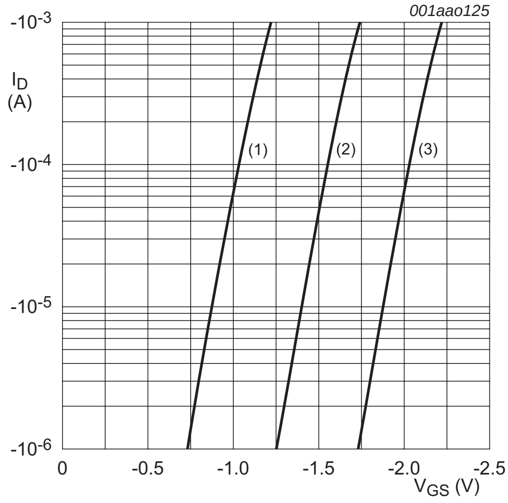
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -10 µA; V_{GS} = 0 V; T_j = 25 °C	-50	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS}; T_j = 25 °C	-1.1	-1.6	-2.1	V
I_{DSS}	drain leakage current	V_{DS} = -50 V; V_{GS} = 0 V; T_j = 25 °C	-	-	-1	µA
		V_{DS} = -50 V; V_{GS} = 0 V; T_j = 150 °C	-	-	-2	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-10	µA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-10	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -100 mA; T_j = 25 °C	-	4.5	7.5	Ω
		V_{GS} = -10 V; I_D = -100 mA; T_j = 150 °C	-	8	13.5	Ω
		V_{GS} = -5 V; I_D = -100 mA; T_j = 25 °C	-	5.7	8.5	Ω
g_{fs}	forward transconductance	V_{DS} = -10 V; I_D = -100 mA; T_j = 25 °C	-	150	-	mS
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	V_{DS} = -25 V; I_D = -200 mA; V_{GS} = -5 V; T_j = 25 °C	-	0.26	0.35	nC
Q_{GS}	gate-source charge		-	0.12	-	nC
Q_{GD}	gate-drain charge		-	0.09	-	nC
C_{iss}	input capacitance	V_{DS} = -25 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	24	36	pF
C_{oss}	output capacitance		-	4.5	-	pF
C_{rss}	reverse transfer capacitance		-	1.3	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -30 V; R_L = 250 Ω; V_{GS} = -10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	13	26	ns
t_r	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	48	96	ns
t_f	fall time		-	25	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = -115 mA; V_{GS} = 0 V; T_j = 25 °C	-0.48	-0.85	-1.2	V



T_j = 25 °C

Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values



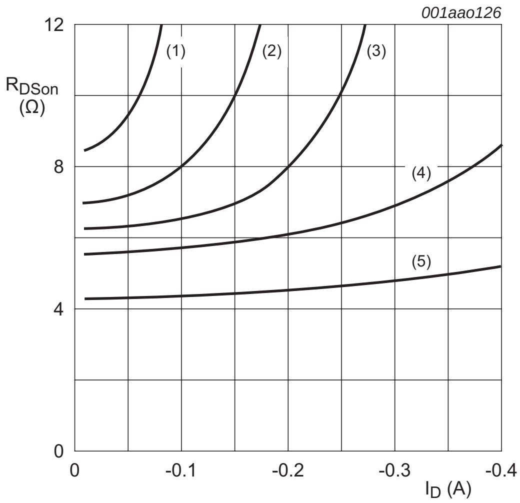
T_j = 25 °C; V_{DS} = -5 V

(1) minimum values

(2) typical values

(3) maximum values

Fig 7. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

(1) V_{GS} = -3.0 V

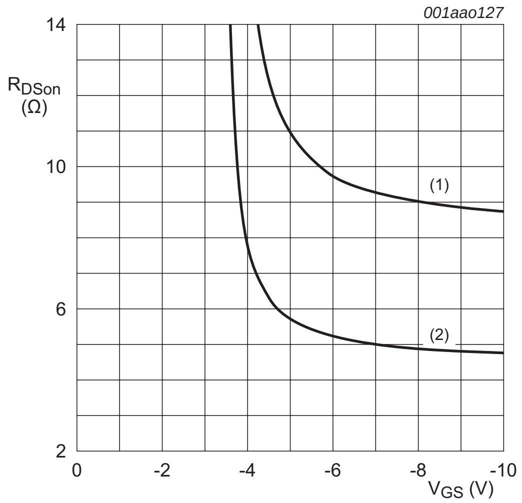
(2) V_{GS} = -3.5 V

(3) V_{GS} = -4.0 V

(4) V_{GS} = -5.0 V

(5) V_{GS} = -10.0 V

Fig 8. Drain-source on-state resistance as a function of drain current; typical values

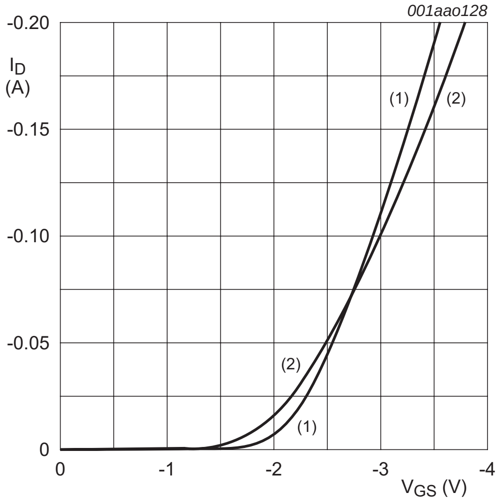


I_D = -200 mA

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

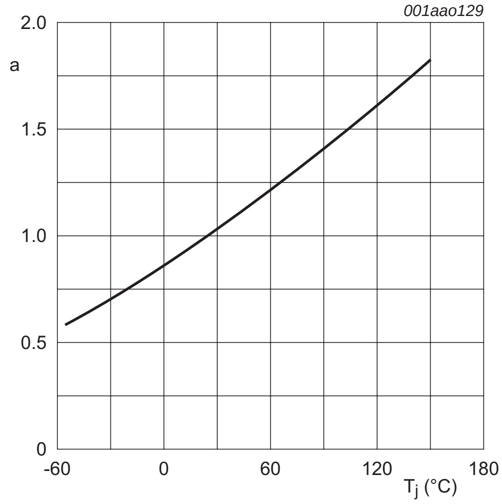


$V_{DS} > I_D \times R_{DSon}$

(1) T_j = 25 °C

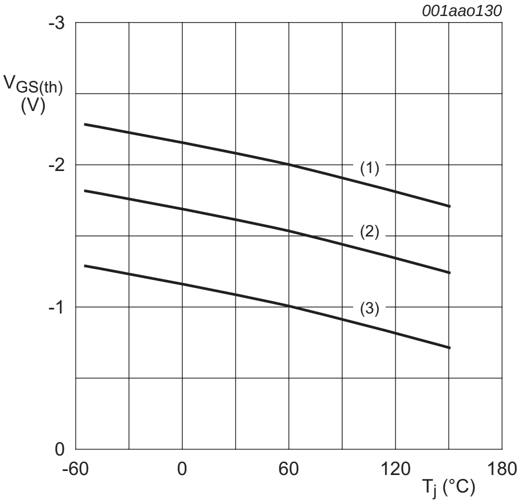
(2) T_j = 150 °C

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



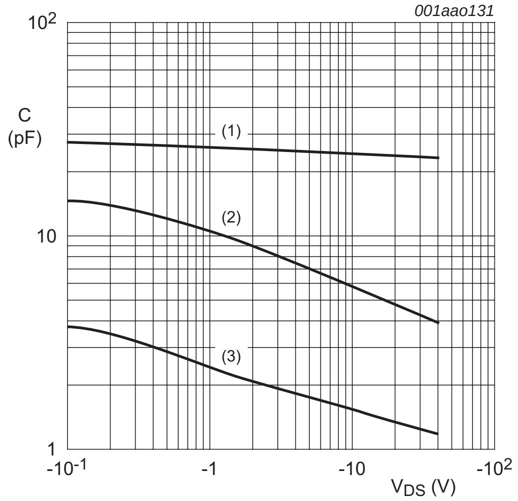
I_D = -0.25 mA; $V_{DS} = V_{GS}$

(1) maximum values

(2) typical values

(3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



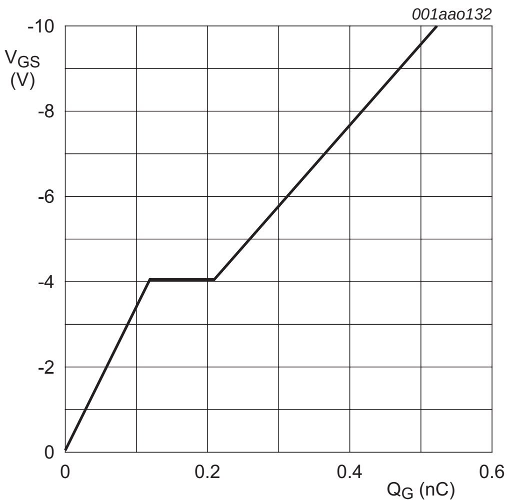
f = 1 MHz, V_{GS} = 0 V

(1) C_{iss}

(2) C_{oss}

(3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = -0.2 A; V_{DS} = -25 V; T_{amb} = 25 °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

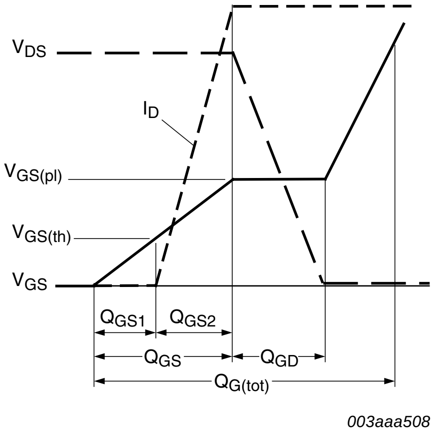
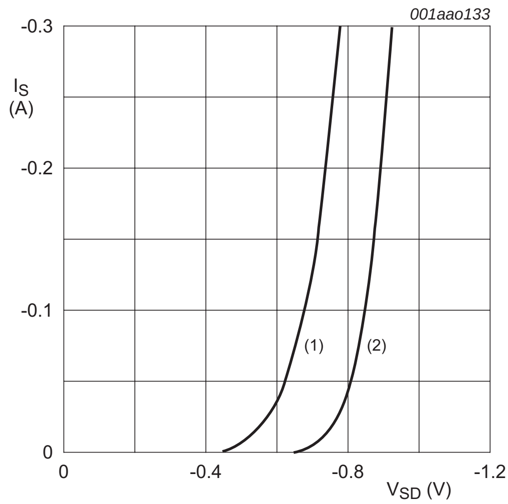


Fig 15. Gate charge waveform definitions



V_{GS} = 0 V

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

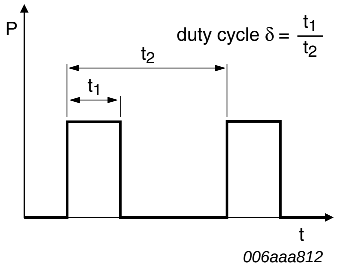


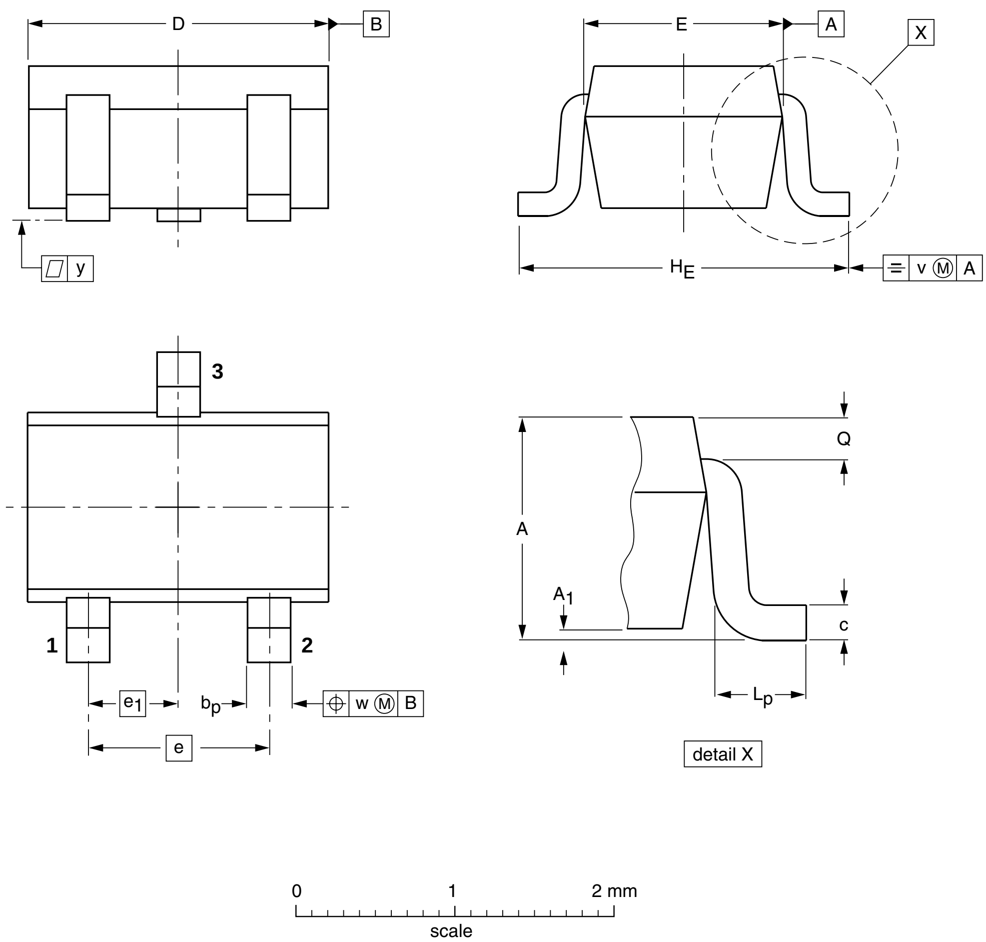
Fig 17. Duty cycle definition

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

9. Package outline

Plastic surface-mounted package; 3 leads **SOT323**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

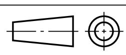
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			~~04-11-04~~ 06-03-16

Fig 18. Package outline SOT323 (SC-70)

10. Soldering

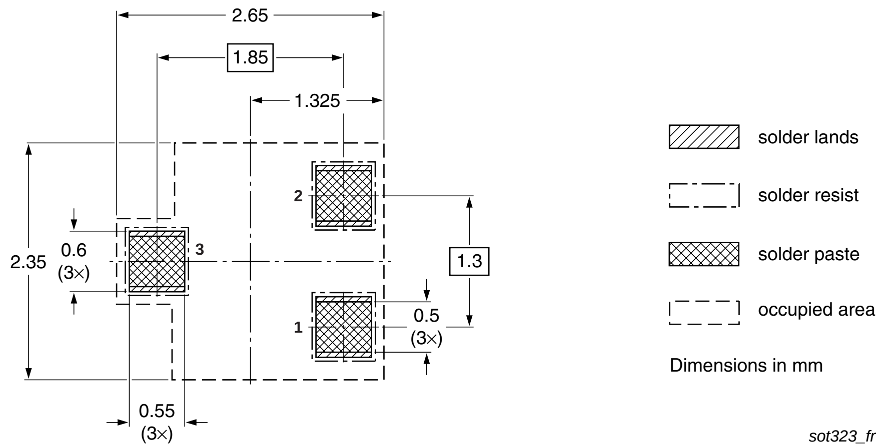


Fig 19. Reflow soldering footprint for SOT323 (SC-70)

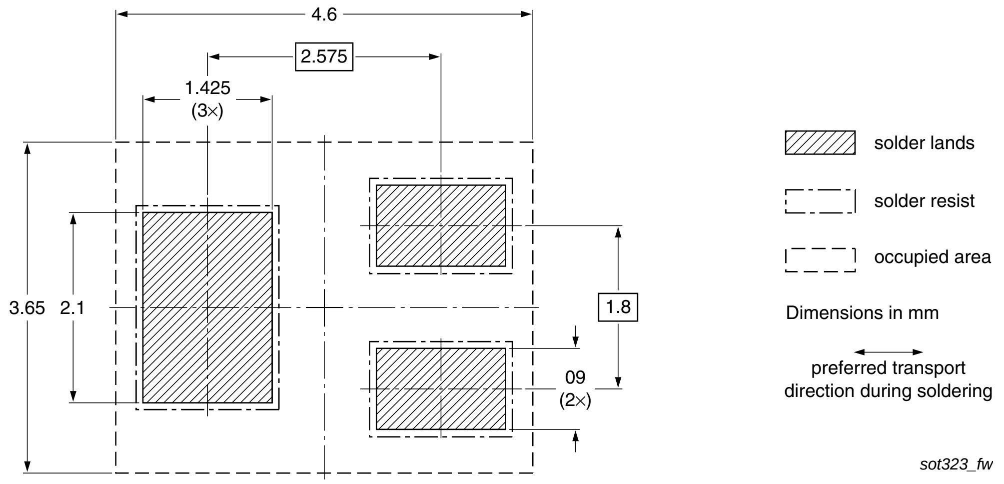


Fig 20. Wave soldering footprint for SOT323 (SC-70)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BSS84AKW v.1	20110523	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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