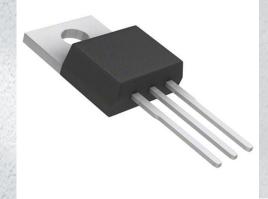


BUK953R5-60E,127 Datasheet

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DiGi Electronics Part Number

Manufacturer Product Number

Description

Manufacturer

Detailed Description

BUK953R5-60E,127-DG

Nexperia USA Inc.

BUK953R5-60E,127

MOSFET N-CH 60V 120A TO220AB

N-Channel 60 V 120A (Tc) 293W (Tc) Through Hole TO-220AB

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
BUK953R5-60E,127	Nexperia USA Inc.
Series:	Product Status:
TrenchMOS™	Obsolete
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
60 V	120A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ ld, Vgs:
5V, 10V	3.4mOhm @ 25A, 10V
Vgs(th) (Max) @ ld:	Gate Charge (Qg) (Max) @ Vgs:
2.1V @ 1mA	95 nC @ 5 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±10V	13490 pF @ 25 V
FET Feature:	Power Dissipation (Max):
	293W (Tc)
Operating Temperature:	Grade:
-55°C ~ 175°C (TJ)	Automotive
Qualification:	Mounting Type:
AEC-Q101	Through Hole
Supplier Device Package:	Package / Case:
ТО-220АВ	TO-220-3

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	



BUK953R5-60E

N-channel TrenchMOS logic level FET 11 September 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in a SOT78 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with VGS(th) rating of greater than 0.5V at 175 °C

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	60	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 1</u>	[1]	-	-	120	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	293	W
Static charac	teristics	·					
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; <u>Fig. 11</u>		-	2.87	3.7	mΩ
Dynamic cha	racteristics	·			1		
Q _{GD}	gate-drain charge	V _{GS} = 5 V; I _D = 25 A; V _{DS} = 48 V; Fig. 13; Fig. 14		-	31	-	nC

[1] Continuous current is limited by package.

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BUK953R5-60E

N-channel TrenchMOS logic level FET

2. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain		
3	S	source		G-UF44
mb	D	mounting base; connected to drain		mbb076 S
			TO-220AB (SOT78A)	

3. Ordering information

Table 3. Ordering in	formation		
Type number	Package		
	Name	Description	Version
BUK953R5-60E	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	60	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ		-	60	V
V _{GS}	gate-source voltage	$T_j \le 175 \ ^{\circ}C; Pulsed$	[1][2]	-15	15	V
		T _j ≤ 175 °C; DC		-10	10	V
ID	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; <u>Fig. 1</u>	[3]	-	120	Α
		T _{mb} = 100 °C; V _{GS} = 5 V; <u>Fig. 1</u>	[3]	-	120	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \ \mu$ s; Fig. 4		-	758	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	293	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drai	n diode					
I _S	source current	T _{mb} = 25 °C	[3]	-	120	А

Product data sheet

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N-channel TrenchMOS logic level FET

Symbol	Parameter	Conditions		Min	Мах	Unit
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^\circ C$		-	758	А
Avalanche rug	gedness	·				,
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$\begin{split} I_D &= 120 \text{ A}; \text{ V}_{\text{sup}} \leq 60 \text{ V}; \text{ R}_{\text{GS}} = 50 \Omega; \\ \text{V}_{\text{GS}} &= 5 \text{ V}; \text{ T}_{\text{j(init)}} = 25 \text{ °C}; \text{ unclamped}; \\ \hline \text{Fig. 3} \end{split}$	[<u>4][5]</u>	-	404	mJ

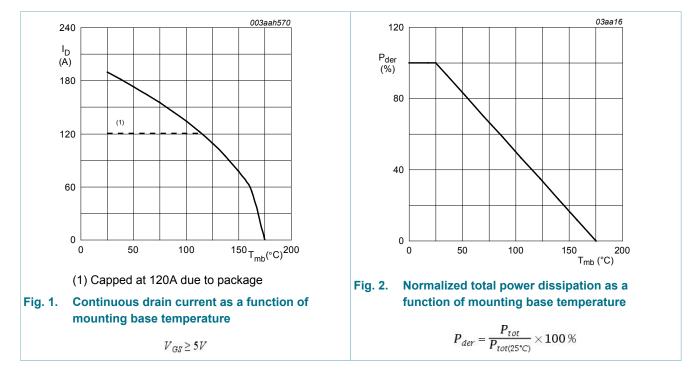
[1] Accumulated pulse duration up to 50 hours delivers zero defect ppm

[2] Significantly longer life times are achieved by lowering T_{j} and or V_{GS}

[3] Continuous current is limited by package.

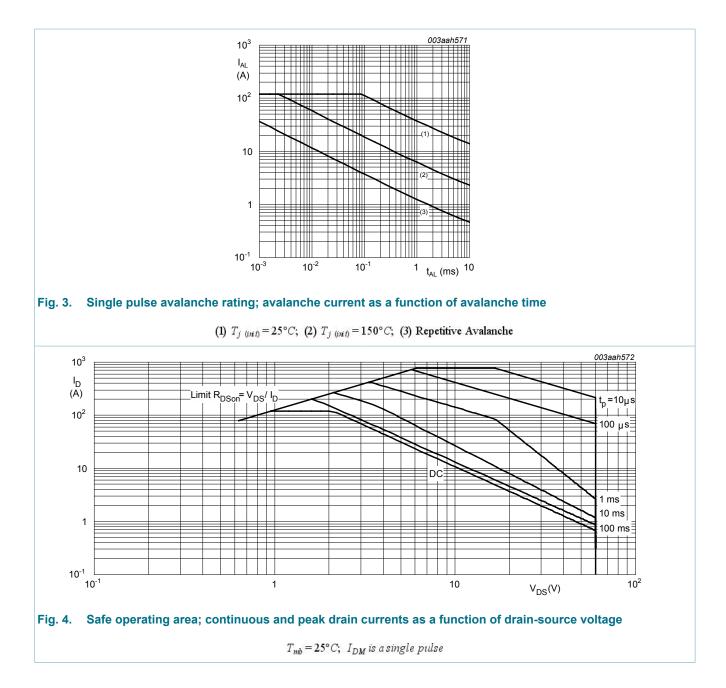
[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[5] Refer to application note AN10273 for further information.



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N-channel TrenchMOS logic level FET



5. Thermal characteristics

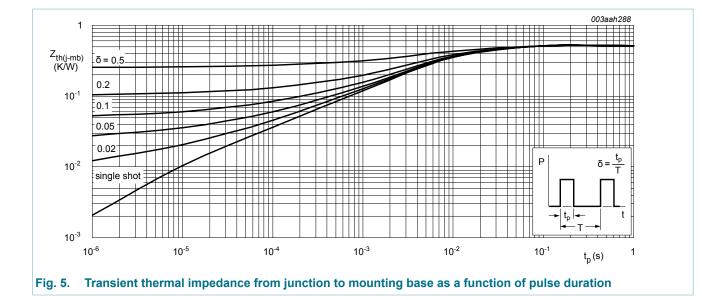
Table 5.	Thermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	0.51	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

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N-channel TrenchMOS logic level FET



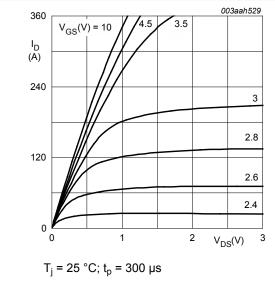
Characteristics 6.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	60	-	-	V
	breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	54	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V
I _{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	0.09	1	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; <u>Fig. 11</u>	-	2.87	3.7	mΩ
	resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	2.63	3.4	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	8.1	mΩ
Dynamic ch	aracteristics	· · ·				
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 48 V; V _{GS} = 5 V;	-	95	-	nC
Q _{GS}	gate-source charge	Fig. 13; Fig. 14	-	20	-	nC

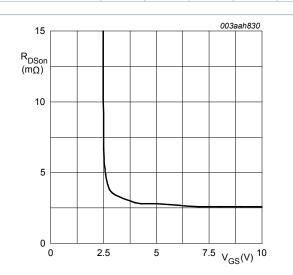
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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Q _{GD}	gate-drain charge		-	31	-	nC
C _{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz;	-	10115	13490	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	822	990	pF
C _{rss}	reverse transfer capacitance		-	427	585	pF
t _{d(on)}	turn-on delay time	V_{DS} = 45 V; R _L = 1.8 Ω; V _{GS} = 5 V;	-	54.2	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$	-	100	-	ns
t _{d(off)}	turn-off delay time		-	158	-	ns
t _f	fall time	_	-	109	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to center of die ; $T_j = 25 \text{ °C}$	-	2.5	-	nH
		from drain lead 6mm from package to centre of die ; $T_j = 25 \text{ °C}$	-	4.5	-	nH
L _S	internal source inductance	from source lead to source bonding pad ; T _j = 25 $^{\circ}$ C	-	7.5	-	nH
Source-dra	in diode				1	,
V _{SD}	source-drain voltage	I_{S} = 25 A; V_{GS} = 0 V; T_{j} = 25 °C; <u>Fig. 16</u>	-	0.78	1.2	V
t _{rr}	reverse recovery time	I_{S} = 20 A; dI_{S}/dt = -100 A/µs; V _{GS} = 0 V;	-	43	-	ns
Q _r	recovered charge	V _{DS} = 25 V	-	67	-	nC





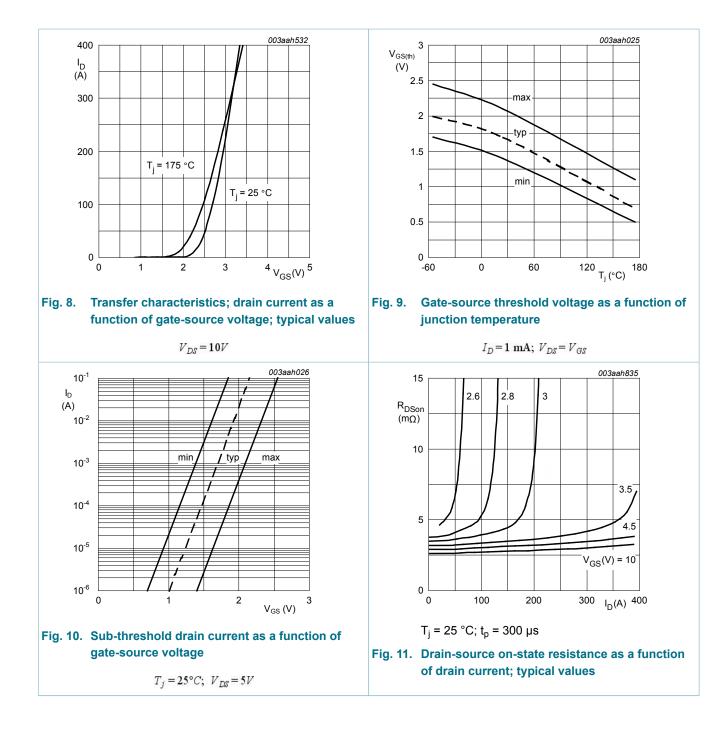




 $T_j = 25^{\circ}C; \ I_D = 25A$

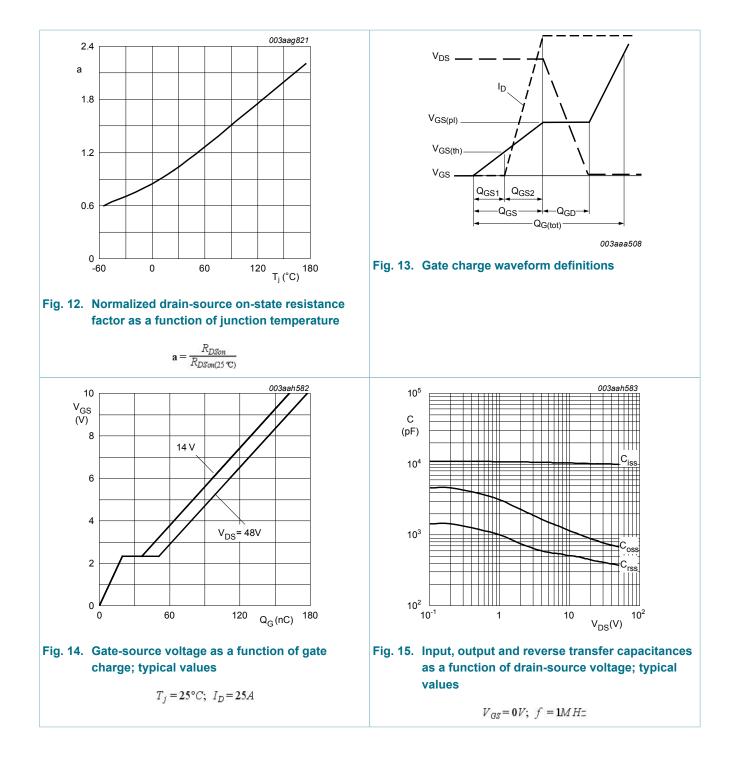
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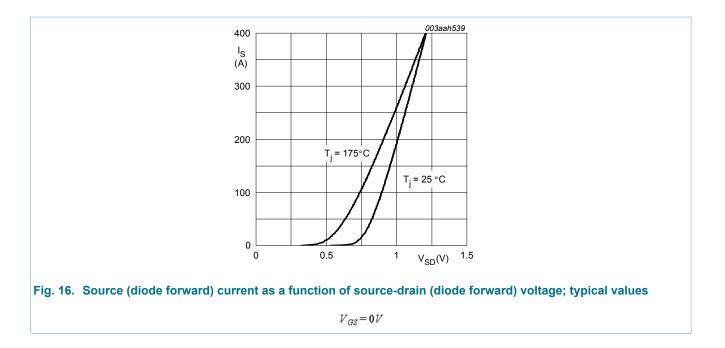
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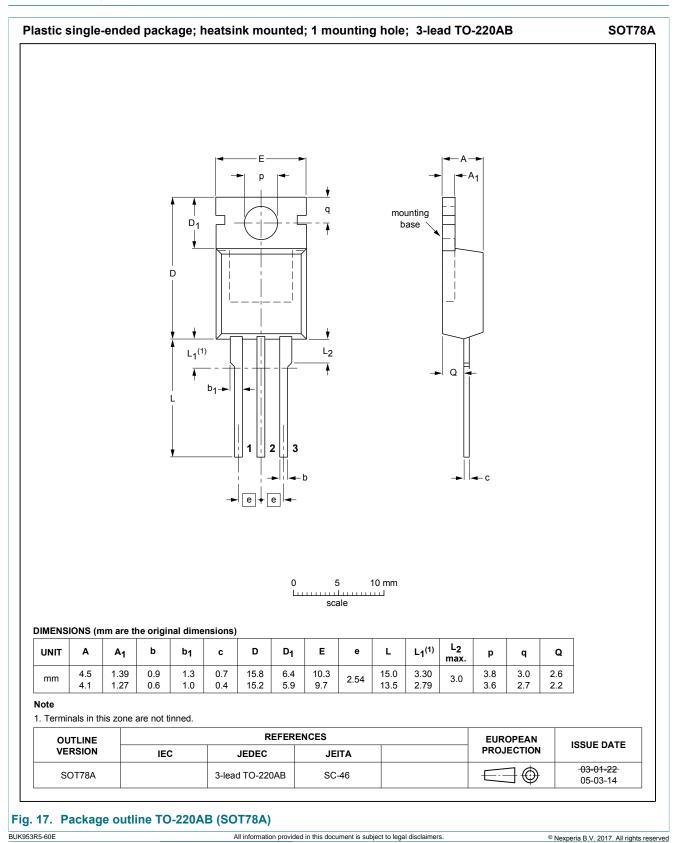
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7. Package outline



Product data sheet

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N-channel TrenchMOS logic level FET

8. Legal information

8.1 Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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