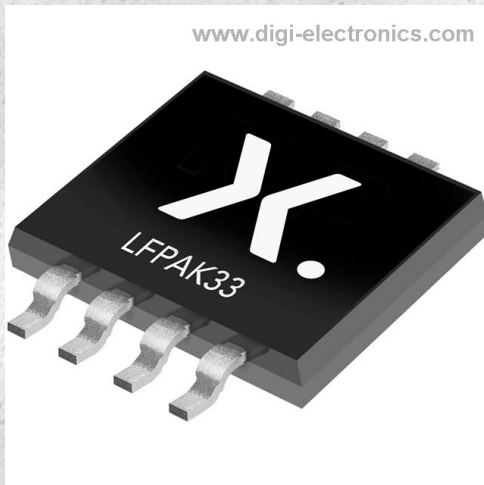


BUK9M156-100EX Datasheet



DiGi Electronics Part Number	BUK9M156-100EX-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	BUK9M156-100EX
Description	MOSFET N-CH 100V 9.3A LFPAK33
Detailed Description	N-Channel 100 V 9.3A (Tc) 36W (Tc) Surface Mount LFPAK33



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:

BUK9M156-100EX

Series:

TrenchMOS™

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

100 V

Drive Voltage (Max Rds On, Min Rds On):

5V

Vgs(th) (Max) @ Id:

2.1V @ 1mA

Vgs (Max):

±10V

FET Feature:

-

Operating Temperature:

-55°C ~ 175°C (Tj)

Qualification:

AEC-Q101

Supplier Device Package:

LFPAK33

Base Product Number:

BUK9M156

Manufacturer:

Nexperia USA Inc.

Product Status:

Active

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

9.3A (Tc)

Rds On (Max) @ Id, Vgs:

150mOhm @ 5A, 10V

Gate Charge (Qg) (Max) @ Vgs:

7.4 nC @ 5 V

Input Capacitance (Ciss) (Max) @ Vds:

695 pF @ 25 V

Power Dissipation (Max):

36W (Tc)

Grade:

Automotive

Mounting Type:

Surface Mount

Package / Case:

SOT-1210, 8-LFPAK33 (5-Lead)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



BUK9M156-100E

N-channel 100 V, 156 mΩ logic level MOSFET in LPAK33

19 September 2016

Product data sheet

1. General description

Logic level N-channel MOSFET in an LPAK33 (Power33) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

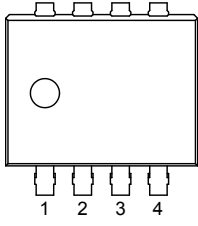
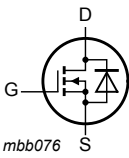
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	9.3	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	36	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	124	156	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}$; $V_{DS} = 80\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	3.2	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	Source	 <p>LFAK33 (SOT1210)</p>	
2	S	Source		
3	S	Source		
4	G	Gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9M156-100E	LFAK33	Plastic single ended surface mounted package (LFAK33); 8 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M156-100E	915610

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$	-10	10	V
		Pulsed; $T_j \leq 175\text{ °C}$	[1][2]	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	36	W
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	9.3	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	6.5	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	37	A

N-channel 100 V, 156 mΩ logic level MOSFET in LPAK33

Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	9.3	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	37	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 9.3 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[3][4]	-	9.6 mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm.
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

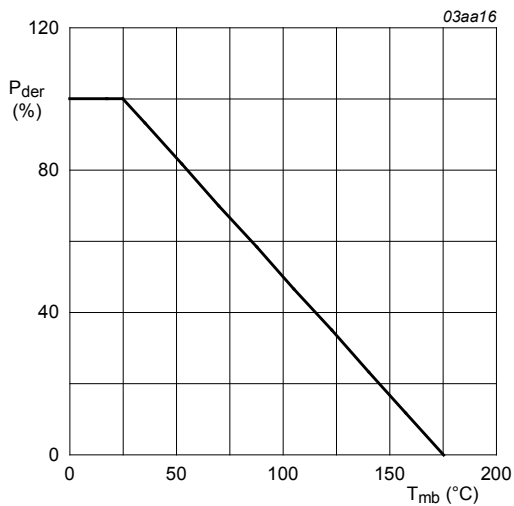
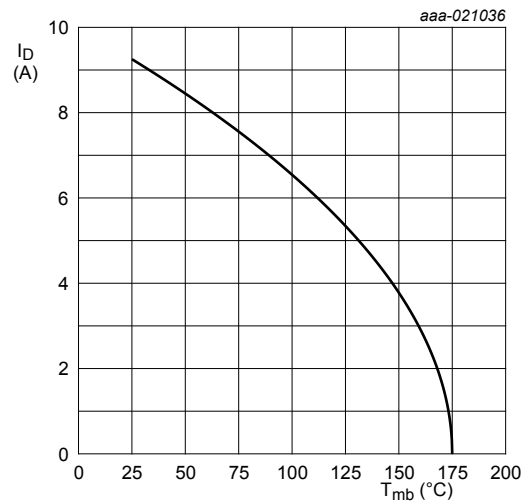


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



V_{GS} ≥ 5 V

Fig. 2. Continuous drain current as a function of mounting base temperature

$$I_D = 9.3A \times \sqrt{\frac{175^{\circ}C - T_{mb}}{150^{\circ}C}} \text{ for } T_{mb} \geq 25^{\circ}C$$

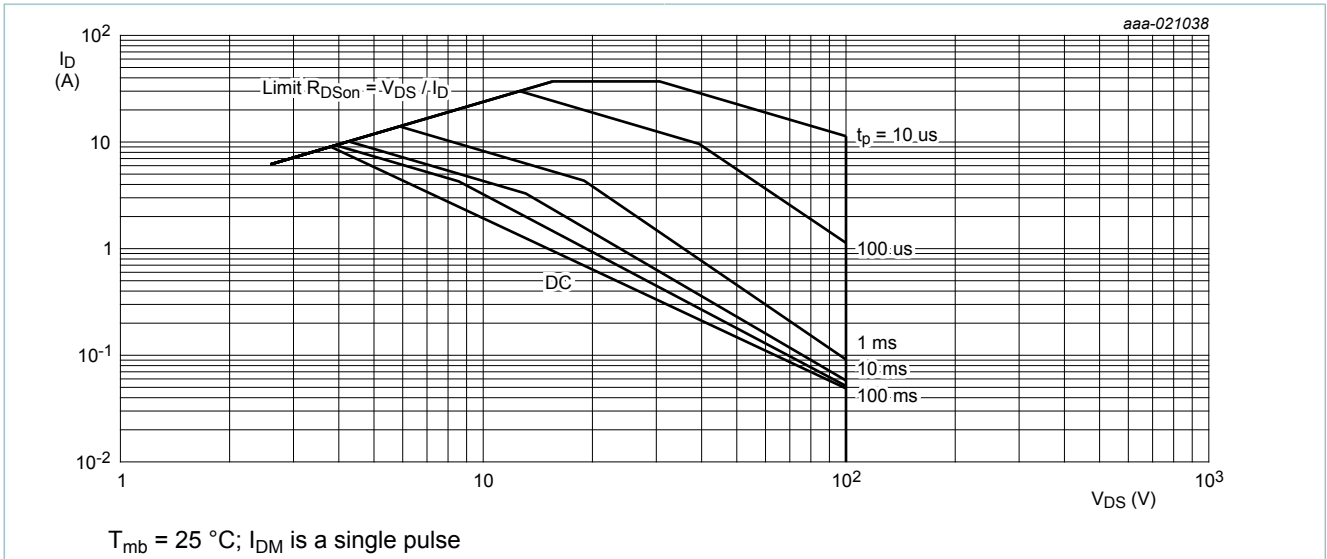


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

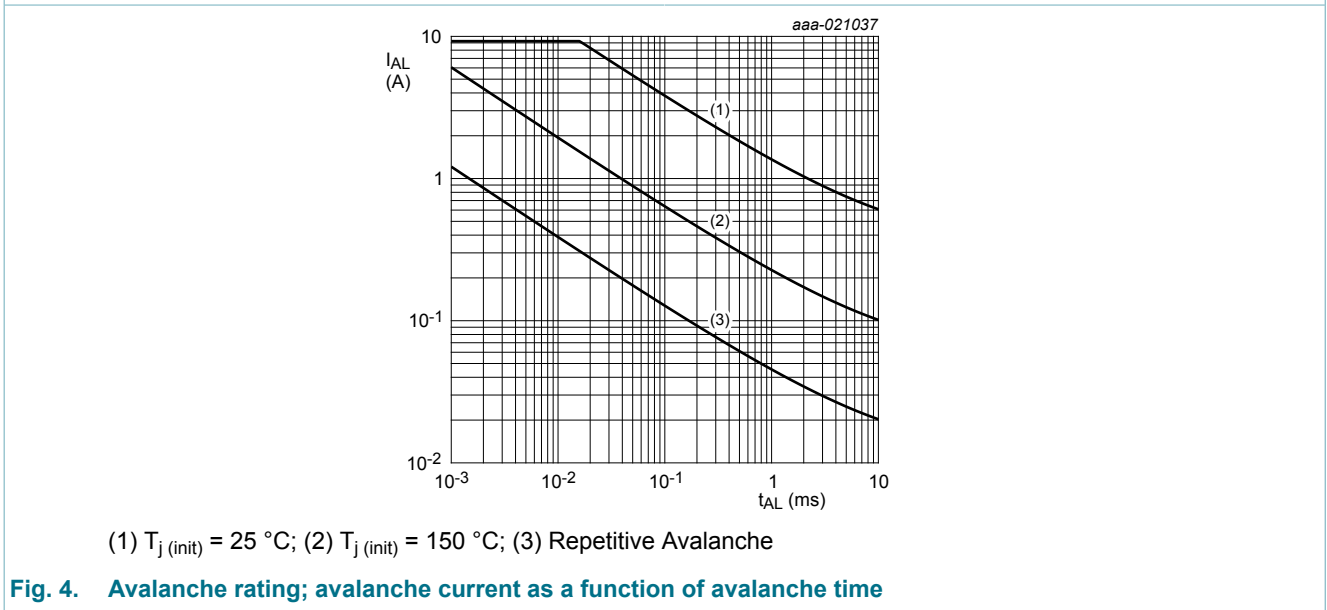


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	3.61	4.17	K/W

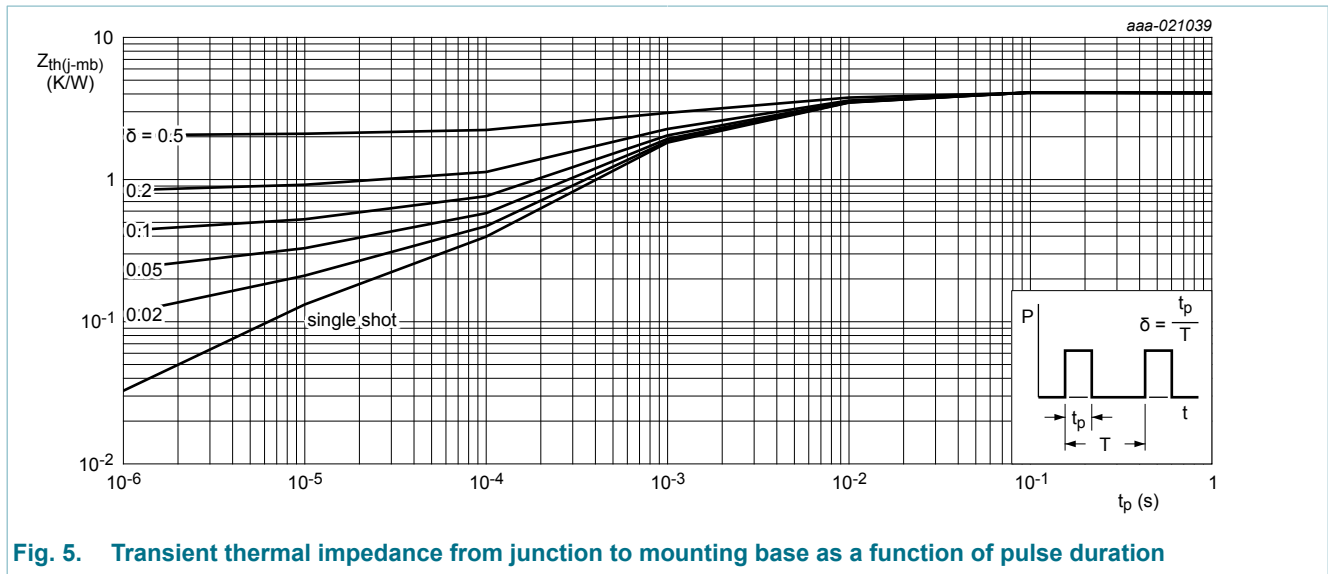


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

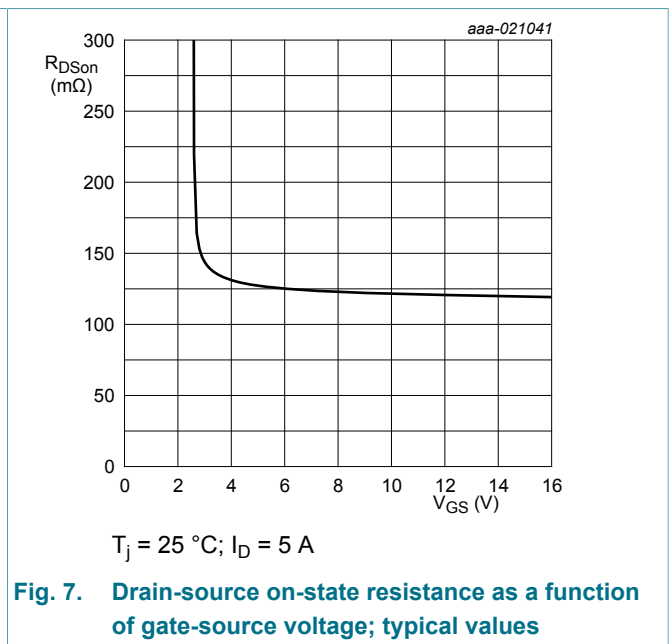
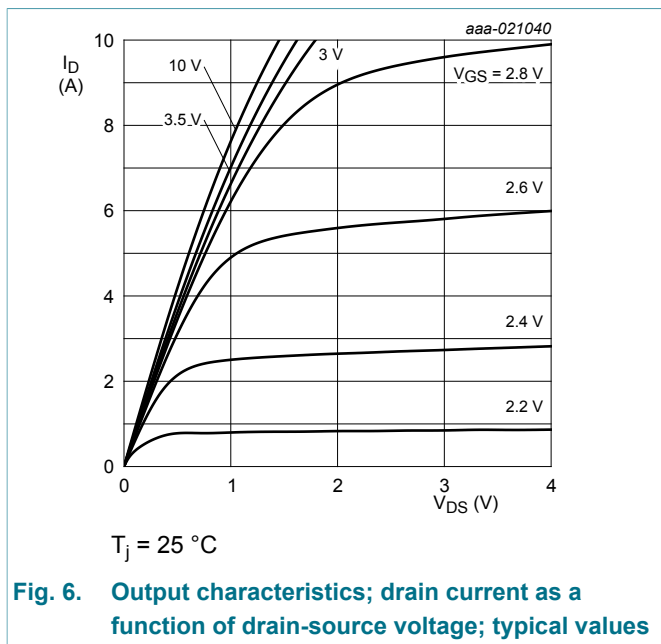
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 9 ; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10	0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.01	1	μA
		$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ Fig. 11	-	124	156	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ Fig. 11	-	120	150	mΩ
		$V_{GS} = 5 V; I_D = 5 A; T_j = 175 \text{ }^\circ C;$ Fig. 12	-	-	420	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 5 A; V_{DS} = 80 V; V_{GS} = 5 V;$ $T_j = 25 \text{ }^\circ C;$ Fig. 13 ; Fig. 14	-	7.4	-	nC
Q_{GS}	gate-source charge		-	1.4	-	nC
Q_{GD}	gate-drain charge		-	3.2	-	nC

N-channel 100 V, 156 mΩ logic level MOSFET in LPAK33

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	523	695	pF
C_{oss}	output capacitance		-	42	50	pF
C_{rss}	reverse transfer capacitance		-	28	39	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 80\text{ V}; R_L = 10\text{ } \Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 5\text{ } \Omega; T_j = 25\text{ }^\circ\text{C}$	-	5.6	-	ns
t_r	rise time		-	8.8	-	ns
$t_{d(off)}$	turn-off delay time		-	11.8	-	ns
t_f	fall time		-	7.2	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	0.92	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	27.6	-	ns
Q_r	recovered charge		-	33.9	-	nC



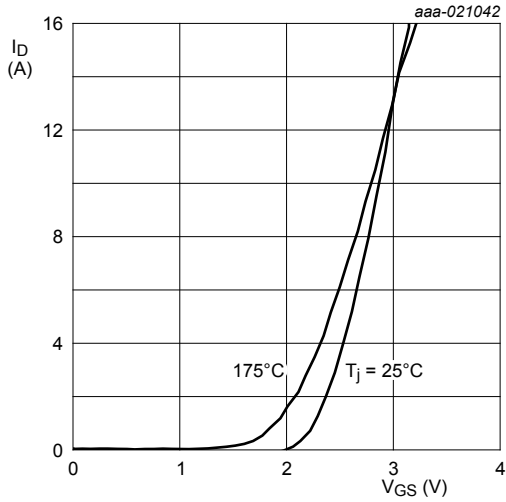


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

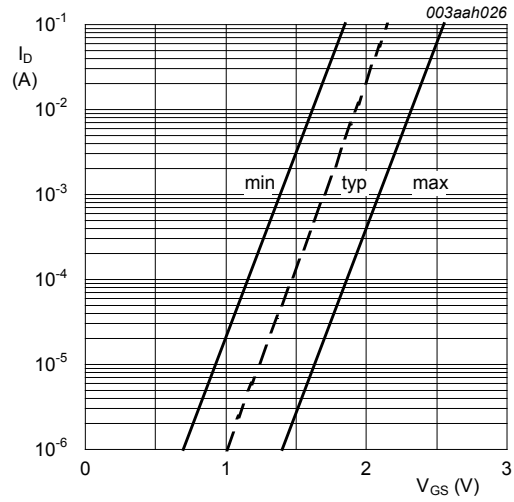


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

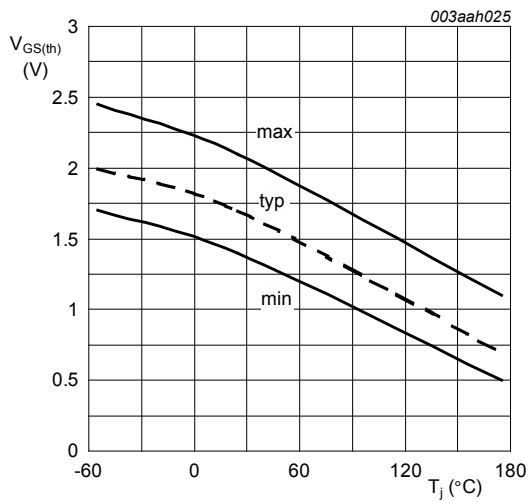


Fig. 10. Gate-source threshold voltage as a function of junction temperature

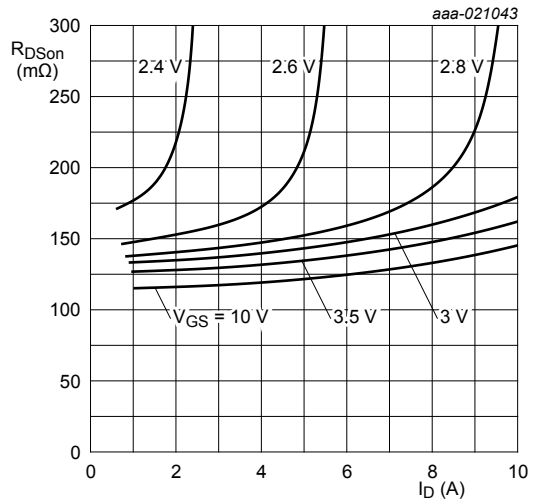


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

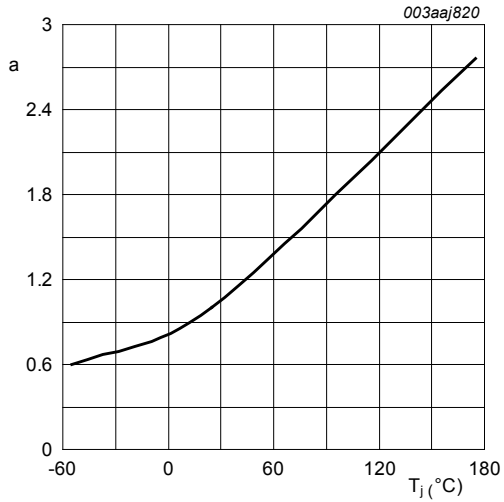
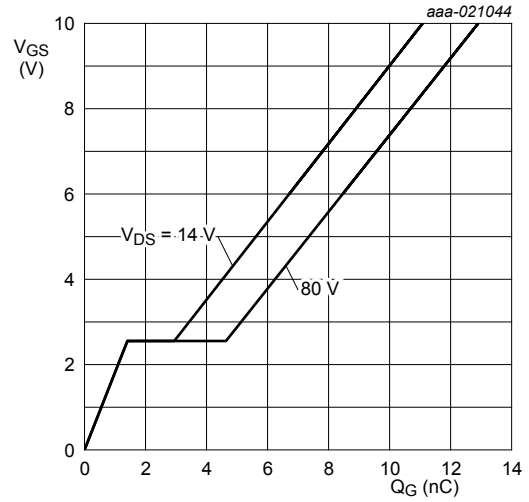


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$



$T_j = 25^{\circ}C; I_D = 5 A$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

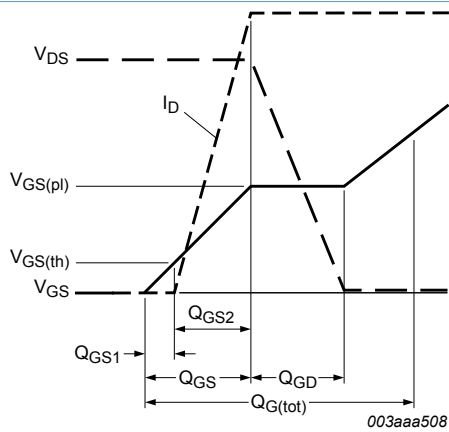
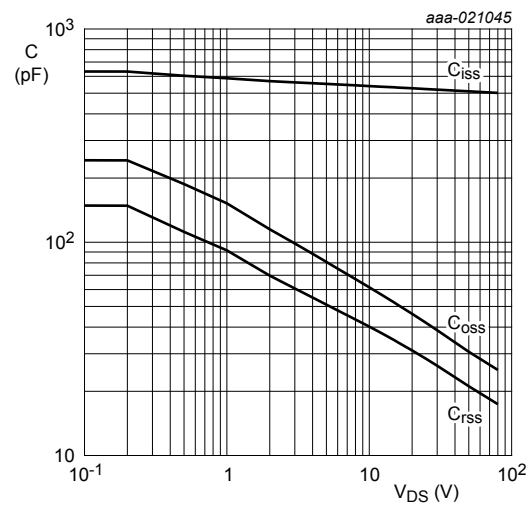
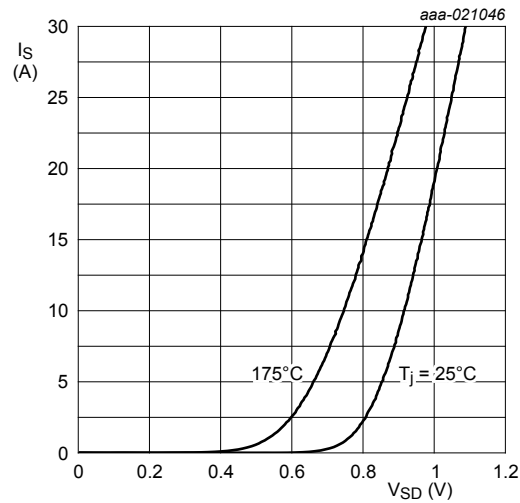


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0 V; f = 1 MHz$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Application information

For guidance on how to use and understand this datasheet, please refer to application note [AN11158](#) "Understanding power MOSFET datasheet parameters".

12. Package outline

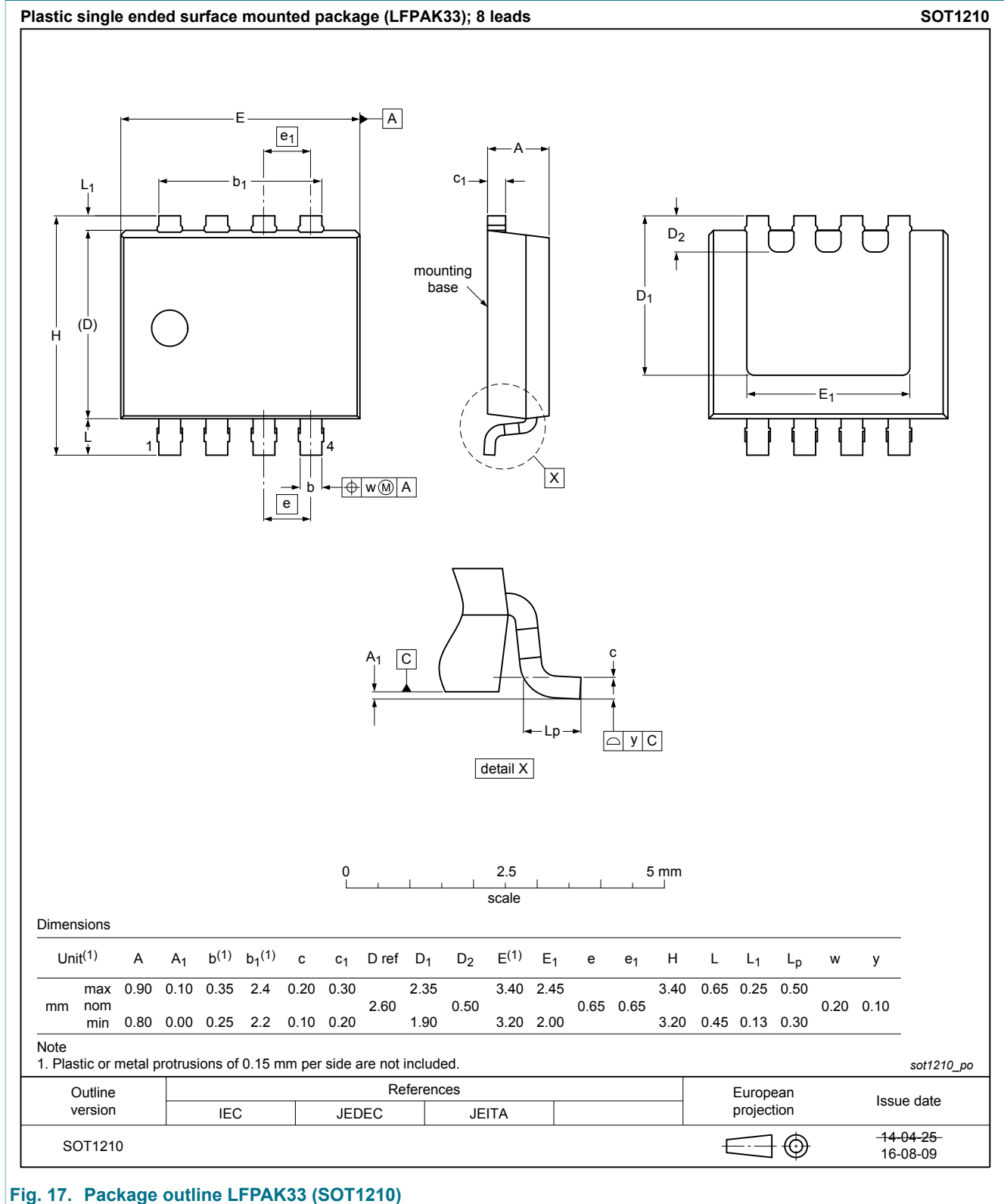


Fig. 17. Package outline LFAK33 (SOT1210)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 19 September 2016

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