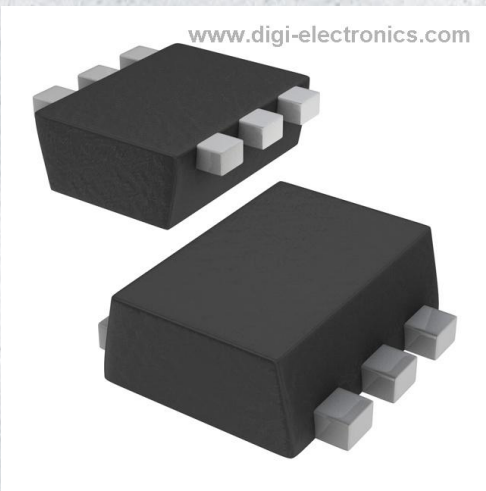
PEMD4,115 Datasheet



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DiGi Electronics Part Number	PEMD4,115-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	PEMD4,115
Description	TRANS PREBIAS 1NPN 1PNP SOT666
Detailed Description	Pre-Biased Bipolar Transistor (BJT) 1 NPN, 1 PNP - Pre-Biased (Dual) 50V 100mA 300mW Surface Mount SOT-666

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
PEMD4,115	Nexperia USA Inc.
Series:	Product Status:
-	Not For New Designs
Transistor Type:	Current - Collector (Ic) (Max):
1 NPN, 1 PNP - Pre-Biased (Dual)	100mA
Voltage - Collector Emitter Breakdown (Max):	Resistor - Base (R1):
50V	10kOhms
Resistor - Emitter Base (R2):	DC Current Gain (hFE) (Min) @ Ic, Vce:
-	200 @ 1mA, 5V
Vce Saturation (Max) @ Ib, Ic:	Current - Collector Cutoff (Max):
150mV @ 500µA, 10mA	1µA
Frequency - Transition:	Power - Max:
-	300mW
Mounting Type:	Package / Case:
Surface Mount	SOT-563, SOT-666
Supplier Device Package:	Base Product Number:
SOT-666	PEMD4

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.21.0095	

PEMD4

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = open

28 December 2022 **Product data sheet**

1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PEMH4

PNP/PNP complement: PEMB4

2. Features and benefits

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs

3. Applications

- Low current peripheral driver
- Replacement for general purpose transistors in digital applications
- Controlling IC inputs

4. Quick reference data

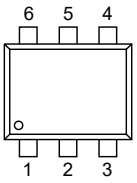
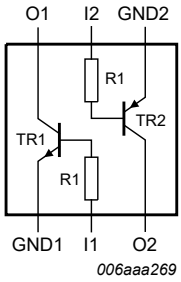
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity							
V_{CEO}	collector-emitter voltage	open base		-	-	50	V
I_O	output current			-	-	100	mA
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ

[1] See section "Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 SOT666	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PEMD4	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	SOT666

7. Marking

Table 4. Marking codes

Type number	Marking code
PEMD4	23

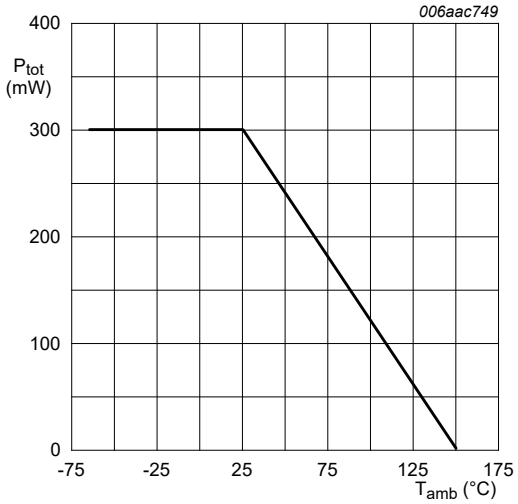
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	5	V
I_O	output current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1] [2]	-	200	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1] [2]	-	300	mW

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Reflow soldering is the only recommended soldering method.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

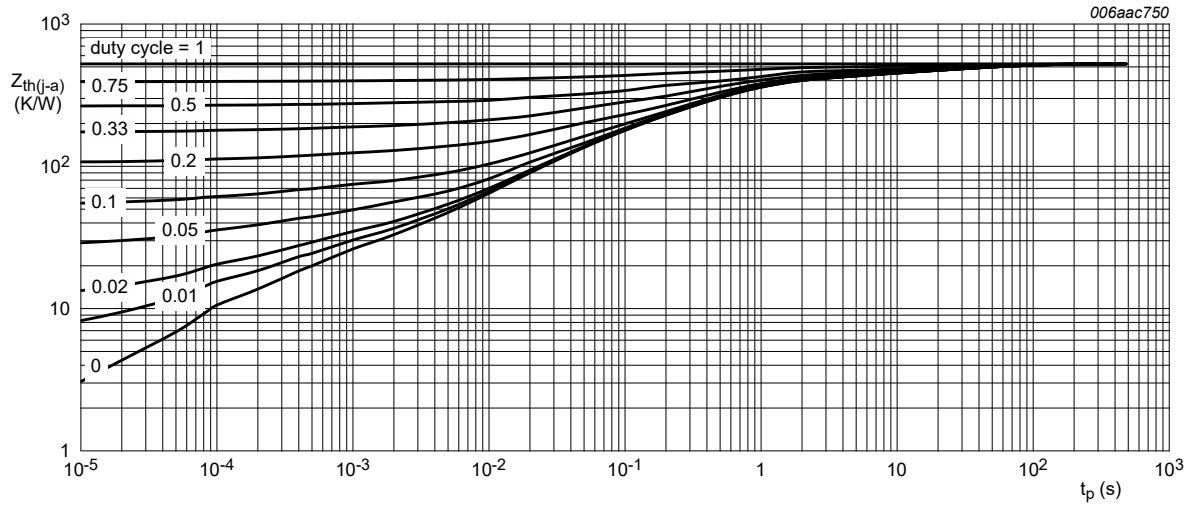
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	416	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Reflow soldering is the only recommended soldering method.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A; T_{amb} = 25 °C		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 2 mA; I_B = 0 A; T_{amb} = 25 °C		50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A; T_{amb} = 25 °C		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A; T_{amb} = 25 °C		-	-	1	µA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C		-	-	50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	100	nA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 1 mA; T_{amb} = 25 °C		200	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; T_{amb} = 25 °C		-	-	150	mV
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
Transistor TR1 (NPN)							
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.5	pF
Transistor TR2 (PNP)							
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	3	pF

[1] See section "Test information" for resistor calculation and test conditions.

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

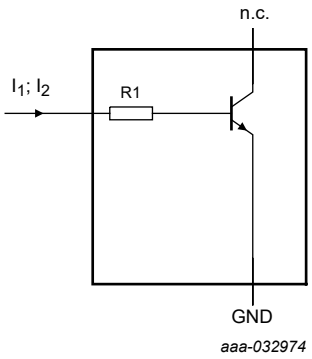


Fig. 3. TR1 (NPN): Resistor test circuit

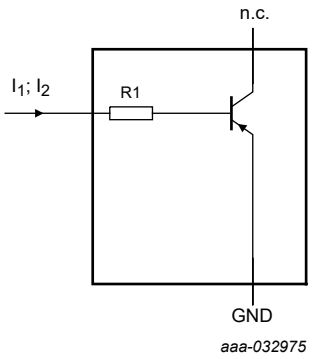


Fig. 4. TR2 (PNP): Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

PEMD4	R1 (kΩ)	R2 (open)	Test conditions	
			I_1	I_2
TR1 (NPN)	10	-	350 µA	450 µA
TR2 (PNP)	10	-	-350 µA	-450 µA

12. Package outline

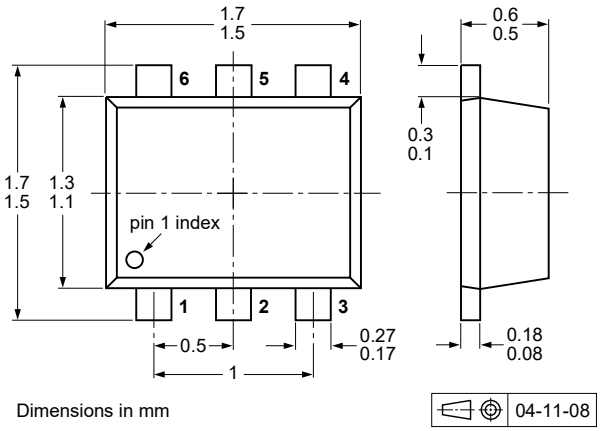


Fig. 5. Package outline SOT666

13. Soldering

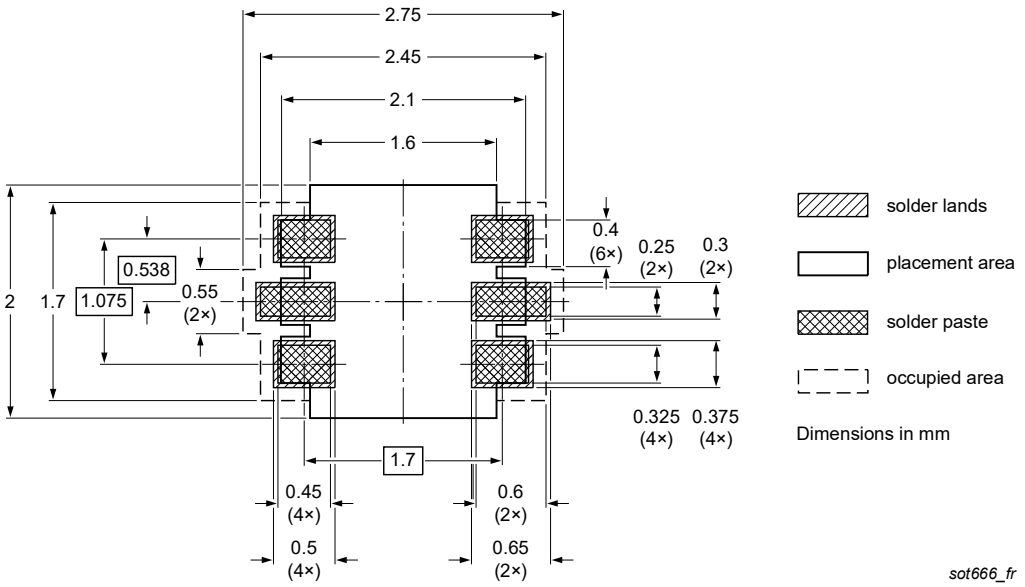


Fig. 6. Reflow soldering footprint for SOT666

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PEMD4 v.3	20221228	Product data sheet	-	PEMD4_PUMD4 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Family data sheet reduced to single type data sheet. • Product(s) changed to non-automotive qualification.			
PEMD4_PUMD4 v.2	20031010	Product data sheet	-	PEMD4_PUMD4 v.1
PEMD4_PUMD4 v.1	20020114	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 28 December 2022

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