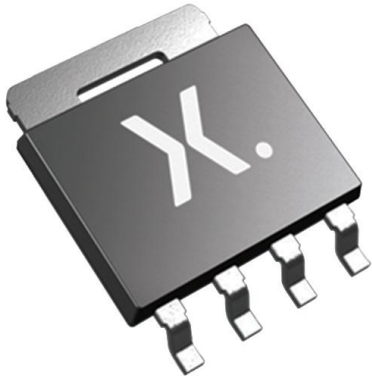


PH3230S,115 Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|---|
| DiGi Electronics Part Number | PH3230S,115-DG |
| Manufacturer | Nexperia USA Inc. |
| Manufacturer Product Number | PH3230S,115 |
| Description | MOSFET N-CH 30V 100A LFPAK |
| Detailed Description | N-Channel 30 V 100A (Tc) Surface Mount LFPAK56, Power-SO8 |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:

PH3230S,115

Series:

-

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

30 V

Rds On (Max) @ Id, Vgs:

3.2mOhm @ 25A, 10V

Gate Charge (Qg) (Max) @ Vgs:

42 nC @ 5 V

FET Feature:

-

Supplier Device Package:

LFPAK56, Power-SO8

Manufacturer:

Nexperia USA Inc.

Product Status:

Obsolete

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

100A (Tc)

Vgs(th) (Max) @ Id:

3V @ 1mA

Input Capacitance (Ciss) (Max) @ Vds:

4100 pF @ 10 V

Mounting Type:

Surface Mount

Package / Case:

SC-100, SOT-669

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

PH3230S

N-channel TrenchMOS intermediate level FET

Rev. 04 — 27 November 2009

Product data sheet

1. Product profile

1.1 General description

Intermediate level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge
- Saves PCB space due to small footprint
- Suitable for logic level gate drive sources

1.3 Applications

- Computer motherboards
- Notebook computers
- DC-to-DC convertors
- Switched-mode power supplies

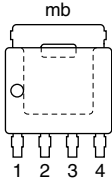
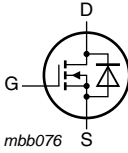
1.4 Quick reference data

Table 1. Quick reference

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|-----|------|------------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$ | - | - | 30 | V |
| I_D | drain current | $T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 and 3 | - | - | 100 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; see Figure 2 | - | - | 62.5 | W |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $V_{GS} = 5\text{ V}$; $I_D = 50\text{ A}$; $V_{DS} = 10\text{ V}$; $T_j = 25\text{ °C}$; see Figure 12 | - | 13 | - | nC |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 and 10 | - | 2.7 | 3.2 | m Ω |

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|--|---|
| 1 | S | source |  |  |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

SOT669 (LFAK)

3. Ordering information

Table 3. Ordering information

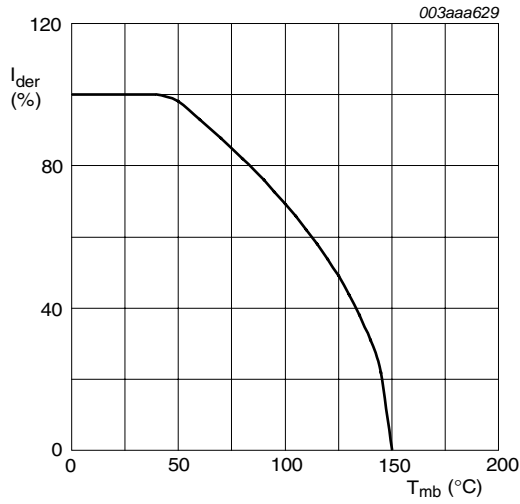
| Type number | Package | | Version |
|-------------|---------|--|---------|
| | Name | Description | |
| PH3230S | LFAK | plastic single-ended surface-mounted package (LFAK); 4 leads | SOT669 |

4. Limiting values

Table 4. Limiting values

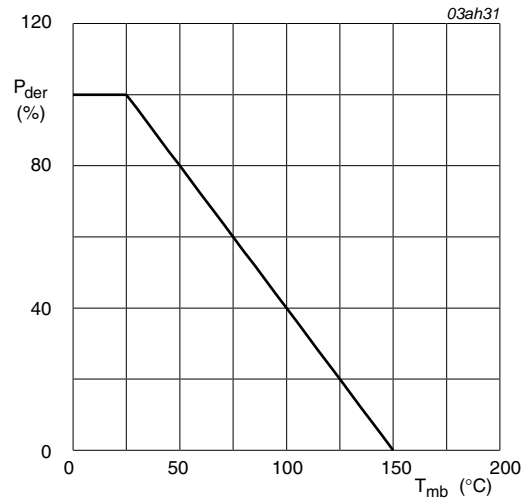
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|---|-----|------|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$ | - | 30 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 and 3 | - | 100 | A |
| | | $V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1 | - | 63 | A |
| I_{DM} | peak drain current | $t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3 | - | 300 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; see Figure 2 | - | 62.5 | W |
| T_{stg} | storage temperature | | -55 | 150 | °C |
| T_j | junction temperature | | -55 | 150 | °C |
| Source-drain diode | | | | | |
| I_S | source current | $T_{mb} = 25\text{ °C}$ | - | 52 | A |
| I_{SM} | peak source current | $t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$ | - | 156 | A |
| Avalanche ruggedness | | | | | |
| $E_{DS(AL)R}$ | repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $V_{sup} = 15\text{ V}$; $R_{GS} \geq 50\text{ }\Omega$ | - | 2.5 | mJ |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 50\text{ A}$; $V_{sup} \leq 15\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$ | - | 250 | mJ |



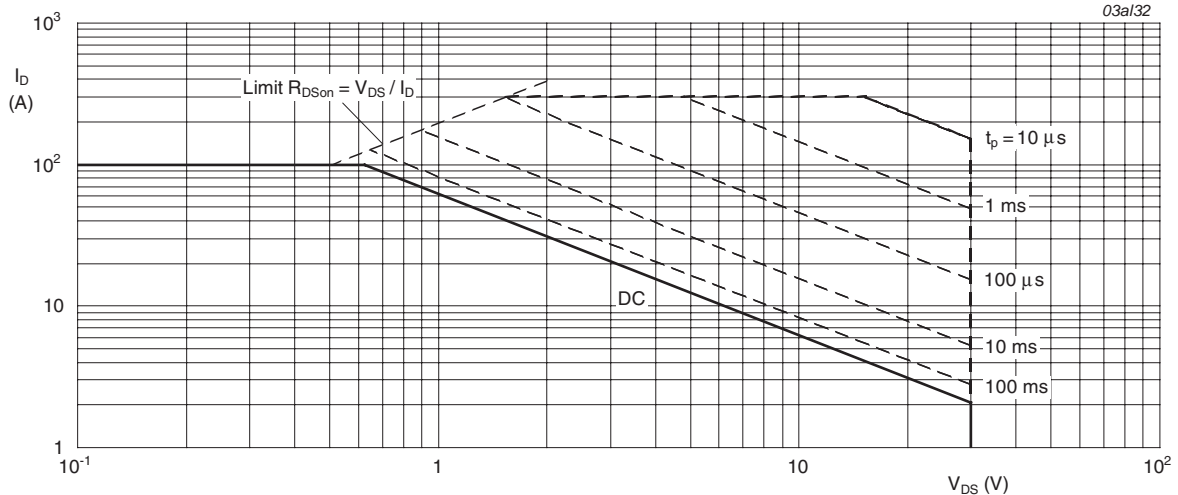
$$V_{GS} \geq 10V I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^\circ C; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------------------------|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | - | 2 | K/W |

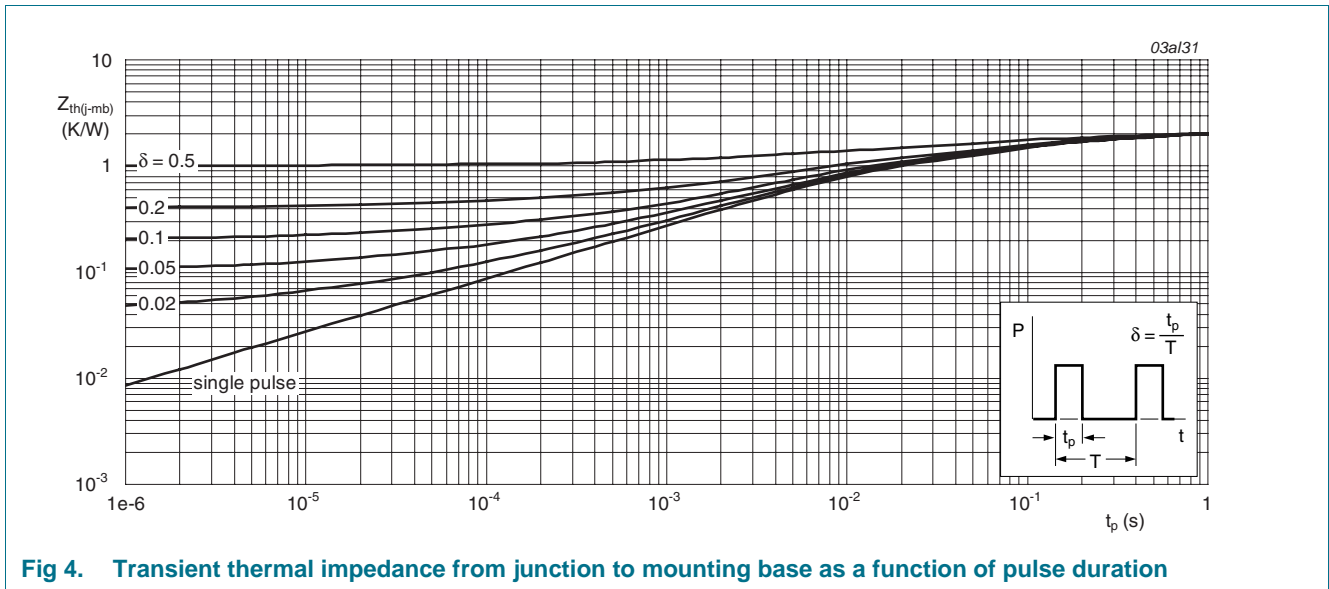
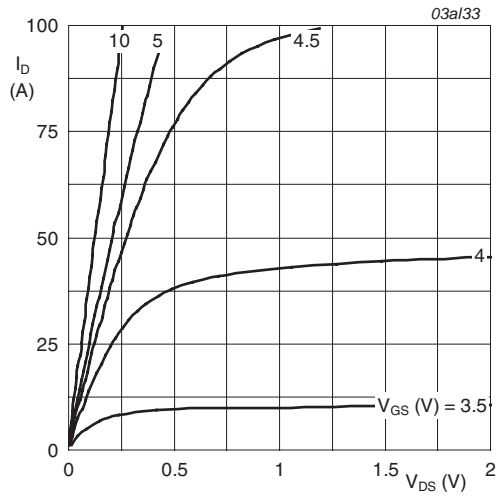


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

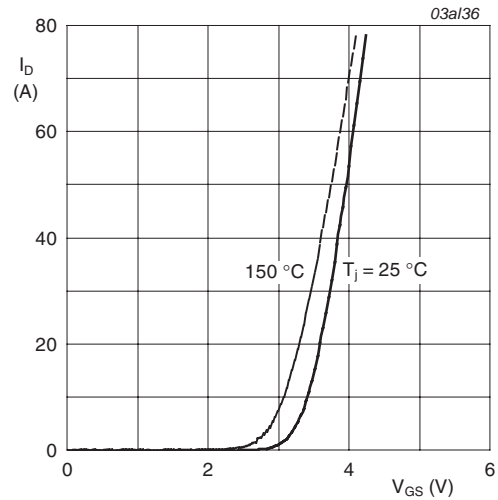
Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|--|-----|------|-----|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 10 \text{ mA}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$ | 30 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 8 | 1 | 2 | 3 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 30 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$ | - | - | 1 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$ | - | 10 | 100 | nA |
| | | $V_{GS} = -20 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$ | - | 10 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 4.5 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 9 | - | 5 | 6.5 | m Ω |
| | | $V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 9 and 10 | - | 2.7 | 3.2 | m Ω |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 11 | - | 0.8 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 20 \text{ A}$; $di_S/dt = -50 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 25 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$ | - | 46 | - | ns |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 50 \text{ A}$; $V_{DS} = 10 \text{ V}$; $V_{GS} = 5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 12 | - | 42 | - | nC |
| Q_{GS} | gate-source charge | | - | 21 | - | nC |
| Q_{GD} | gate-drain charge | | - | 13 | - | nC |
| C_{iss} | input capacitance | $V_{DS} = 10 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 13 | - | 4100 | - | pF |
| C_{oss} | output capacitance | | - | 1150 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 750 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 10 \text{ V}$; $R_L = 0.4 \text{ } \Omega$; $V_{GS} = 10 \text{ V}$; $R_{G(ext)} = 4.7 \text{ } \Omega$; $T_j = 25 \text{ }^\circ\text{C}$ | - | 14 | - | ns |
| t_r | rise time | | - | 37 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 85 | - | ns |
| t_f | fall time | | - | 37 | - | ns |
| g_{fs} | transfer conductance | $V_{DS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 14 | 39 | 75 | - | S |



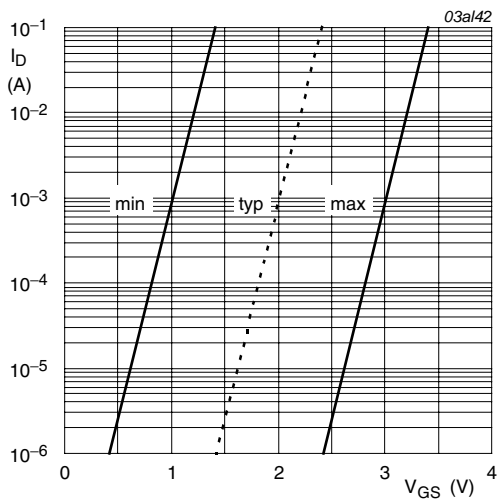
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



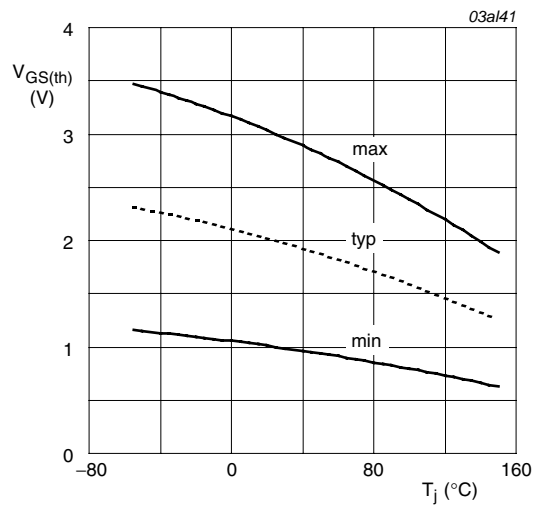
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



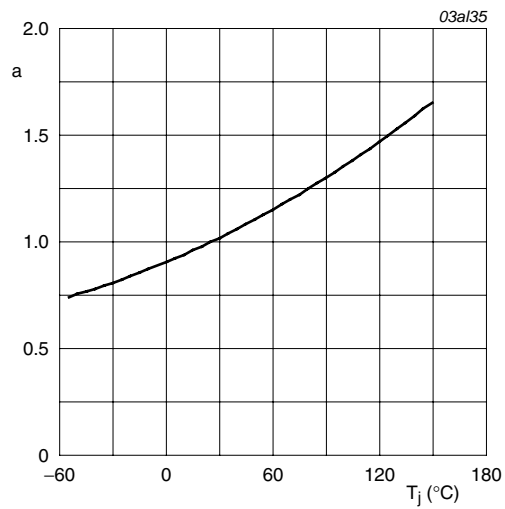
$T_j = 25^\circ\text{C}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



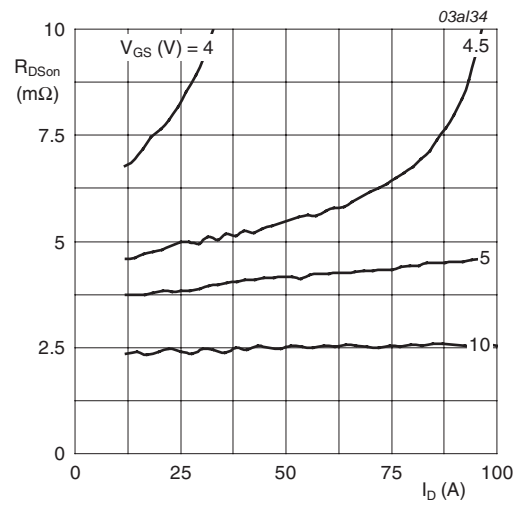
$I_D = 1\text{mA}$; $V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



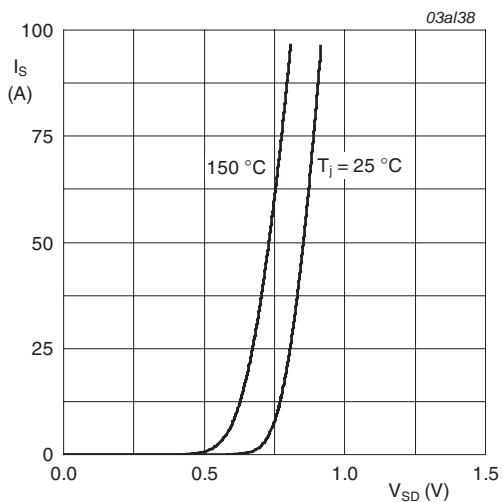
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



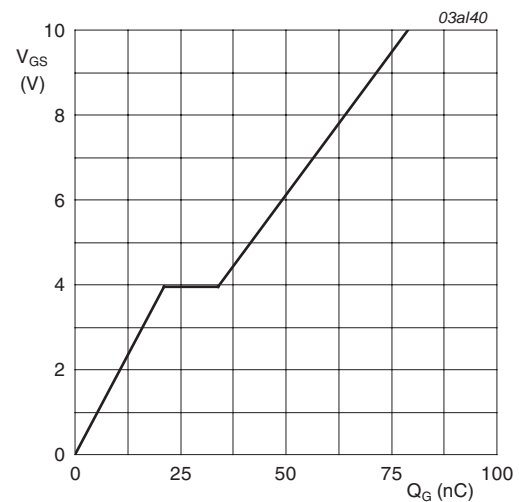
$T_j = 25^{\circ}\text{C}$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values



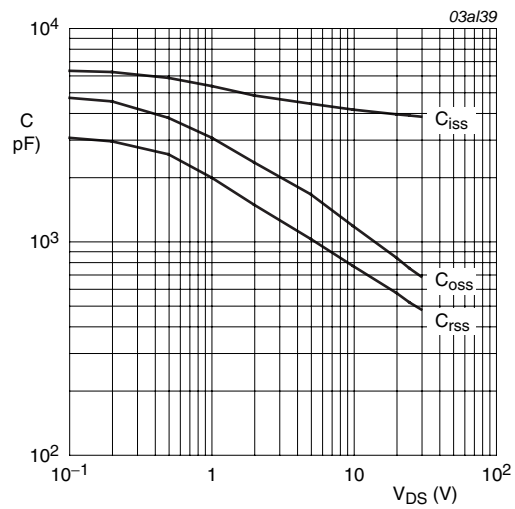
$T_j = 25^{\circ}\text{C}$ and $150^{\circ}\text{C}; V_{GS} = 0\text{V}$

Fig 11. Source current as a function of source-drain voltage; typical values



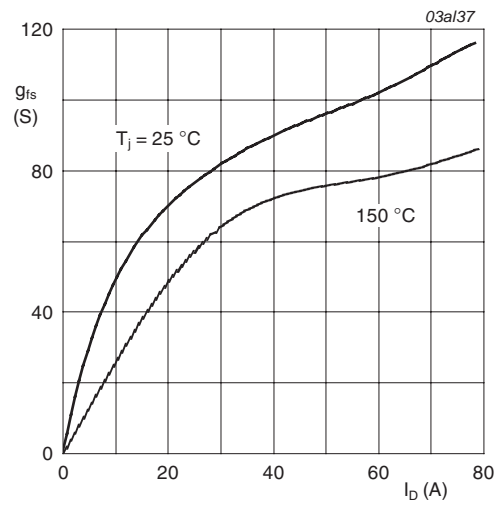
$T_j = 25^{\circ}\text{C}; I_D = 50\text{A}; V_{DD} = 10\text{V}$

Fig 12. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0V; f = 1MHz$$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$$T_j = 25^\circ C \text{ and } 150^\circ C; V_{DS} > I_D \times R_{DS(on)}$$

Fig 14. Forward transconductance as a function of drain current; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

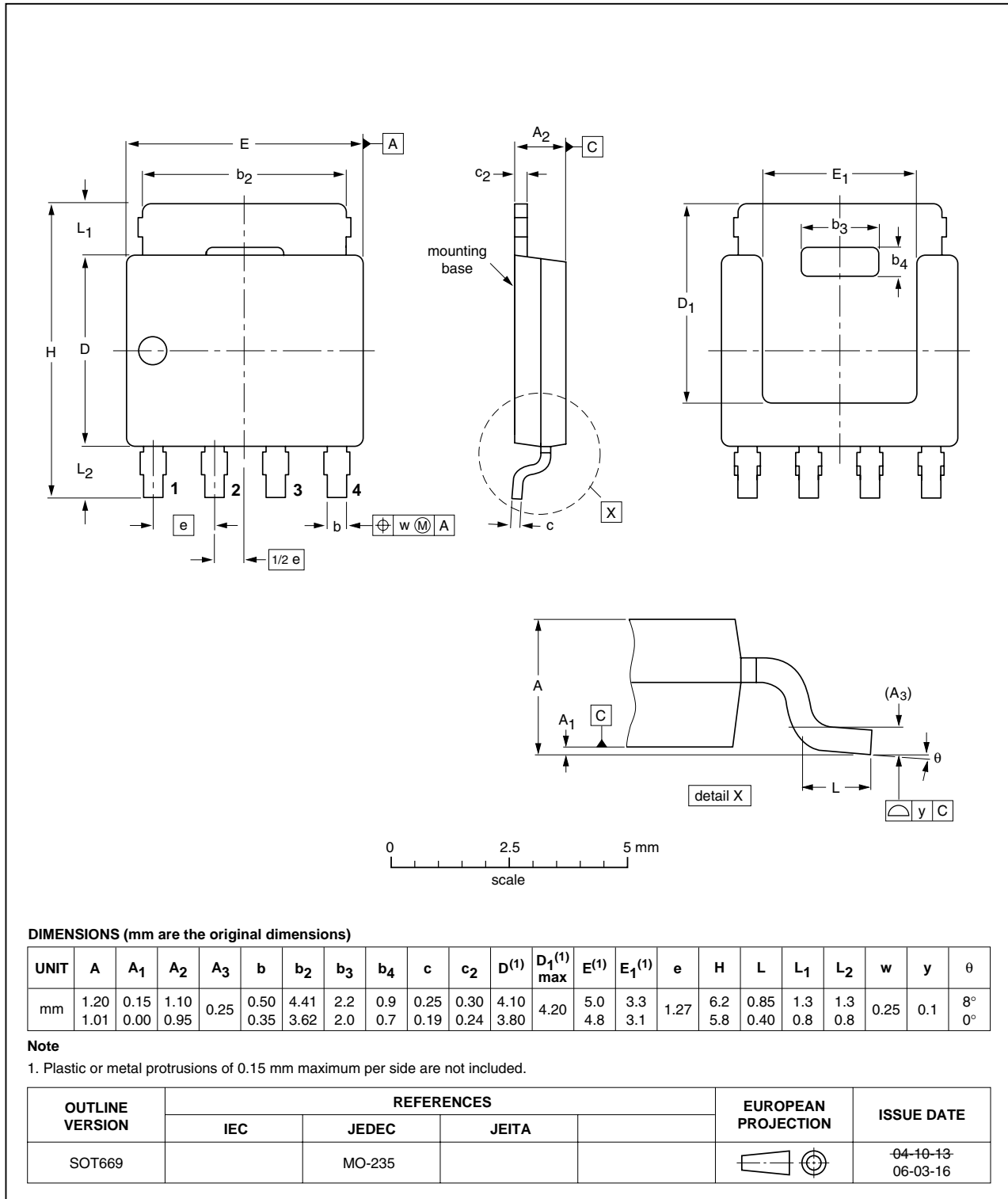


Fig 15. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------------------|--------------|---|---------------|------------|
| PH3230S_4 | 20091127 | Product data sheet | - | PH3230S-03 |
| Modifications: | | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. | | |
| PH3230S-03 (9397 750 12756) | 20040302 | Product data | - | PH3230S-02 |
| PH3230S-02 (9397 750 11279) | 20030423 | Product data | - | PH3230S-01 |
| PH3230S-01 (9397 750 11078) | 20030212 | Preliminary data | - | - |

9. Legal information

9.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 27 November 2009

Document identifier: PH3230S_4

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