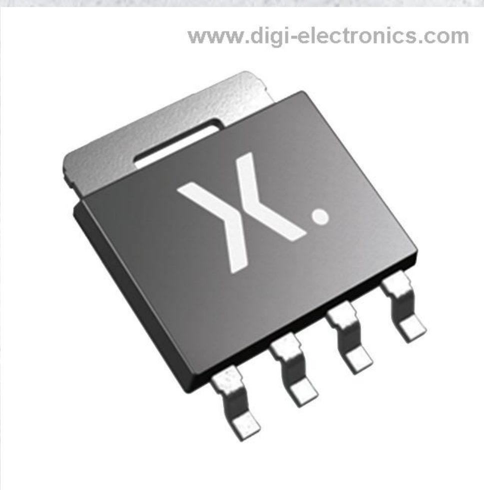
PH6325L,115 Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	PH6325L,115-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	PH6325L,115
Description	MOSFET N-CH 25V 78.7A LFPAK56
Detailed Description	N-Channel 25 V 78.7A (Tc) 62.5W (Tc) Surface Mount LFPAK56, Power-SO8

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RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
PH6325L,115	Nexperia USA Inc.
Series:	Product Status:
TrenchMOS™	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
25 V	78.7A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
4.5V, 10V	6.3mOhm @ 25A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
2V @ 1mA	13.3 nC @ 4.5 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	1871 pF @ 12 V
FET Feature:	Power Dissipation (Max):
-	62.5W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
LFPAK56, Power-SO8	SC-100, SOT-669
Base Product Number:	
PH6325	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

PH6325L

N-channel 25 V 6.3 mΩ logic level MOSFET in LFPAK

Rev. 2 — 22 December 2011 Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS^{TM} technology

1.2 Features and benefits

- Low thermal resistance
- Low threshold voltage
- Optimized for use in DC-to-DC converters
- Very low switching and conduction losses

1.3 Applications

- DC-to-DC convertors
- Notebook computers
- Switched-mode power supplies
- Voltage regulators

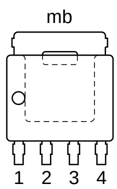
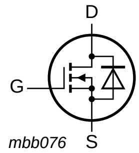
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	25	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1; see Figure 3	-	-	78.7	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	-	62.5	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see Figure 9; see Figure 10	-	7.4	9.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 9; see Figure 10	-	4.7	6.3	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 12 V; see Figure 11; see Figure 12	-	3.3	-	nC
$Q_{G(tot)}$	total gate charge		-	13.3	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		
			SOT669 (LFPAK; Power-SO8)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PH6325L	LFPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Limiting values

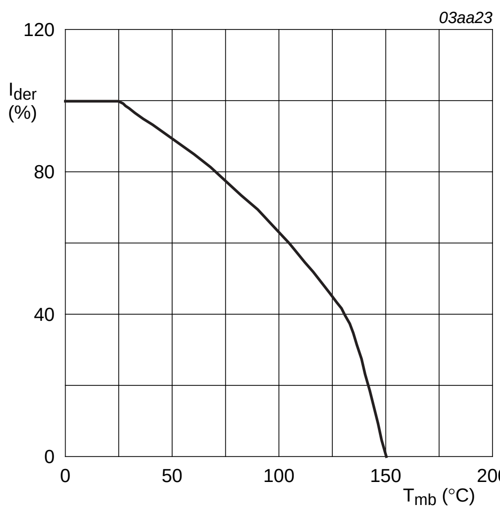
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; see Figure 1	-	49.6	A
		V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1; see Figure 3	-	78.7	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C; see Figure 3	-	236	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	62.5	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	52	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C	-	208	A
Avalanche ruggedness					
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	t_p = 0.015 ms; unclamped; R_{GS} = 50 Ω; I_D = 3.4 A; V_{DD} = 25 V; V_{GS} = 10 V [1][2]	-	1.2	mJ
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 34 A; V_{DD} = 25 V; t_p = 0.15 ms; unclamped; R_{GS} = 50 Ω	-	115	mJ

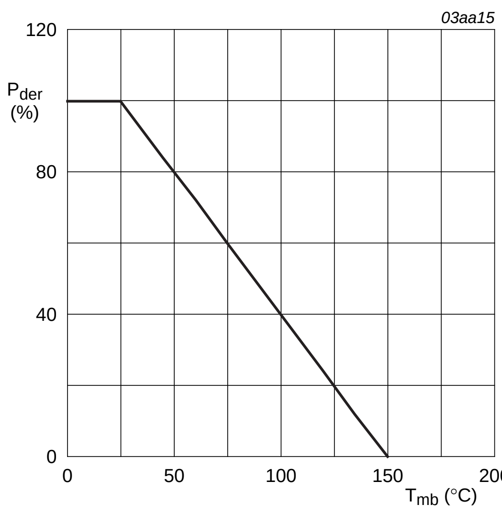
[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



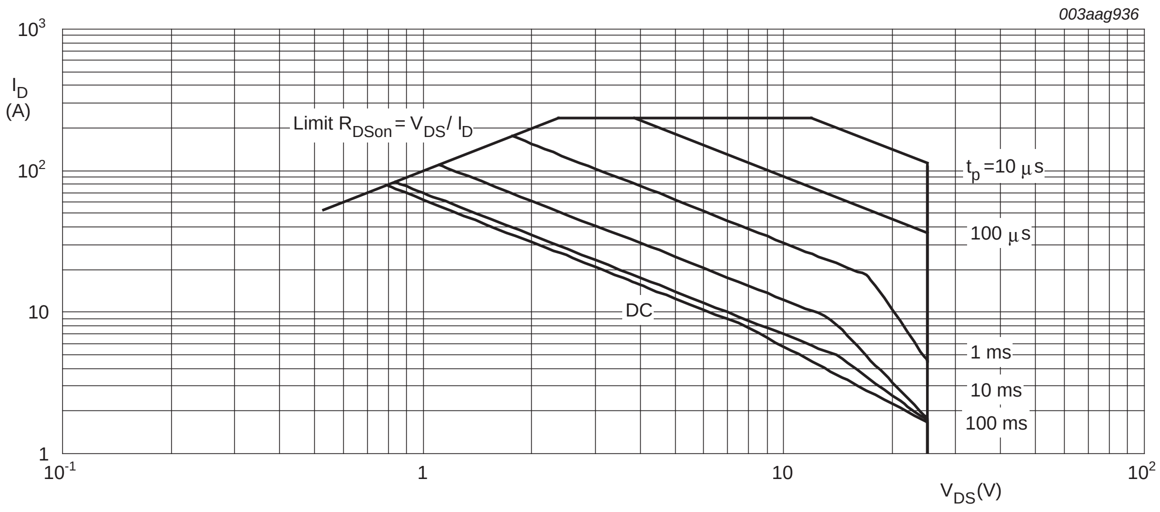
$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25\,°C$; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W

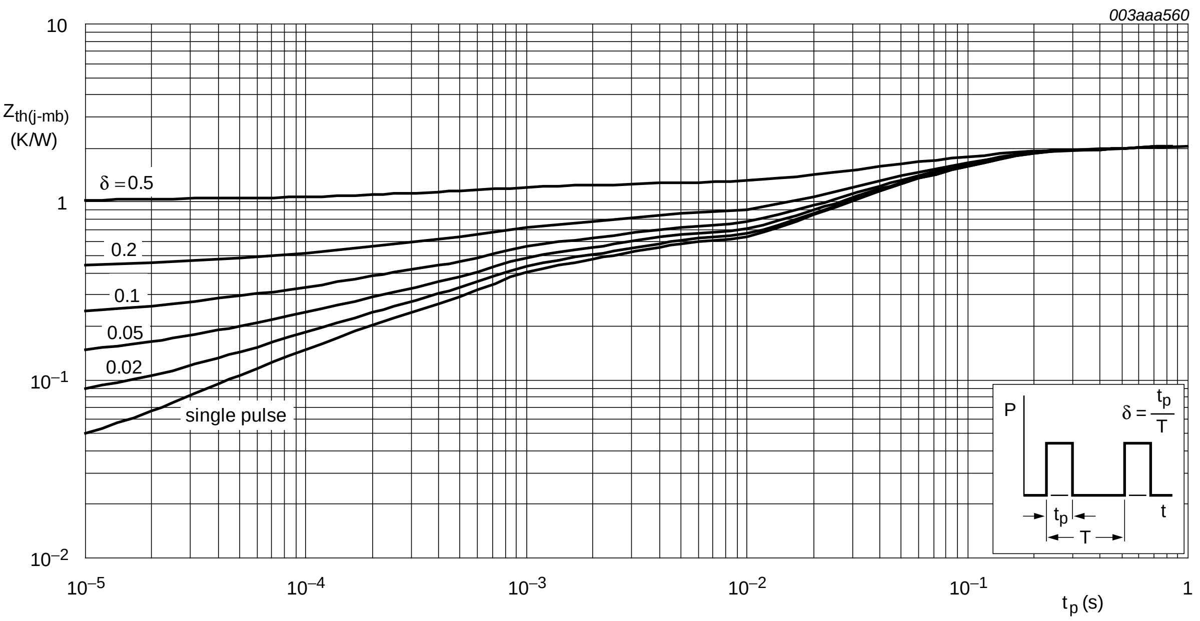


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

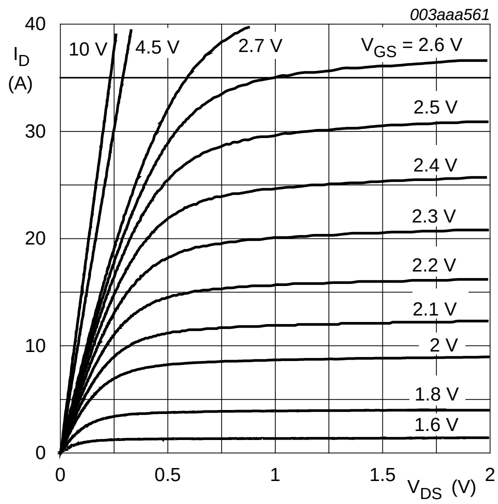
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 7; see Figure 8	-	-	2.2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 7; see Figure 8	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 7; see Figure 8	1	1.5	2	V
I_{DSS}	drain leakage current	V_{DS} = 25 V; V_{GS} = 0 V; T_j = 25 °C	-	0.06	1	µA
		V_{DS} = 25 V; V_{GS} = 0 V; T_j = 150 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; see Figure 9; see Figure 10	-	7.5	10.1	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 °C; see Figure 9; see Figure 10	-	11.8	15.2	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see Figure 9; see Figure 10	-	7.4	9.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 9; see Figure 10	-	4.7	6.3	mΩ
R_G	internal gate resistance	f = 1 MHz	-	1.8	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see Figure 11; see Figure 12	-	13.3	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 4.5 V	-	11.1	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see Figure 11; see Figure 12	-	4.9	-	nC
Q_{GS1}	pre-threshold gate-source charge		-	2.6	-	nC
Q_{GS2}	post-threshold gate-source charge		-	2.3	-	nC
Q_{GD}	gate-drain charge		-	3.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 12 V; see Figure 11; see Figure 12	-	2.4	-	V
C_{iss}	input capacitance	V_{DS} = 0 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	2420	-	pF
		V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 13; see Figure 14	-	1871	-	pF
C_{oss}	output capacitance		-	517	-	pF
C_{rss}	reverse transfer capacitance		-	179	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; V_{GS} = 4.5 V; $R_{G(ext)}$ = 4.7 Ω; I_D = 25 A	-	25	-	ns
t_r	rise time		-	25	-	ns
$t_{d(off)}$	turn-off delay time		-	32	-	ns
t_f	fall time		-	12	-	ns

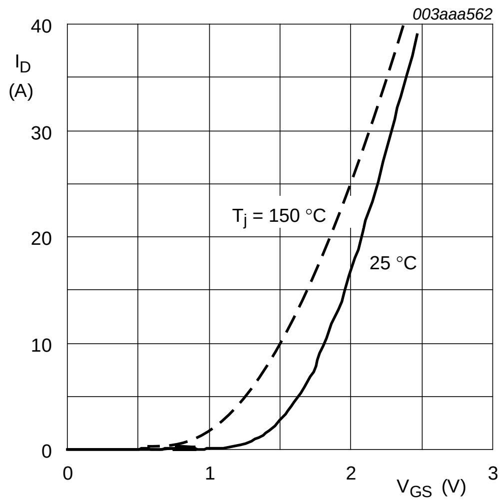
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	-	33	-	ns
Q_r	recovered charge		-	13	-	nC



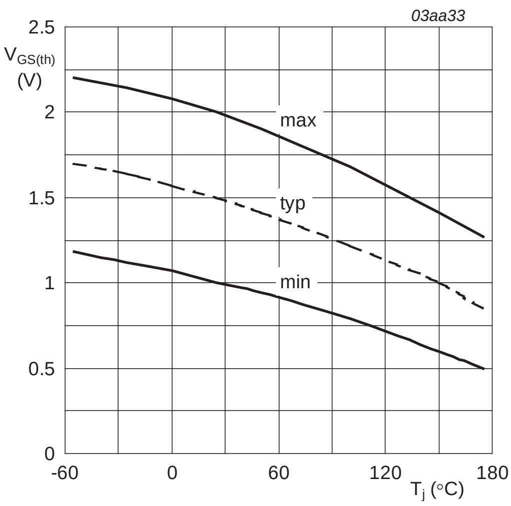
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



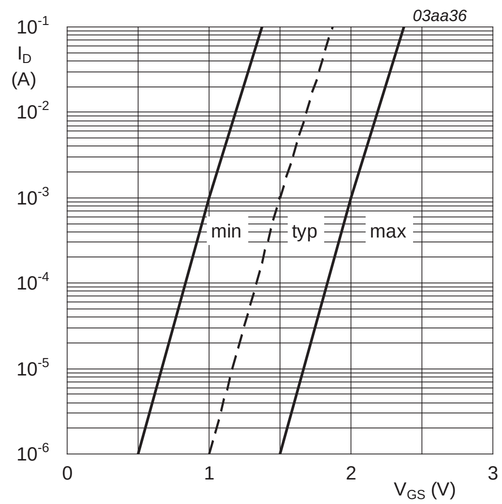
T_j = 25 °C and 150 °C; V_{DS} > I_D X R_{DSon}

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



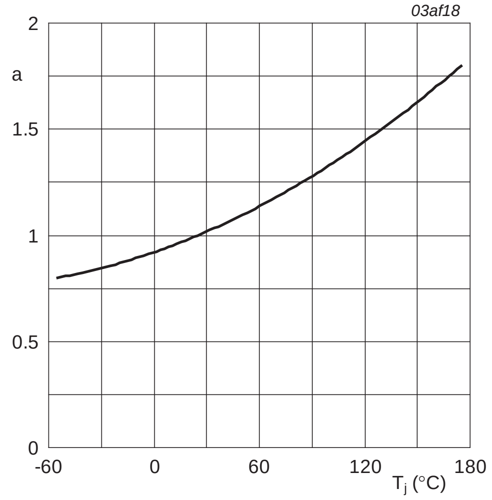
$$I_D = 1mA; V_{DS} = V_{GS}$$

Fig 7. Gate-source threshold voltage as a function of junction temperature



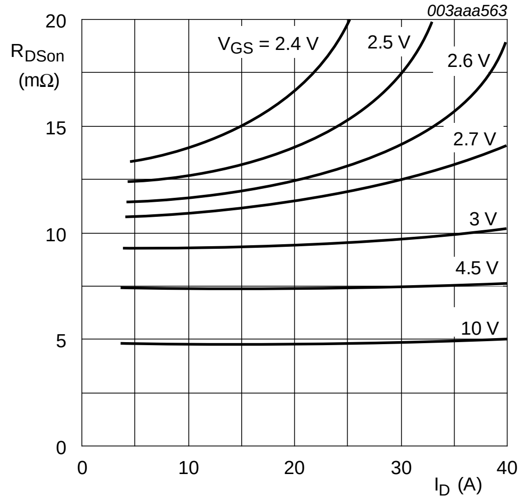
T_j = 25 °C; V_{DS} = 5 V

Fig 8. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C

Fig 10. Drain-source on-state resistance as a function of drain current; typical values

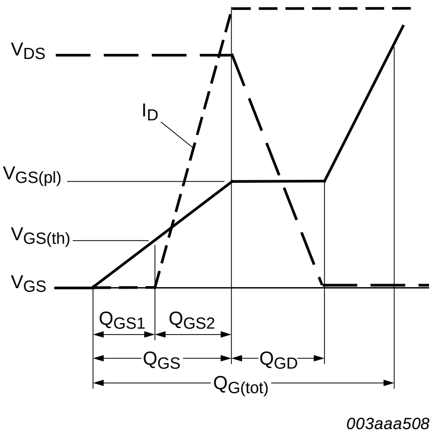
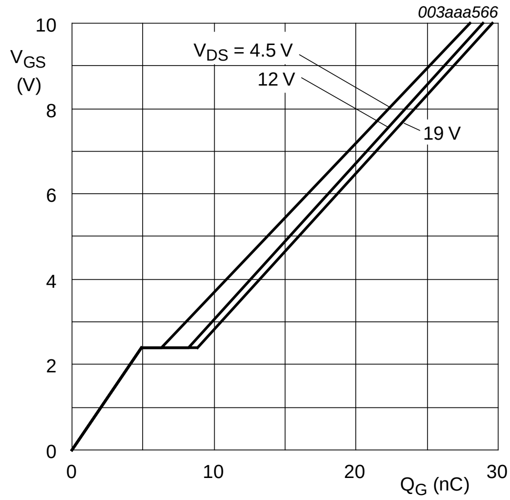
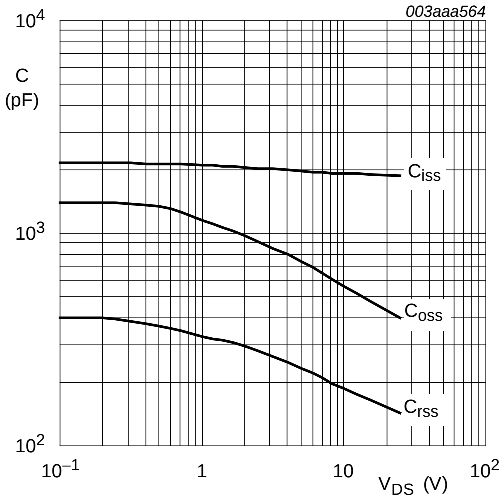


Fig 11. Gate charge waveform definitions



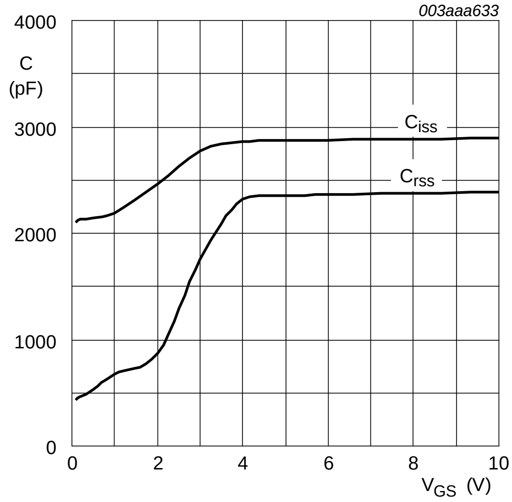
I_D = 25 A; V_{DS} = 4.5 V, 12 V and 19 V

Fig 12. Gate-source voltage as a function of gate charge; typical values



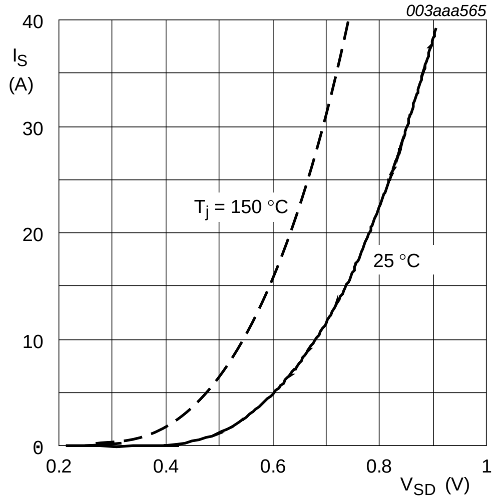
V_{GS} = 0 V; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



T_j = 25 °C and 150 °C; V_{DS} = 0 V

Fig 14. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

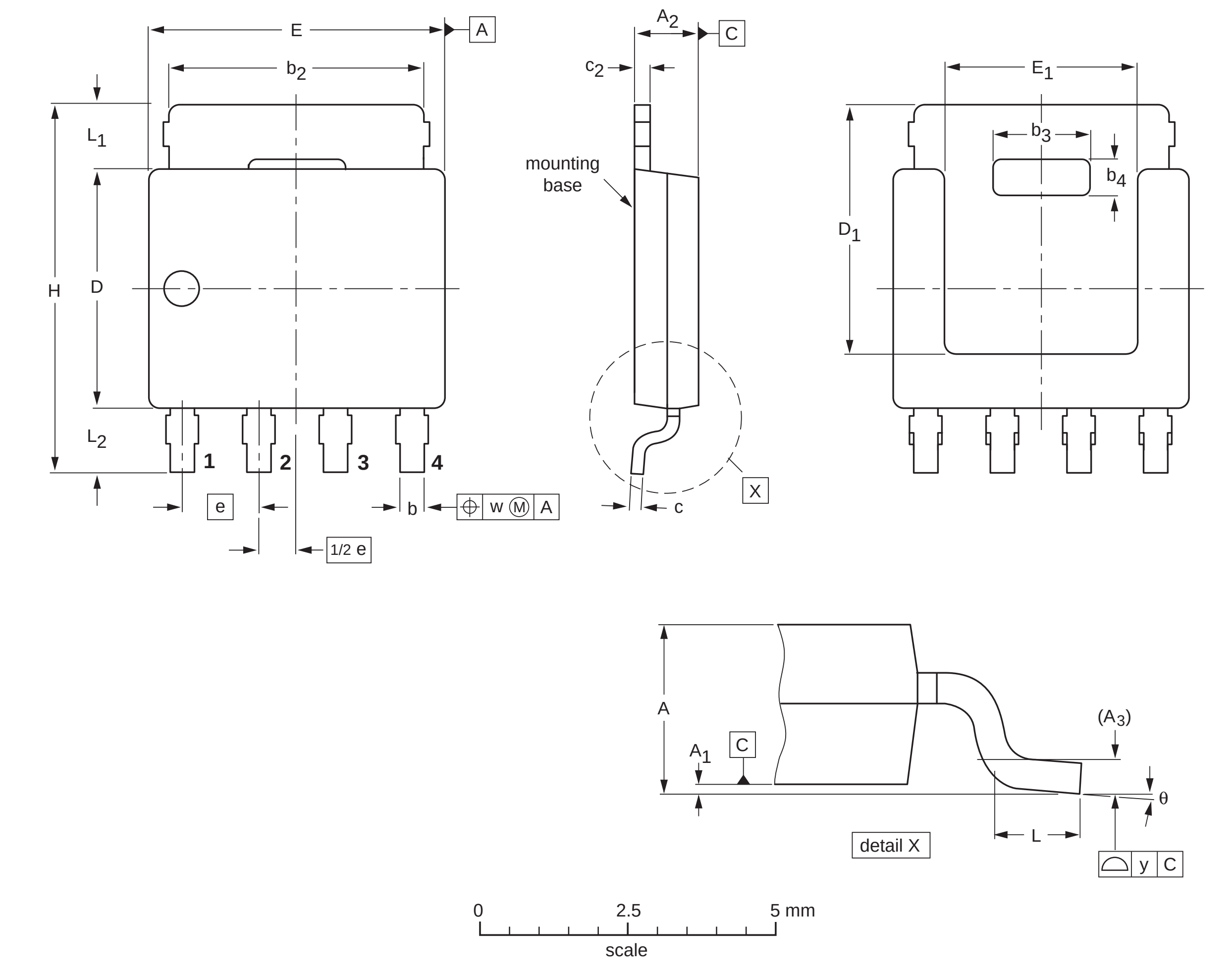


T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPAK; Power-SO8); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1) max	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~06-03-16~~ 11-03-25

Fig 16. Package outline SOT669 (LFPAK; Power-SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH6325L v.2	20111222	Product data sheet	-	PH6325L v.1
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Status changed from preliminary to product.			
PH6325L v.1	20040428	Preliminary data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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10. Contact information

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