PMV48XPAR Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	PMV48XPAR-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	PMV48XPAR
Description	MOSFET P-CH 20V 3.5A TO236AB
Detailed Description	P-Channel 20 V 3.5A (Ta) 510mW (Ta), 4.15W (Tc) Surface Mount TO-236AB

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
PMV48XPAR	Nexperia USA Inc.
Series:	Product Status:
-	Active
FET Type:	Technology:
P-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
20 V	3.5A (Ta)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
2.5V, 4.5V	55mOhm @ 2.4A, 4.5V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
1.25V @ 250µA	11 nC @ 4.5 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±12V	1000 pF @ 10 V
FET Feature:	Power Dissipation (Max):
-	510mW (Ta), 4.15W (Tc)
Operating Temperature:	Grade:
150°C (TJ)	Automotive
Qualification:	Mounting Type:
AEC-Q100	Surface Mount
Supplier Device Package:	Package / Case:
TO-236AB	TO-236-3, SC-59, SOT-23-3
Base Product Number:	
PMV48	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

PMV48XPA

20 V, P-channel Trench MOSFET

10 March 2014 Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- Very fast switching
- AEC-Q101 qualified

3. Applications

- High-side loadswitch
- High-speed line driver
- Relay driver
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_{amb} = 25 °C		-	-	-20	V
V_{GS}	gate-source voltage			-12	-	12	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-	-3.5	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -2.4 A; T_j = 25 °C		-	48	55	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

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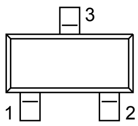
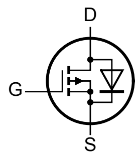
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 TO-236AB (SOT23)	 017aaa094
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV48XPA	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code [1]
PMV48XPA	%DZ

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_{amb} = 25 °C		-	-20	V
V_{GS}	gate-source voltage			-12	12	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-3.5	A
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-2.2	A
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-14	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	510	mW
			[1]	-	930	mW
		T_{sp} = 25 °C		-	4150	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-1	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

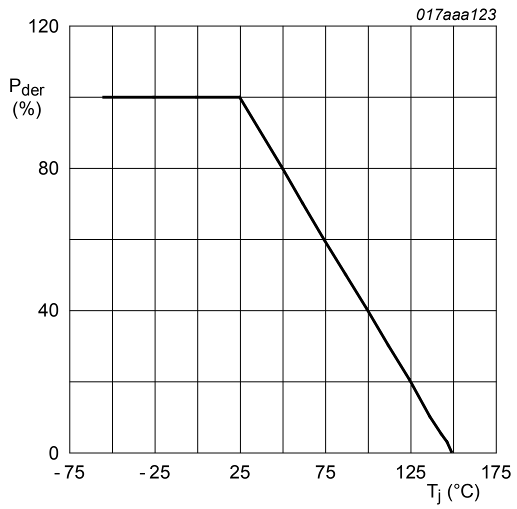


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

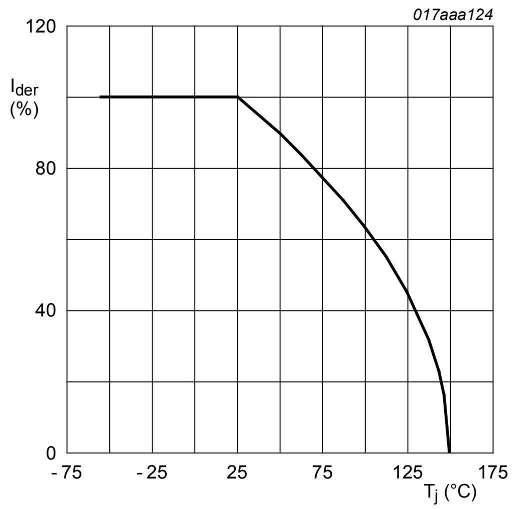
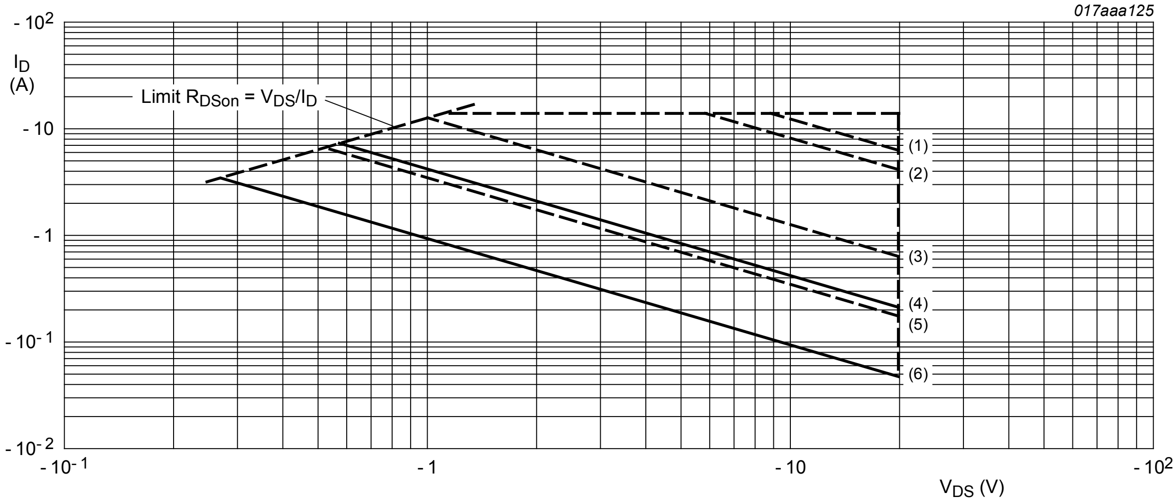


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$



I_{DM} = single pulse

(1) t_p = 100 µs

(2) t_p = 1 ms

(3) t_p = 10 ms

(4) DC; T_{sp} = 25 °C

(5) t_p = 100 ms

(6) DC; T_{amb} = 25 °C; drain mounting pad 6 cm^2

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

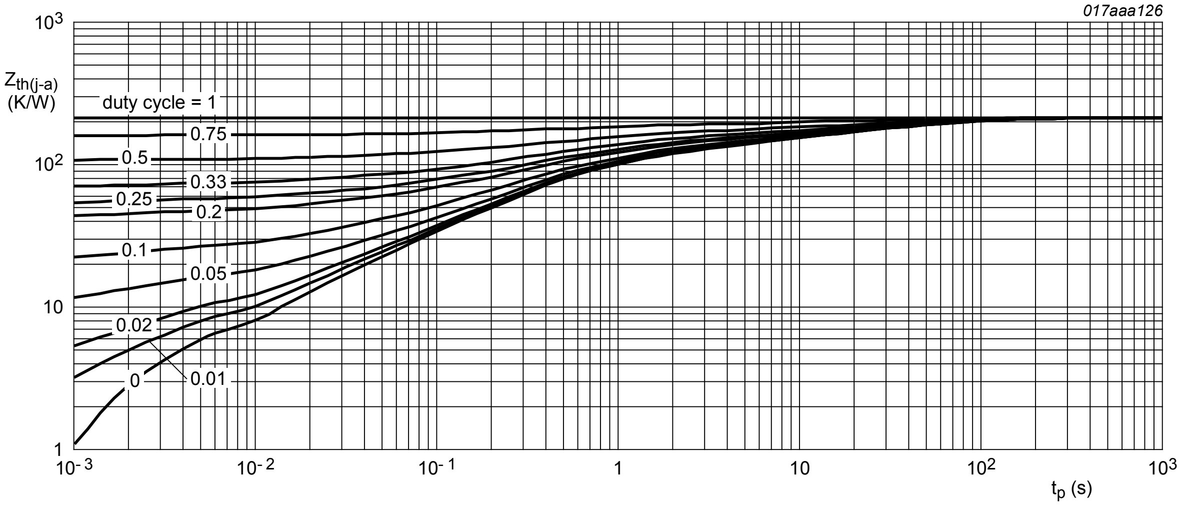
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	213	245	K/W
			[2]	-	117	135	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	25	30	K/W

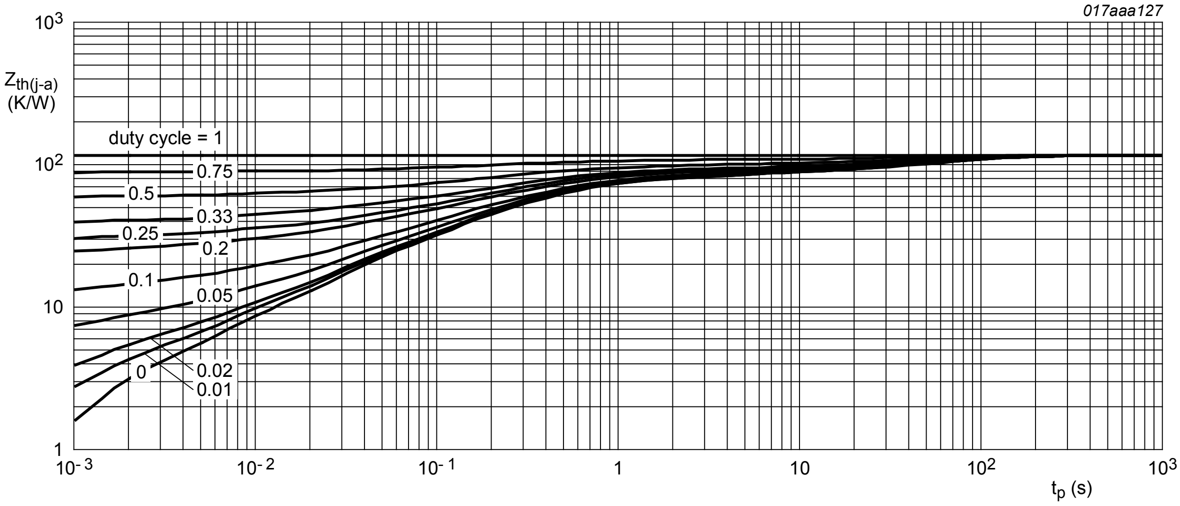
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2.



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



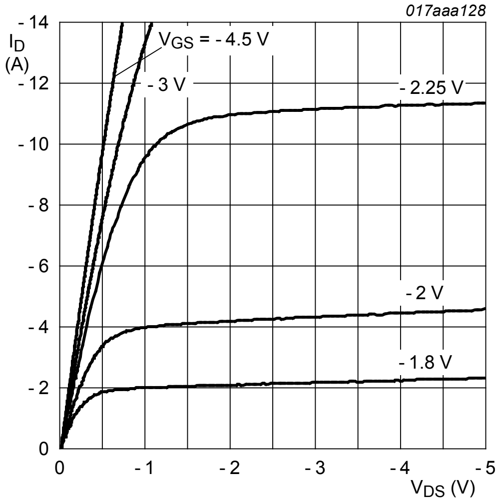
FR4 PCB, mounting pad for drain 6 cm^2

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

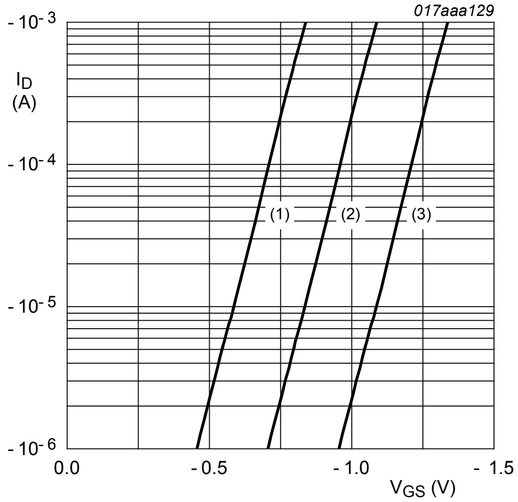
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 μA; V_{GS} = 0 V; T_j = 25 °C		-20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 μA; V_{DS} = V_{GS}; T_j = 25 °C		-0.75	-1	-1.25	V
I_{DSS}	drain leakage current	V_{DS} = -20 V; V_{GS} = 0 V; T_{amb} = 25 °C		-	-	-1	μA
I_{GSS}	gate leakage current	V_{GS} = -12 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -2.4 A; T_j = 25 °C		-	48	55	mΩ
		V_{GS} = -4.5 V; I_D = -2.4 A; T_j = 150 °C		-	70	80	mΩ
		V_{GS} = -2.5 V; I_D = -2 A; T_j = 25 °C		-	71	81	mΩ
g_{fs}	forward transconductance	V_{DS} = -12 V; I_D = -2 A; T_j = 25 °C		-	12	-	S
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = -10 V; I_D = -1 A; V_{GS} = -4.5 V; T_j = 25 °C		-	8.5	11	nC
Q_{GS}	gate-source charge			-	1.8	-	nC
Q_{GD}	gate-drain charge			-	1.8	-	nC
C_{iss}	input capacitance	V_{DS} = -10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	1000	-	pF
C_{oss}	output capacitance			-	130	-	pF
C_{rss}	reverse transfer capacitance			-	90	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -10 V; I_D = -1 A; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	11	-	ns
t_r	rise time			-	13	-	ns
$t_{d(off)}$	turn-off delay time			-	61	-	ns
t_f	fall time			-	23	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = -2.4 A; V_{GS} = 0 V; T_j = 25 °C		-	-0.82	-1.2	V



T_j = 25 °C

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



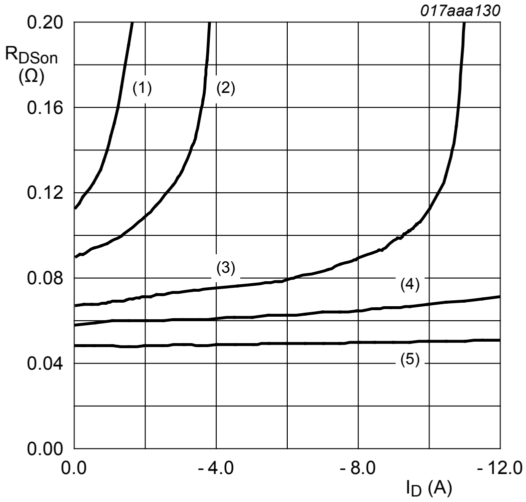
T_j = 25 °C; V_{DS} = -3 V

(1) minimum values

(2) typical values

(3) maximum values

Fig. 7. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

(1) V_{GS} = -1.8 V

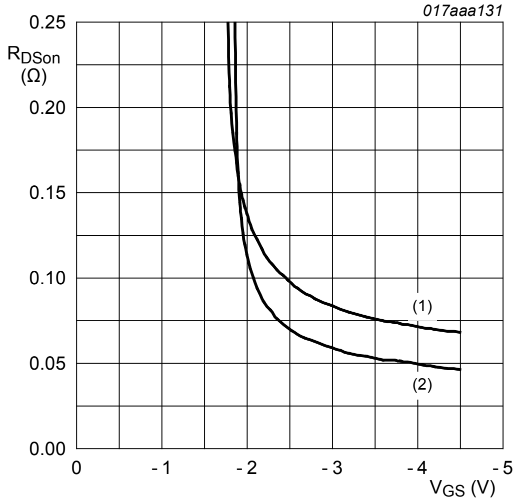
(2) V_{GS} = -2.0 V

(3) V_{GS} = -2.25 V

(4) V_{GS} = -3.0 V

(5) V_{GS} = -4.5 V

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

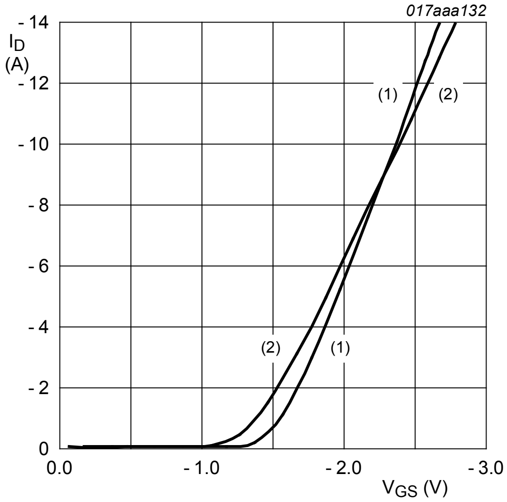


I_D = -2.4 A

(1) T_j = 125 °C

(2) T_j = 25 °C

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$

(1) T_j = 25 °C

(2) T_j = 150 °C

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

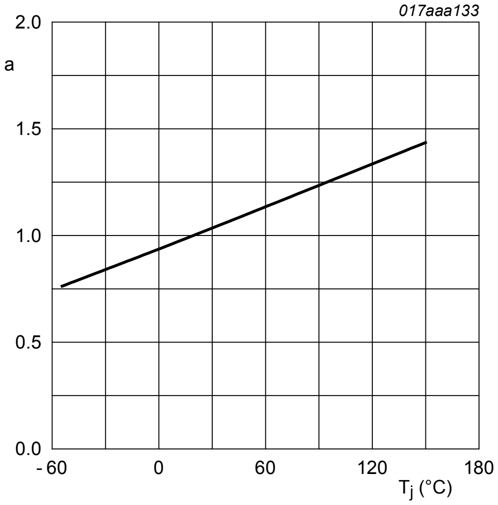
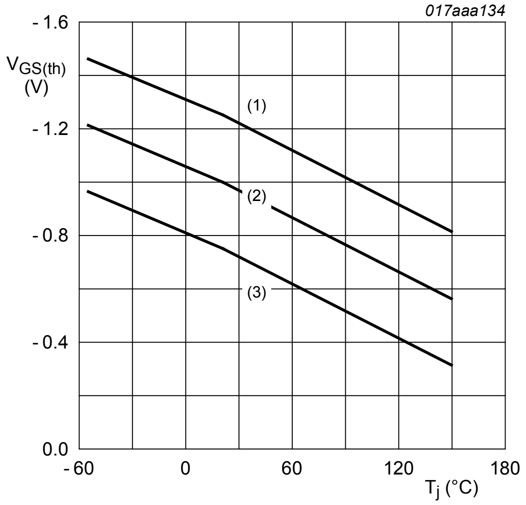


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$



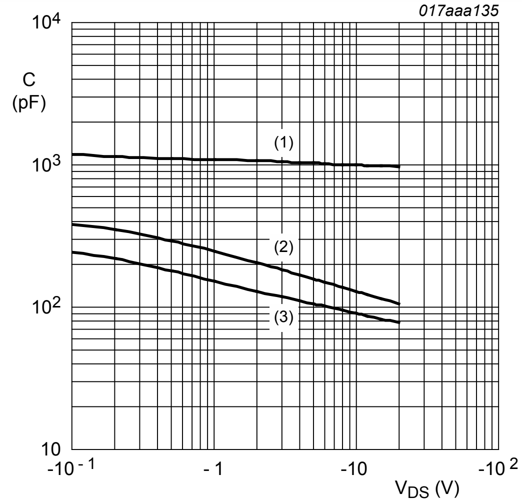
I_D = -0.25 mA; $V_{DS} = V_{GS}$

(1) maximum values

(2) typical values

(3) minimum values

Fig. 12. Gate-source threshold voltage as a function of junction temperature



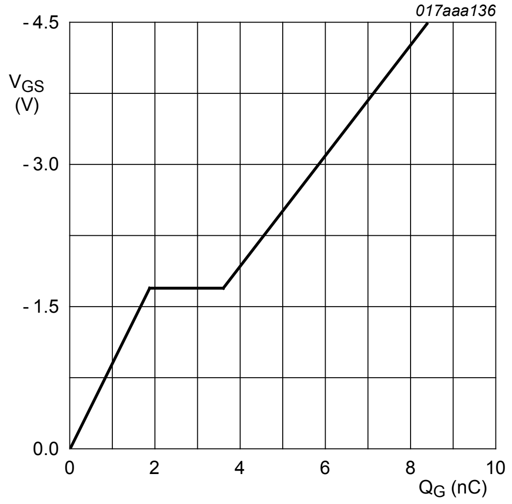
f = 1 MHz; V_{GS} = 0 V

(1) C_{iss}

(2) C_{oss}

(3) C_{rss}

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = -2.4 A; V_{DS} = -10 V; T_{amb} = 25 °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

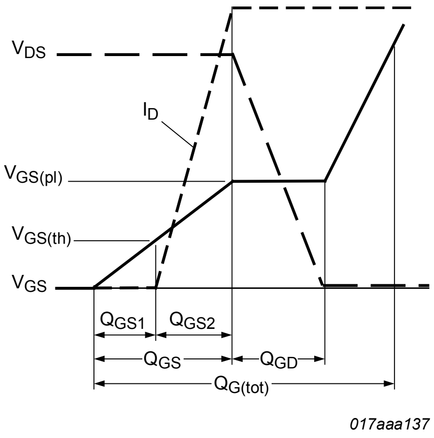
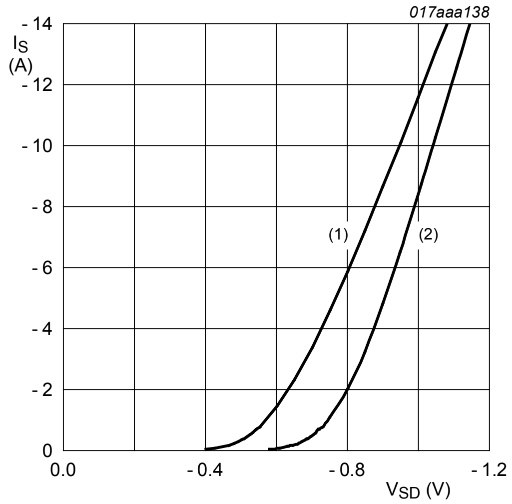


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

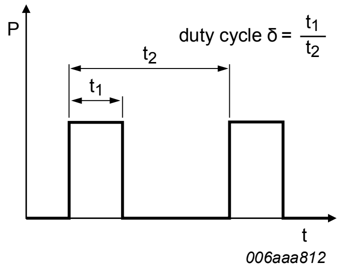


Fig. 17. Duty cycle definition

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

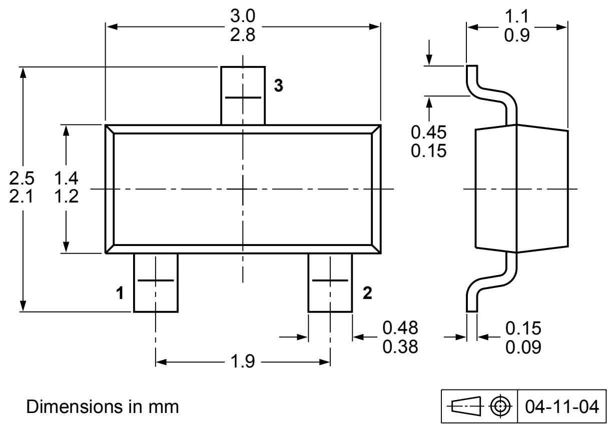


Fig. 18. Package outline TO-236AB (SOT23)

13. Soldering

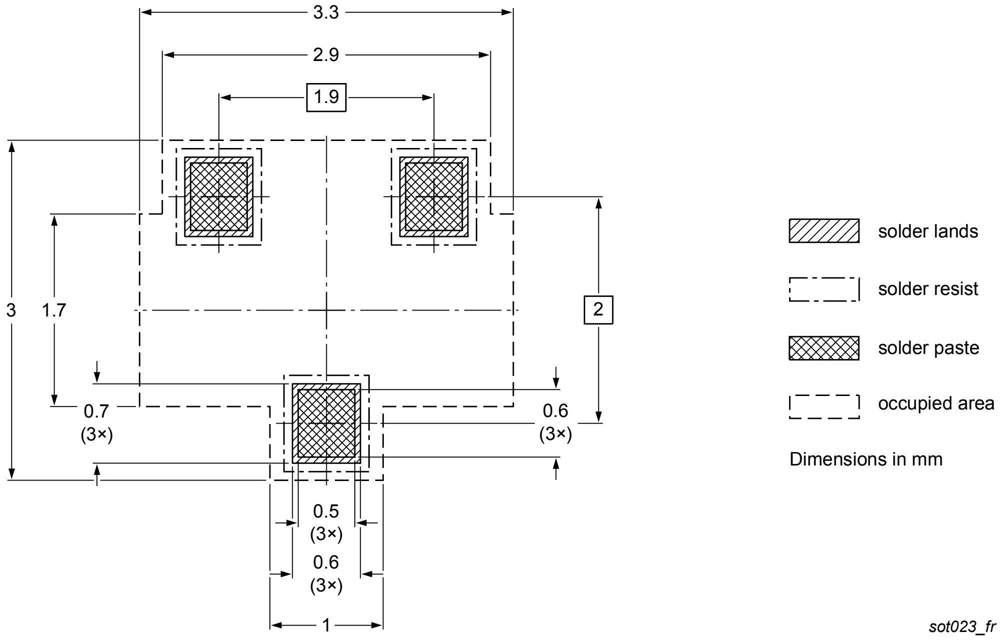


Fig. 19. Reflow soldering footprint for TO-236AB (SOT23)

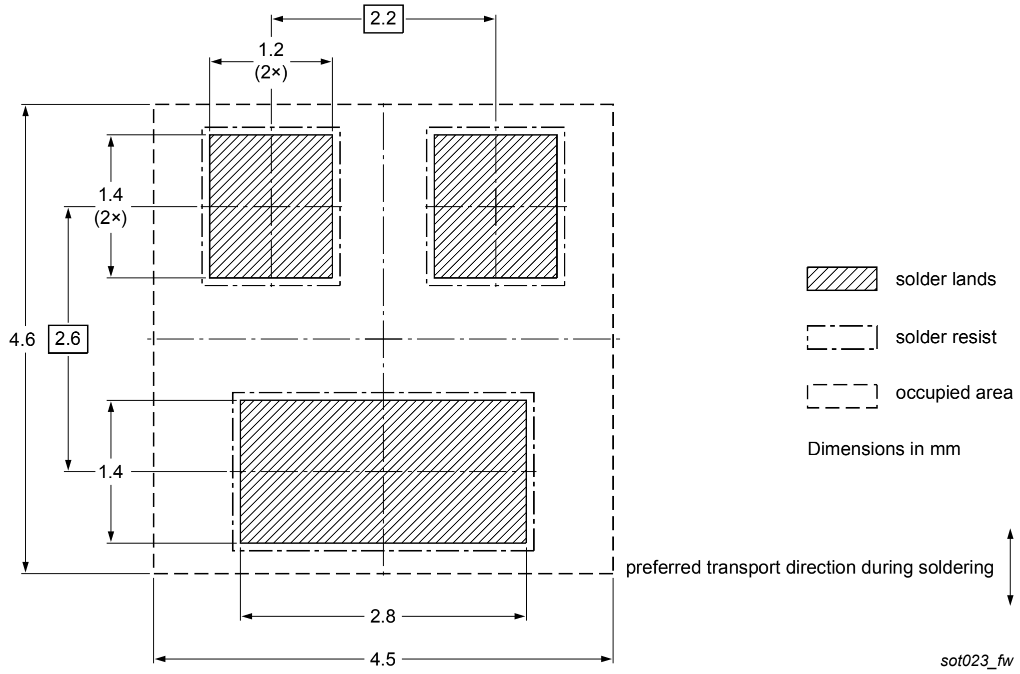


Fig. 20. Wave soldering footprint for TO-236AB (SOT23)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMV48XPA v.1	20140310	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contents

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Date of release: 10 March 2014

DiGi Electronics

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