

PMV52ENEAR Datasheet



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DiGi Electronics Part Number	PMV52ENEAR-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	PMV52ENEAR
Description	MOSFET N-CH 30V 3.2A TO236AB
Detailed Description	N-Channel 30 V 3.2A (Ta) 630mW (Ta), 5.7W (Tc) Surface Mount TO-236AB



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Purchase and inquiry

Manufacturer Product Number:

PMV52ENEAR

Series:

-

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

30 V

Drive Voltage (Max Rds On, Min Rds On):

4.5V, 10V

Vgs(th) (Max) @ Id:

2.5V @ 250µA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 175°C (Tj)

Qualification:

AEC-Q101

Supplier Device Package:

TO-236AB

Base Product Number:

PMV52

Manufacturer:

Nexperia USA Inc.

Product Status:

Active

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

3.2A (Ta)

Rds On (Max) @ Id, Vgs:

70mOhm @ 3.2A, 10V

Gate Charge (Qg) (Max) @ Vgs:

3.3 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

100 pF @ 15 V

Power Dissipation (Max):

630mW (Ta), 5.7W (Tc)

Grade:

Automotive

Mounting Type:

Surface Mount

Package / Case:

TO-236-3, SC-59, SOT-23-3

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



PMV52ENEAR

30 V, N-channel Trench MOSFET

7 May 2019

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Extended temperature range $T_j = 175\text{ °C}$
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 1 kV HBM (class H1C)
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

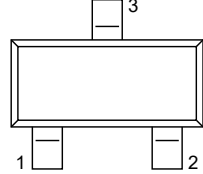
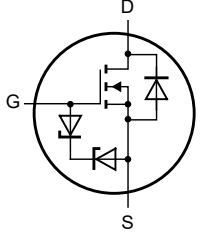
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	30	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	3.2	A
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 3.2\text{ A}; T_j = 25\text{ °C}$	-	52	70	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm^2 .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-236AB (SOT23)</p>	 <p>017aaa255</p>
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV52ENEA	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PMV52ENEA	HQ%

[1] % = placeholder for manufacturing site code

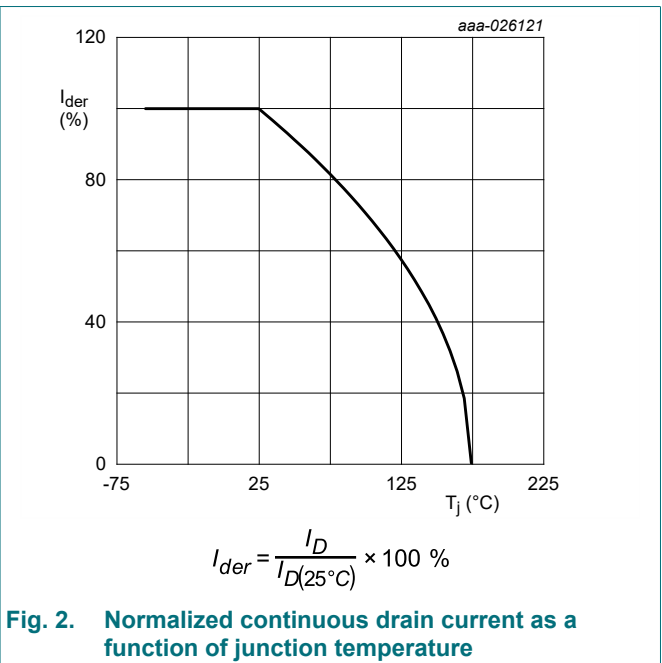
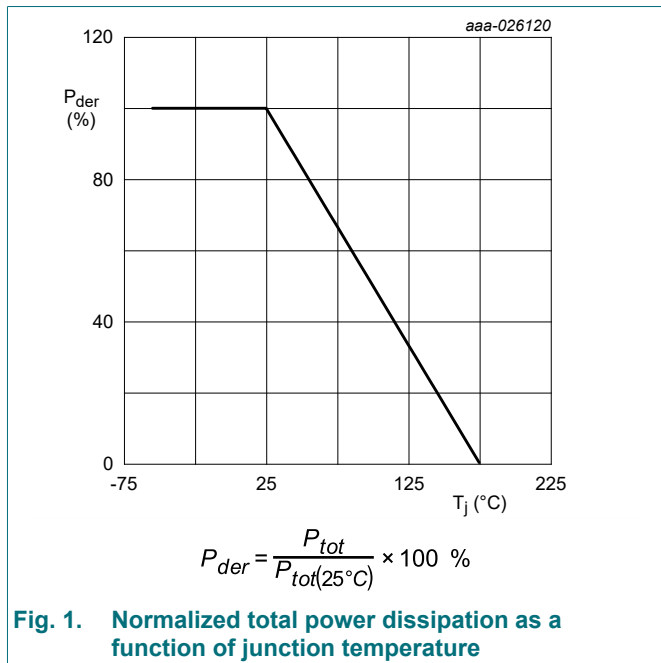
8. Limiting values

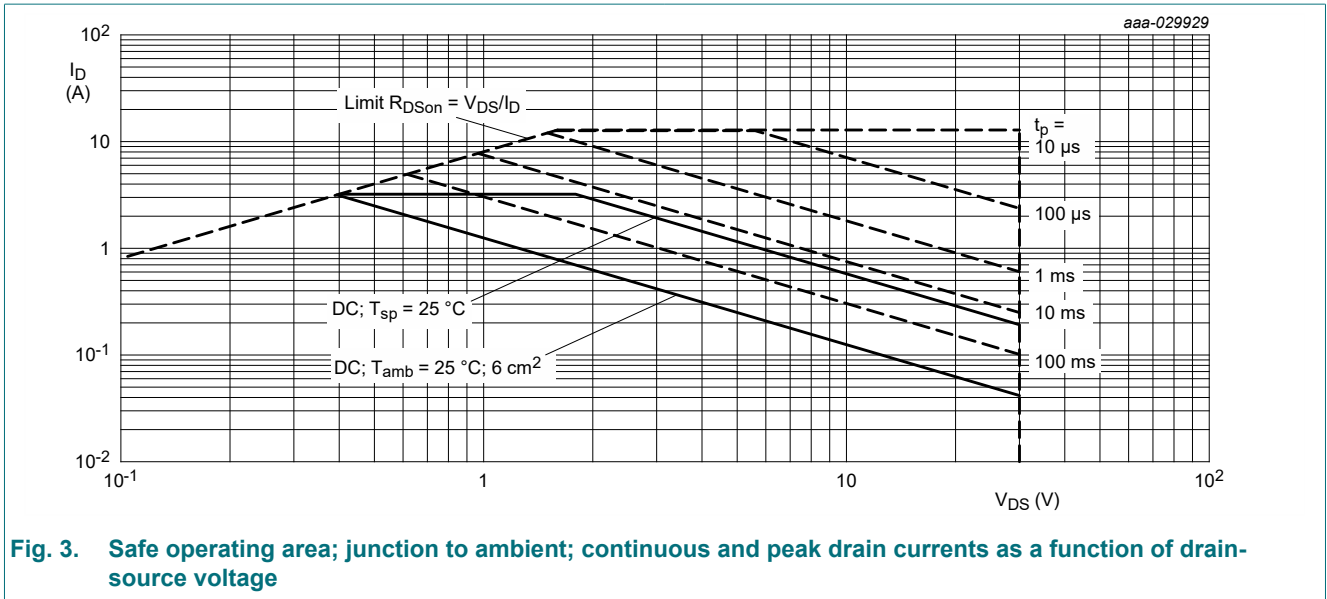
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	3.2	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	13	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	630	mW
			[1]	-	1.25	W
		T _{sp} = 25 °C		-	5.7	W
T _j	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.3	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[3]	-	1000	V
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(initial)} = 25 °C; I _D = 0.25 A; DUT in avalanche (unclamped)		-	3.8	mJ

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	195	235	K/W
			[2]	-	100	120	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	18	26	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

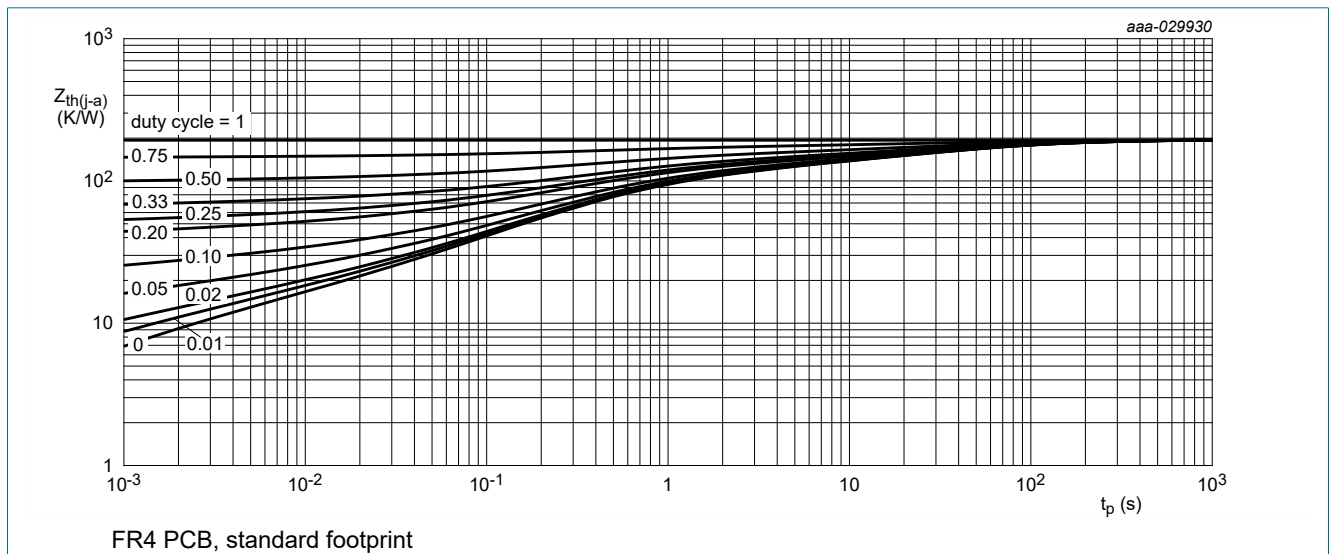


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

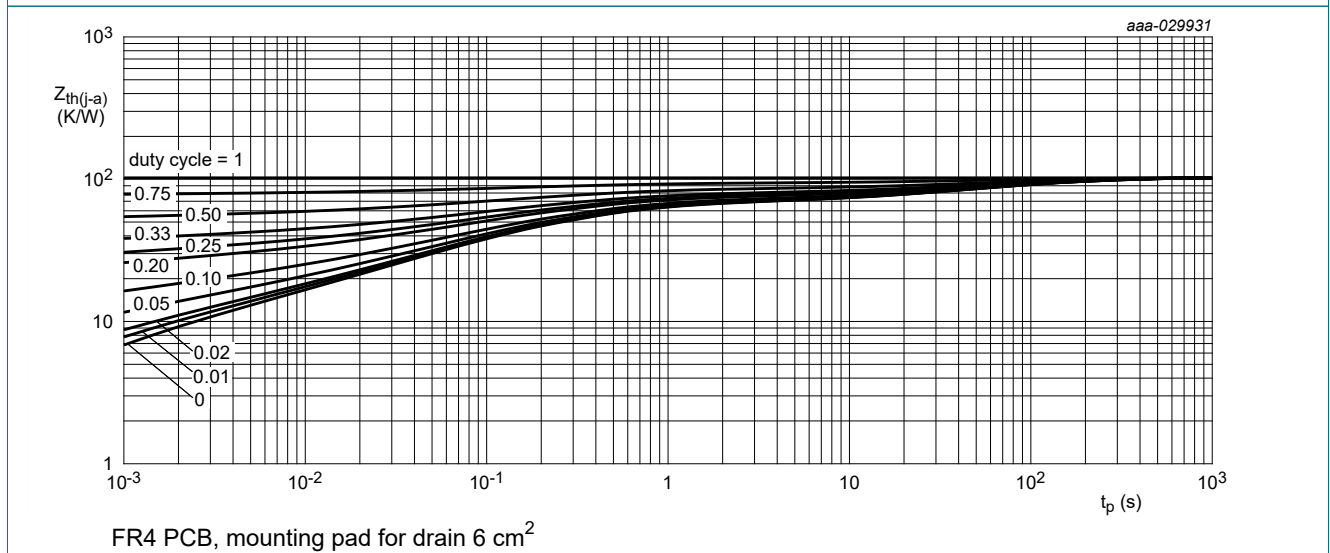


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1	1.5	2.5	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	2	μA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-2	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 3.2 A; T_j = 25 \text{ }^\circ C$	-	52	70	m Ω
		$V_{GS} = 10 V; I_D = 3.2 A; T_j = 175 \text{ }^\circ C$	-	93	124	m Ω
		$V_{GS} = 4.5 V; I_D = 2.7 A; T_j = 25 \text{ }^\circ C$	-	70	100	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V; I_D = 3.2 A; T_j = 25 \text{ }^\circ C$	-	5	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$	-	2	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 V; I_D = 3.2 A; V_{GS} = 10 V; T_j = 25 \text{ }^\circ C$	-	2.2	3.3	nC
Q_{GS}	gate-source charge		-	0.3	-	nC
Q_{GD}	gate-drain charge		-	0.6	-	nC
C_{iss}	input capacitance	$V_{DS} = 15 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	100	-	pF
C_{oss}	output capacitance		-	30	-	pF
C_{rss}	reverse transfer capacitance		-	19	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V; I_D = 3.2 A; V_{GS} = 10 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	2	-	ns
t_r	rise time		-	13	-	ns
$t_{d(off)}$	turn-off delay time		-	6	-	ns
t_f	fall time		-	3	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.3 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 1 A; di/dt = -100 A/\mu s; V_{GS} = 0 V; V_{DS} = 15 V; T_j = 25 \text{ }^\circ C$	-	6	-	ns
Q_r	recovered charge	$V_{DS} = 15 V; T_j = 25 \text{ }^\circ C$	-	1	-	nC

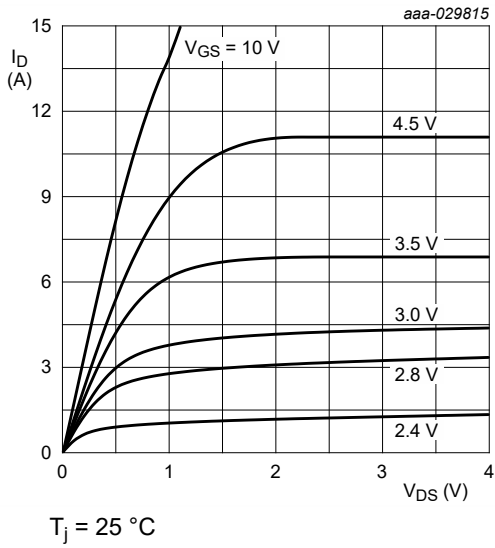


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

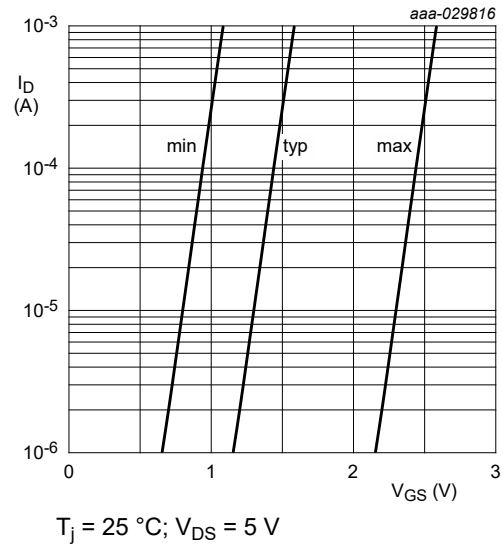


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

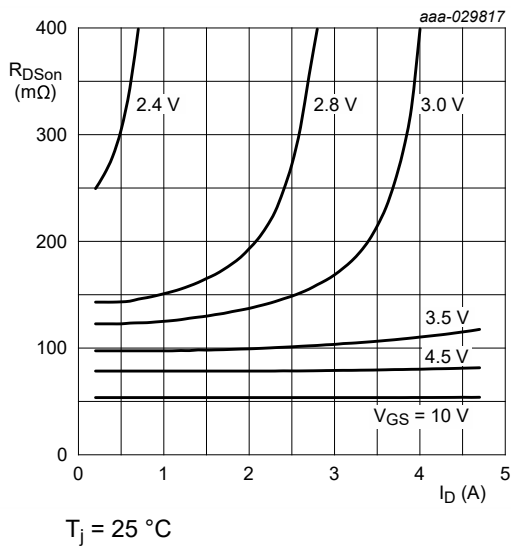


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

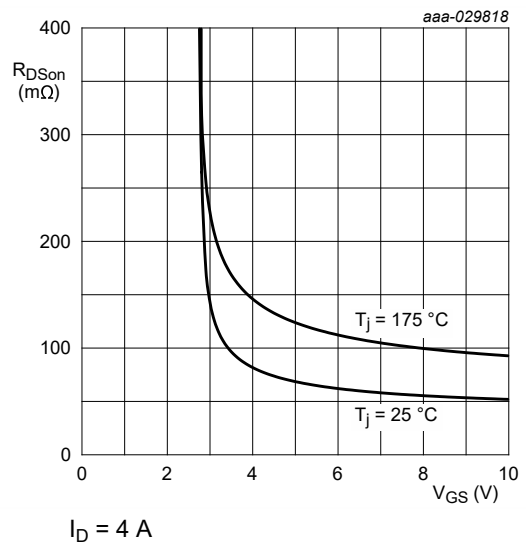
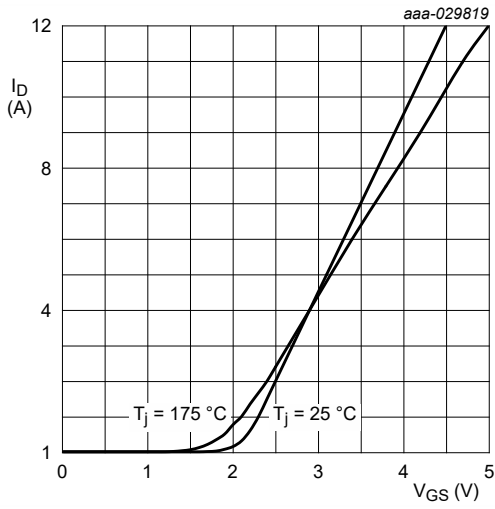
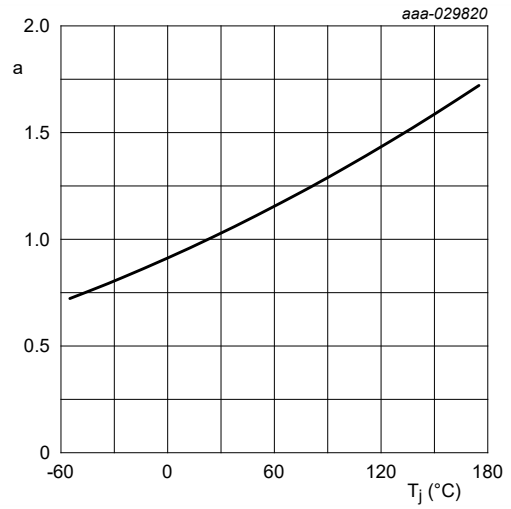


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



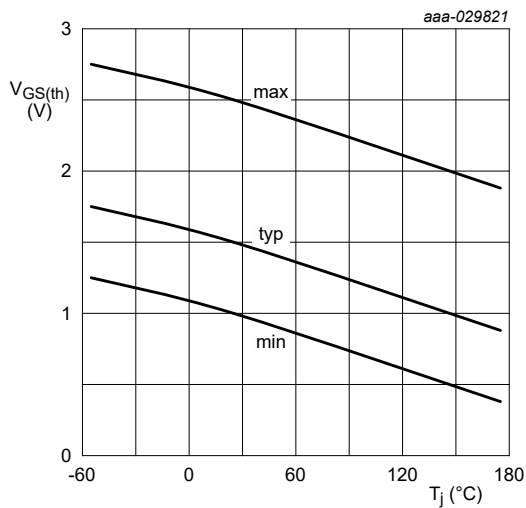
$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



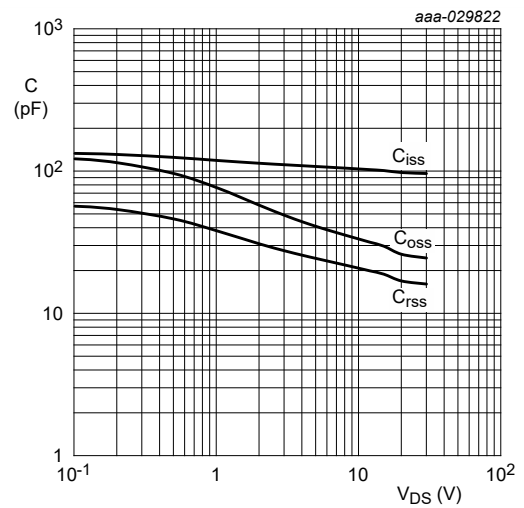
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



$$I_D = 250 \mu A; V_{DS} = V_{GS}$$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

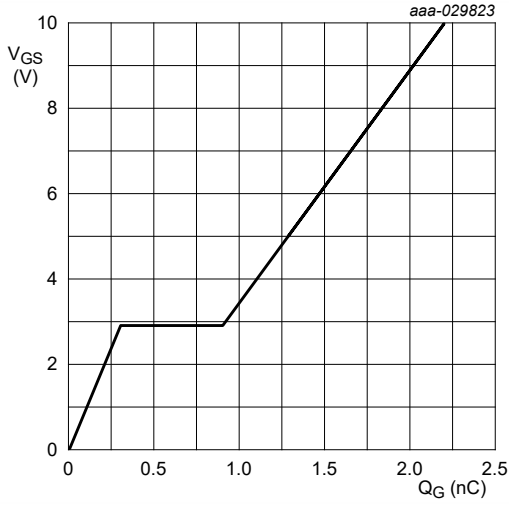


Fig. 14. Gate-source voltage as a function of gate charge; typical values

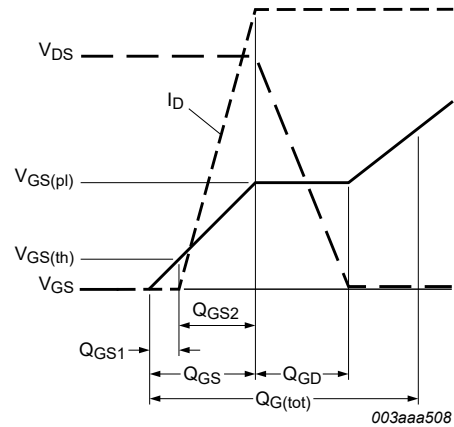


Fig. 15. Gate charge waveform definitions

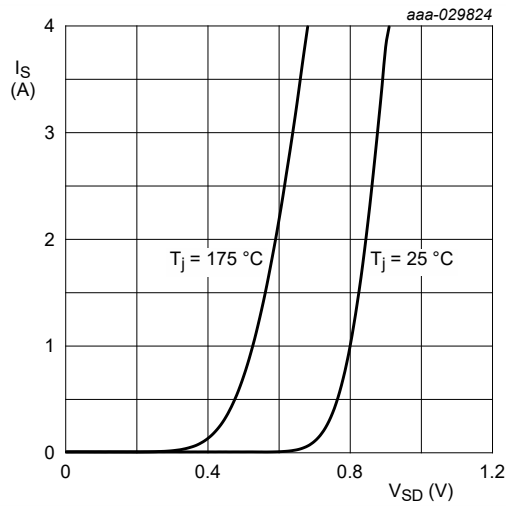


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

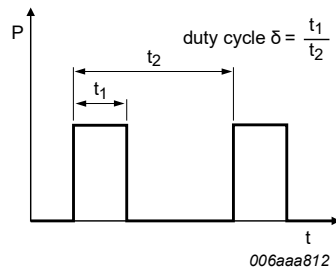


Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

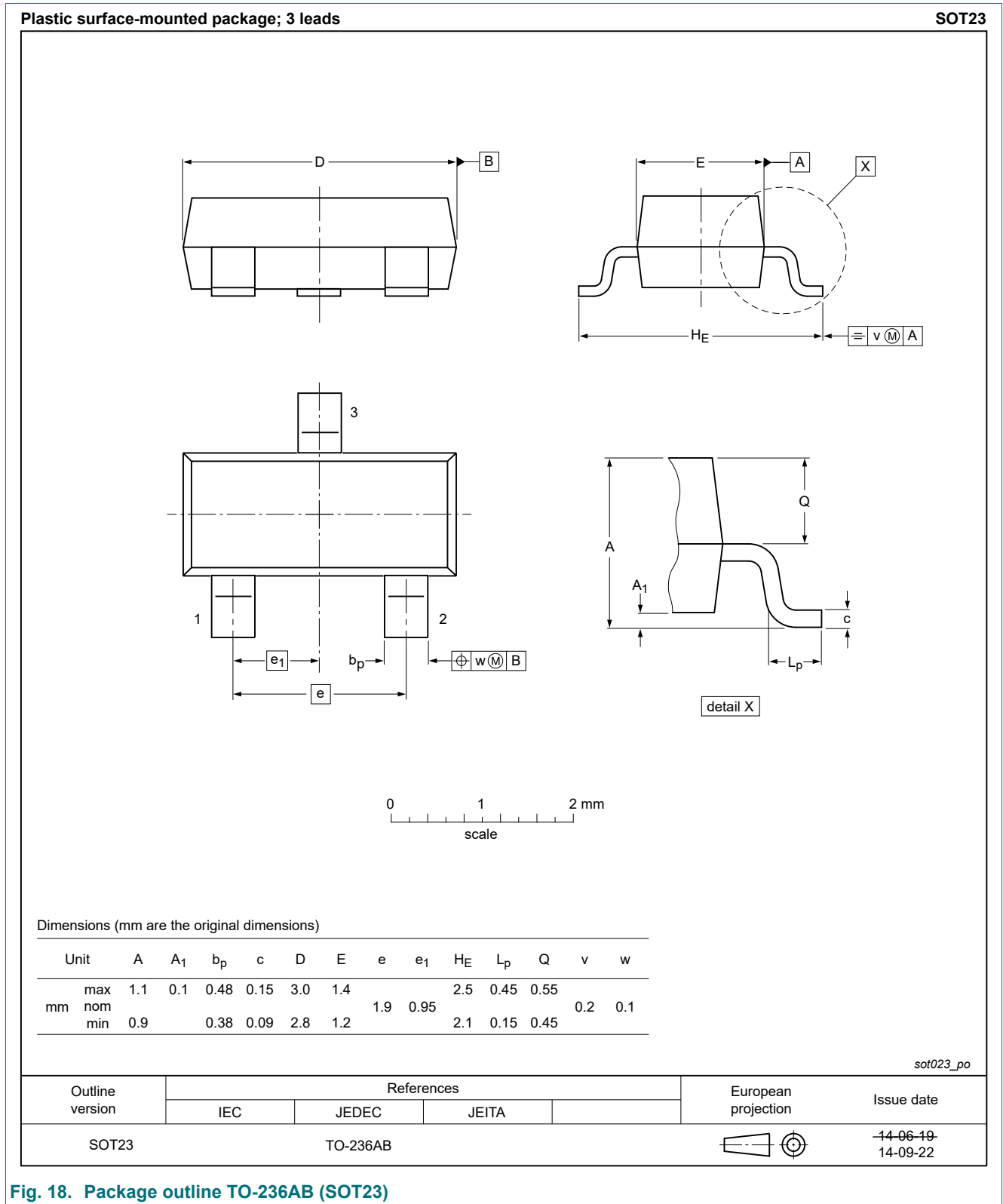


Fig. 18. Package outline TO-236AB (SOT23)

13. Soldering

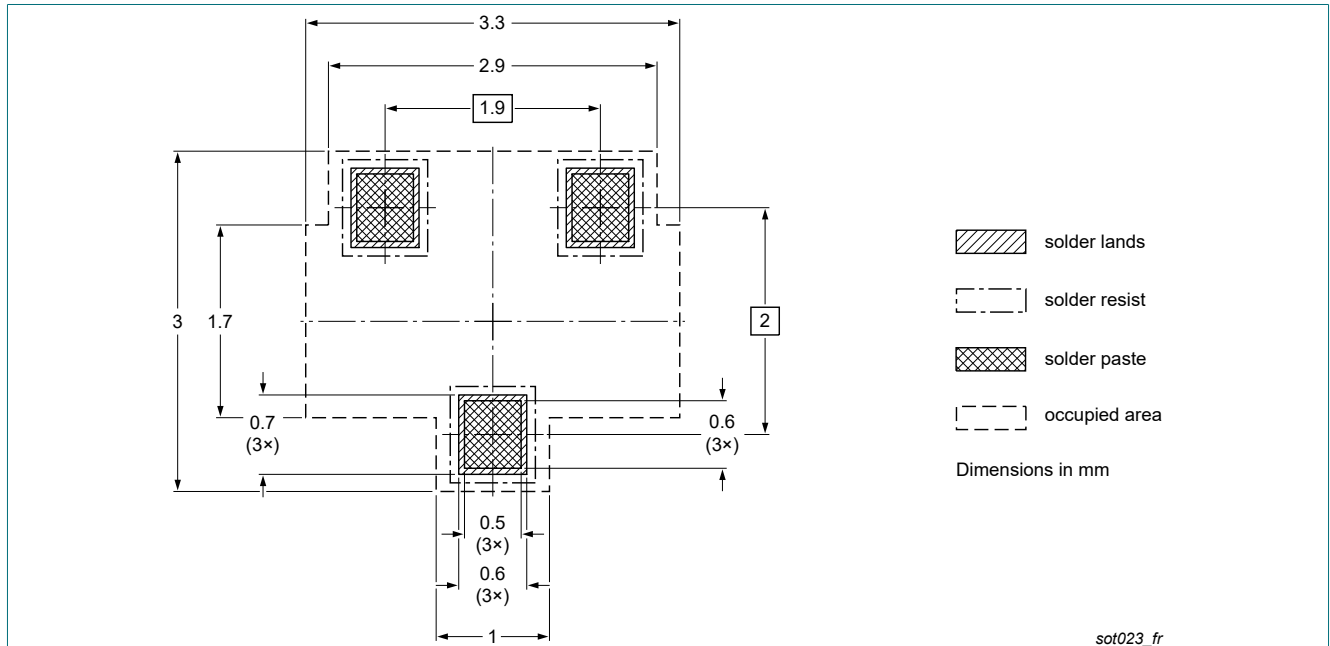


Fig. 19. Reflow soldering footprint for TO-236AB (SOT23)

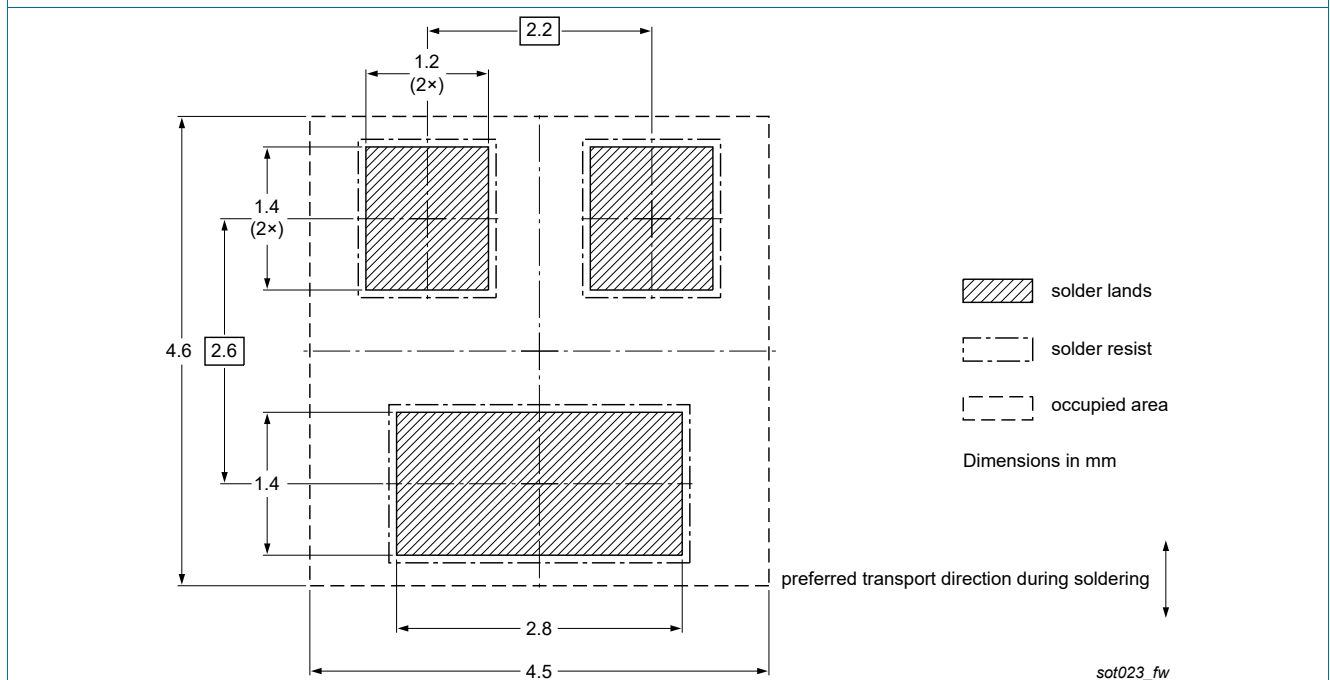


Fig. 20. Wave soldering footprint for TO-236AB (SOT23)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMV52ENEA v.1	20190507	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 7 May 2019

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