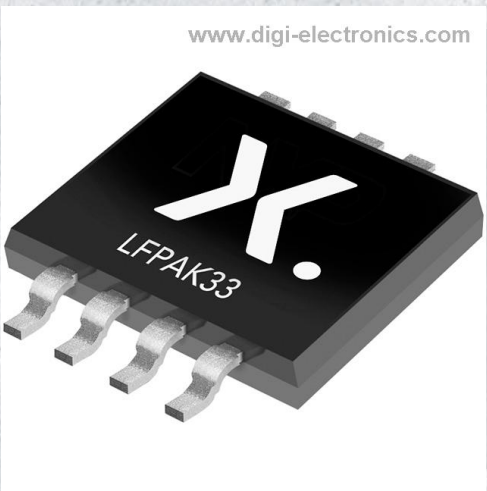
PSMN040-100MSEX Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	PSMN040-100MSEX-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	PSMN040-100MSEX
Description	MOSFET N-CH 100V 30A LFPAK33
Detailed Description	N-Channel 100 V 30A (Tj) 91W (Tc) Surface Mount L FPAK33

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
PSMN040-100MSEX	Nexperia USA Inc.
Series:	Product Status:
-	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
100 V	30A (Tj)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
10V	36.6mOhm @ 10A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
4V @ 1mA	30 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	1470 pF @ 50 V
FET Feature:	Power Dissipation (Max):
-	91W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 175°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
LFPAK33	SOT-1210, 8-LFPAK33 (5-Lead)
Base Product Number:	
PSMN040	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

PSMN040-100MSE

N-channel 100 V 36.6 mΩ standard level MOSFET in LFPAK33 designed specifically for high power PoE applications

26 March 2013 **Product data sheet**

1. General description

New standards and proprietary approaches are enabling Power-over-Ethernet (PoE) systems capable of delivering up to 90W to each powered device (PD). Such solutions place increased demands on the power sourcing equipment (PSE) in terms of “soft-start”, thermal management and power density requirements.

2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Low Rdson for low conduction losses
- Ultra reliable LFPAK33 package for superior thermal and ruggedness performance
- Very low I_{DSS}

3. Applications

- High power PoE applications (60W and higher)
- IEEE802.3at and proprietary solutions

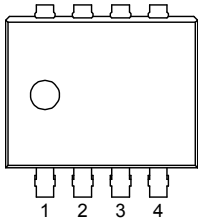
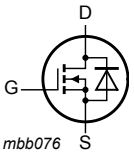
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	100	V
I_D	drain current	$T_j = 25$ °C; $V_{GS} = 10$ V; Fig. 1		-	-	30	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 2		-	-	91	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A; $T_j = 25$ °C; Fig. 13		-	29.4	36.6	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 10$ A; $V_{DS} = 50$ V; $T_j = 25$ °C; Fig. 14; Fig. 15		-	10.7	-	nC
$Q_{G(tot)}$	total gate charge			-	30	-	nC
Avalanche Ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 30$ A; $V_{sup} \leq 100$ V; $R_{GS} = 50$ Ω; unclamped; Fig. 3		-	-	54	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN040-100MSE	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 4 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN040-100MSE	M40E10

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C; $R_{GS} = 20$ kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10$ V; $T_j = 25$ °C; Fig. 1		-	30	A
		$V_{GS} = 10$ V; $T_{mb} = 100$ °C; Fig. 1		-	21	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C; Fig. 4		-	121	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 2		-	91	W
T_{stg}	storage temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	70	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C		-	121	A
Avalanche Ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 30 A; $V_{sup} \leq 100$ V; R_{GS} = 50 Ω; unclamped; Fig. 3		-	54	mJ

[1] Continuous current is limited by package.

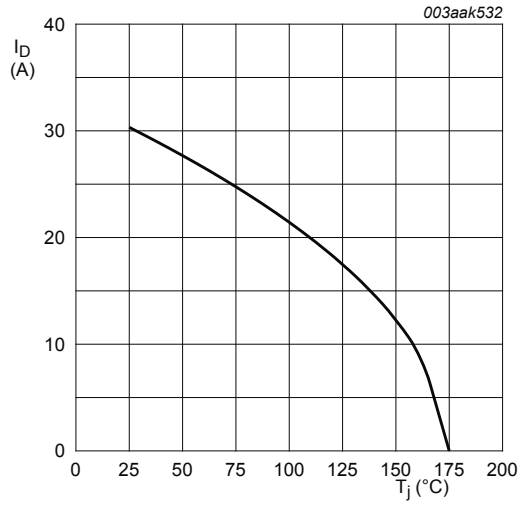


Fig. 1. Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10V$

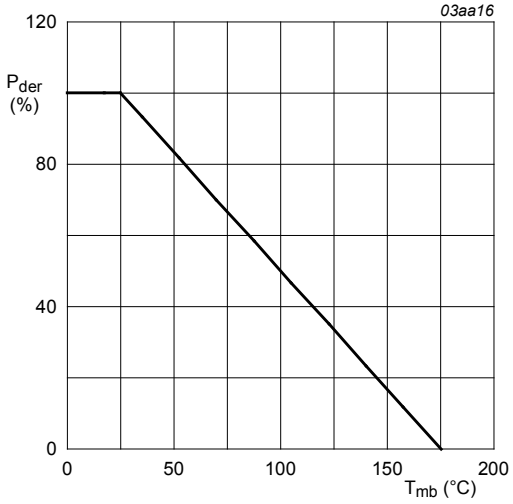


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

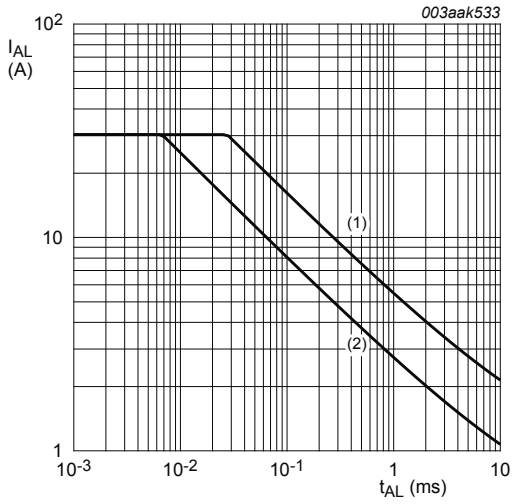


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 100°C$

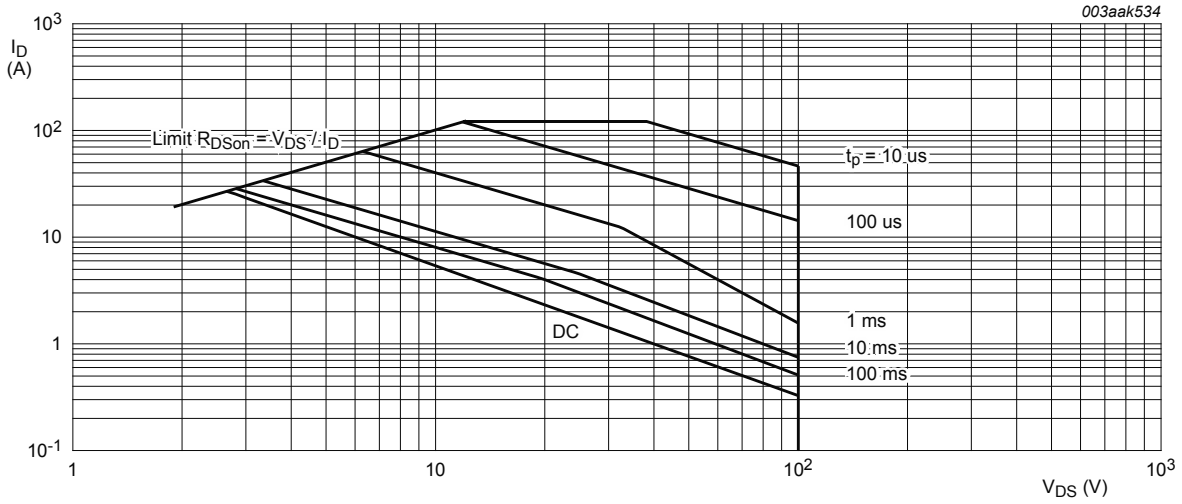


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25°C$; I_{DM} *is a single pulse*

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	1.44	1.65	K/W

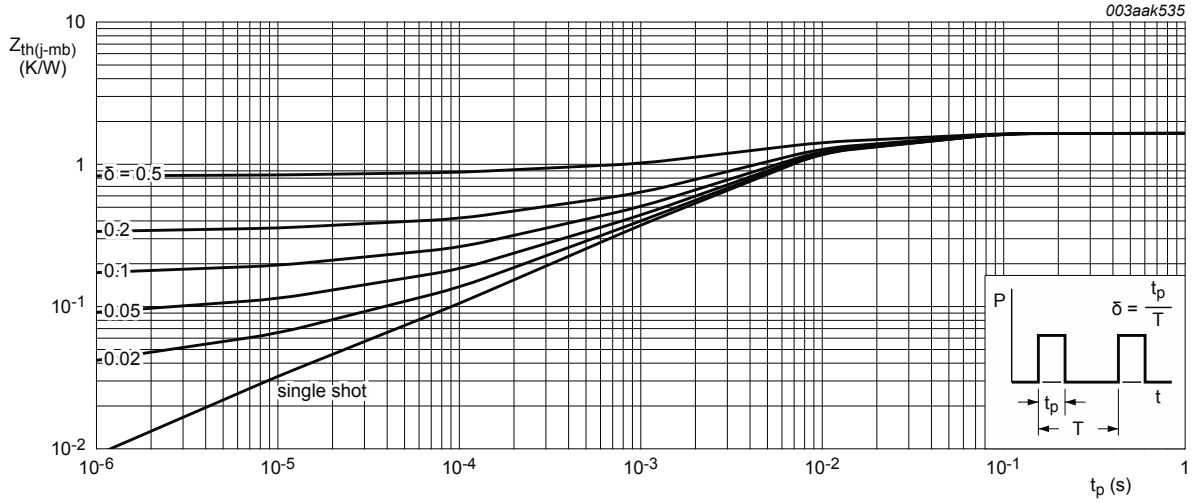


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11		2.3	3.3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 10		-	-	4.6	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 10		1	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.05	1	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 100 °C; Fig. 12; Fig. 13		-	-	66	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 175 °C; Fig. 12; Fig. 13		-	-	99	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 13		-	29.4	36.6	mΩ
R_G	gate resistance	f = 10 MHz		-	1.65	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		-	30	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C		-	24	-	nC
Q_{GS}	gate-source charge	I_D = 10 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		-	7.6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	4.5	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	3.1	-	nC
Q_{GD}	gate-drain charge			-	10.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 10 A; V_{DS} = 50 V; T_j = 25 °C; Fig. 14; Fig. 15		-	5.6	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	1470	-	pF
C_{oss}	output capacitance			-	110	-	pF
C_{rss}	reverse transfer capacitance			-	80	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	8.3	-	ns
t_r	rise time			-	14.1	-	ns
$t_{d(off)}$	turn-off delay time			-	18.7	-	ns
t_f	fall time			-	13	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 20 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.82	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C		-	41	-	ns
Q_r	recovered charge			-	75	-	nC

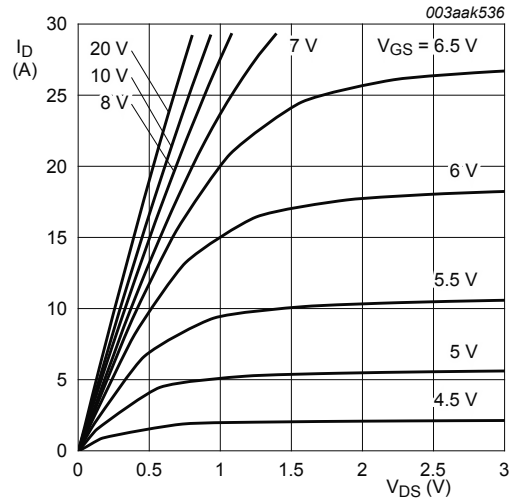


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

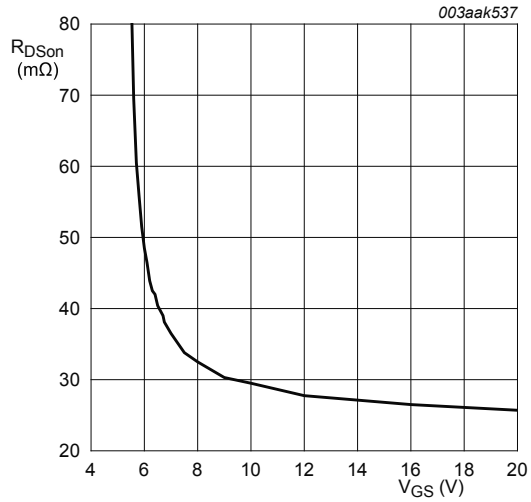


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C;\ I_D = 10A$

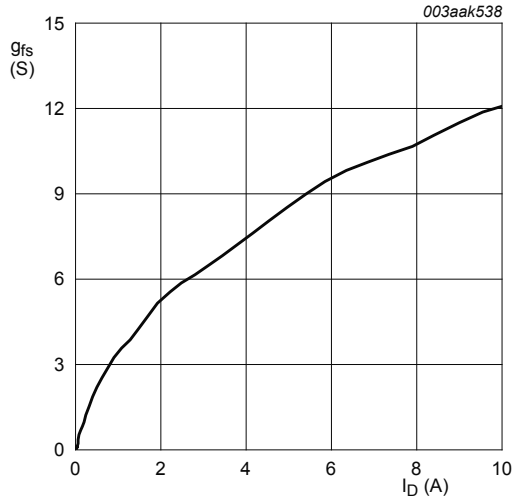


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25°C;\ V_{DS} = 10V$

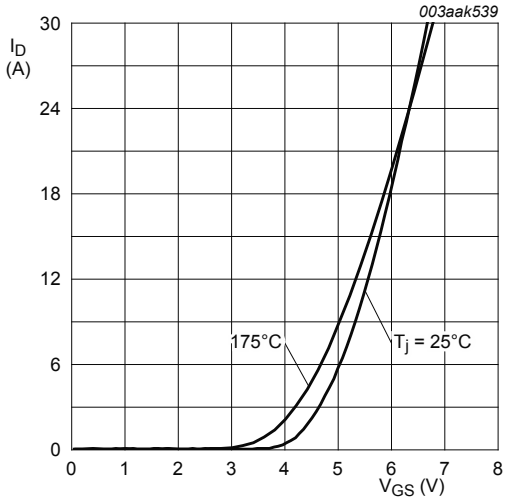


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

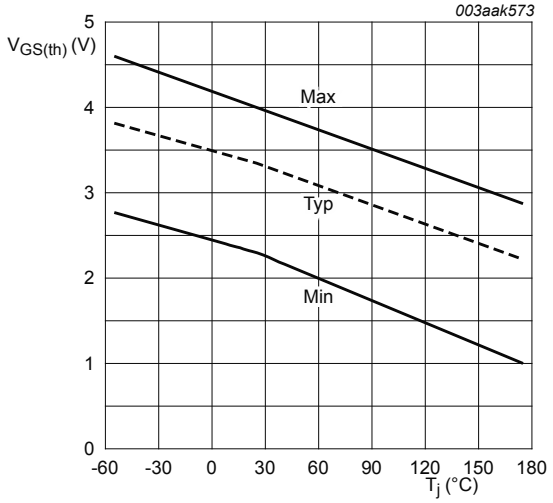


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\ \text{mA};\ V_{DS} = V_{GS}$

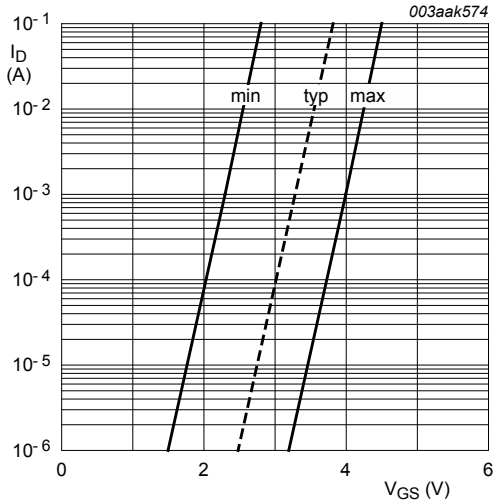


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\,°C;\ V_{DS} = 5V$

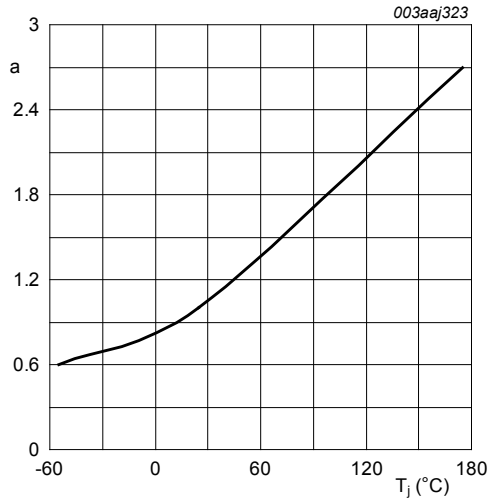


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

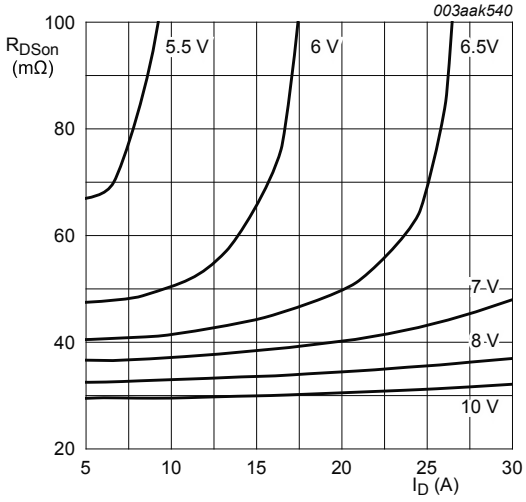


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

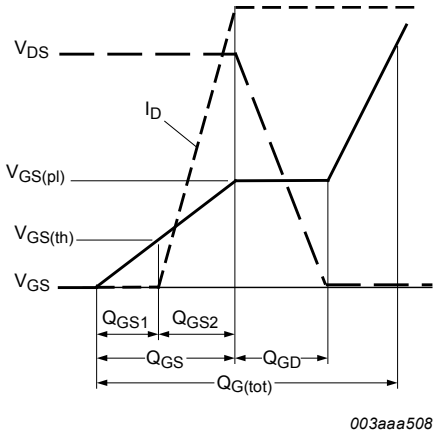


Fig. 14. Gate charge waveform definitions

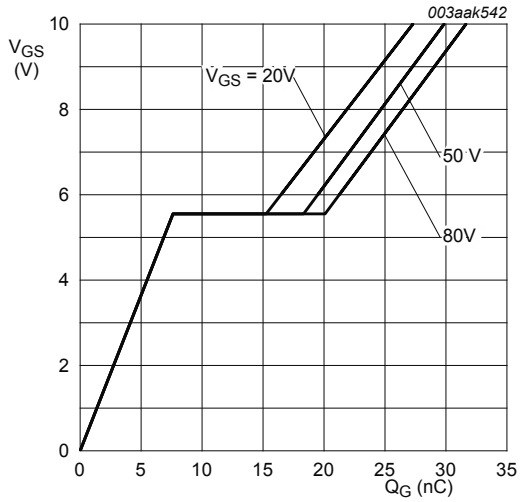


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 10A$

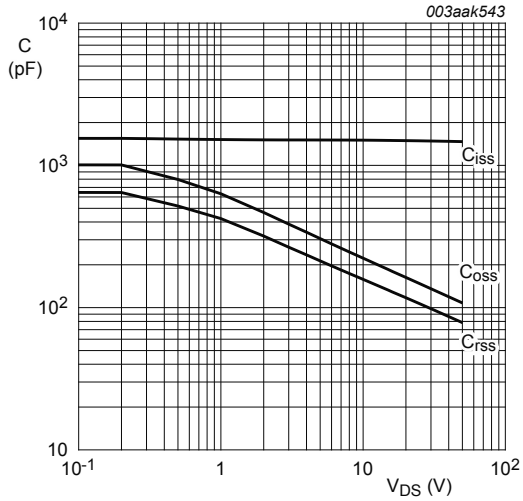


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V;\ f = 1MHz$

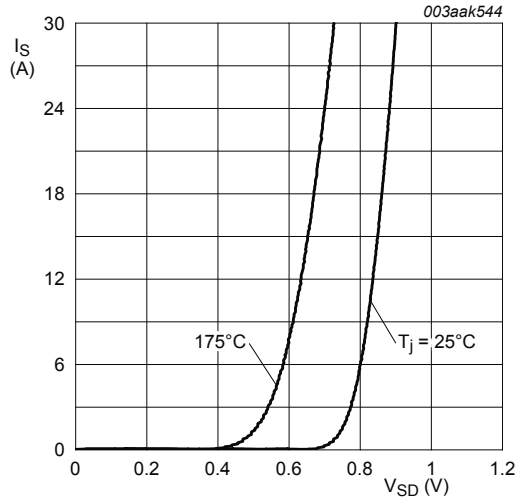
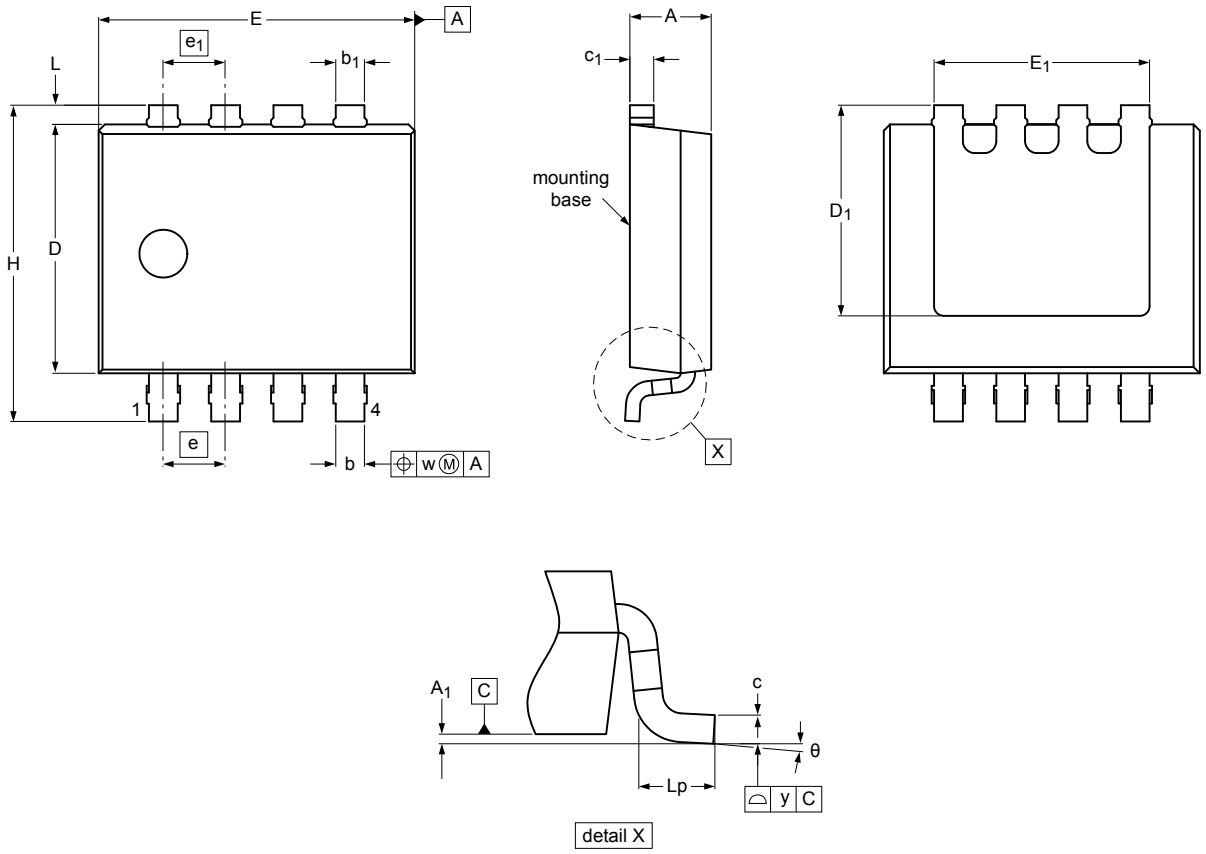


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

11. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit(1)		A	A_1	b	b_1	c	c_1	D(1)	D_1	E(1)	E_1	e	e_1	H	L	L_p	w	y	θ
mm	max	0.90	0.10	0.35	0.35	0.20	0.30	2.70	2.35	3.40	2.45			3.40	0.25	0.50			8°
	nom											0.65	0.65				0.20	0.10	
	min	0.80	0.00	0.25	0.25	0.10	0.20	2.50	1.90	3.20	2.00			3.20	0.13	0.30			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~11-12-19~~ 12-03-12

Fig. 18. Package outline LFPAK33 (SOT1210)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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