PSMN2R0-25MLDX Datasheet

DiGi Electronics Part Number	PSMN2R0-25MLDX-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	PSMN2R0-25MLDX
Description	MOSFET N-CH 25V 70A LFPAK33
Detailed Description	N-Channel 25 V 70A (Tc) 74W (Tc) Surface Mount LF PAK33

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
PSMN2R0-25MLDX	Nexperia USA Inc.
Series:	Product Status:
-	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
25 V	70A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
4.5V, 10V	2.27mOhm @ 25A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
2.2V @ 1mA	34.4 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	2490 pF @ 12 V
FET Feature:	Power Dissipation (Max):
Schottky Diode (Body)	74W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 175°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
LFPAK33	SOT-1210, 8-LFPAK33 (5-Lead)
Base Product Number:	
PSMN2R0	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

PSMN2R0-25MLD

N-channel 25 V, 2.1 mΩ logic level MOSFET in LFPAK33 using NextPowerS3 Technology

8 April 2016 **Product data sheet**

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK33 package. NextPowerS3 portfolio utilising Nexperia's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETS with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- Ultra low Q_G, Q_{GD} and Q_{OSS} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1 µA leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Mini Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Exposed leads for optimal visual solder inspection

3. Applications

- On-board DC:DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

4. Quick reference data

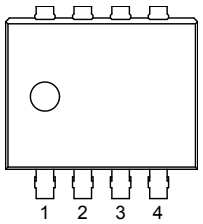
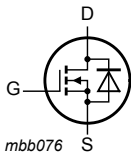
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	25	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	70	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	74	W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	2.5	3.06	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	1.86	2.27	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	34.4	-	nC
		I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	15.9	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	18.9	-	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	3.8	-	nC
Source-drain diode							
S	softness factor	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 12 V; Fig. 16		-	0.9	-	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R0-25MLD	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 8 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R0-25MLD	2D025L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	25	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	25	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	74	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	70	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	70	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	555	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	HBM		800	-	V
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	62	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	555	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 25 A; V_{sup} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 0.89 ms	[1]	-	361	mJ

[1] Protected by 100% test

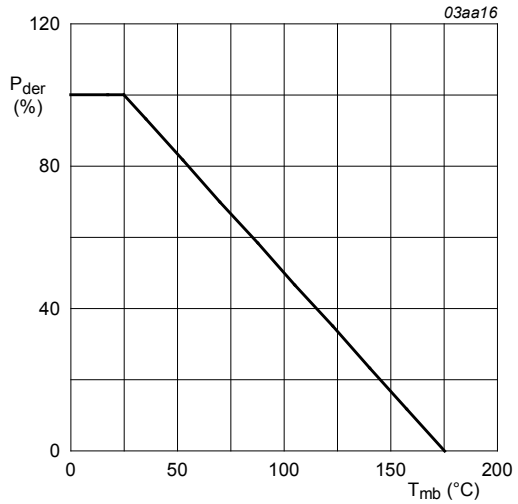
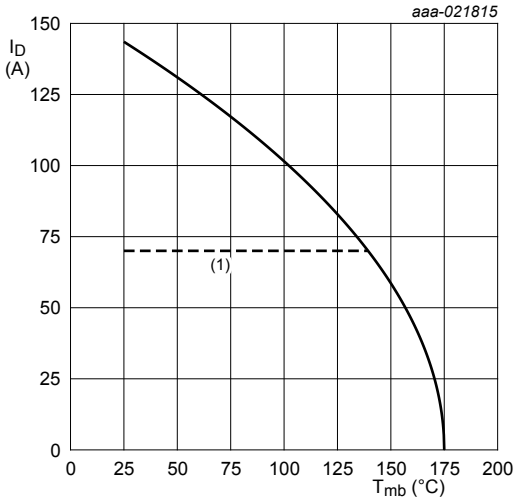


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

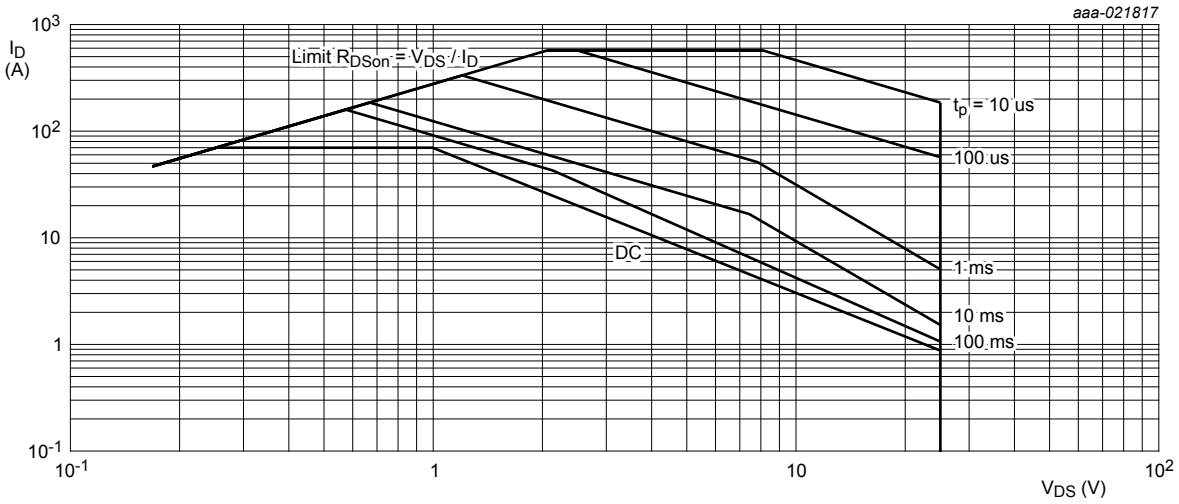


$V_{GS} \geq 10$ V

(1) Capped at 70A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$I_D = 144A \times \sqrt{\frac{175°C - T_{mb}}{150°C}} \quad for \quad T_{mb} \geq 25°C$$



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	1.56	2.02	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5		-	57	-	K/W
		Fig. 6		-	178	-	K/W

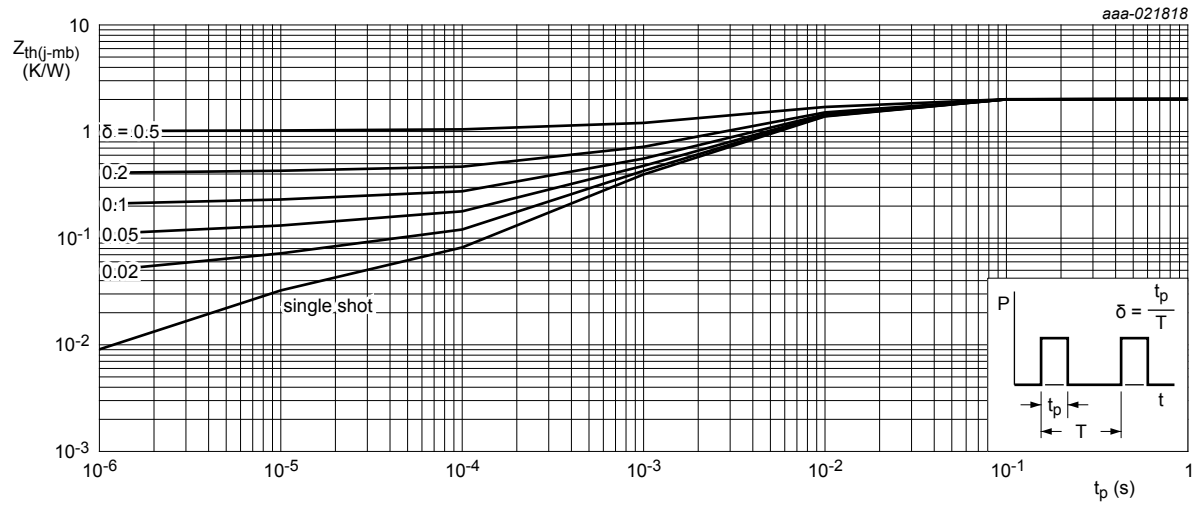


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

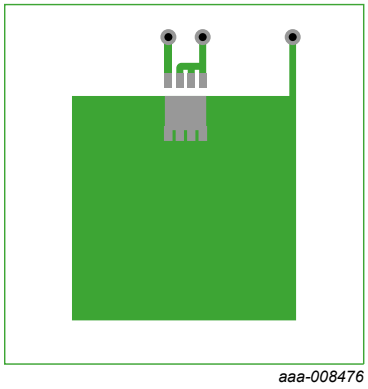


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

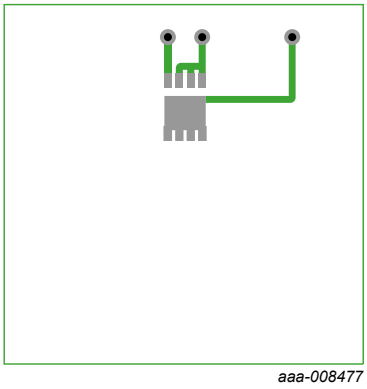


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

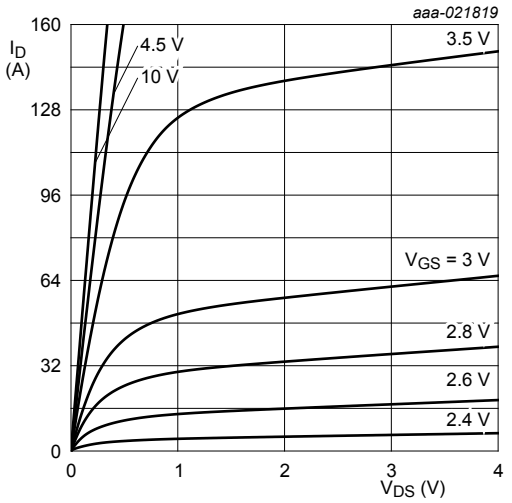
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		25	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		1.2	1.65	2.2	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 175 °C		-	-4.5	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 20 V; V_{GS} = 0 V; T_j = 125 °C		-	9.9	-	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	2.5	3.06	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 175 °C; Fig. 10; Fig. 11		-	-	5.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	1.86	2.27	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 10; Fig. 11		-	-	3.86	mΩ
R_G	gate resistance	f = 1 MHz		-	0.75	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	34.4	-	nC
		I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	15.9	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	18.9	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	6.4	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	3.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	2.6	-	nC
Q_{GD}	gate-drain charge			-	3.8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 12 V; Fig. 12; Fig. 13		-	2.8	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	2490	-	pF
C_{oss}	output capacitance			-	1132	-	pF
C_{rss}	reverse transfer capacitance			-	167	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.6 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω		-	15.7	-	ns
t_r	rise time			-	18.4	-	ns
$t_{d(off)}$	turn-off delay time			-	17.8	-	ns
t_f	fall time			-	11.7	-	ns

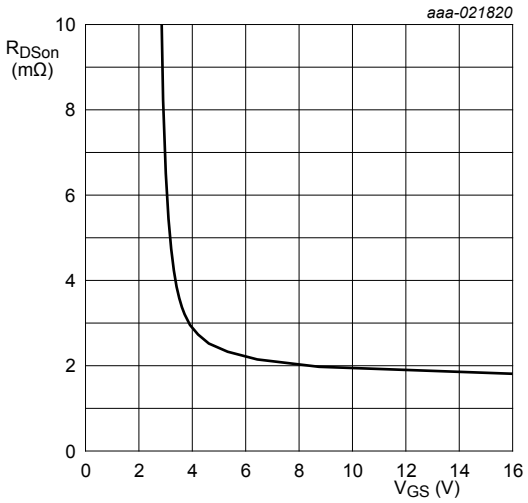
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 12 V; f = 1 MHz; T_j = 25 °C		-	19.7	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 20 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 12 V; Fig. 16		-	26.7	-	ns
Q_r	recovered charge		[1]	-	16.3	-	nC
t_a	reverse recovery rise time			-	14	-	ns
t_b	reverse recovery fall time			-	12.8	-	ns
S	softness factor			-	0.9	-	

[1] includes capacitive recovery



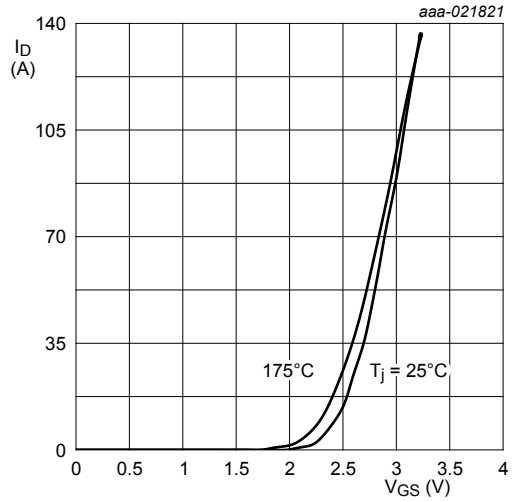
T_j = 25 °C

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values



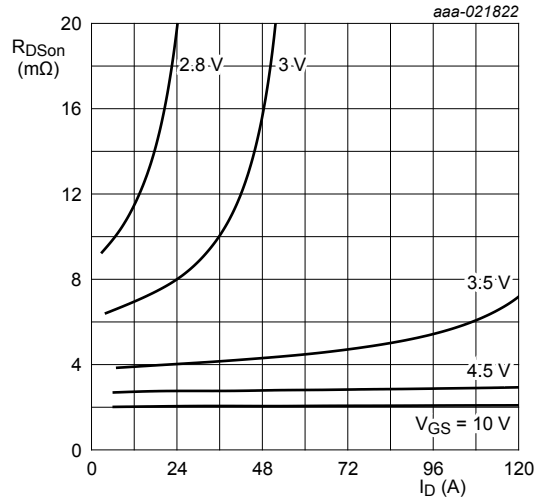
T_j = 25 °C; I_D = 25 A

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



V_{DS} = 12 V

Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



T_j = 25 °C

Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

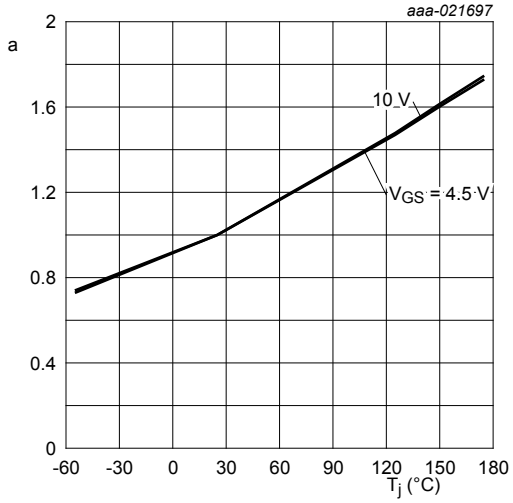
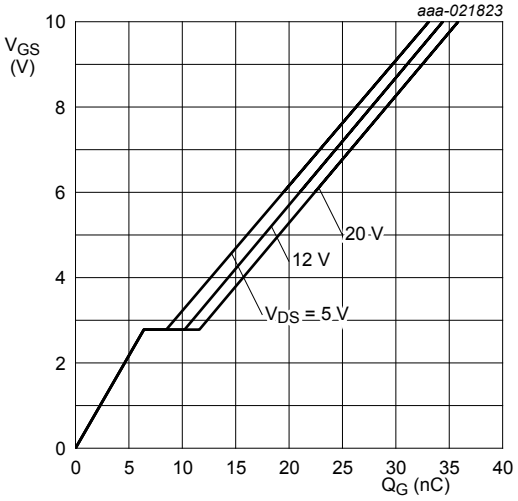


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$



T_j = 25 °C; I_D = 25 A

Fig. 12. Gate-source voltage as a function of gate charge; typical values

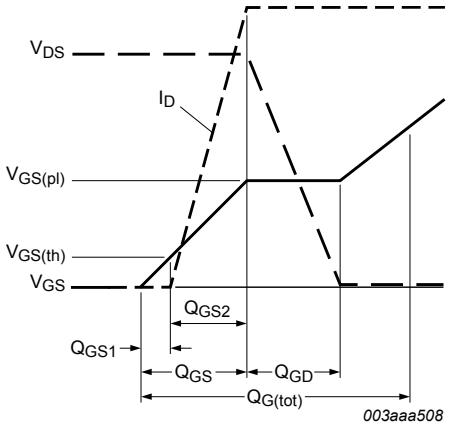
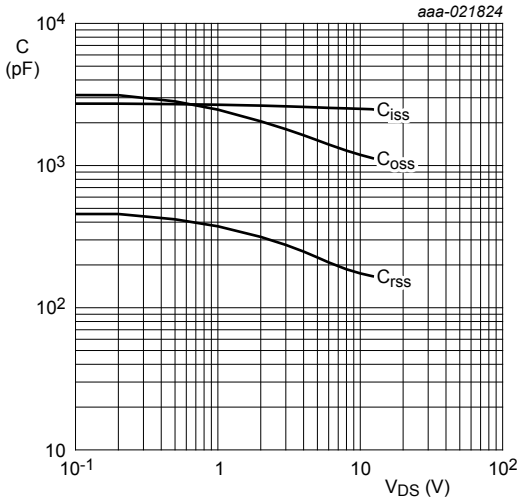
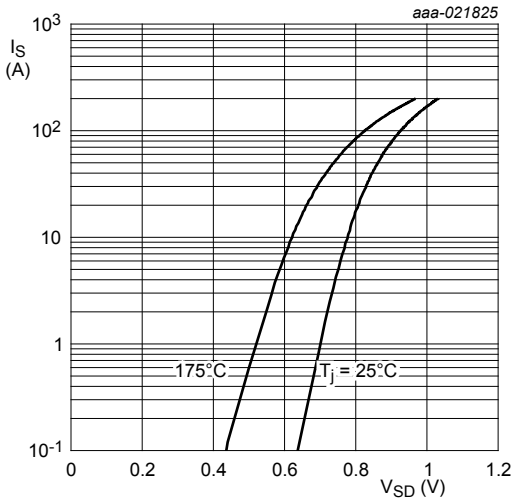


Fig. 13. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

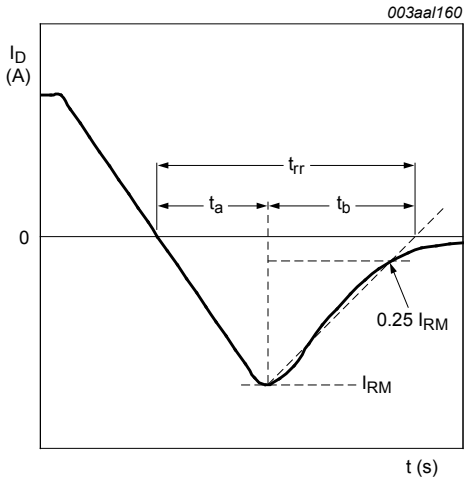
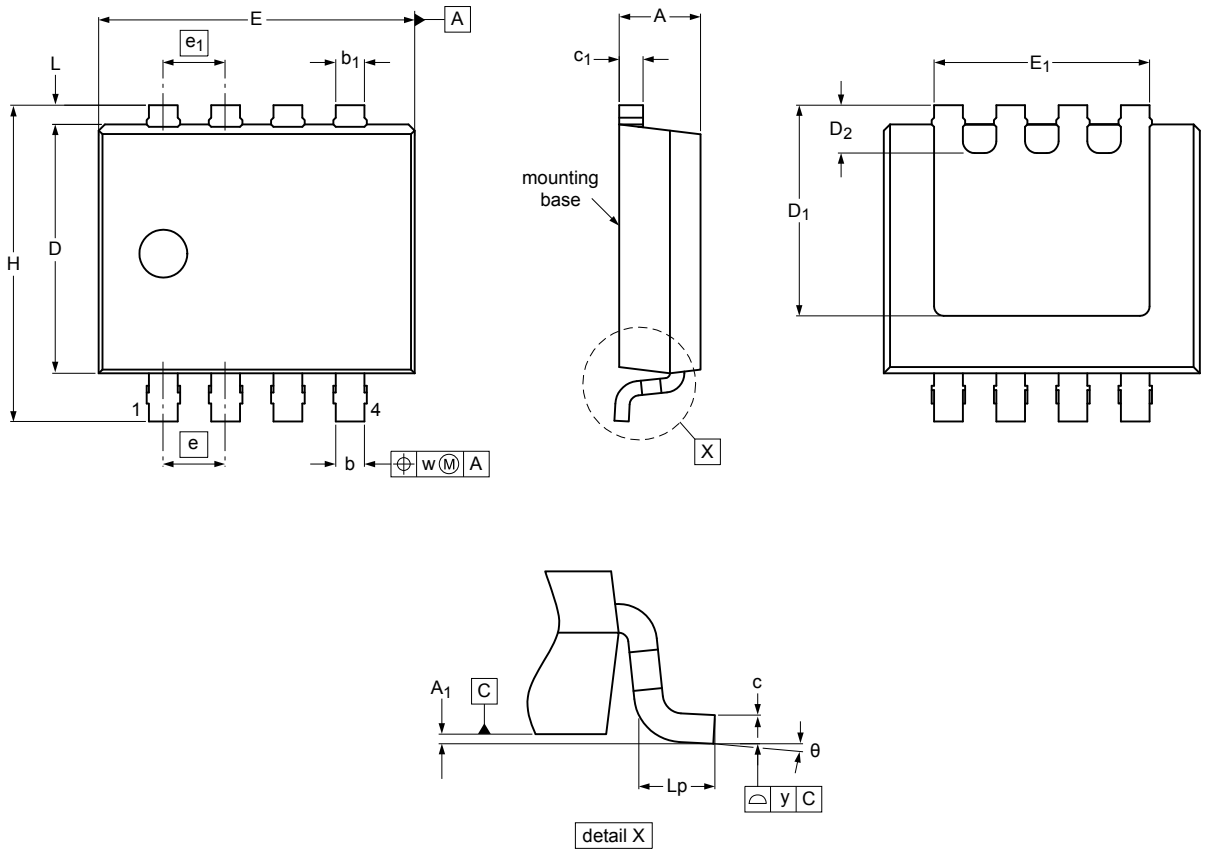


Fig. 16. Reverse recovery timing definition

11. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit(1)		A	A_1	b	b_1	c	c_1	D(1)	D_1	D_2	E(1)	E_1	e	e_1	H	L	L_p	w	y	θ
mm	max	0.90	0.10	0.35	0.35	0.20	0.30	2.70	2.35		3.40	2.45			3.40	0.25	0.50			8°
	nom									0.50			0.65	0.65				0.20	0.10	
	min	0.80	0.00	0.25	0.25	0.10	0.20	2.50	1.90		3.20	2.00			3.20	0.13	0.30			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~12-03-12~~ 14-04-25

Fig. 17. Package outline LFPAK33 (SOT1210)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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13. Contents

For more information, please visit: http://www.nexperia.com
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