

# PSMN6R3-120ESQ Datasheet



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DiGi Electronics Part Number	PSMN6R3-120ESQ-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	PSMN6R3-120ESQ
Description	MOSFET N-CH 120V 70A I2PAK
Detailed Description	N-Channel 120 V 70A (Tc) 405W (Tc) Through Hole I2PAK



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## Purchase and inquiry

Manufacturer Product Number:

PSMN6R3-120ESQ

Series:

-

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

120 V

Drive Voltage (Max Rds On, Min Rds On):

10V

Vgs(th) (Max) @ Id:

4V @ 250 $\mu$ A

Vgs (Max):

$\pm$ 20V

FET Feature:

-

Operating Temperature:

-55 $^{\circ}$ C ~ 175 $^{\circ}$ C (Tj)

Supplier Device Package:

I2PAK

Manufacturer:

Nexperia USA Inc.

Product Status:

Obsolete

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25 $^{\circ}$ C:

70A (Tc)

Rds On (Max) @ Id, Vgs:

6.7mOhm @ 25A, 10V

Gate Charge (Qg) (Max) @ Vgs:

207.1 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

11384 pF @ 60 V

Power Dissipation (Max):

405W (Tc)

Mounting Type:

Through Hole

Package / Case:

TO-262-3 Long Leads, I2PAK, TO-262AA

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



# PSMN6R3-120ES

N-channel 120 V 6.7 mΩ standard level MOSFET in I2PAK

8 May 2013

Product data sheet

## 1. General description

Standard level N-channel MOSFET in I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic power supply equipment.

## 2. Features and benefits

- High efficiency due to low switching and conduction losses
- Improved dynamic avalanche performance
- Suitable for standard level gate drive
- I2PAK package for slimline adaptors & height constrained applications

## 3. Applications

- AC-to-DC power supply
- Synchronous rectification
- Motor control
- Slimline adaptors & chargers

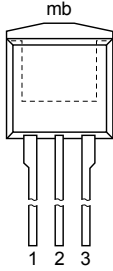
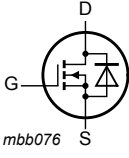
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	120	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 1</a>	-	-	70	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	405	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>	4	5.7	6.7	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 60\text{ V}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	61.9	-	nC
$Q_{G(tot)}$	total gate charge		-	207.1	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 70\text{ A}$ ; $V_{sup} \leq 120\text{ V}$ ; unclamped; $R_{GS} = 50\text{ Ω}$ ; <a href="#">Fig. 3</a>	-	-	532	mJ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>I2PAK (SOT226)</p>	
2	D	drain		
3	S	source		
mb	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN6R3-120ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	120	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	120	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	70	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 1</a>	-	70	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 4</a>	-	280	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	405	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	70	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	280	A

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 70\text{ A}$ ; $V_{\text{sup}} \leq 120\text{ V}$ ; unclamped; $R_{GS} = 50\text{ }\Omega$ ; <a href="#">Fig. 3</a>	-	532	mJ

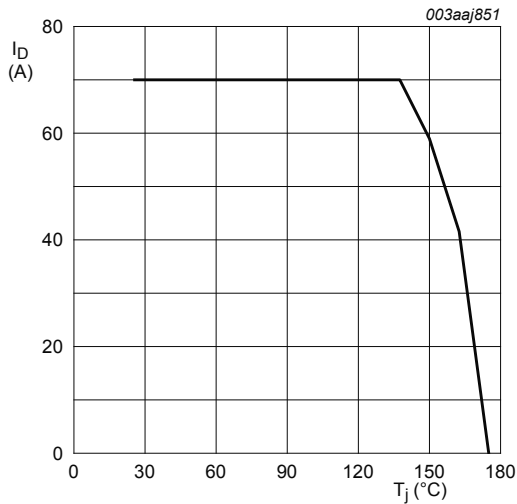


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

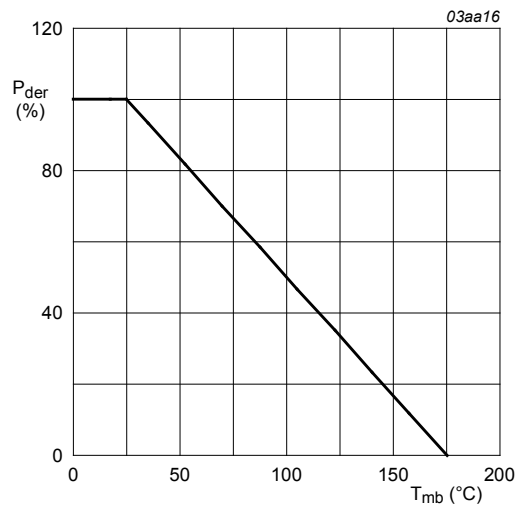


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

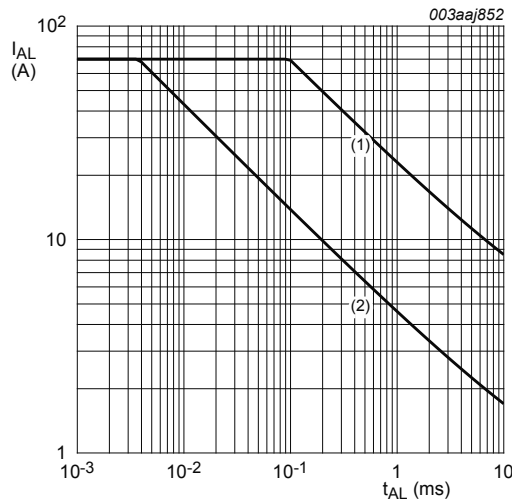
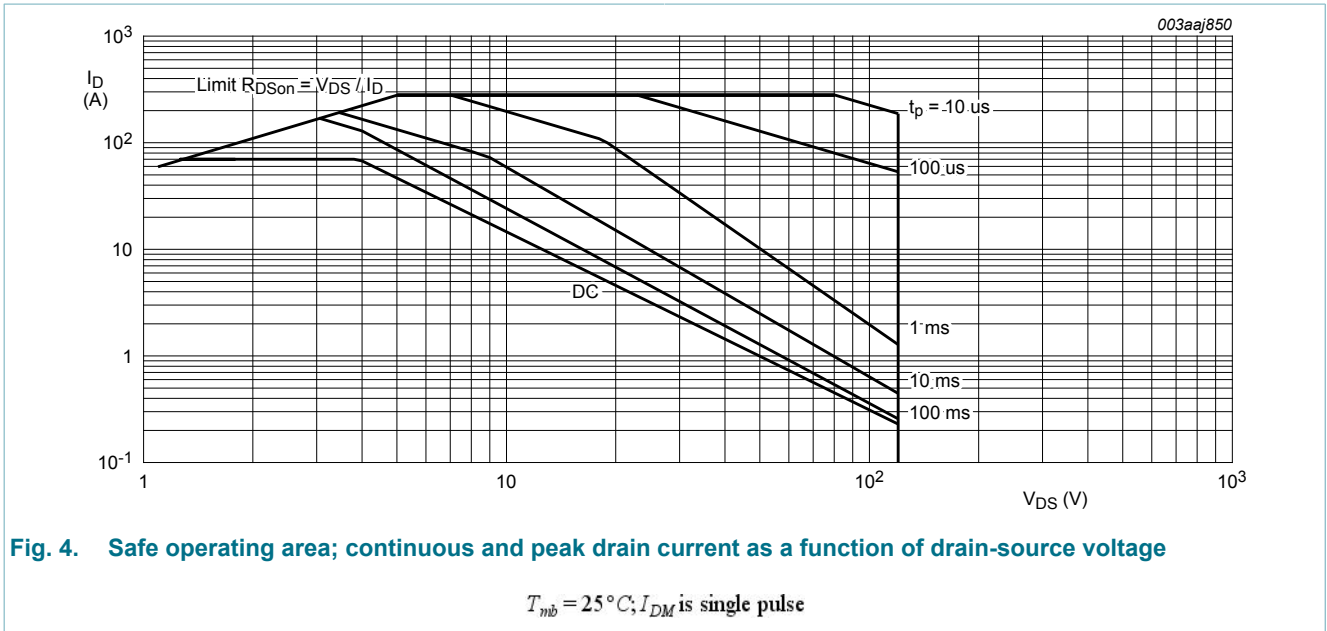


Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

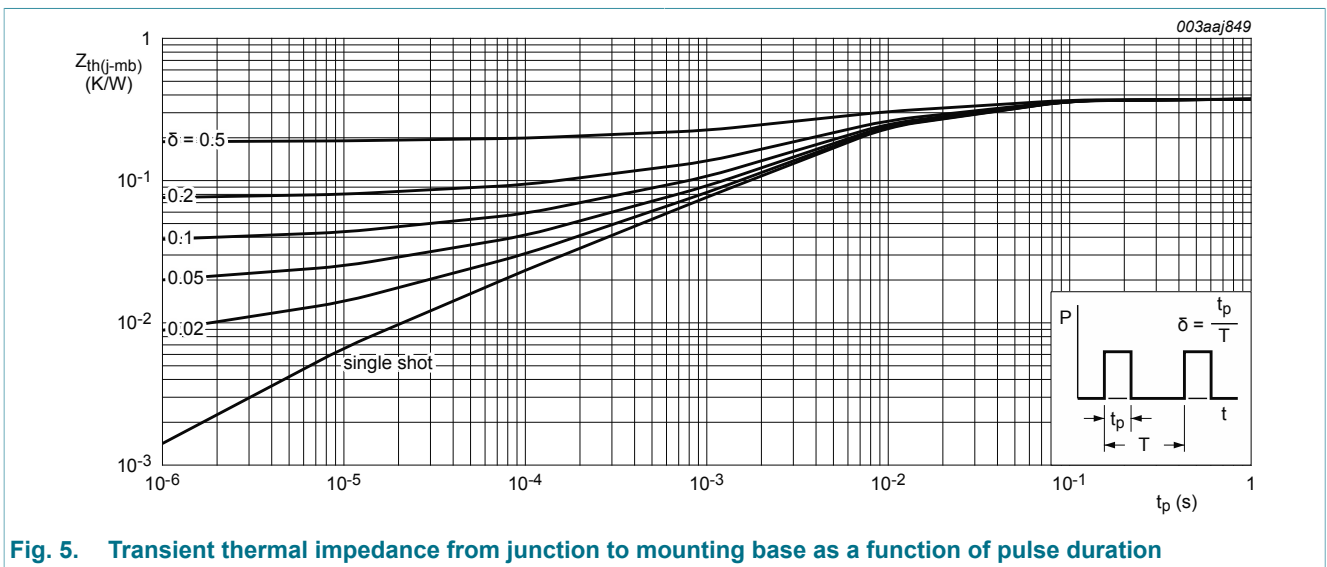
- (1) Single-pulse;  $T_j = 25\text{ °C}$ .
- (2) Single-pulse;  $T_j = 125\text{ °C}$ .



## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.3	0.37	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	65	-	K/W



## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	120	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 10; Fig. 11</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 10; Fig. 11</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 10; Fig. 11</a>	-	-	4.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 120 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS} = 120 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a>	4	5.7	6.7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 13; Fig. 12</a>	-	16.5	19.4	mΩ
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}$	0.44	0.88	1.76	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 14; Fig. 15</a>	-	207.1	-	nC
$Q_{GS}$	gate-source charge		-	43.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	29.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	13.4	-	nC
$Q_{GD}$	gate-drain charge		-	61.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V};$ <a href="#">Fig. 14; Fig. 15</a>	-	4.3	-	V
$C_{iss}$	input capacitance	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	11384	-	pF
$C_{oss}$	output capacitance		-	534	-	pF
$C_{rss}$	reverse transfer capacitance		-	358	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 60 \text{ V}; R_L = 2.4 \text{ } \Omega; V_{GS} = 10 \text{ V};$	-	42.1	-	ns
$t_r$	rise time	$R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	58.2	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(off)}$	turn-off delay time		-	142.1	-	ns
$t_f$	fall time		-	67.7	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 17}$	-	0.79	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	76.1	-	ns
$Q_r$	recovered charge	$V_{DS} = 60\text{ V}$	-	264.2	-	nC

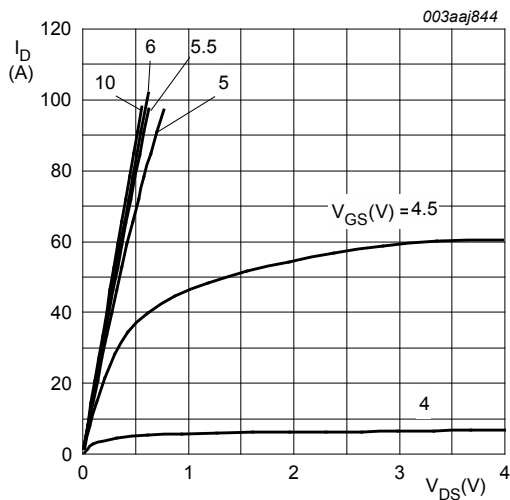


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$

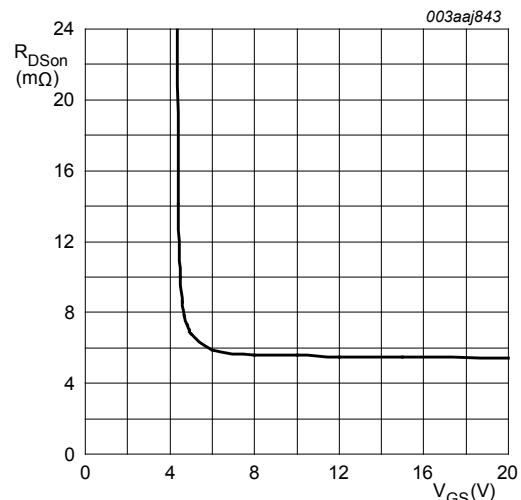


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$

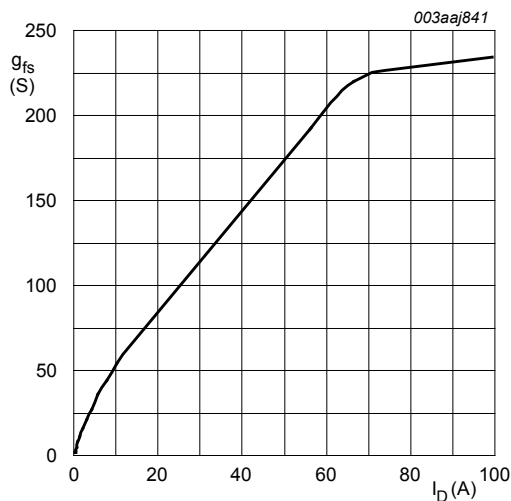


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 10\text{ V}$

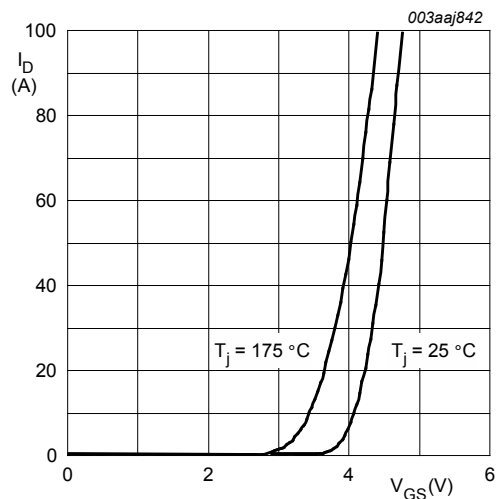
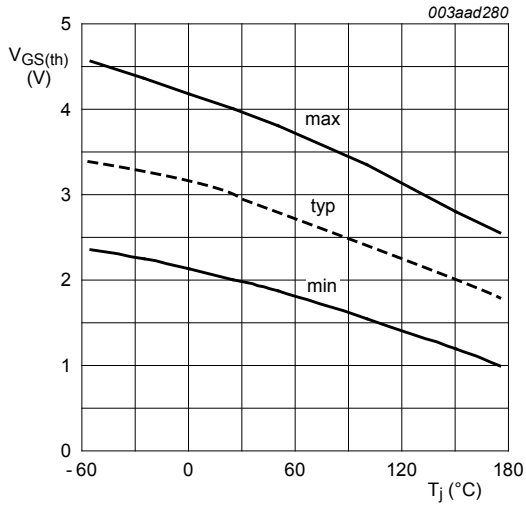


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

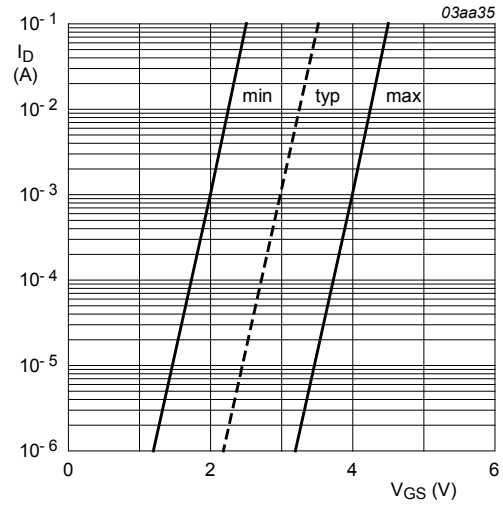
$V_{DS} > I_D \times R_{DS(on)}$





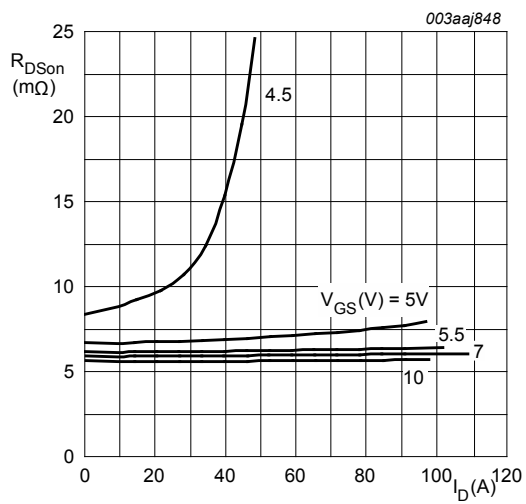
**Fig. 10. Gate-source threshold voltage as a function of junction temperature**

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$



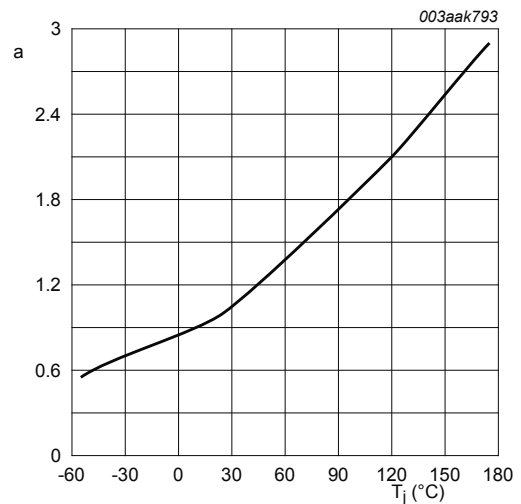
**Fig. 11. Sub-threshold drain current as a function of gate-source voltage**

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$



**Fig. 12. Drain-source on-state resistance as a function of drain current; typical values**

$$T_j = 25^\circ\text{C}$$



**Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

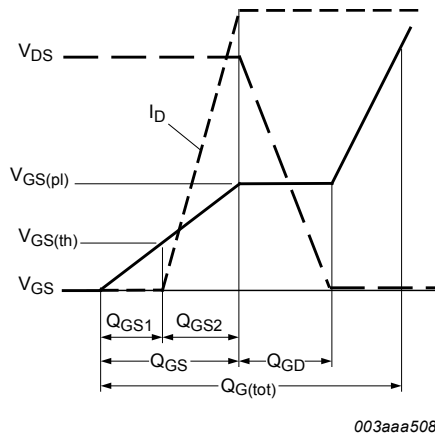


Fig. 14. Gate charge waveform definitions

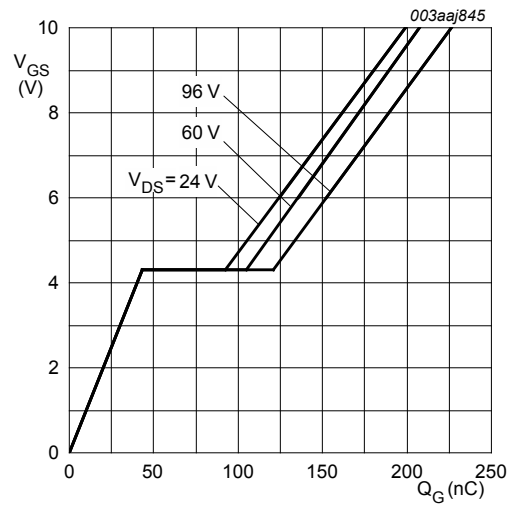


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_J = 25^\circ\text{C}; I_D = 25\text{ A}$$

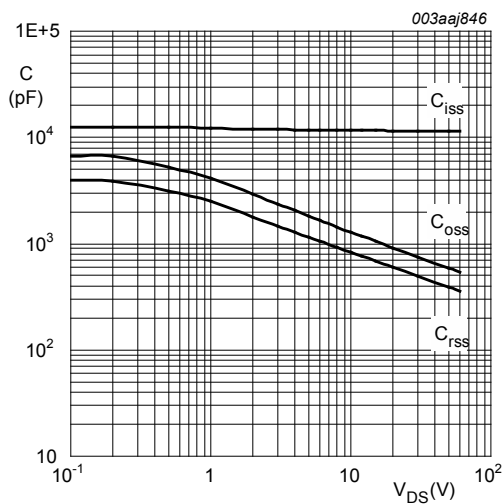


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

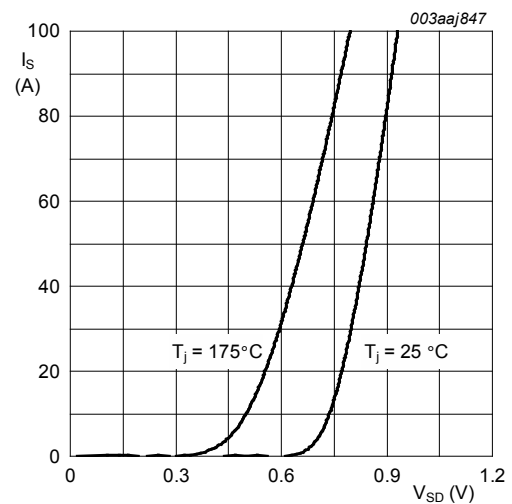


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0\text{ V}$$

### 10. Package outline

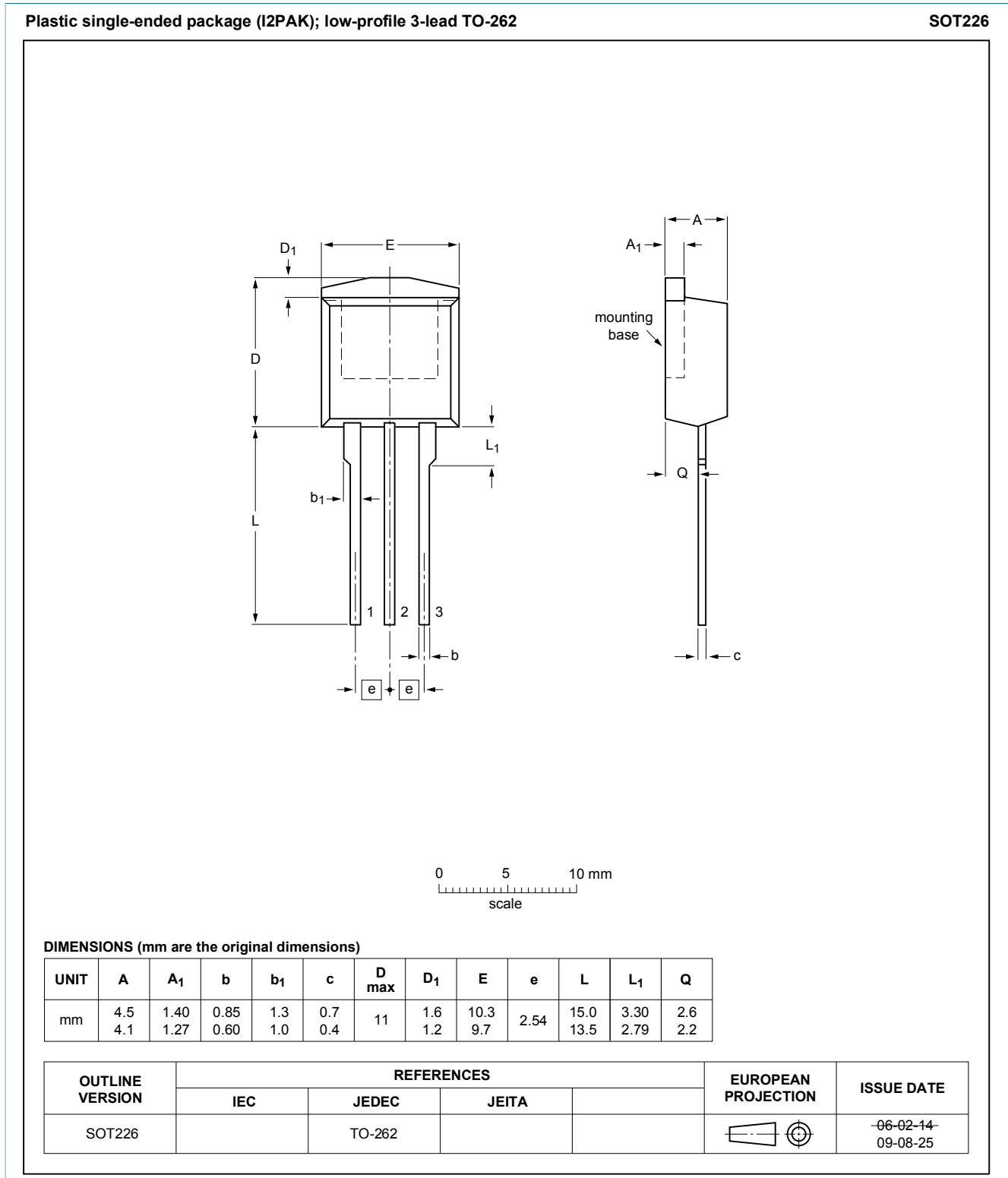


Fig. 18. Package outline I2PAK (SOT226)

## 11. Legal information

### 11.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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