

PUMB10,115 Datasheet

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DiGi Electronics Part Number	PUMB10,115-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	PUMB10,115
Description	TRANS PREBIAS 2PNP 50V 6TSSOP
Detailed Description	Pre-Biased Bipolar Transistor (BJT) 2 PNP - Pre-Biased (Dual) 50V 100mA 180MHz 300mW Surface Mount 6-TSSOP



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Purchase and inquiry

Manufacturer Product Number:

PUMB10,115

Series:

-

Transistor Type:

2 PNP - Pre-Biased (Dual)

Voltage - Collector Emitter Breakdown (Max):

50V

Resistor - Emitter Base (R2):

47kOhms

Vce Saturation (Max) @ Ib, Ic:

100mV @ 250µA, 5mA

Frequency - Transition:

180MHz

Grade:

Automotive

Mounting Type:

Surface Mount

Supplier Device Package:

6-TSSOP

Manufacturer:

Nexperia USA Inc.

Product Status:

Active

Current - Collector (Ic) (Max):

100mA

Resistor - Base (R1):

2.2kOhms

DC Current Gain (hFE) (Min) @ Ic, Vce:

100 @ 10mA, 5V

Current - Collector Cutoff (Max):

100nA

Power - Max:

300mW

Qualification:

AEC-Q101

Package / Case:

6-TSSOP, SC-88, SOT-363

Base Product Number:

PUMB10

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.21.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



PUMB10

50 V, 100 mA PNP/PNP resistor-equipped double transistor;
 $R1 = 2.2 \text{ k}\Omega$, $R2 = 47 \text{ k}\Omega$

30 March 2023

Product data sheet

1. General description

PNP/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PUMD10

NPN/NPN complement: PUMH10

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- Low current peripheral driver
- Controlling IC inputs
- Replaces general-purpose transistors in digital applications

4. Quick reference data

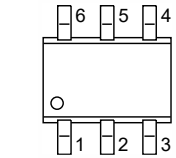
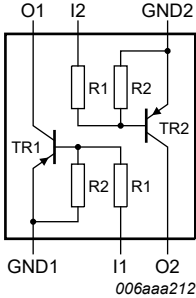
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-50	V
I_O	output current		-	-	-100	mA
R1	bias resistor 1 (input)		1.54	2.2	2.86	$\text{k}\Omega$
R2/R1	bias resistor ratio		17	21	26	

50 V, 100 mA PNP/PNP resistor-equipped double transistor; R1 = 2.2 k Ω , R2 = 47 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>TSSOP6 (SOT363)</p>	 <p>006aaa212</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMB10	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PUMB10	B%0

[1] % = placeholder for manufacturing site code

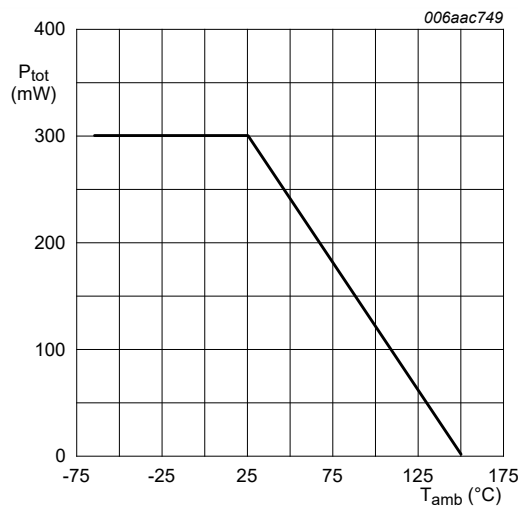
50 V, 100 mA PNP/PNP resistor-equipped double transistor; R1 = 2.2 kΩ, R2 = 47 kΩ

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor					
V_{CBO}	collector-base voltage	open emitter	-	-50	V
V_{CEO}	collector-emitter voltage	open base	-	-50	V
V_{EBO}	emitter-base voltage	open collector	-	-5	V
V_I	input voltage		-12	5	V
I_O	output current		-	-100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	200	mW
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	300	mW
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-65	150	°C
T_{stg}	storage temperature		-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

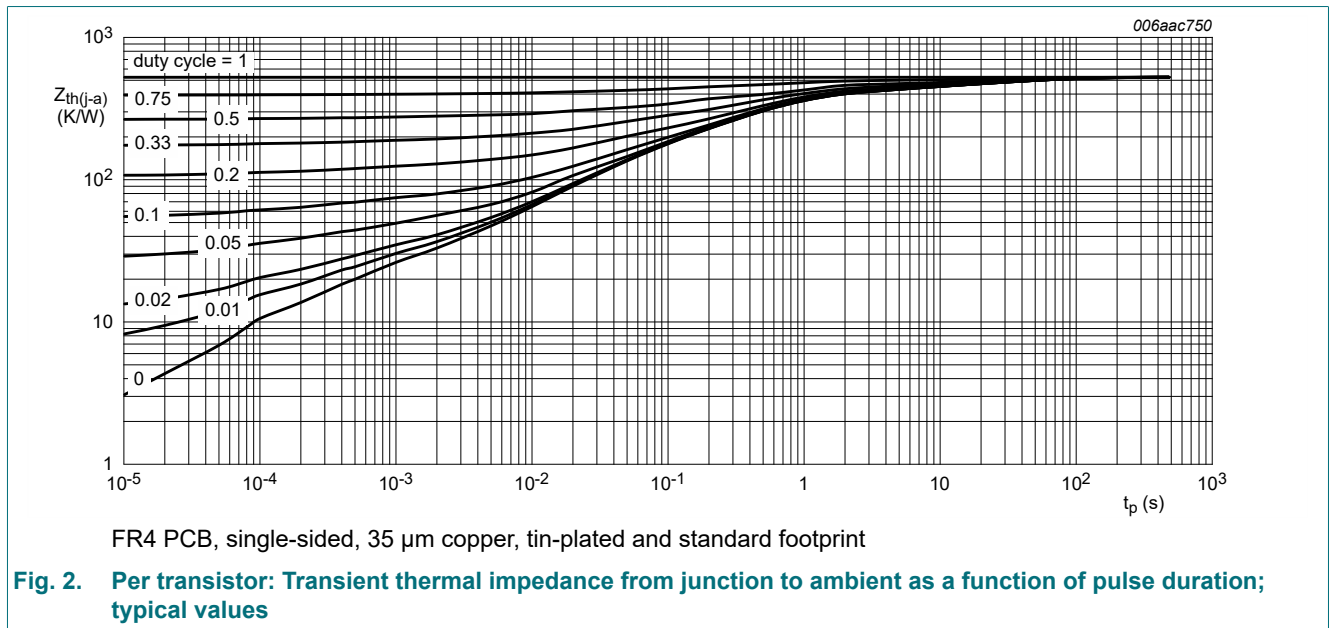
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

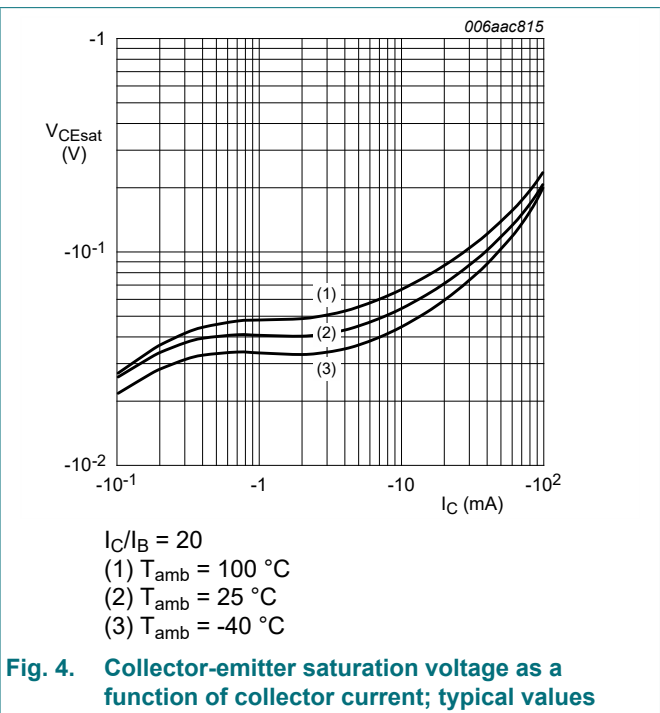
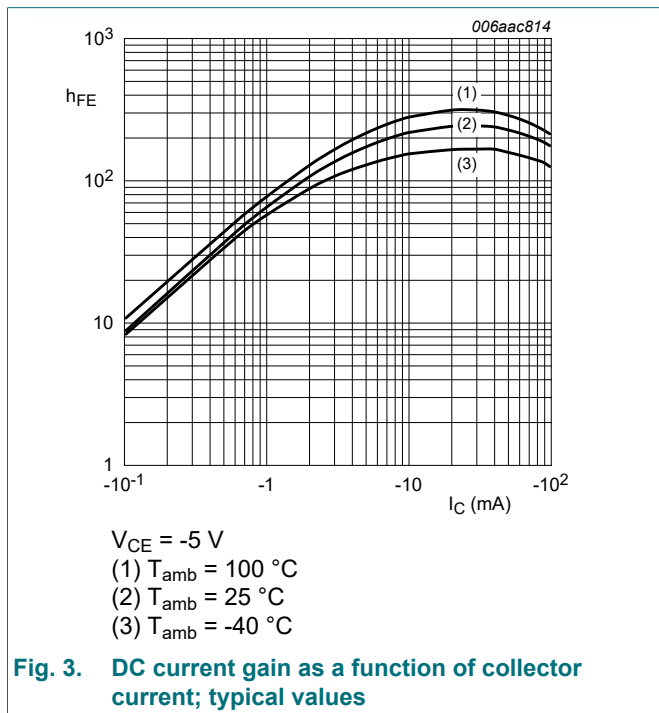


10. Characteristics

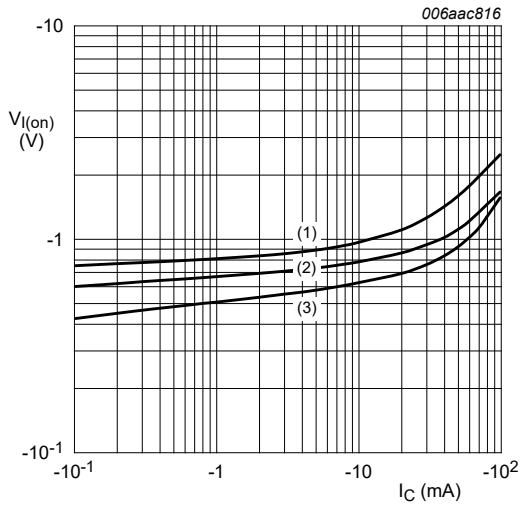
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = -100 \mu\text{A}$; $I_E = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = -2 \text{ mA}$; $I_B = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = -50 \text{ V}$; $I_E = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30 \text{ V}$; $I_B = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
		$V_{CE} = -30 \text{ V}$; $I_B = 0 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}$; $I_C = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	-180	μA
h_{FE}	DC current gain	$V_{CE} = -5 \text{ V}$; $I_C = -10 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -5 \text{ mA}$; $I_B = -0.25 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	-100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 \text{ V}$; $I_C = -100 \mu\text{A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-0.6	-0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3 \text{ V}$; $I_C = -5 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-1.1	-0.75	-	V
R1	bias resistor 1 (input)		1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		17	21	26	
C_c	collector capacitance	$V_{CB} = -10 \text{ V}$; $I_E = 0 \text{ A}$; $i_e = 0 \text{ A}$; $f = 1 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	3	pF
f_T	transition frequency	$V_{CE} = -5 \text{ V}$; $I_C = -10 \text{ mA}$; $f = 100 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	180	-	MHz

[1] Characteristics of built-in transistor

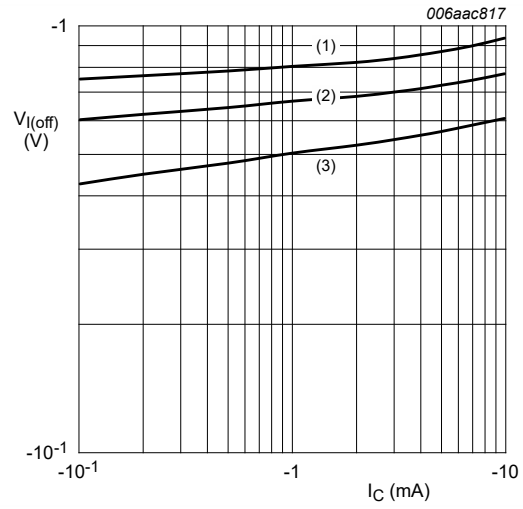


50 V, 100 mA PNP/PNP resistor-equipped double transistor; R1 = 2.2 kΩ, R2 = 47 kΩ



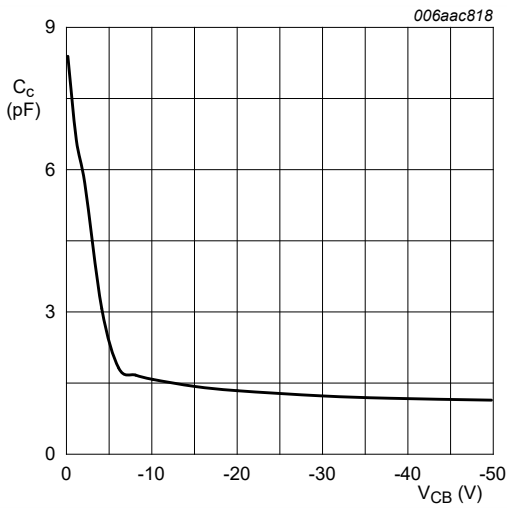
$V_{CE} = -0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 5. On-state input voltage as a function of collector current; typical values



$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 6. Off-state input voltage as a function of collector current; typical values



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 7. Collector capacitance as a function of collector-base voltage; typical values

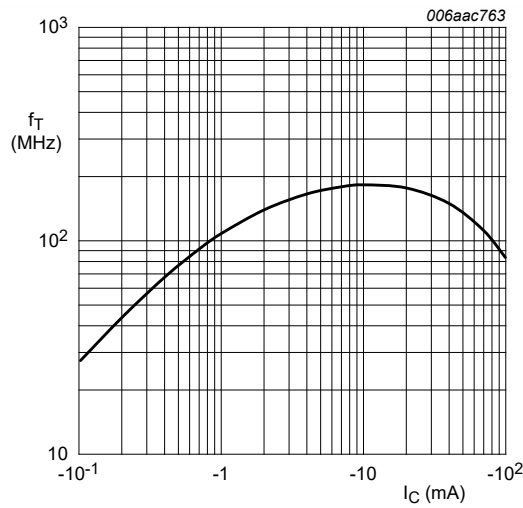


Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

50 V, 100 mA PNP/PNP resistor-equipped double transistor; R1 = 2.2 kΩ, R2 = 47 kΩ

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

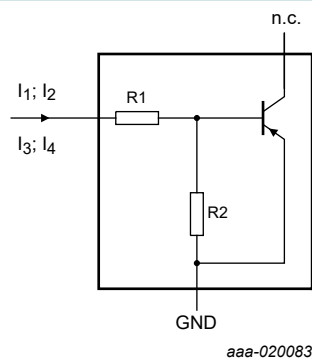


Fig. 9. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
PUMB10	2.2	47	-90 μA	-140 μA	55 μA	105 μA

12. Package outline

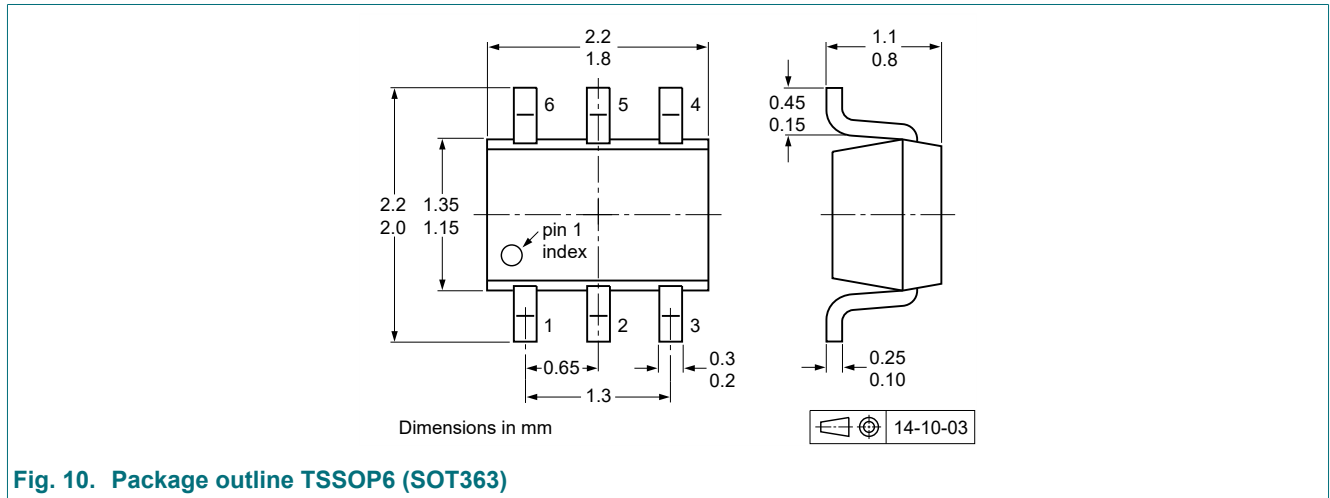


Fig. 10. Package outline TSSOP6 (SOT363)

13. Soldering

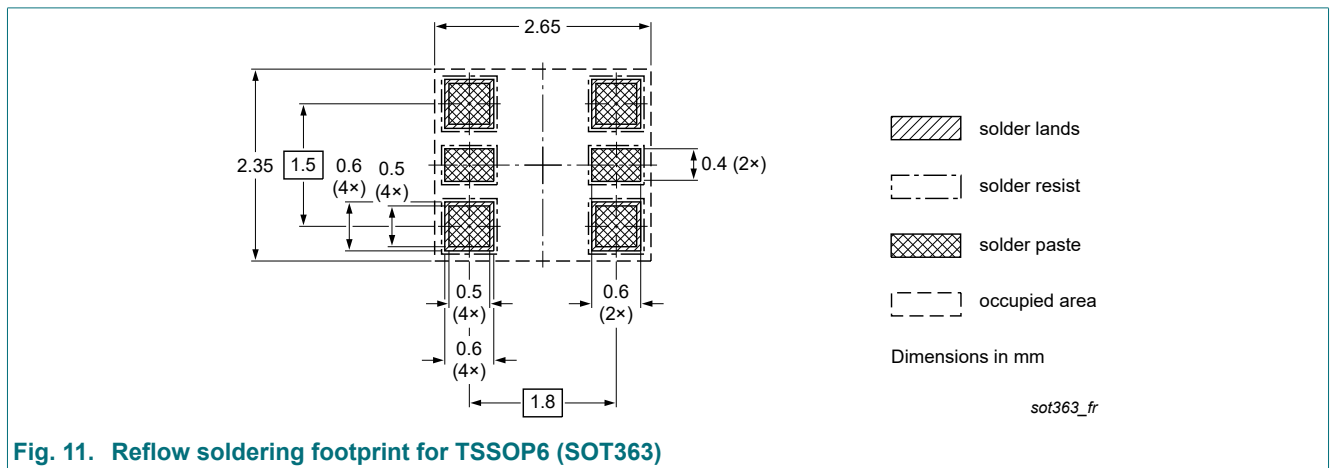


Fig. 11. Reflow soldering footprint for TSSOP6 (SOT363)

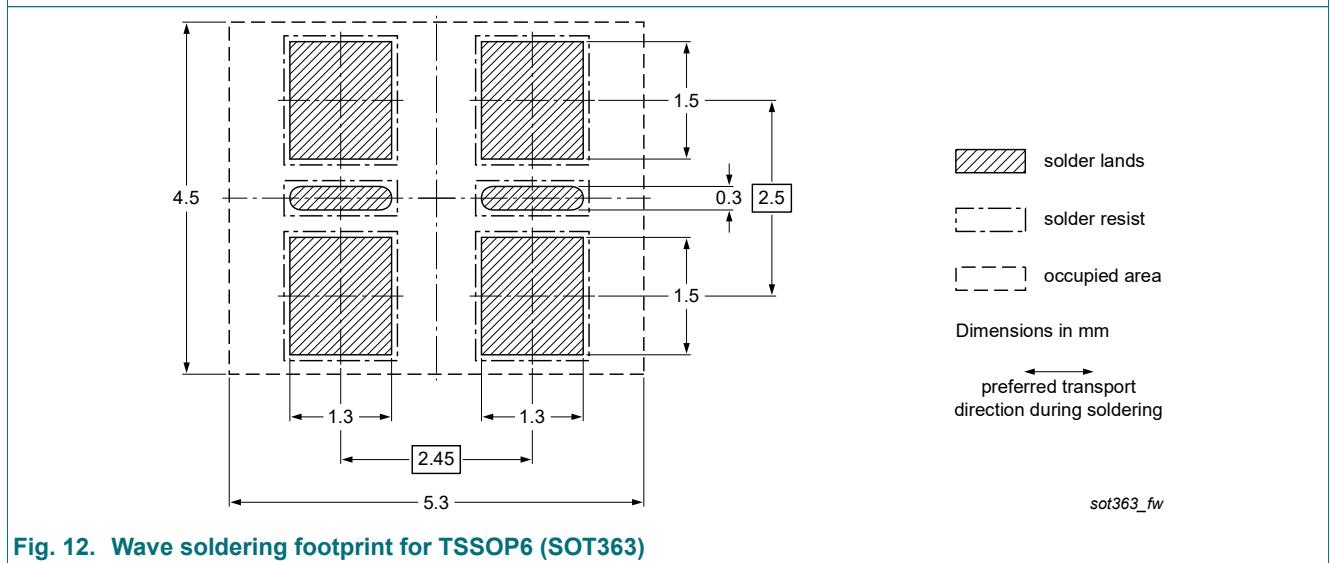


Fig. 12. Wave soldering footprint for TSSOP6 (SOT363)

50 V, 100 mA PNP/PNP resistor-equipped double transistor; R1 = 2.2 k Ω , R2 = 47 k Ω

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMB10 v.4	20230330	Product data sheet	-	PEMB10_ PUMB10 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Family data sheet reduced to single type data sheet. Packing information is removed. 			
PEMB10_ PUMB10 v.3	20120103	Product data sheet	-	PEMB10_ PUMB10 v.2
PEMB10_ PUMB10 v.2	20031003	Product data sheet	-	PEMB10 v.1
PEMB10 v.1	20010914	Preliminary specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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