

PUMD15/ZLF Datasheet



| | |
|------------------------------|---|
| DiGi Electronics Part Number | PUMD15/ZLF-DG |
| Manufacturer | Nexperia USA Inc. |
| Manufacturer Product Number | PUMD15/ZLF |
| Description | TRANS PREBIAS |
| Detailed Description | Pre-Biased Bipolar Transistor (BJT) 1 NPN, 1 PNP - P re-Biased (Dual) 50V 100mA 230MHz, 180MHz 300m W Surface Mount 6-TSSOP |

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Purchase and inquiry

Manufacturer Product Number:

PUMD15/ZLF

Series:

-

Transistor Type:

1 NPN, 1 PNP - Pre-Biased (Dual)

Voltage - Collector Emitter Breakdown (Max):

50V

Resistor - Emitter Base (R2):

4.7kOhms

Vce Saturation (Max) @ Ib, Ic:

150mV @ 500µA, 10mA

Frequency - Transition:

230MHz, 180MHz

Grade:

Automotive

Mounting Type:

Surface Mount

Supplier Device Package:

6-TSSOP

Manufacturer:

Nexperia USA Inc.

Product Status:

Obsolete

Current - Collector (Ic) (Max):

100mA

Resistor - Base (R1):

4.7kOhms

DC Current Gain (hFE) (Min) @ Ic, Vce:

30 @ 10mA, 5V

Current - Collector Cutoff (Max):

1µA

Power - Max:

300mW

Qualification:

AEC-Q101

Package / Case:

6-TSSOP, SC-88, SOT-363

Base Product Number:

PUMD15

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

0000.00.0000

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

OBSOLETE



PUMD15

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
 $R1 = 4.7 \text{ k}\Omega$, $R2 = 4.7 \text{ k}\Omega$

31 March 2023

Product data sheet

1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PUMH15

PNP/PNP complement: PUMB15

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplified circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- Low current peripheral driver
- Controlling IC inputs
- Replacement of general purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------------------|---------------------------|------------|-----|-----|-----|-----|------------|
| Per transistor | | | | | | | |
| V_{CEO} | collector-emitter voltage | open base | [1] | - | - | 50 | V |
| I_o | output current | | [1] | - | - | 100 | mA |
| R1 | bias resistor 1 (input) | | [2] | 3.3 | 4.7 | 6.1 | k Ω |
| R2/R1 | bias resistor ratio | | [2] | 0.8 | 1 | 1.2 | |

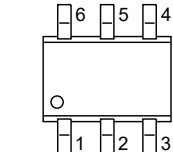
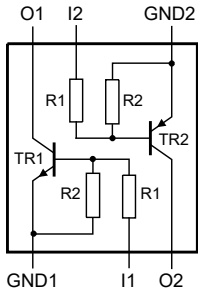
[1] For the PNP transistor (TR2) with negative polarity.

[2] See section "Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|------------------------|--|--|
| 1 | GND1 | GND (emitter) TR1 |  <p>TSSOP6 (SOT363)</p> |  <p>006aaa143</p> |
| 2 | I1 | input (base) TR1 | | |
| 3 | O2 | output (collector) TR2 | | |
| 4 | GND2 | GND (emitter) TR2 | | |
| 5 | I2 | input (base) TR2 | | |
| 6 | O1 | output (collector) TR1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|------------------------|---------|---|------------------------|
| | Name | Description | Version |
| PUMD15 | TSSOP6 | plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body | SOT363 |

7. Marking

Table 4. Marking codes

| Type number | Marking code[1] |
|-------------|-----------------|
| PUMD15 | D0% |

[1] % = placeholder for manufacturing site code

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 4.7 kΩ, R2 = 4.7 kΩ

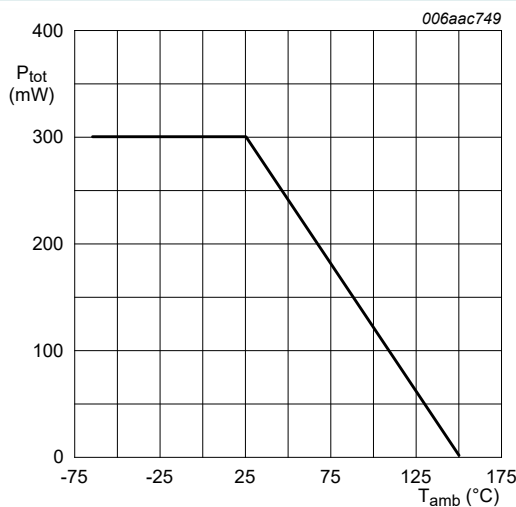
8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------------------|---------------------------|-----------------------------|-----|-----|-----|------|
| Per transistor | | | | | | |
| V_{CBO} | collector-base voltage | open emitter | [1] | - | 50 | V |
| V_{CEO} | collector-emitter voltage | open base | [1] | - | 50 | V |
| V_{EBO} | emitter-base voltage | open collector | [1] | - | 10 | V |
| V_I | input voltage | TR1 (NPN) | | -10 | 30 | V |
| | | TR2 (PNP) | | -30 | 10 | V |
| I_O | output current | | [1] | - | 100 | mA |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ °C}$ | [2] | - | 200 | mW |
| Per device | | | | | | |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ °C}$ | [2] | - | 300 | mW |
| T_j | junction temperature | | | - | 150 | °C |
| T_{amb} | ambient temperature | | | -65 | 150 | °C |
| T_{stg} | storage temperature | | | -65 | 150 | °C |

[1] For the PNP transistor (TR2) with negative polarity.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

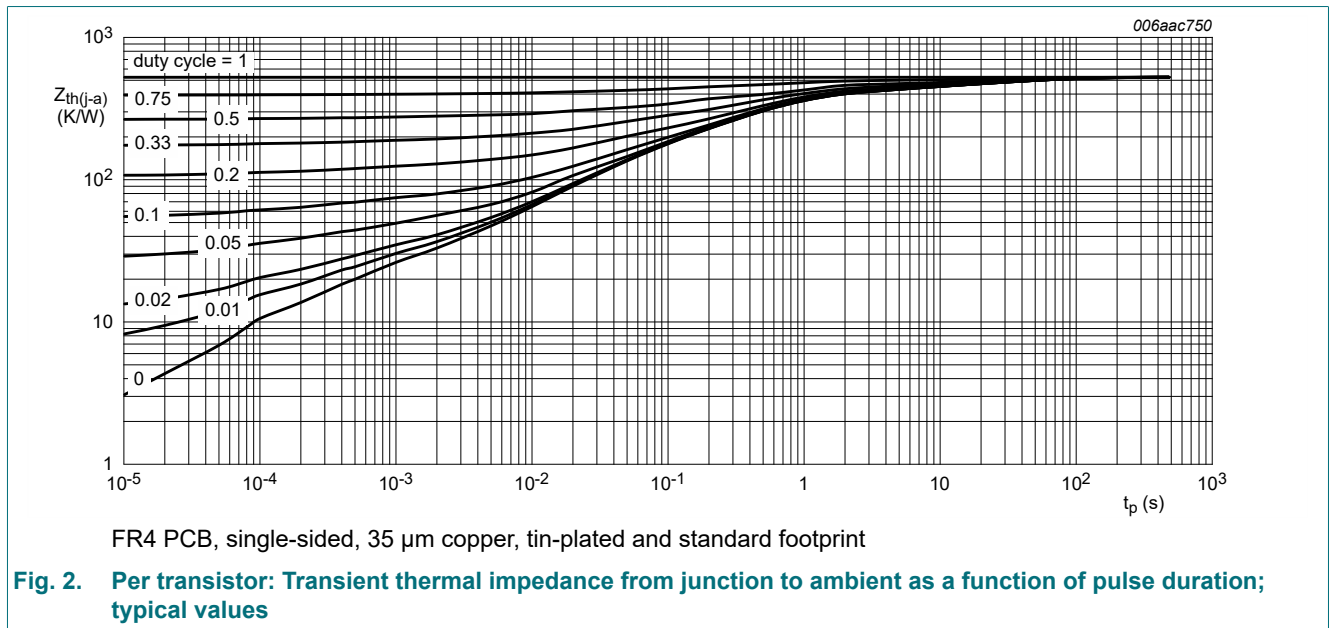
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------------------|---|-------------|-----|-----|-----|-----|------|
| Per transistor | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 625 | K/W |
| Per device | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 417 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 4.7 kΩ, R2 = 4.7 kΩ

10. Characteristics

Table 7. Characteristics

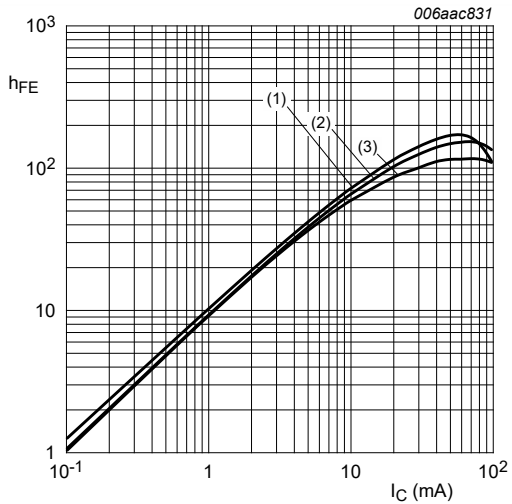
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------|---|-----|-----|-----|-----|---------------|
| Per transistor | | | | | | | |
| $V_{(BR)CBO}$ | collector-base breakdown voltage | $I_C = 100 \mu\text{A}$; $I_E = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | 50 | - | - | V |
| $V_{(BR)CEO}$ | collector-emitter breakdown voltage | $I_C = 2 \text{ mA}$; $I_B = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | 50 | - | - | V |
| I_{CBO} | collector-base cut-off current | $V_{CB} = 50 \text{ V}$; $I_E = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | - | - | 100 | nA |
| I_{CEO} | collector-emitter cut-off current | $V_{CE} = 30 \text{ V}$; $I_B = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | - | - | 100 | nA |
| | | $V_{CE} = 30 \text{ V}$; $I_B = 0 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$ | [1] | - | - | 5 | μA |
| I_{EBO} | emitter-base cut-off current | $V_{EB} = 5 \text{ V}$; $I_C = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | - | - | 900 | μA |
| h_{FE} | DC current gain | $V_{CE} = 5 \text{ V}$; $I_C = 10 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | 30 | - | - | |
| V_{CEsat} | collector-emitter saturation voltage | $I_C = 10 \text{ mA}$; $I_B = 0.5 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | - | - | 150 | mV |
| $V_{I(off)}$ | off-state input voltage | $V_{CE} = 5 \text{ V}$; $I_C = 100 \mu\text{A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | - | 1.1 | 0.5 | V |
| $V_{I(on)}$ | on-state input voltage | $V_{CE} = 0.3 \text{ V}$; $I_C = 20 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | 2.5 | 1.9 | - | V |
| R1 | bias resistor 1 (input) | | [2] | 3.3 | 4.7 | 6.1 | kΩ |
| R2/R1 | bias resistor ratio | | [2] | 0.8 | 1 | 1.2 | |
| TR1 (NPN) | | | | | | | |
| C_c | collector capacitance | $V_{CB} = 10 \text{ V}$; $I_E = 0 \text{ A}$; $i_e = 0 \text{ A}$; $f = 1 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | | - | - | 2.5 | pF |
| f_T | transition frequency | $V_{CE} = 5 \text{ V}$; $I_C = 10 \text{ mA}$; $f = 100 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [3] | - | 230 | - | MHz |
| TR2 (PNP) | | | | | | | |
| C_c | collector capacitance | $V_{CB} = -10 \text{ V}$; $I_E = 0 \text{ A}$; $i_e = 0 \text{ A}$; $f = 1 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | | - | - | 3 | pF |
| f_T | transition frequency | $V_{CE} = -5 \text{ V}$; $I_C = -10 \text{ mA}$; $f = 100 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [3] | - | 180 | - | MHz |

[1] For the PNP transistor (TR2) with negative polarity.

[2] See section "Test information" for resistor calculation and test conditions.

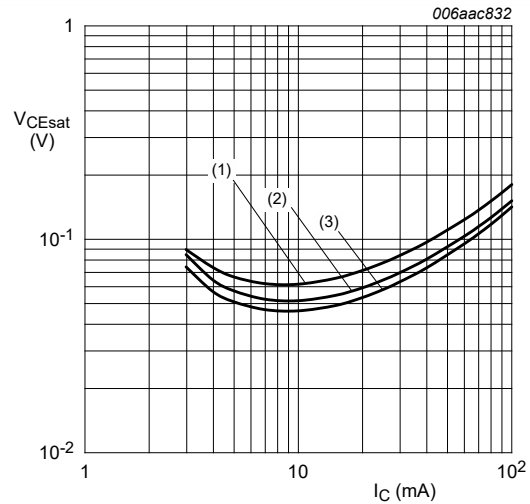
[3] Characteristics of built-in transistor

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 4.7 kΩ, R2 = 4.7 kΩ



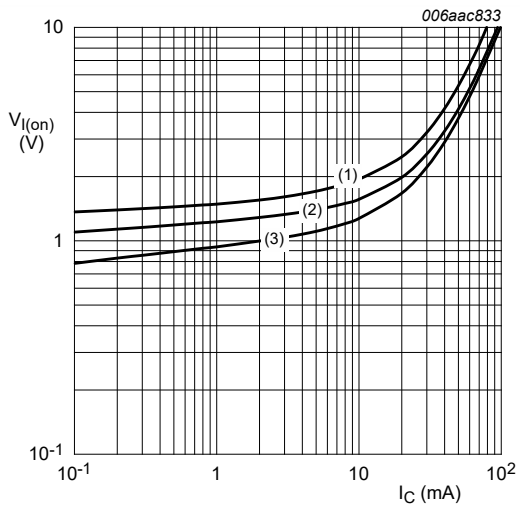
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values



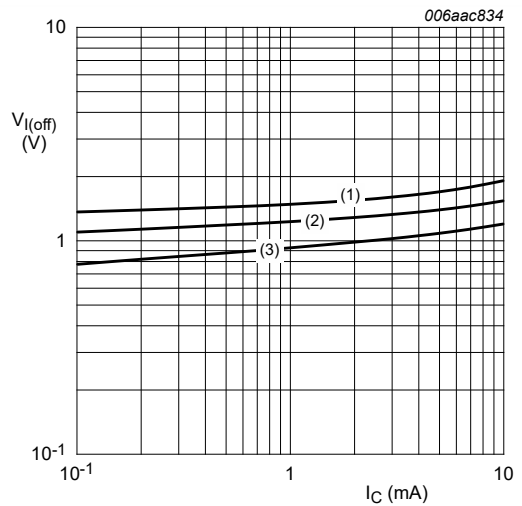
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig. 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CE} = 0.3\text{ V}$
 (1) $T_{amb} = -40\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

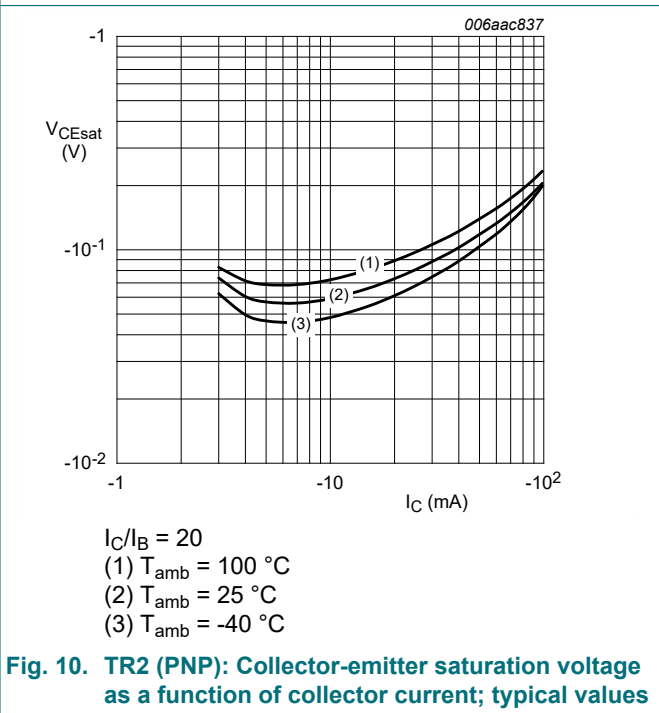
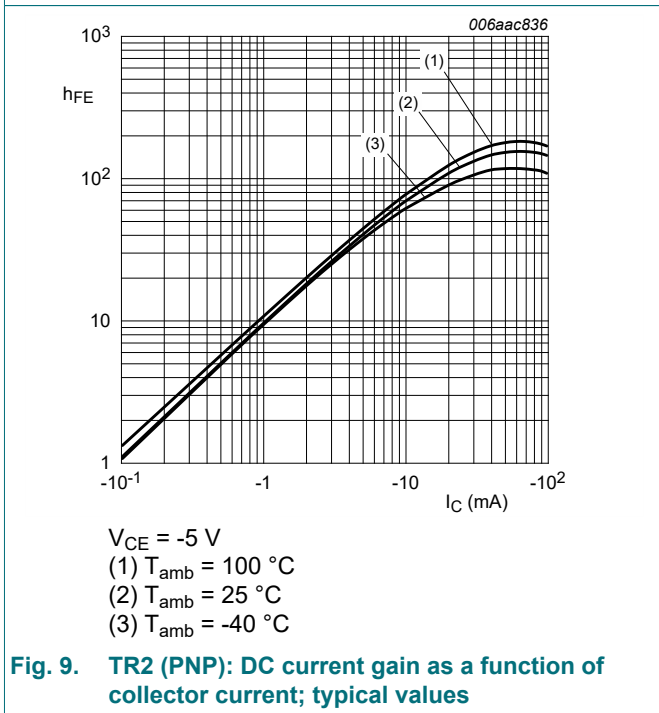
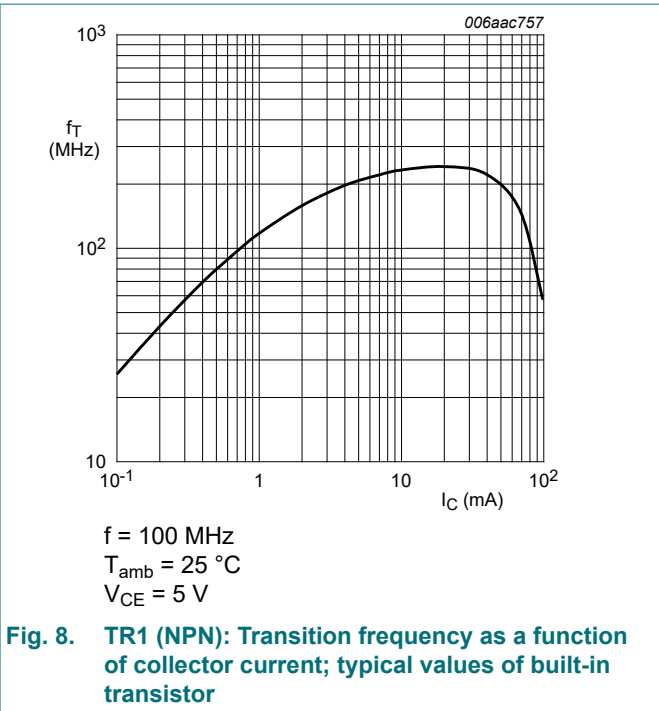
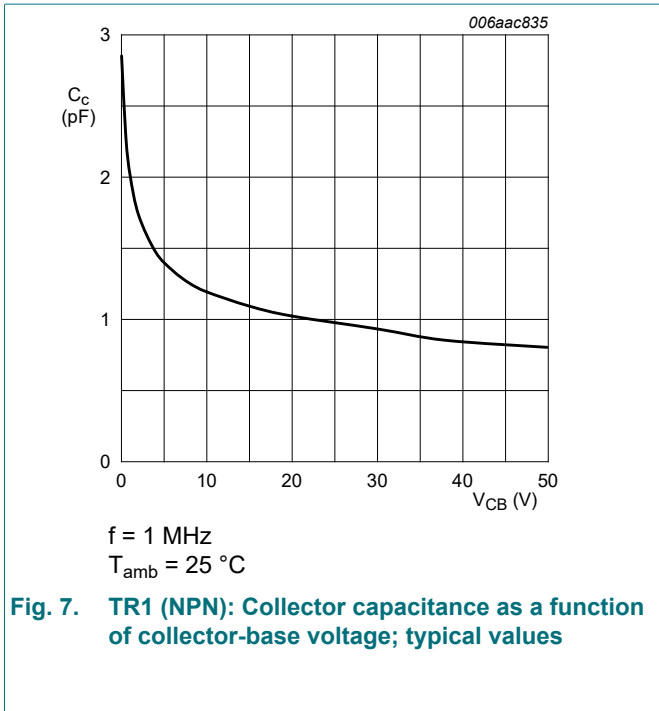
Fig. 5. TR1 (NPN): On-state input voltage as a function of collector current; typical values



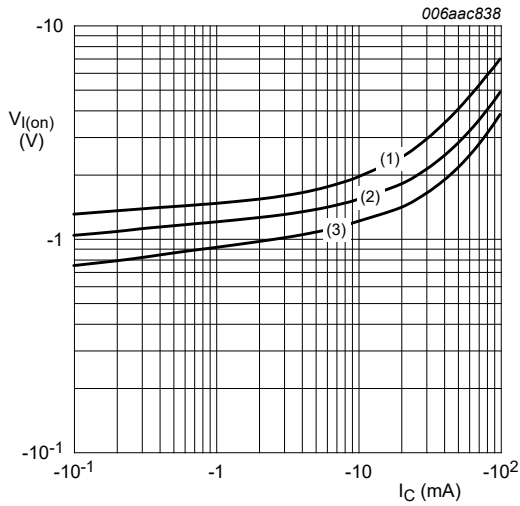
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = -40\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig. 6. TR1 (NPN): Off-state input voltage as a function of collector current; typical values

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 4.7 kΩ, R2 = 4.7 kΩ

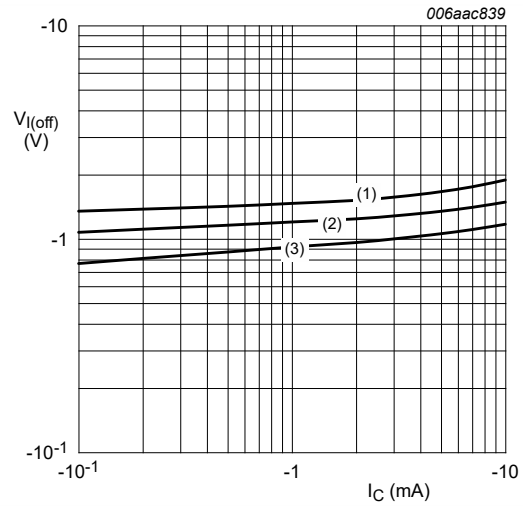


50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 4.7 kΩ, R2 = 4.7 kΩ



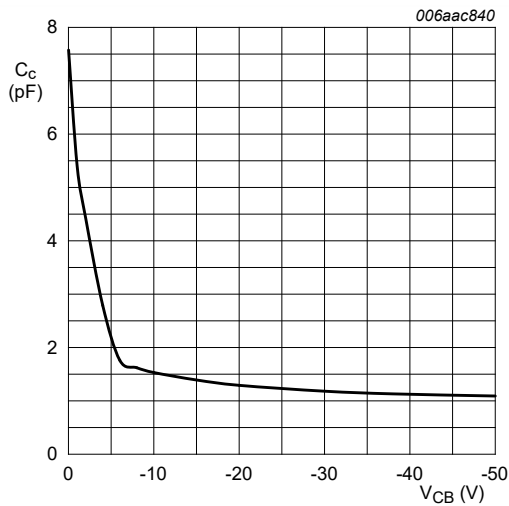
$V_{CE} = -0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 11. TR2 (PNP): On-state input voltage as a function of collector current; typical values



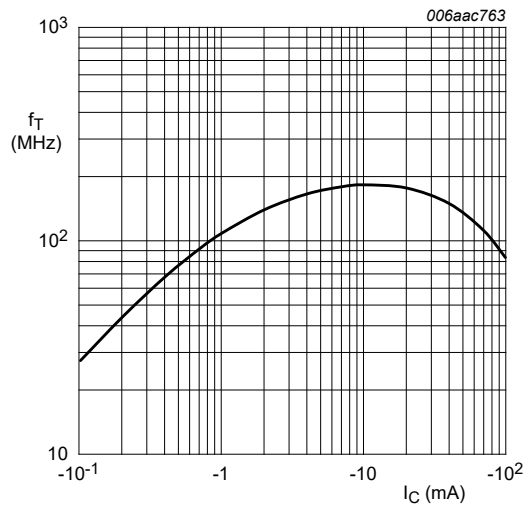
$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



$f = 1 \text{ MHz}$
 $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 13. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values



$f = 100 \text{ MHz}$
 $T_{amb} = 25 \text{ }^\circ\text{C}$
 $V_{CE} = -5 \text{ V}$

Fig. 14. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

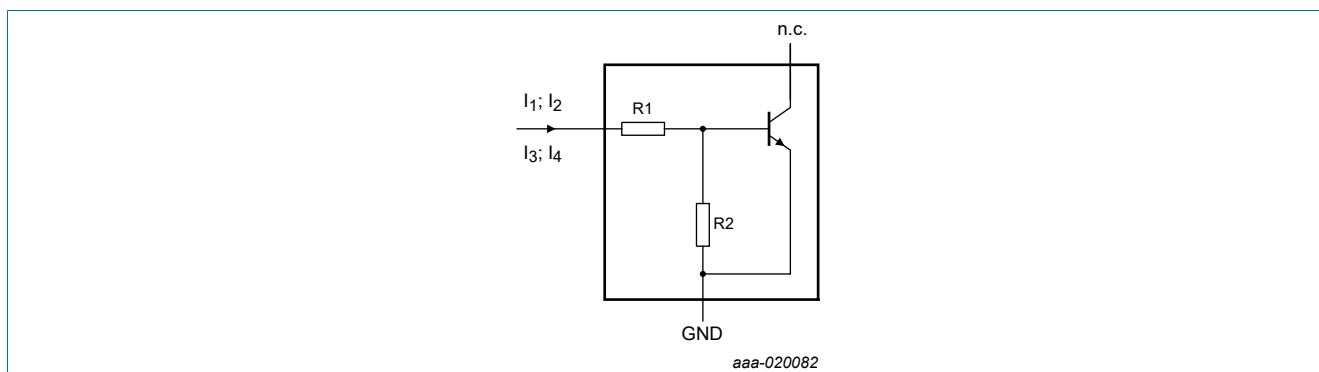


Fig. 15. NPN transistor: Resistor test circuit

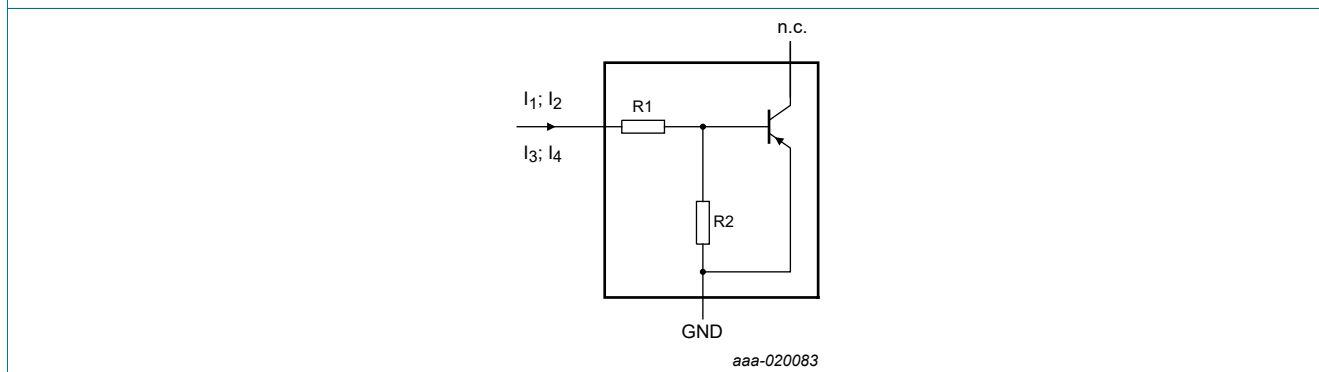


Fig. 16. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

| PUMD15 | R1 (kΩ) | R2 (kΩ) | Test conditions | | | |
|-----------|---------|---------|-----------------|----------------|----------------|----------------|
| | | | I ₁ | I ₂ | I ₃ | I ₄ |
| TR1 (NPN) | 4.7 | 4.7 | 600 μA | 700 μA | -600 μA | -700 μA |
| TR2 (PNP) | 4.7 | 4.7 | -600 μA | -700 μA | 600 μA | 700 μA |

12. Package outline

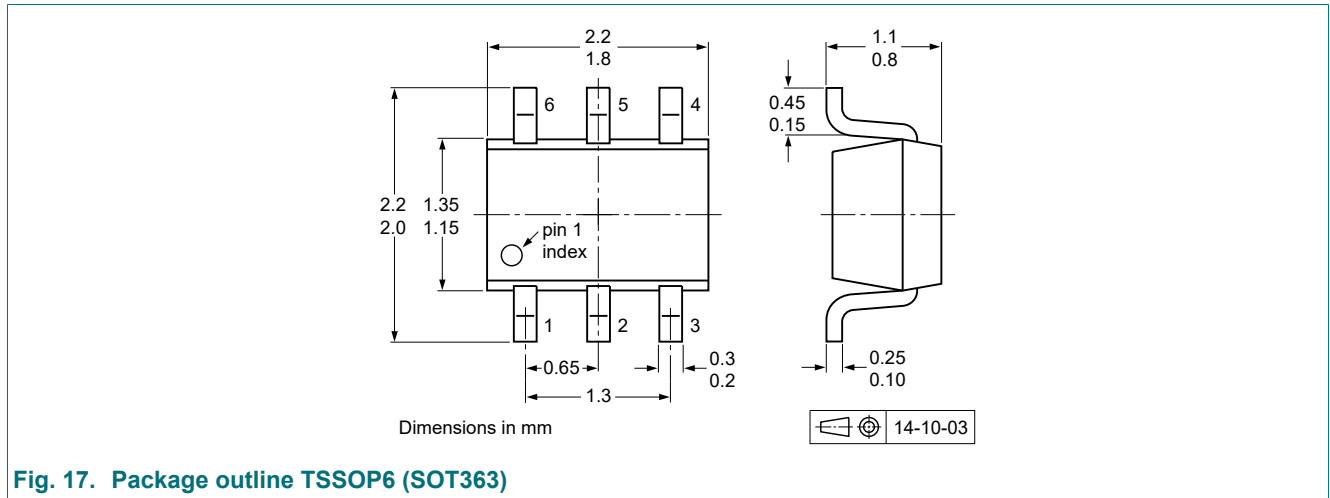


Fig. 17. Package outline TSSOP6 (SOT363)

13. Soldering

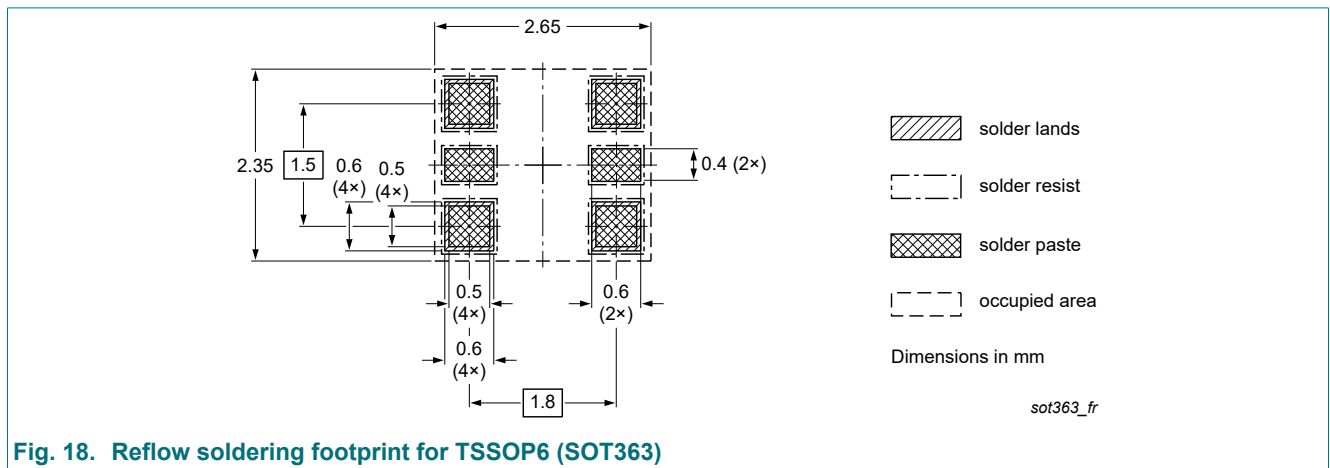


Fig. 18. Reflow soldering footprint for TSSOP6 (SOT363)

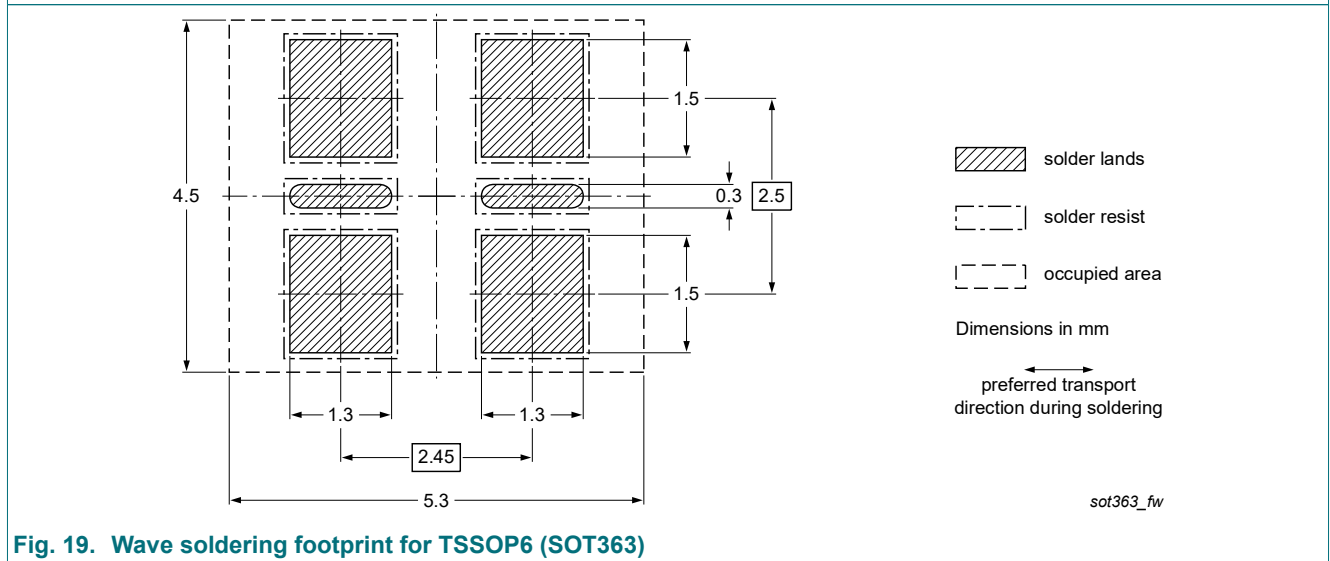


Fig. 19. Wave soldering footprint for TSSOP6 (SOT363)

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 4.7 kΩ, R2 = 4.7 kΩ

14. Revision history

Table 9. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|---|-----------------------|---------------|-------------------|
| PUMD15 v.5 | 20230331 | Product data sheet | - | PEMD15_PUMD15 v.4 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Family data sheet reduced to single type data sheet. Packing information removed. | | | |
| PEMD15_PUMD15 v.4 | 20111219 | Product data sheet | - | PEMD15_PUMD15 v.3 |
| PEMD15_PUMD15 v.3 | 20090902 | Product data sheet | - | PEMD15_PUMD15 v.2 |
| PEMD15_PUMD15 v.2 | 20050425 | Product data sheet | - | PUMD15 v.1 |
| PUMD15 v.1 | 20040204 | Product specification | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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