

# PUMD30,115 Datasheet

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DiGi Electronics Part Number	PUMD30,115-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	PUMD30,115
Description	TRANS PREBIAS 1NPN 1PNP 6TSSOP
Detailed Description	Pre-Biased Bipolar Transistor (BJT) 1 NPN, 1 PNP - Pre-Biased (Dual) 50V 100mA 300mW Surface Mount 6-TSSOP



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## Purchase and inquiry

Manufacturer Product Number:

PUMD30,115

Series:

-

Transistor Type:

1 NPN, 1 PNP - Pre-Biased (Dual)

Voltage - Collector Emitter Breakdown (Max):

50V

Resistor - Emitter Base (R2):

-

Vce Saturation (Max) @ Ib, Ic:

150mV @ 500µA, 10mA

Frequency - Transition:

-

Grade:

Automotive

Mounting Type:

Surface Mount

Supplier Device Package:

6-TSSOP

Manufacturer:

Nexperia USA Inc.

Product Status:

Active

Current - Collector (Ic) (Max):

100mA

Resistor - Base (R1):

2.2kOhms

DC Current Gain (hFE) (Min) @ Ic, Vce:

30 @ 20mA, 5V

Current - Collector Cutoff (Max):

1µA

Power - Max:

300mW

Qualification:

AEC-Q100

Package / Case:

6-TSSOP, SC-88, SOT-363

Base Product Number:

PUMD30

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.21.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



# PUMD30

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
R1 = 2.2 k $\Omega$ , R2 = open

31 March 2023

Product data sheet

## 1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PUMH30

PNP/PNP complement: PUMB30

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplified circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

## 3. Applications

- Low current peripheral driver
- Cost-saving alternative for BC847BPN
- Controlling IC inputs
- Switching loads

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
V <sub>CEO</sub>	collector-emitter voltage	open base	[1]	-	-	50	V
I <sub>O</sub>	output current		[1]	-	-	100	mA
R1	bias resistor 1 (input)		[2]	1.54	2.2	2.86	k $\Omega$

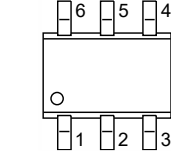
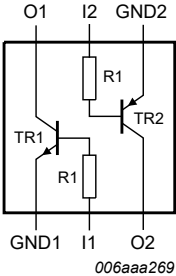
[1] For the PNP transistor with negative polarity.

[2] See section "Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = open

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p><b>TSSOP6 (SOT363)</b></p>	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
<a href="#">PUMD30</a>	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	<a href="#">SOT363</a>

## 7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMD30	%B3

[1] % = placeholder for manufacturing site code

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = open

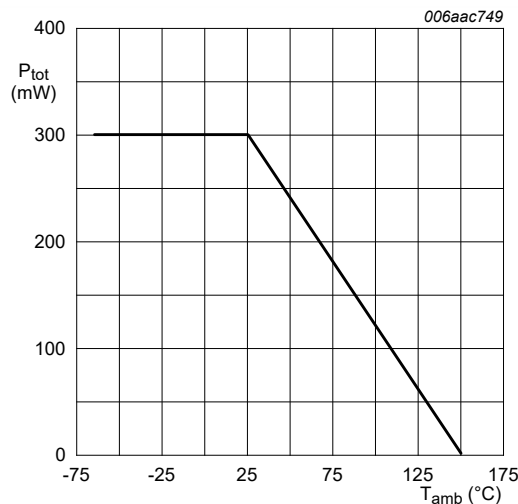
## 8. Limiting values

**Table 5. Limiting values**
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor</b>						
V <sub>CBO</sub>	collector-base voltage	open emitter	[1]	-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	[1]	-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	[1]	-	5	V
I <sub>O</sub>	output current		[1]	-	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[2]	-	200	mW
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[2]	-	300	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] For the PNP transistor with negative polarity.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35  $\mu$ m copper, tin-plated and standard footprint

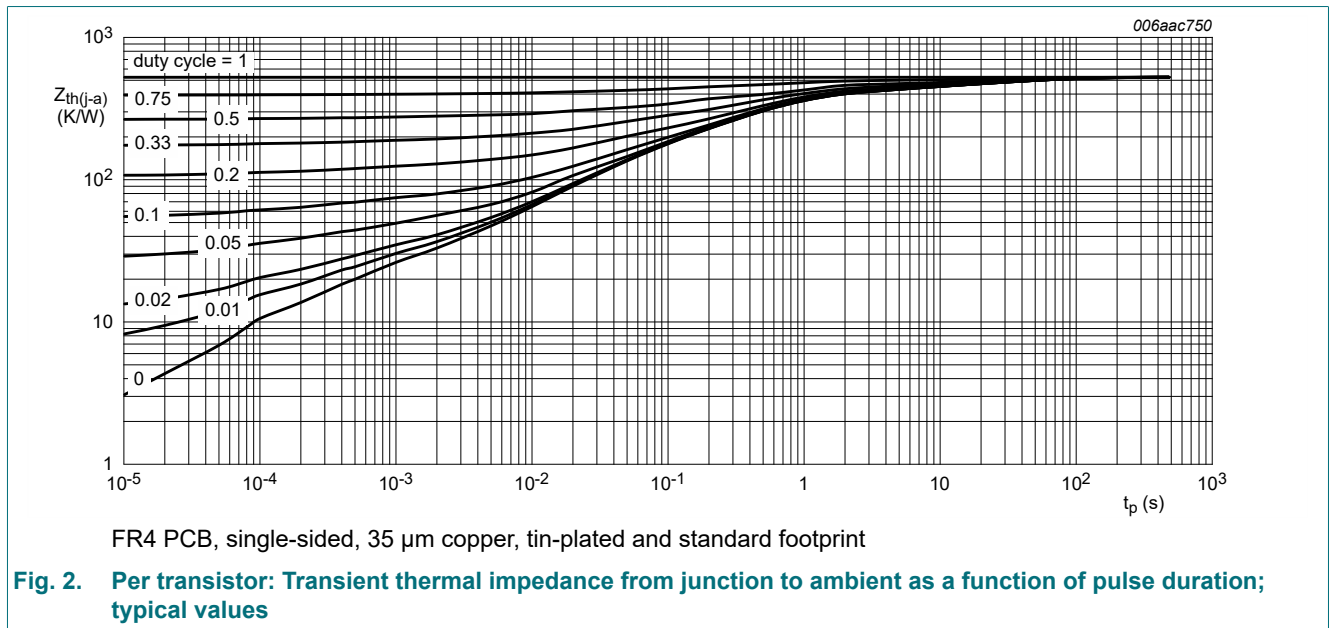
**Fig. 1. Per device: Power derating curve**

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	416	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

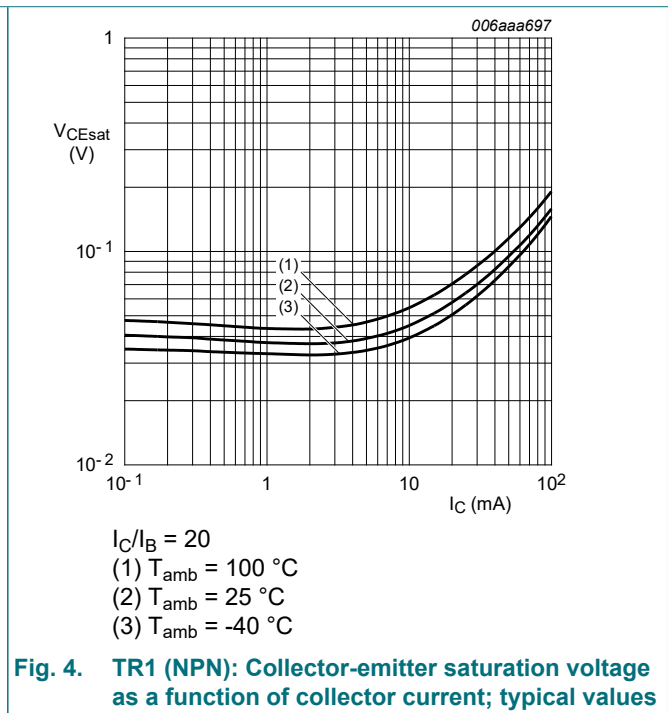
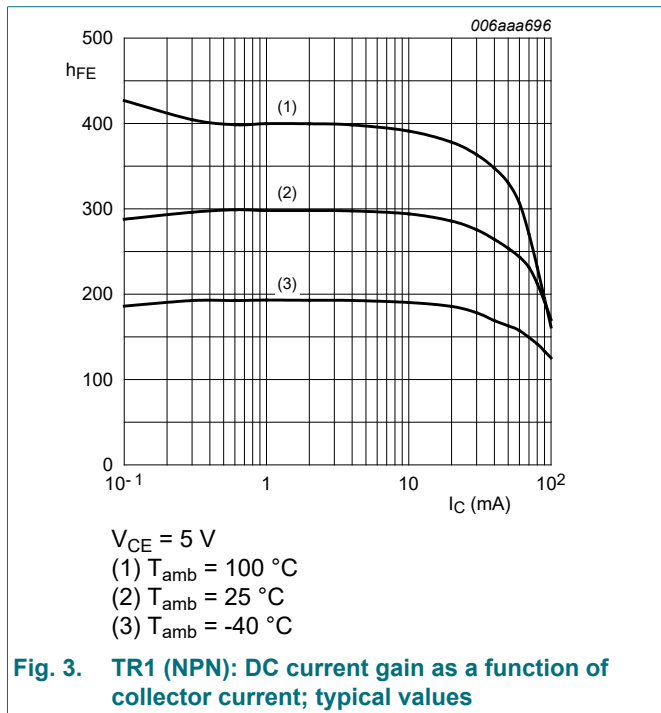


## 10. Characteristics

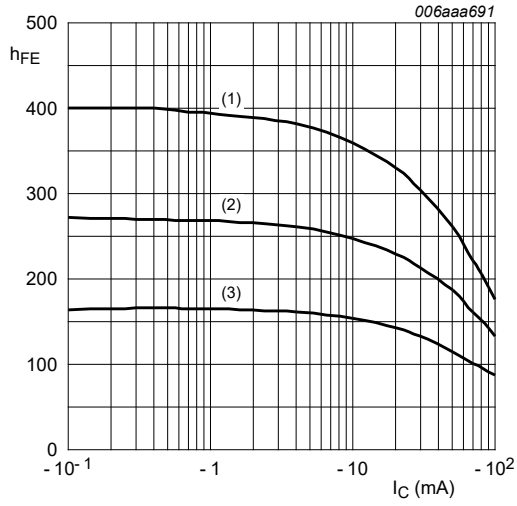
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \mu A; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	[1]	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	[1]	50	-	-	V
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50 \text{ V}; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	[1]	-	-	100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	[1]	-	-	100	nA
		$V_{CE} = 30 \text{ V}; I_B = 0 A; T_j = 150 \text{ }^\circ C$	[1]	-	-	5	$\mu A$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 A; T_{amb} = 25 \text{ }^\circ C$	[1]	-	-	100	nA
$h_{FE}$	DC current gain	$V_{CE} = 5 \text{ V}; I_C = 20 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	[1]	30	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	[1]	-	-	150	mV
R1	bias resistor 1 (input)		[2]	1.54	2.2	2.86	kΩ
<b>TR1 (NPN)</b>							
$C_c$	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 A; i_e = 0 A; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$		-	-	2.5	pF
<b>TR2 (PNP)</b>							
$C_c$	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = 0 A; i_e = 0 A; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$		-	-	3	pF

- [1] For the PNP transistor with negative polarity.  
 [2] See section "Test information" for resistor calculation and test conditions.

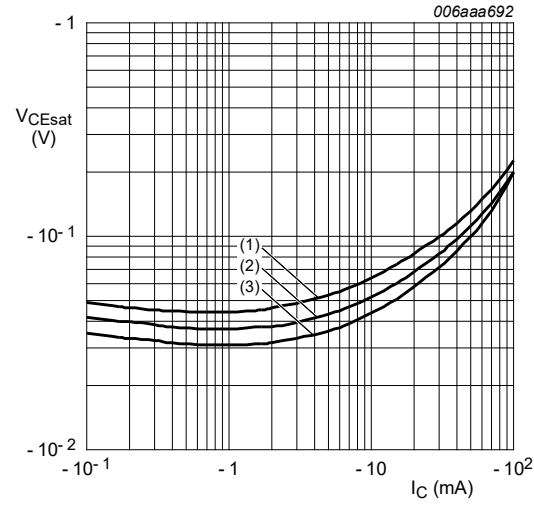


50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 2.2 kΩ, R2 = open



$V_{CE} = -5\text{ V}$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -40\text{ °C}$

Fig. 5. TR2 (PNP): DC current gain as a function of collector current; typical values



$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -40\text{ °C}$

Fig. 6. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 2.2 kΩ, R2 = open

## 11. Test information

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

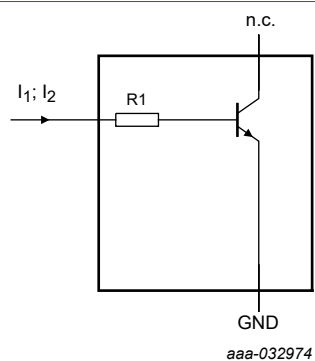


Fig. 7. TR1 (NPN): Resistor test circuit

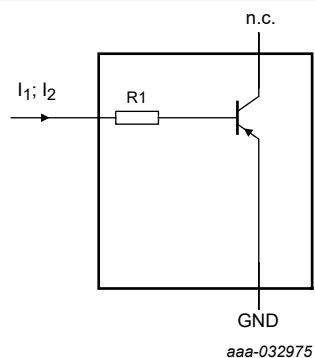


Fig. 8. TR2 (PNP): Resistor test circuit

### Resistor test conditions

Table 8. Resistor test conditions

PUMD30	R1 (kΩ)	R2 (kΩ)	Test conditions	
			I <sub>1</sub>	I <sub>2</sub>
TR1 (NPN)	2.2	open	750 μA	950 μA
TR2 (PNP)	2.2	open	-750 μA	-950 μA

## 12. Package outline

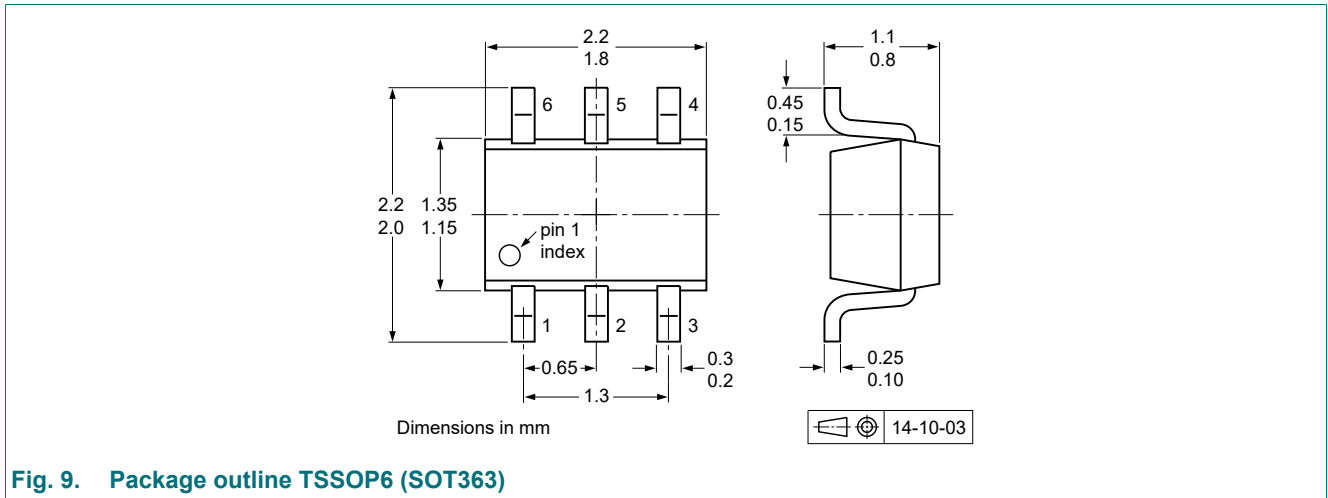


Fig. 9. Package outline TSSOP6 (SOT363)

## 13. Soldering

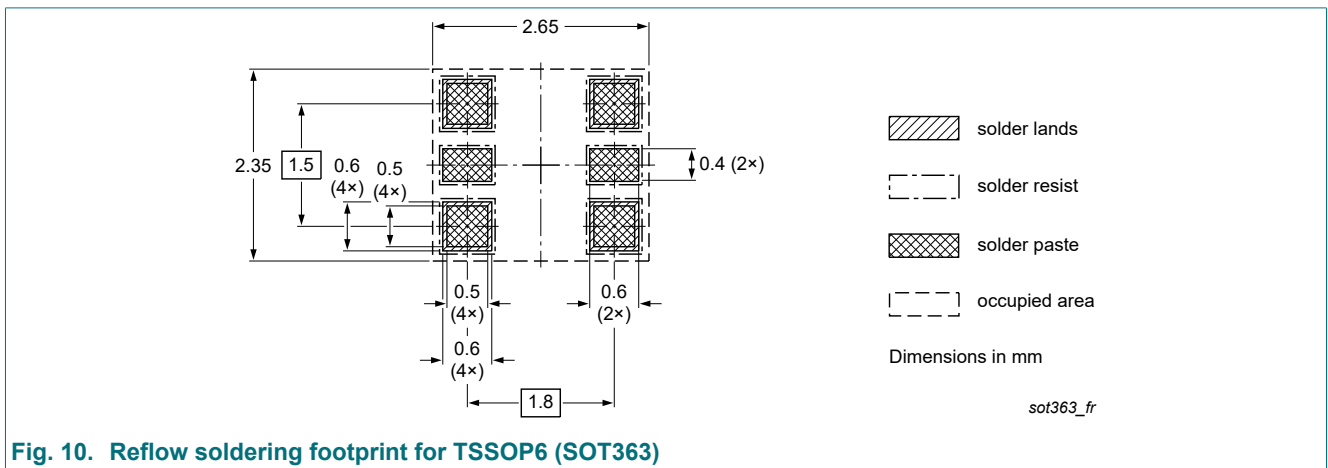


Fig. 10. Reflow soldering footprint for TSSOP6 (SOT363)

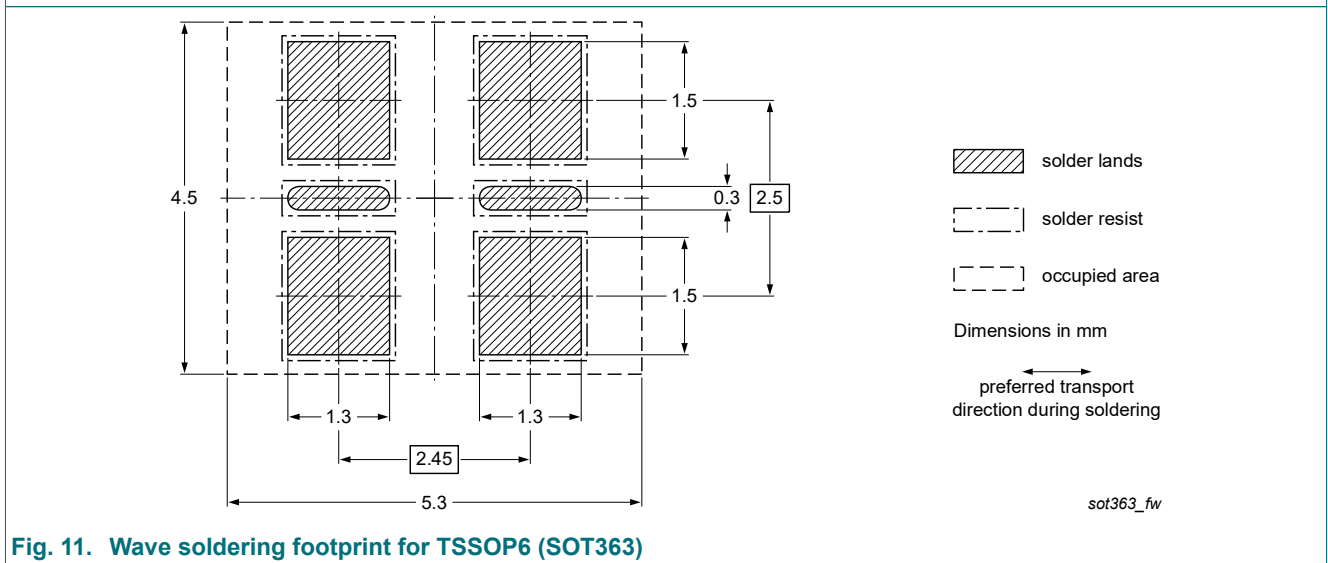


Fig. 11. Wave soldering footprint for TSSOP6 (SOT363)

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = open

## 14. Revision history

**Table 9. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD30 v.2	20230331	Product data sheet	-	PEMD30_PUMD30 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Family data sheet reduced to single type data sheet.</li> <li>Packing information removed.</li> </ul>			
PEMD30_PUMD30 v.1	20060331	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = open

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Date of release: 31 March 2023

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