

# PUMD48,115 Datasheet

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DiGi Electronics Part Number	PUMD48,115-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	PUMD48,115
Description	TRANS PREBIAS 1NPN 1PNP 6TSSOP
Detailed Description	Pre-Biased Bipolar Transistor (BJT) 1 NPN, 1 PNP - Pre-Biased (Dual) 50V 100mA 300mW Surface Mount 6-TSSOP



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## Purchase and inquiry

**Manufacturer Product Number:**

PUMD48,115

**Series:**

-

**Transistor Type:**

1 NPN, 1 PNP - Pre-Biased (Dual)

**Voltage - Collector Emitter Breakdown (Max):**

50V

**Resistor - Emitter Base (R2):**

47kOhms

**Vce Saturation (Max) @ Ib, Ic:**

150mV @ 500µA, 10mA / 100mV @ 250µA, 5mA

**Frequency - Transition:**

-

**Mounting Type:**

Surface Mount

**Supplier Device Package:**

6-TSSOP

**Manufacturer:**

Nexperia USA Inc.

**Product Status:**

Active

**Current - Collector (Ic) (Max):**

100mA

**Resistor - Base (R1):**

47kOhms, 2.2kOhms

**DC Current Gain (hFE) (Min) @ Ic, Vce:**

80 @ 5mA, 5V / 100 @ 10mA, 5V

**Current - Collector Cutoff (Max):**

1µA

**Power - Max:**

300mW

**Package / Case:**

6-TSSOP, SC-88, SOT-363

**Base Product Number:**

PUMD48

## Environmental & Export classification

**RoHS Status:**

ROHS3 Compliant

**REACH Status:**

REACH Unaffected

**HTSUS:**

8541.21.0095

**Moisture Sensitivity Level (MSL):**

1 (Unlimited)

**ECCN:**

EAR99



# PUMD48

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
 $R1 = 47 \text{ k}\Omega$ ,  $R2 = 47 \text{ k}\Omega$  and  $R1 = 2.2 \text{ k}\Omega$ ,  $R2 = 47 \text{ k}\Omega$

1 October 2022

Product data sheet

## 1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

## 3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

## 4. Quick reference data

Table 1. Quick reference data

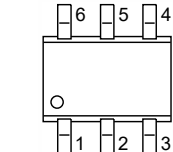
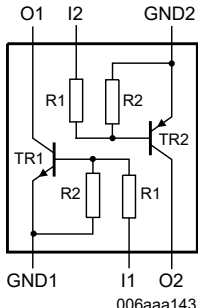
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>							
$V_{CEO}$	collector-emitter voltage	open base		-	-	50	V
$I_O$	output current			-	-	100	mA
<b>Transistor TR1 (NPN)</b>							
R1	bias resistor 1 (input)		[1]	33	47	61	k $\Omega$
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
<b>Transistor TR2 (PNP)</b>							
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	k $\Omega$
R2/R1	bias resistor ratio		[1]	17	21	26	

[1] See section "Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
 $R1 = 47 \text{ k}\Omega$ ,  $R2 = 47 \text{ k}\Omega$  and  $R1 = 2.2 \text{ k}\Omega$ ,  $R2 = 47 \text{ k}\Omega$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>TSSOP6 (SOT363)</p>	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
<a href="#">PUMD48</a>	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	<a href="#">SOT363</a>

## 7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMD48	4%8

[1] % = placeholder for manufacturing site code

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
R1 = 47 k $\Omega$ , R2 = 47 k $\Omega$  and R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

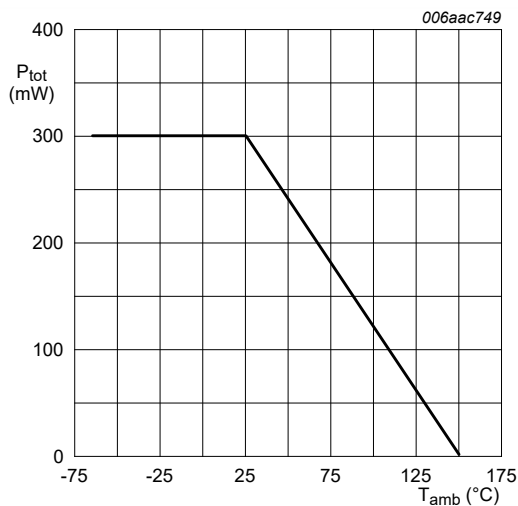
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>						
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector TR1 (NPN)		-	10	V
		open collector TR2 (PNP)		-	-5	V
V <sub>I</sub>	input voltage	positive (input voltage TR1)		-	40	V
		negative (input voltage TR1)		-	-10	V
		positive (input voltage TR2)		-	5	V
		negative (input voltage TR2)		-	-12	V
I <sub>O</sub>	output current			-	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	200	mW
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	300	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35  $\mu$ m copper, tin-plated and standard footprint

**Fig. 1. Per device: Power derating curve**

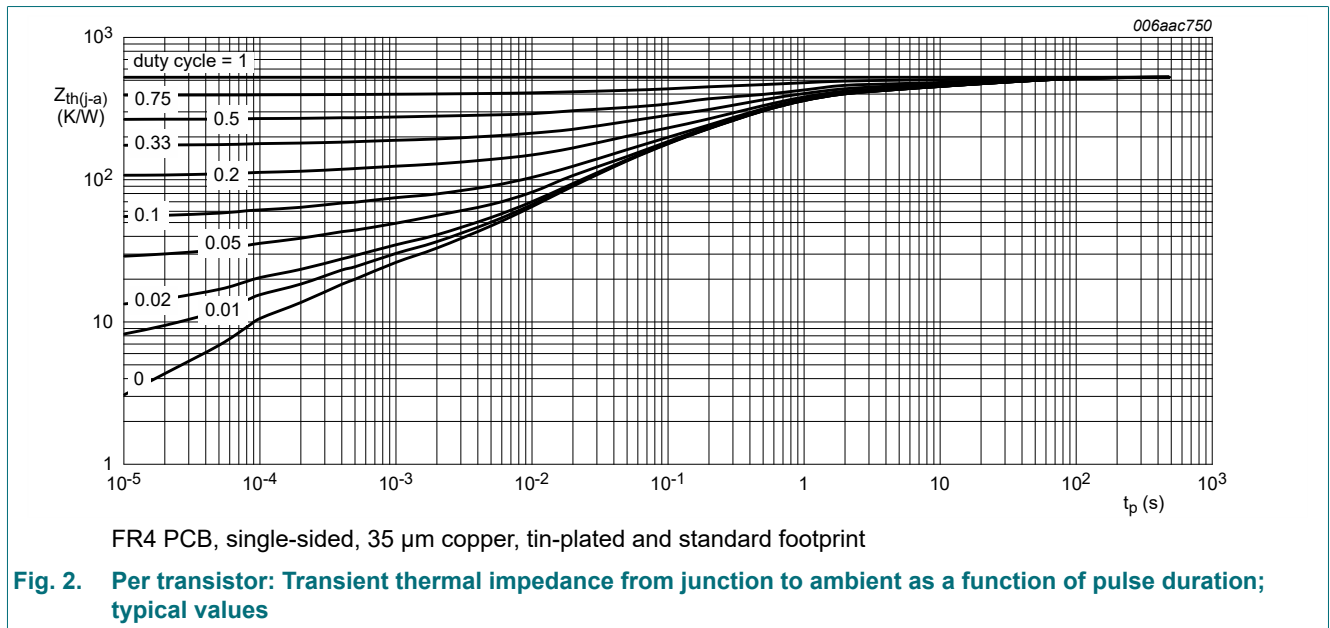
50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
 R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
R1 = 47 k $\Omega$ , R2 = 47 k $\Omega$  and R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

## 10. Characteristics

**Table 7. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor; for the PNP transistor with negative polarity</b>							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\text{ }\mu\text{A}$ ; $I_E = 0\text{ A}$	50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2\text{ mA}$ ; $I_B = 0\text{ A}$	50	-	-	V	
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50\text{ V}$ ; $I_E = 0\text{ A}$	-	-	100	nA	
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$	-	-	1	$\mu\text{A}$	
		$V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$ ; $T_J = 150\text{ }^{\circ}\text{C}$	-	-	5	$\mu\text{A}$	
<b>Transistor TR1 (NPN)</b>							
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}$ ; $I_C = 0\text{ A}$	-	-	90	$\mu\text{A}$	
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}$ ; $I_C = 5\text{ mA}$	80	-	-		
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}$ ; $I_B = 0.5\text{ mA}$	-	-	100	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$ ; $I_C = 100\text{ }\mu\text{A}$	-	1.2	0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$ ; $I_C = 2\text{ mA}$	3	1.6	-	V	
R1	bias resistor 1 (input)		[1]	33	47	61	k $\Omega$
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}$ ; $I_E = 0\text{ A}$ ; $i_e = 0\text{ A}$ ; $f = 1\text{ MHz}$	-	-	2.5	pF	
$f_T$	transition frequency	$V_{CE} = 5\text{ V}$ ; $I_C = 10\text{ mA}$ ; $f = 100\text{ MHz}$	[2]	-	230	-	MHz
<b>Transistor TR2 (PNP)</b>							
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}$ ; $I_C = 0\text{ A}$	-	-	-180	$\mu\text{A}$	
$h_{FE}$	DC current gain	$V_{CE} = -5\text{ V}$ ; $I_C = -10\text{ mA}$	100	-	-		
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -5\text{ mA}$ ; $I_B = -0.25\text{ mA}$	-	-	-100	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5\text{ V}$ ; $I_C = -100\text{ }\mu\text{A}$	-	-0.6	-0.5	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3\text{ V}$ ; $I_C = -5\text{ mA}$	-1.1	-0.75	-	V	
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	k $\Omega$
R2/R1	bias resistor ratio		[1]	17	21	26	
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}$ ; $I_E = 0\text{ A}$ ; $i_e = 0\text{ A}$ ; $f = 1\text{ MHz}$	-	-	3	pF	
$f_T$	transition frequency	$V_{CE} = -5\text{ V}$ ; $I_C = -10\text{ mA}$ ; $f = 100\text{ MHz}$	[2]	-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
 R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

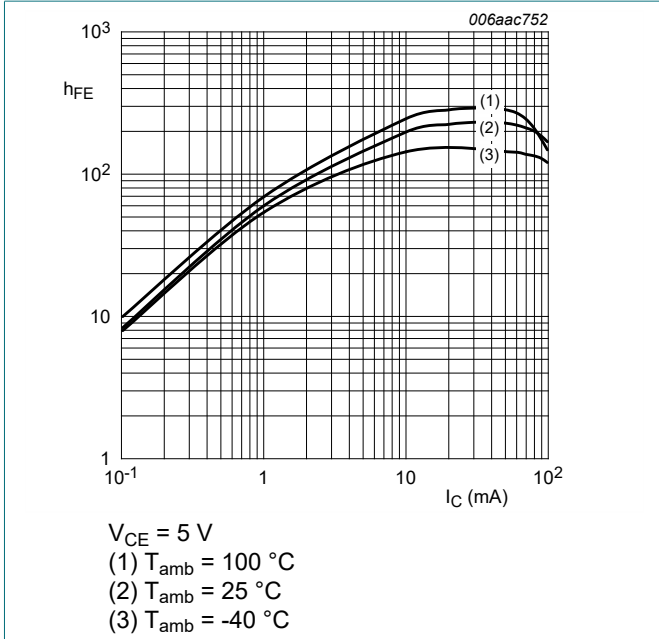


Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values

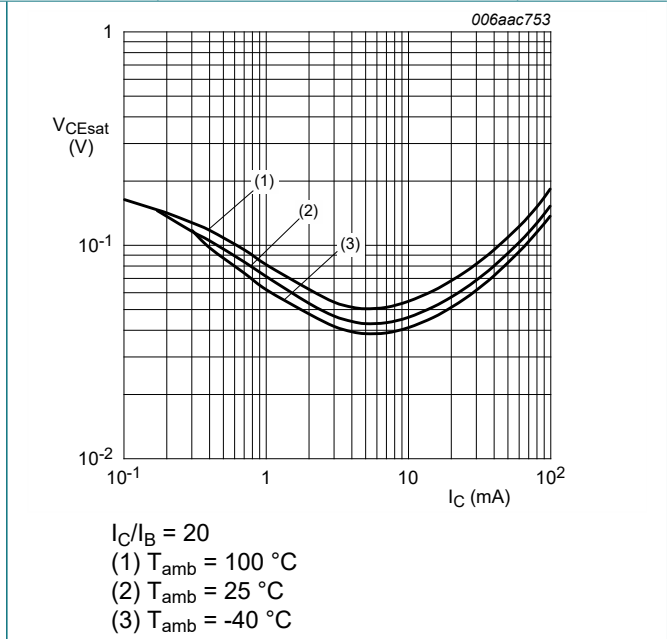


Fig. 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

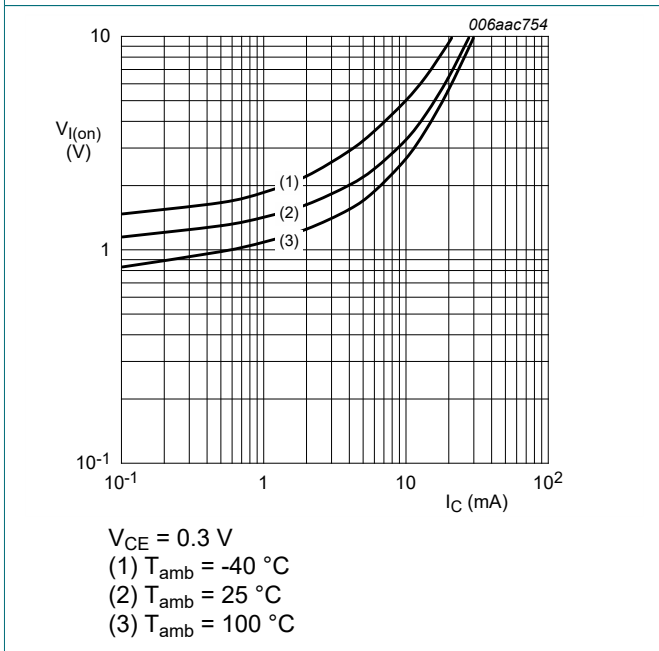


Fig. 5. TR1 (NPN): On-state input voltage as a function of collector current; typical values

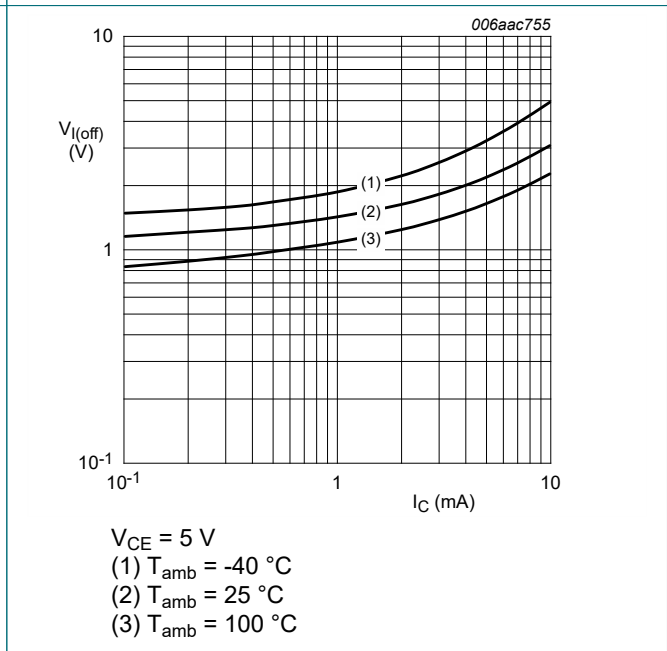
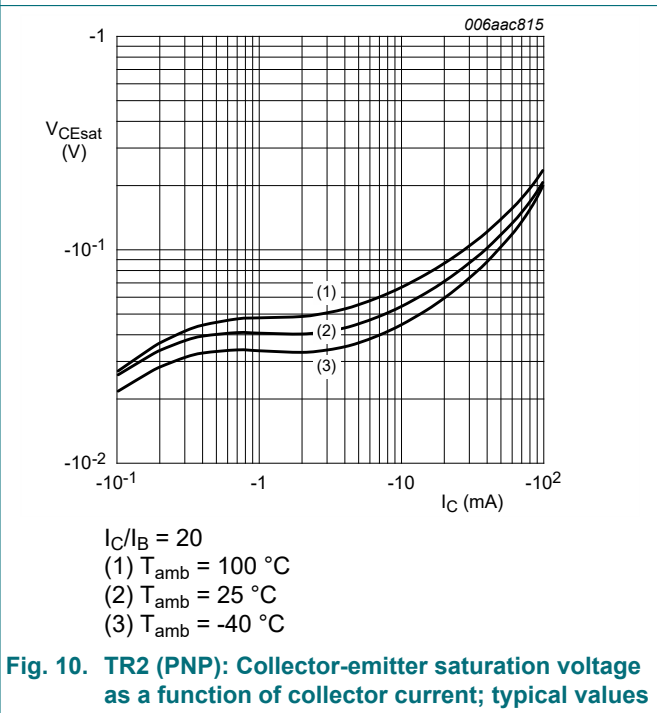
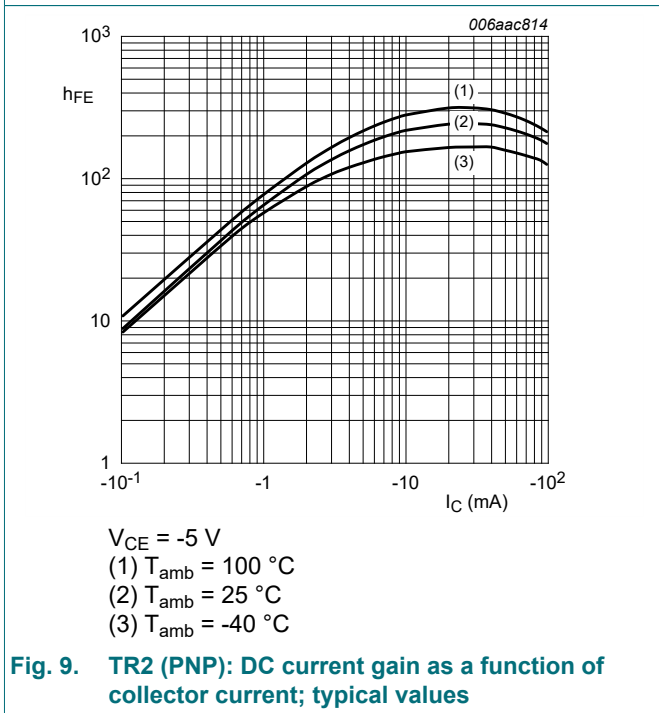
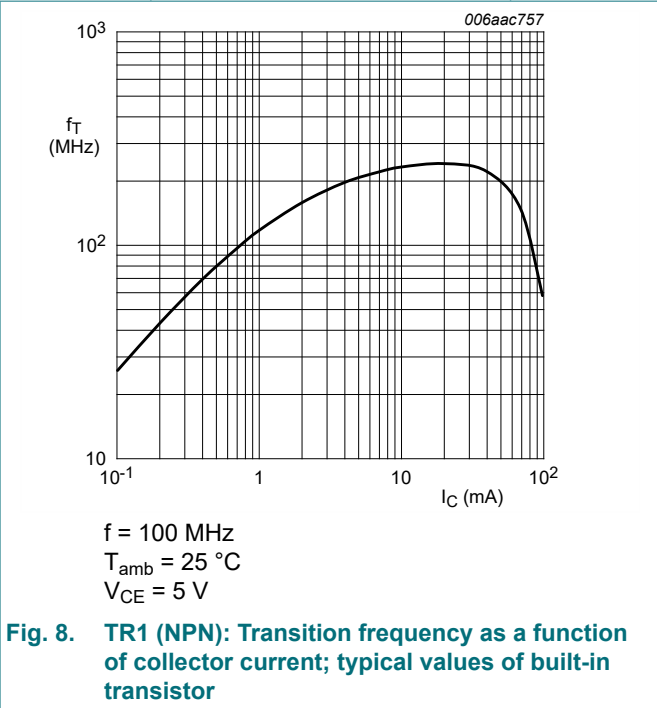
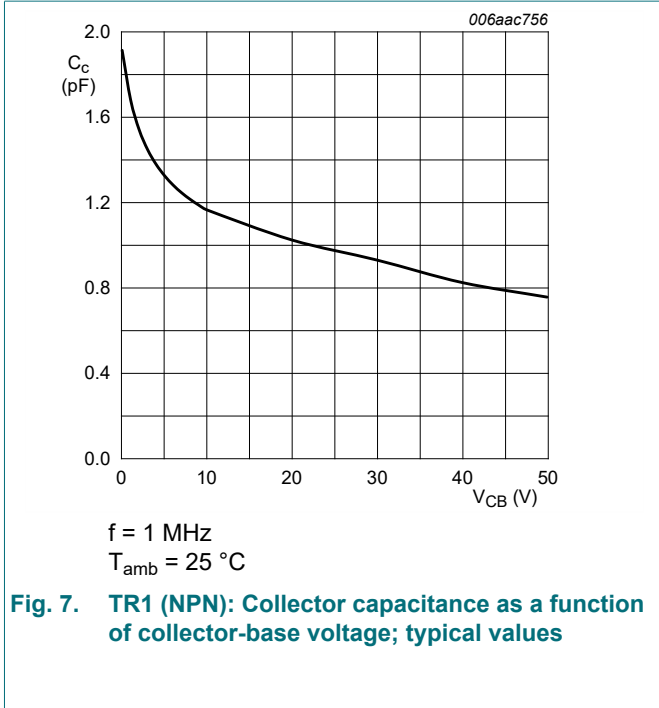


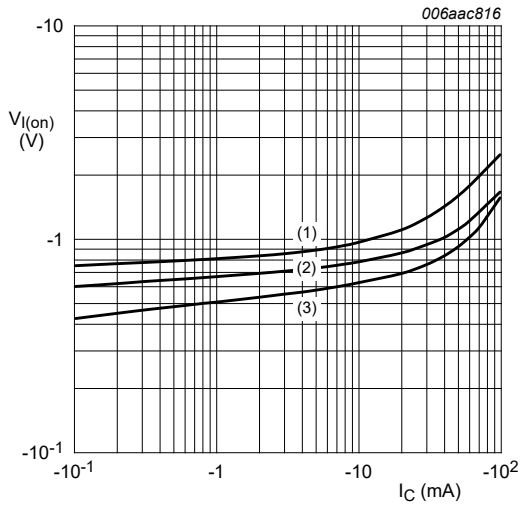
Fig. 6. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
 R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

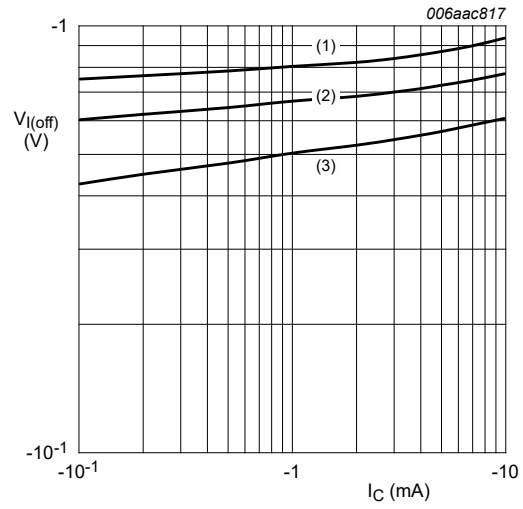


50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
 $R1 = 47 \text{ k}\Omega$ ,  $R2 = 47 \text{ k}\Omega$  and  $R1 = 2.2 \text{ k}\Omega$ ,  $R2 = 47 \text{ k}\Omega$



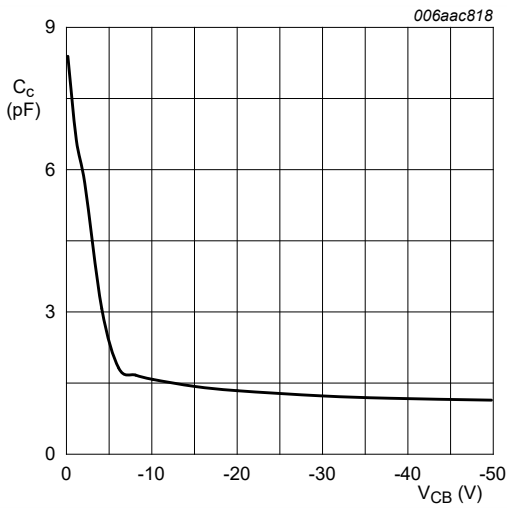
$V_{CE} = -0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig. 11. TR2 (PNP): On-state input voltage as a function of collector current; typical values**



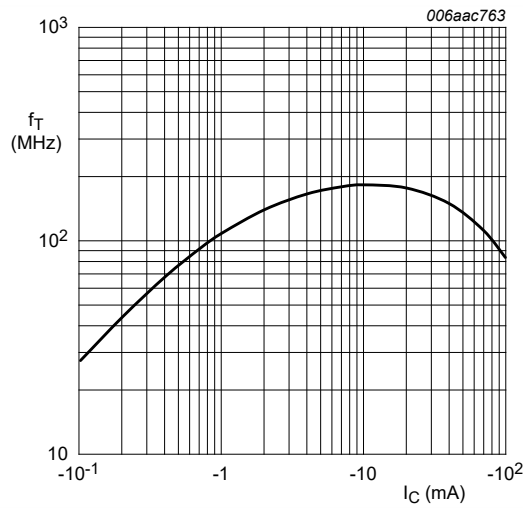
$V_{CE} = -5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig. 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values**



$f = 1 \text{ MHz}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig. 13. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values**



$f = 100 \text{ MHz}$   
 $T_{amb} = 25 \text{ }^\circ\text{C}$   
 $V_{CE} = -5 \text{ V}$

**Fig. 14. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor**

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

## 11. Test information

### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

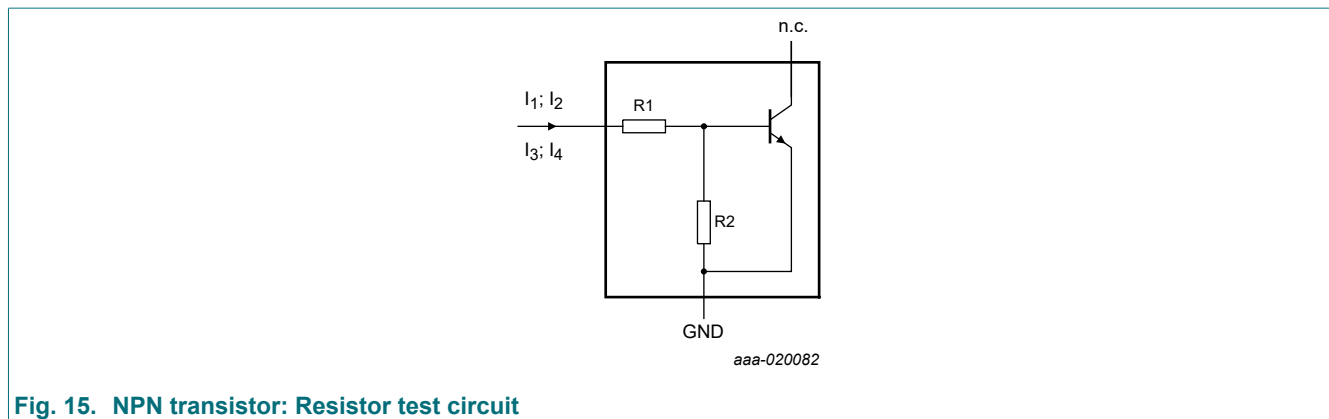


Fig. 15. NPN transistor: Resistor test circuit

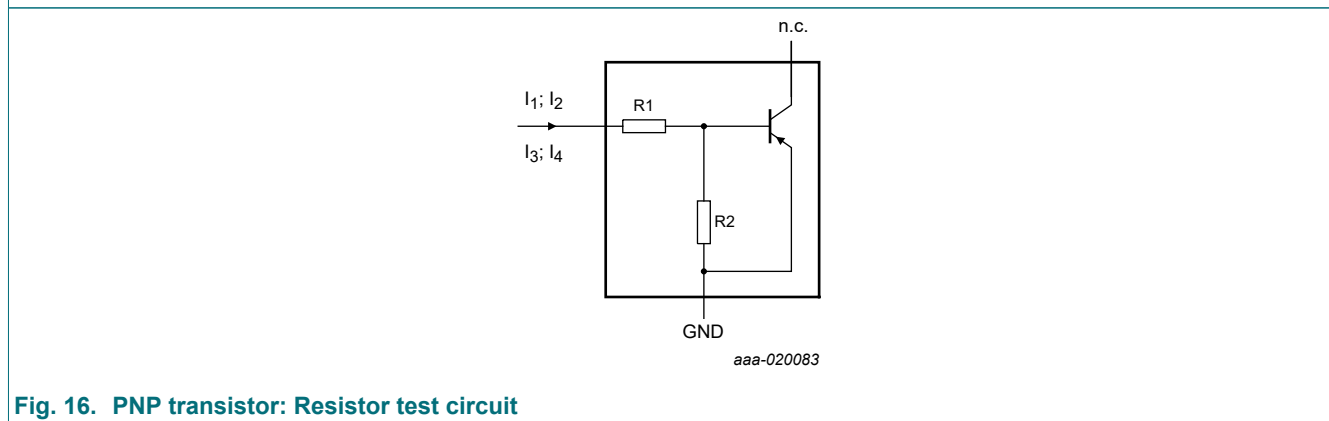


Fig. 16. PNP transistor: Resistor test circuit

### Resistor test conditions

Table 8. Resistor test conditions

PUMD48	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>
TR1 (NPN)	47	47	55 μA	105 μA	-55 μA	-105 μA
TR2 (PNP)	2.2	47	-90 μA	-140 μA	55 μA	105 μA

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
 R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

## 12. Package outline

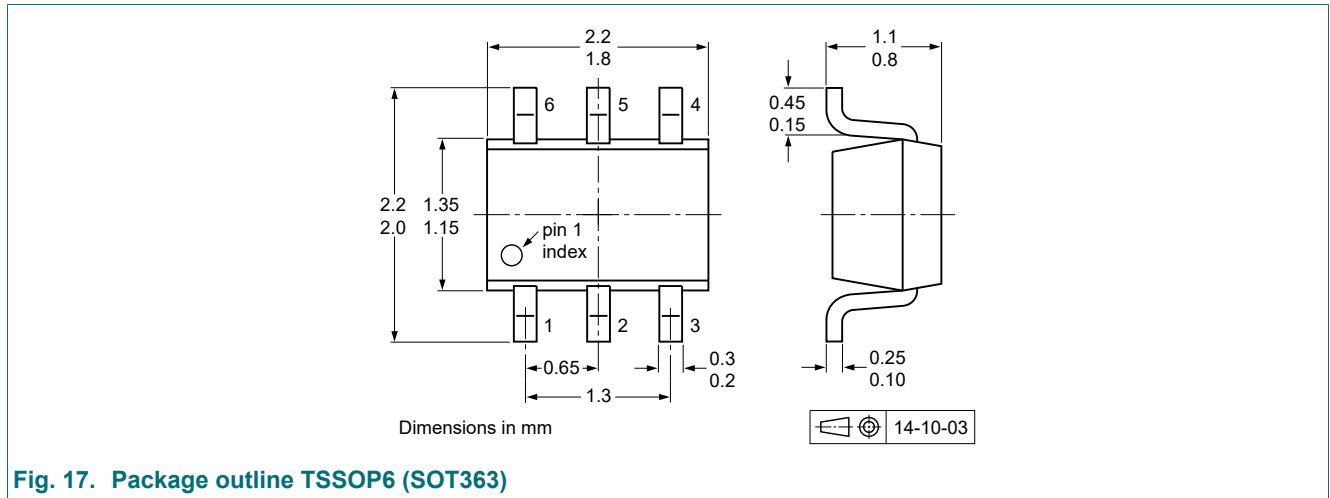


Fig. 17. Package outline TSSOP6 (SOT363)

## 13. Soldering

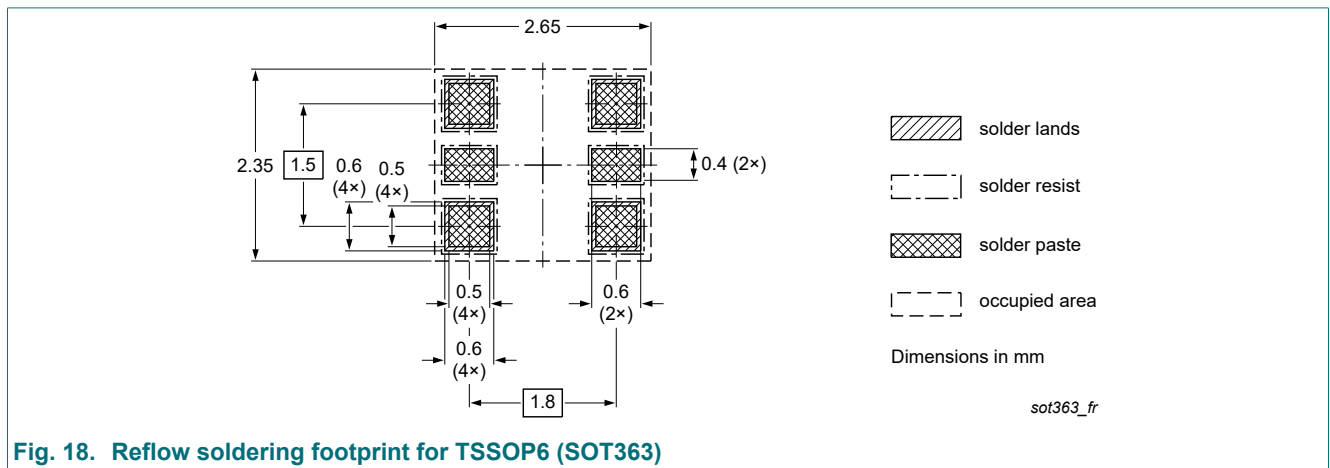


Fig. 18. Reflow soldering footprint for TSSOP6 (SOT363)

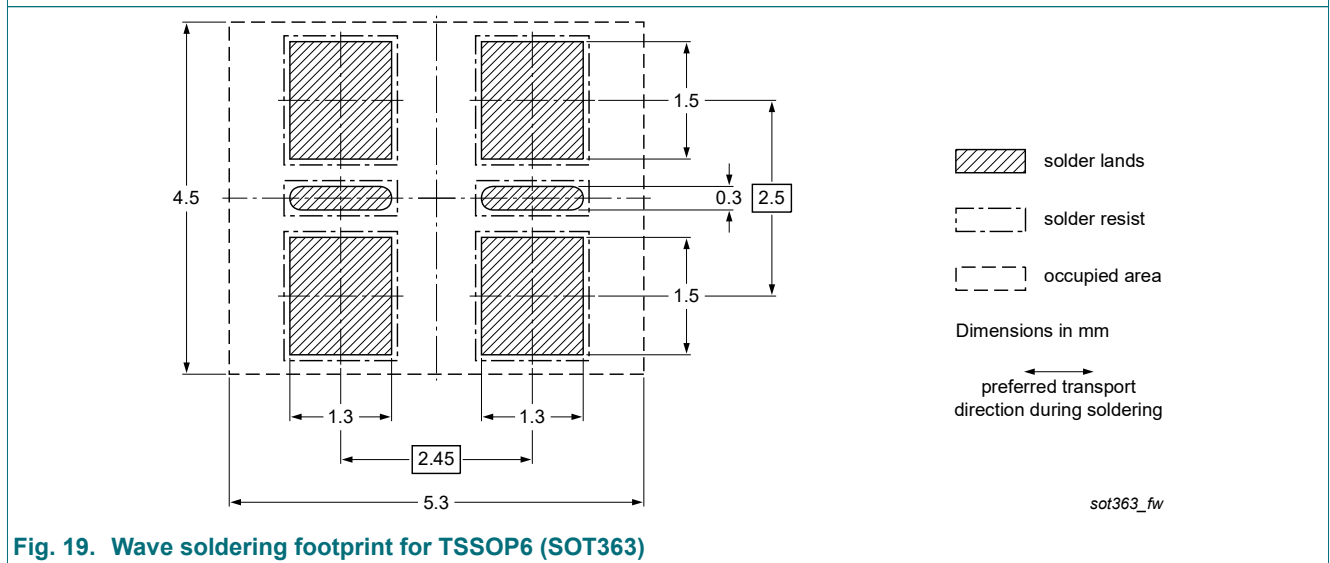


Fig. 19. Wave soldering footprint for TSSOP6 (SOT363)

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
R1 = 47 k $\Omega$ , R2 = 47 k $\Omega$  and R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

## 14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD48 v.7	20221001	Product data sheet	-	PEMD48_PUMD48 v.6
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Family data sheet reduced to single type data sheet.</li> <li>Product changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s).</li> <li>Packing information is removed.</li> </ul>			
PEMD48_PUMD48 v.6	20120124	Product data sheet	-	PEMD48_PUMD48 v.5
PEMD48_PUMD48 v.5	20100413	Product data sheet	-	PEMD48_PUMD48 v.4
PEMD48_PUMD48 v.4	20040624	Product specification	-	PEMD48_PUMD48 v.3
PEMD48_PUMD48 v.3	20040602	Product specification	-	PUMD48 v.2 PEMD48 v.2
PUMD48 v.2	20010201	Product specification	-	PUMD48 v.1
PUMD48 v.1	19990422	Product specification	-	-
PEMD48 v.2	20011107	Product specification	-	PEMD48 v.1
PEMD48 v.1	20010924	Preliminary specification	-	-

**50 V, 100 mA NPN/PNP resistor-equipped double transistor;****R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ**

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## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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**50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
R1 = 47 k $\Omega$ , R2 = 47 k $\Omega$  and R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$**

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Date of release: 1 October 2022

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