

# **PUMH10/ZLH Datasheet**



DiGi Electronics Part Number

PUMH10/ZLH-DG

Manufacturer

Nexperia USA Inc.

Manufacturer Product Number

PUMH10/ZLH

Description

TRANS PREBIAS

**Detailed Description** 

Pre-Biased Bipolar Transistor (BJT) 2 NPN - Pre-Bia sed (Dual) 50V 100mA 230MHz 300mW Surface Mo

unt 6-TSSOP

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## **Purchase and inquiry**

Manufacturer Product Number:	Manufacturer:
PUMH10/ZLH	Nexperia USA Inc.
Series:	Product Status:
	Obsolete
Transistor Type:	Current - Collector (Ic) (Max):
2 NPN - Pre-Biased (Dual)	100mA
Voltage - Collector Emitter Breakdown (Max):	Resistor - Base (R1):
50V	2.2kOhms
Resistor - Emitter Base (R2):	DC Current Gain (hFE) (Min) @ Ic, Vce:
47kOhms	100 @ 10mA, 5V
Vce Saturation (Max) @ lb, lc:	Current - Collector Cutoff (Max):
100mV @ 250μA, 5mA	100nA
Frequency - Transition:	Power - Max:
230MHz	300mW
Grade:	Qualification:
Automotive	AEC-Q101
Mounting Type:	Package / Case:
Surface Mount	6-TSSOP, SC-88, SOT-363
Supplier Device Package:	Base Product Number:
6-TSSOP	PUMH10

## **Environmental & Export classification**

0000.00.0000

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	OBSOLETE
HTSUS:	



# **PUMH10**

50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$ 

1 October 2022

Product data sheet

## 1. General description

NPN/NPN double Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PUMD10 PNP/PNP complement: PUMB10

### 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- · Simplifies circuit design
- · Reduces component count
- Reduces pick and place costs

## 3. Applications

- · Low current peripheral driver
- · Control of IC inputs
- · Replaces general-purpose transistors in digital applications

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
Per transistor	Per transistor							
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-	50	V	
Io	output current			-	-	100	mA	
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	kΩ	
R2/R1	bias resistor ratio		[1]	17	21	26		

[1] See "Section 11: Test information" for resistor calculation and test conditions.



50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$ 

## 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1		O1 I2 GND2
2	l1	input (base) TR1		
3	O2	output (collector) TR2	6 5 4	R1 R2
4	GND2	GND (emitter) TR2		TR2
5	12	input (base) TR2		R2 R1
6	01	output (collector) TR1	☐1 ☐2 ☐3	
			TSSOP6 (SOT363)	<del></del>
				GND1 I1 O2 sym063

## 6. Ordering information

**Table 3. Ordering information** 

Type number	Package				
	Name	Description	Version		
PUMH10		plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363		

## 7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMH10	н%0

[1] % = placeholder for manufacturing site code

### 50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

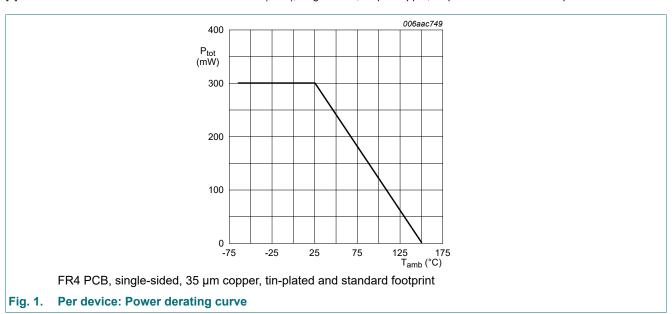
## 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit		
Per transisto	Per transistor							
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V		
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V		
V <sub>EBO</sub>	emitter-base voltage	open collector		-	5	V		
V <sub>I</sub>	input voltage	positive		-	12	V		
		negative		-	-5	V		
Io	output current			-	100	mA		
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	200	mW		
Per device						'		
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[1]	-	300	mW		
T <sub>j</sub>	junction temperature			-	150	°C		
T <sub>amb</sub>	ambient temperature			-65	150	°C		
T <sub>stg</sub>	storage temperature			-65	150	°C		

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.



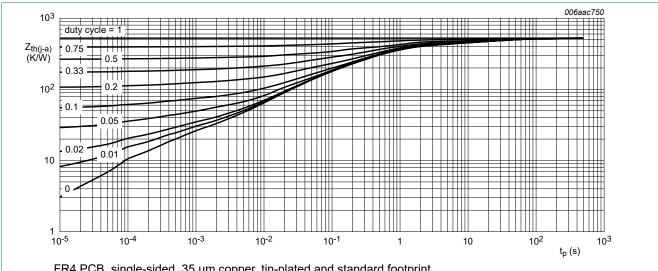
50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$ 

## 9. Thermal characteristics

#### **Table 6. Thermal characteristics**

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device						,	
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; Fig. 2. typical values

### 50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

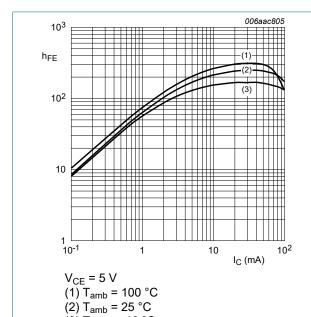
## 10. Characteristics

#### **Table 7. Characteristics**

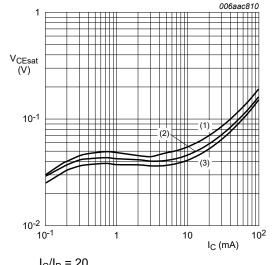
 $T_{amb}$  = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transist	or		1	_			
V <sub>(BR)CBO</sub>	collector-base breakdown voltage	$I_C = 100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$		50	-	-	V
V <sub>(BR)CEO</sub>	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		50	-	-	V
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A	$V_{CB} = 50 \text{ V; } I_E = 0 \text{ A}$		-	100	nA
I <sub>CEO</sub>	collector-emitter cut-off	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A		-	-	100	nA
	current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C		-	-	5	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A		-	-	180	μA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 10 mA		100	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 5 mA; I <sub>B</sub> = 0.25 mA		-	-	100	mV
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 μA		-	0.6	0.5	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 5 mA		1.1	0.75	-	V
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	17	21	26	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = 0 A; i <sub>e</sub> = 0 A; f = 1 MHz		-	-	2.5	pF
f <sub>T</sub>	transition frequency	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 10 mA; f = 100 MHz	[2]	-	230	-	MHz

- See "Section 11: Test information" for resistor calculation and test conditions.
- Characteristics of built-in transistor



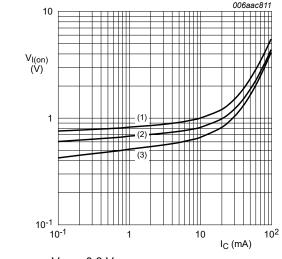




- $I_{\rm C}/I_{\rm B}=20$
- (1) T<sub>amb</sub> = 100 °C
- (2) T<sub>amb</sub> = 25 °C
- (3)  $T_{amb} = -40 \, ^{\circ}C$

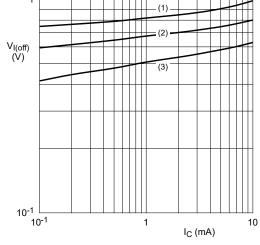
Fig. 4. Collector-emitter saturation voltage as a function of collector current; typical values

### 50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$



 $V_{CE} = 0.3 V$ 

(1) T<sub>amb</sub> = -40 °C (2) T<sub>amb</sub> = 25 °C (3) T<sub>amb</sub> = 100 °C



006aac812

V<sub>CE</sub> = 5 V (1) T<sub>amb</sub> = -40 °C (2) T<sub>amb</sub> = 25 °C (3) T<sub>amb</sub> = 100 °C

Fig. 5. On-state input voltage as a function of collector | Fig. 6. current; typical values



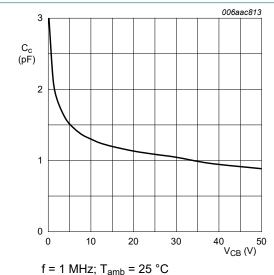
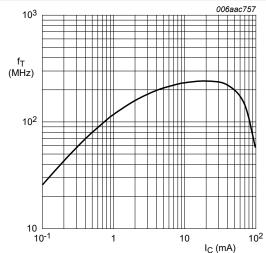


Fig. 7. Collector capacitance as a function of collectorbase voltage; typical values



f = 100 MHz

 $T_{amb} = 25 \, ^{\circ}C$ 

 $V_{CE} = 5 V$ 

Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$ 

## 11. Test information

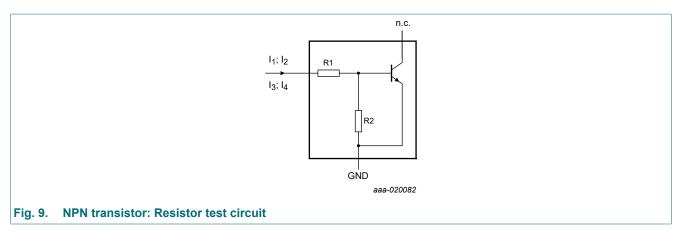
#### **Resistor calculation**

• Calculation of bias resistor 1 (R1)

$$R_{I} = \frac{V(I_{2}) - V(I_{1})}{I_{2} - I_{1}}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I4) - V(I3)}{R1 \cdot (I4 - I3)} - 1$$



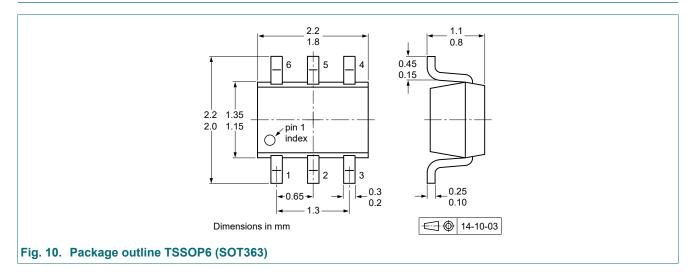
### **Resistor test conditions**

**Table 8. Resistor test conditions** 

PUMH10	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>1</sub>	l <sub>2</sub>	l <sub>3</sub>	14
TR1 (NPN)	2.2	47	90 μΑ	140 μΑ	-55 μΑ	-105 μA
TR2 (NPN)	2.2	47	90 μΑ	140 μΑ	-55 μΑ	-105 µA

50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$ 

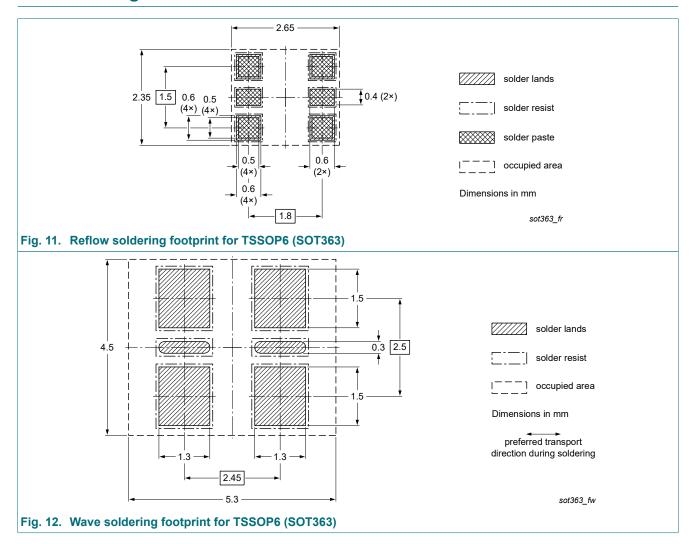
## 12. Package outline



8 / 12

### 50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

## 13. Soldering



9 / 12

## 50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

## 14. Revision history

#### Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes	
PUMH10 v.5	20221001	Product data sheet	-	PEMH10_ PUMH10 v.4	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Family data sheet reduced to single type data sheet.</li> <li>Product changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s).</li> </ul>				
PEMH10_ PUMH10 v.4	20111220	Product data sheet	-	PEMH10_ PUMH10 v.3	
PEMH10_ PUMH10 v.3	20031020	Product data sheet	-	PUMH10 v.2	
PUMH10 v.2	20011022	Preliminary specification	-	PUMH10 v.1	
PUMH10 v.1	20000801	Product specification	-	-	

1 October 2022

#### 50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

## 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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### 50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

## **Contents**

1.	General description	1
2.	Features and benefits	1
3.	Applications	1
4.	Quick reference data	1
5.	Pinning information	2
6.	Ordering information	2
7.	Marking	2
8.	Limiting values	3
9.	Thermal characteristics	4
10.	Characteristics	5
11.	Test information	7
12.	Package outline	8
13.	Soldering	9
14.	Revision history	.10
15.	Legal information	.11

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