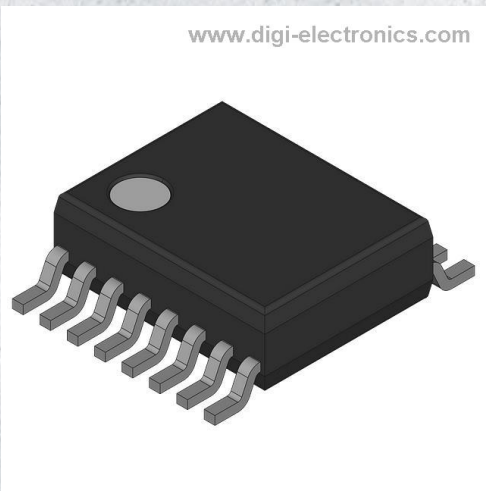
74HC4049DB,112 Datasheet



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DiGi Electronics Part Number	74HC4049DB,112-DG
Manufacturer	NXP Semiconductors
Manufacturer Product Number	74HC4049DB,112
Description	IC BUFFER INVERT 6V 16SSOP
Detailed Description	IC Channel

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74HC4049DB,112	NXP Semiconductors
Series:	Product Status:
74HC	Active
Base Product Number:	
74HC4049	

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
Vendor Undefined	REACH Unaffected

74HC4049

Hex inverting HIGH-to-LOW level shifter

Rev. 9 — 12 March 2024 Product data sheet

1. General description

The 74HC4049 is a hex inverter with over-voltage tolerant inputs. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in HIGH-to-LOW level shifting applications.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Overvoltage tolerant inputs to 15 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4049D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4049PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

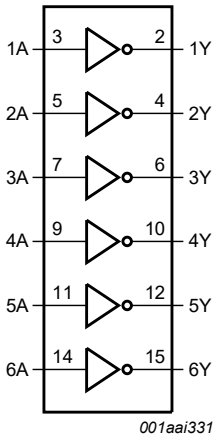


Fig. 1. Logic symbol

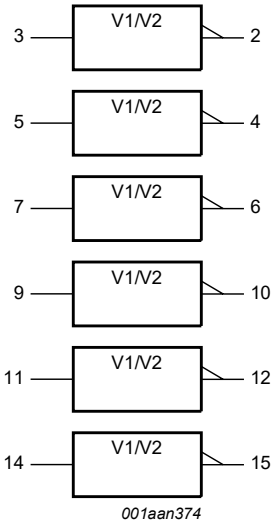


Fig. 2. IEC logic symbol

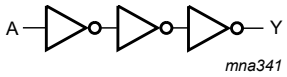
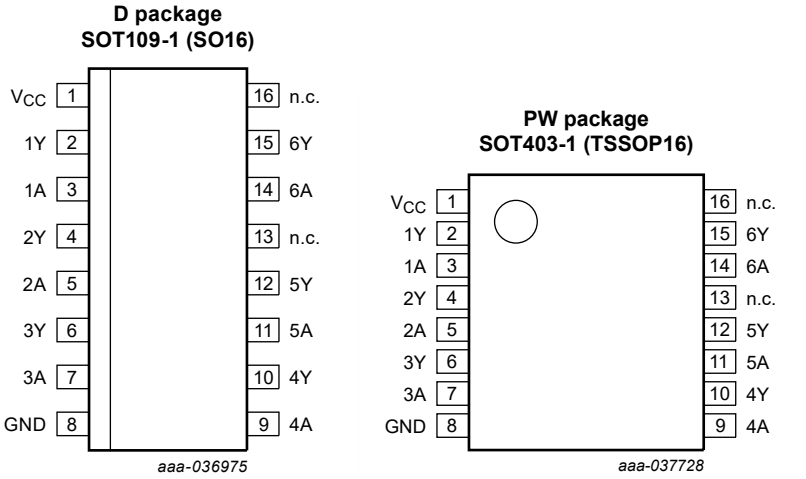


Fig. 3. Logic diagram (one level shifter)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 10, 12, 15	output
1A, 2A, 3A, 4A, 5A, 6A	3, 5, 7, 9, 11, 14	input
GND	8	ground (0 V)
n.c.	13, 16	not connected

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	**nY**
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
V_{IK}	input clamping voltage		-0.5	+16	V
I_{IK}	input clamping current	V_I < -0.5 V	-20	-	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	-	±20	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-	-50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

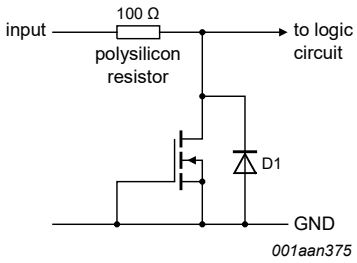


Fig. 4. Input protection for the 74HC4049

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	15	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V; V_I = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V; V_I = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V; V_I = 6.0 V	-	-	83	ns/V
		V_{CC} = 6.0 V; V_I = 10.0 V	-	-	81	ns/V
		V_{CC} = 6.0 V; V_I = 15.0 V	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.3	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.1	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.7	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	1.8	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.3	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
		V_I = 15 V; V_{CC} = 2.0 V to 6.0 V	-	-	±0.5	-	±5.0	-	±5.0	µA
I_{CC}	supply current	V_I = 15 V or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	2.0	-	20	-	40	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

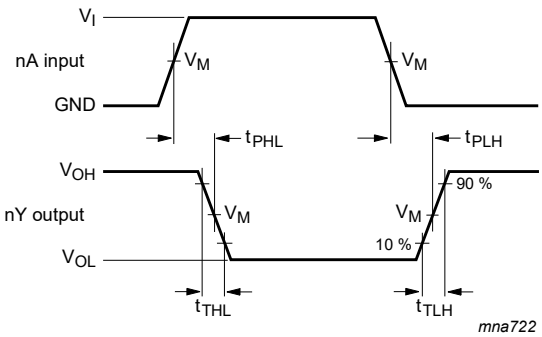
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Fig. 5 [1]								
		V_{CC} = 2.0 V	-	28	85	-	105	-	130	ns
		V_{CC} = 4.5 V	-	10	17	-	21	-	26	ns
		V_{CC} = 5 V; C_L = 15 pF	-	8	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	8	14	-	18	-	22	ns
t_t	transition time	nY; see Fig. 5 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [3]	-	14	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

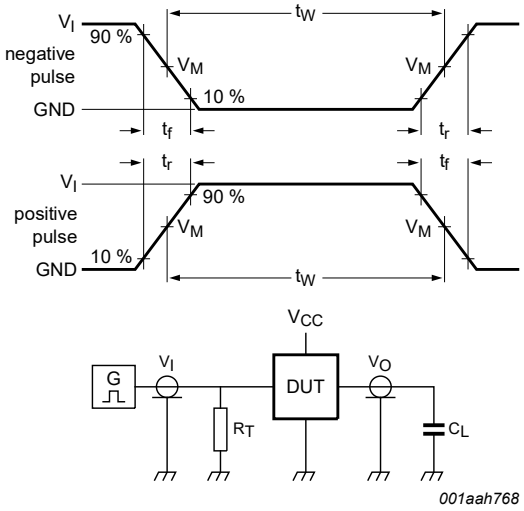


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. The input (nA) to output (nY) propagation delays

Table 8. Measurement points

Input	Output
V_M	V_M
0.5V_{CC}	0.5V_{CC}



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

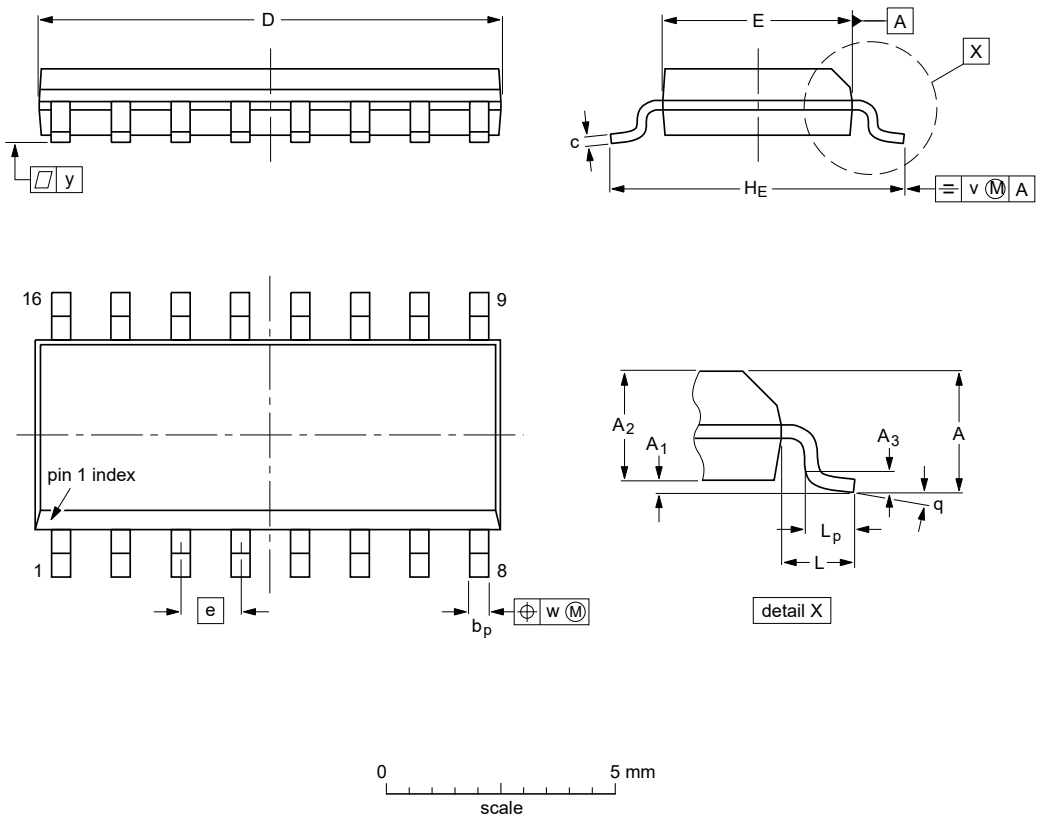
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Input		Load	Test
V_I	**t_r, t_f**	**C_L**	
V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

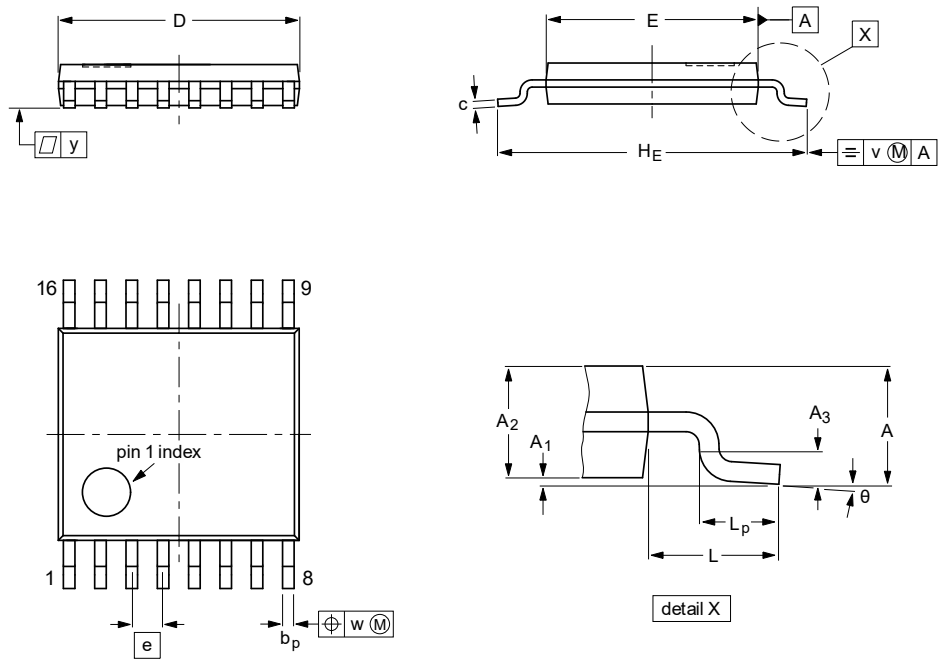
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

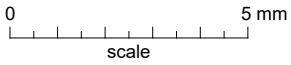
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4049 v.9	20240312	Product data sheet	-	74HC4049 v.8.1
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 7 and Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74HC4049 v.8.1	20231018	Product data sheet	-	74HC4049 v.7
Modifications:	• Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated. • Type number 74HC4049DB (SOT338-1 / SSOP16) removed.			
74HC4049 v.7	20160205	Product data sheet	-	74HC4049 v.6
Modifications:	• Type number 74HC4049N (SOT38-4) removed.			
74HC4049 v.6	20130108	Product data sheet	-	74HC4049 v.5
Modifications:	• New general description.			
74HC4049 v.5	20120803	Product data sheet	-	74HC4049 v.4
Modifications:	• Measurement points added to Fig. 5 (errata).			
74HC4049 v.4	20111212	Product data sheet	-	74HC4049 v.3
74HC4049 v.3	20101230	Product data sheet	-	74HC4049_CNV v.2
74HC4049_CNV v.2	19970827	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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