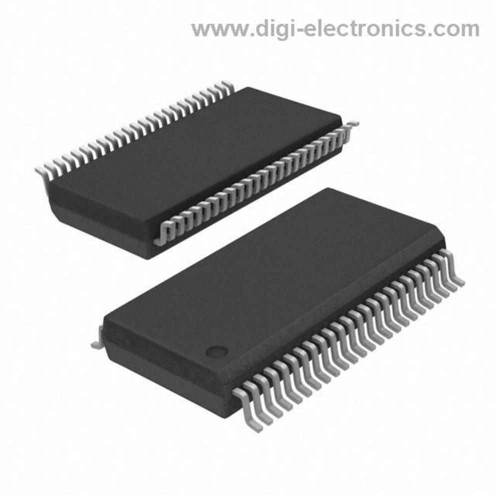
GTL2000DGG,118 Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	GTL2000DGG,118-DG
Manufacturer	NXP Semiconductors
Manufacturer Product Number	GTL2000DGG,118
Description	IC TRANSLATOR BIDIR 48TSSOP
Detailed Description	Voltage Level Translator Bidirectional 1 Circuit 22 Channel 48-TSSOP

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
GTL2000DGG,118	NXP Semiconductors
Series:	Product Status:
-	Obsolete
Translator Type:	Channel Type:
Voltage Level	Bidirectional
Number of Circuits:	Channels per Circuit:
1	22
Voltage - VCCA:	Voltage - VCCB:
1 V ~ 5.5 V	1 V ~ 5.5 V
Input Signal:	Output Signal:
-	-
Output Type:	Data Rate:
Open Drain	-
Operating Temperature:	Features:
-40°C ~ 85°C (TA)	Auto-Direction Sensing
Mounting Type:	Package / Case:
Surface Mount	48-TFSOP (0.240", 6.10mm Width)
Supplier Device Package:	Base Product Number:
48-TSSOP	GTL2000

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

INTEGRATED CIRCUITS

DATA SHEET

GTL2000

22-bit bi-directional low voltage translator

Product data 2003 Apr 01
Supersedes data of 2000 Jan 25

Philips
Semiconductors

22-bit bi-directional low voltage translator GTL2000

FEATURES

- 22-bit bi-directional low voltage translator
- Allows voltage level translation between 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V busses which allows direct interface with GTL, GTL+, LVTTL/TTL and 5 V CMOS levels
- Provides bi-directional voltage translation with no direction pin
- Low 6.5 Ω RDS_{ON} resistance between input and output pins (Sn/Dn)
- Supports hot insertion
- No power supply required - Will not latch up
- 5 V tolerant inputs
- Low stand-by current
- Flow-through pinout for ease of printed circuit board trace routing
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V per JESD22-C101
- Package offer: SSOP48, TSSOP48

APPLICATIONS

- Any application that requires bi-directional or unidirectional voltage level translation from any voltage between 1.0 V & 5.0 V to any voltage between 1.0 V & 5.0 V
- The open drain construction with no direction pin is ideal for bi-directional low voltage (e.g., 1.0 V, 1.2 V, 1.5 V, or 1.8 V) processor I^2C port translation to the normal 3.3 V and/or 5.0 V I^2C bus signal levels or GTL/GTL+ translation to LVTTL/TTL signal levels.

DESCRIPTION

The Gunning Transceiver Logic — Transceiver Voltage Clamps (GTL-TVC) provide high-speed voltage translation with low ON-state resistance and minimal propagation delay. The GTL2000 provides 22 NMOS pass transistors (Sn and Dn) with a common gate (G_{REF}) and a reference transistor (S_{REF} and D_{REF}). The device allows bi-directional voltage translations between 1.0 V and 5.0 V without use of a direction pin.

When the Sn or Dn port is low the clamp is in the ON-state and a low resistance connection exists between the Sn and Dn ports. Assuming the higher voltage is on the Dn port, when the Dn port is high, the voltage on the Sn port is limited to the voltage set by the reference transistor (S_{REF}). When the Sn port is high, the Dn port is pulled to V_{CC} by the pull up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control.

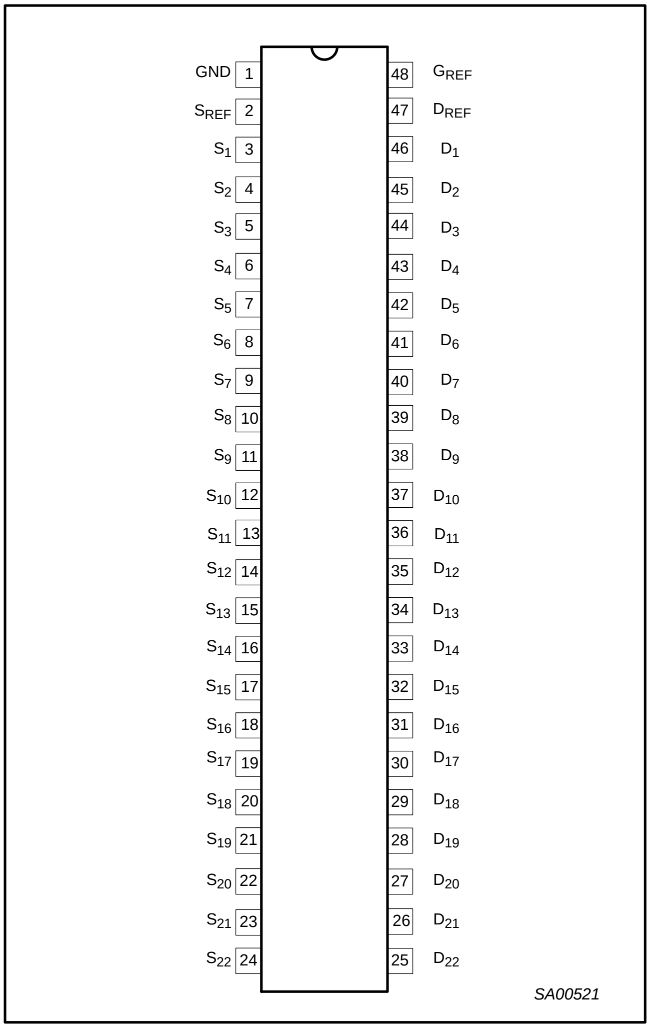
All transistors have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the transistors is symmetrical. Because all transistors in the device are identical, S_{REF} and D_{REF} can be located on any of the other twenty-two matched Sn/Dn transistors, allowing for easier board layout. The translator’s transistors provides excellent ESD protection to lower voltage devices and at the same time protect less ESD resistant devices.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DWG NUMBER
48-Pin Plastic SSOP	-40 to +85 °C	GTL2000DL	GTL2000DL	SOT370-1
48-Pin Plastic TSSOP	-40 to +85 °C	GTL2000DGG	GTL2000DGG	SOT362-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	GND	Ground (0 V)
2	S_{REF}	Source of reference transistor
3 - 24	S_n	Port S_1 to Port S_{22}
25 - 46	D_n	Port D_1 to Port D_{22}
47	D_{REF}	Drain of reference transistor
48	G_{REF}	Gate of reference transistor

FUNCTION TABLE

HIGH to LOW translation assuming Dn is at the higher voltage level

GREF	DREF	SREF	In-Dn	Out-Sn	Transistor
H	H	0 V	X	X	Off
H	H	V_{TT}	H	V_{TT}^1	On
H	H	V_{TT}	L	L^2	On
L	L	0 - V_{TT}	X	X	Off

H = High voltage level
L = Low voltage level
X = Don't Care

NOTES:
1. Sn is not pulled up or pulled down.
2. Sn follows the Dn input low.
3. G_{REF} should be at least 1.5 V higher than S_{REF} for best translator operation.
4. V_{TT} is equal to the S_{REF} voltage.

FUNCTION TABLE

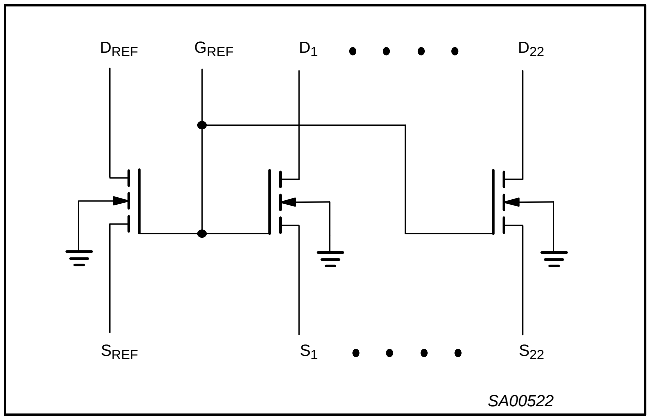
LOW to HIGH translation assuming Dn is at the higher voltage level

GREF	DREF	SREF	In-Sn	Out-Dn	Transistor
H	H	0 V	X	X	Off
H	H	V_{TT}	V_{TT}	H^1	nearly off
H	H	V_{TT}	L	L^2	On
L	L	0 - V_{TT}	X	X	Off

H = High voltage level
L = Low voltage level
X = Don't Care

NOTES:
1. Dn is pulled up to V_{CC} through an external resistor.
2. Dn follows the Sn input low.
3. G_{REF} should be at least 1.5 V higher than S_{REF} for best translator operation.
4. V_{TT} is equal to the S_{REF} voltage.

CLAMP SCHEMATIC



APPLICATIONS

Bi-directional translation

For the bi-directional clamping configuration, higher voltage to lower voltage or lower voltage to higher voltage, the G_{REF} input must be connected to D_{REF} and both pins pulled to high side V_{CC} through a pull-up resistor (typically 200 kΩ). A filter capacitor on D_{REF} is recommended. The processor output can be totem pole or open drain (pull up resistors may be required) and the chipset output can be totem pole or open drain (pull up resistors are required to pull the Dn outputs to V_{CC}). However, if either output is totem pole, data must be uni-directional or the outputs must be 3-statable and the outputs must be controlled by some direction control mechanism to prevent high to low contentions in either direction. If both outputs are open drain, no direction control is needed. The opposite side of the reference transistor (S_{REF}) is connected to the processor core power supply voltage. When D_{REF} is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V V_{CC} supply and S_{REF} is set between1.0 V to V_{CC} - 1.5 V, the output of each Sn has a maximum output voltage equal to S_{REF} and the output of each Dn has a maximum output voltage equal to V_{CC}.

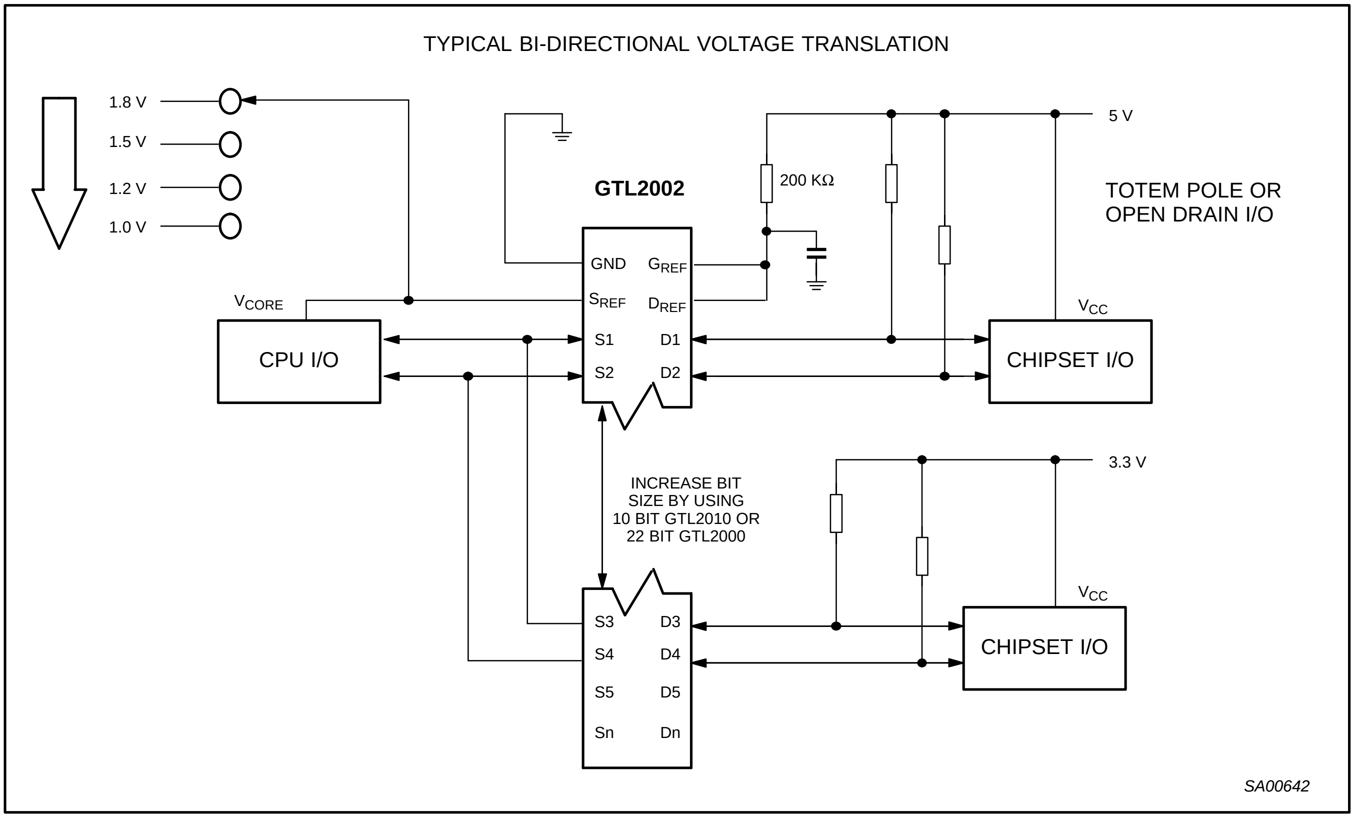


Figure 1. Bi-directional translation to multiple higher voltage levels such as an I^2C bus application

Uni-directional down translation

For uni-directional clamping, higher voltage to lower voltage, the G_{REF} input must be connected to $D_{REF}$and both pins pulled to the higher side V_{CC} through a pull-up resistor (typically 200 kΩ). A filter capacitor on D_{REF} is recommended. Pull up resistors are required if the chipset I/O are open drain. The opposite side of the reference transistor (S_{REF}) is connected to the processor core supply voltage. When D_{REF} is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V V_{CC} supply and S_{REF} is set between 1.0 V to V_{CC} - 1.5 V, the output of each Sn has a maximum output voltage equal to S_{REF}.

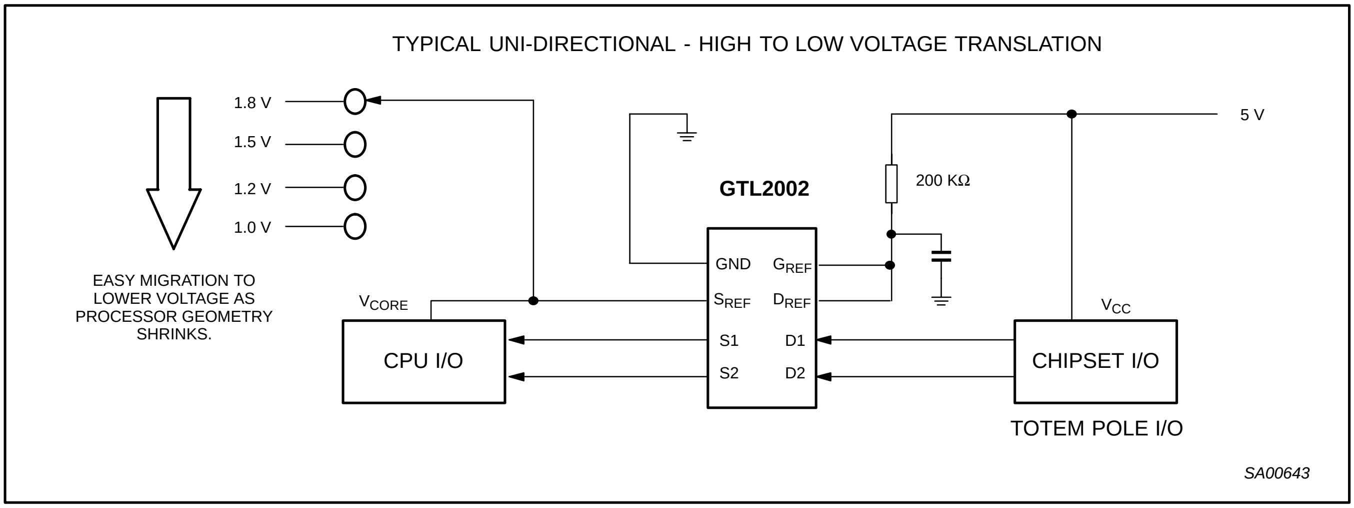


Figure 2. Uni-directional down translation, to protect low voltage processor pins

Uni-directional up translation

For uni-directional up translation, lower voltage to higher voltage, the reference transistor is connected the same as for a down translation. A pull-up resistor is required on the higher voltage side (Dn or Sn) to get the full high level, since the GTL-TVC device will only pass the reference source (S_{REF}) voltage as a high when doing an up translation. The driver on the lower voltage side only needs pull-up resistors if it is open drain.

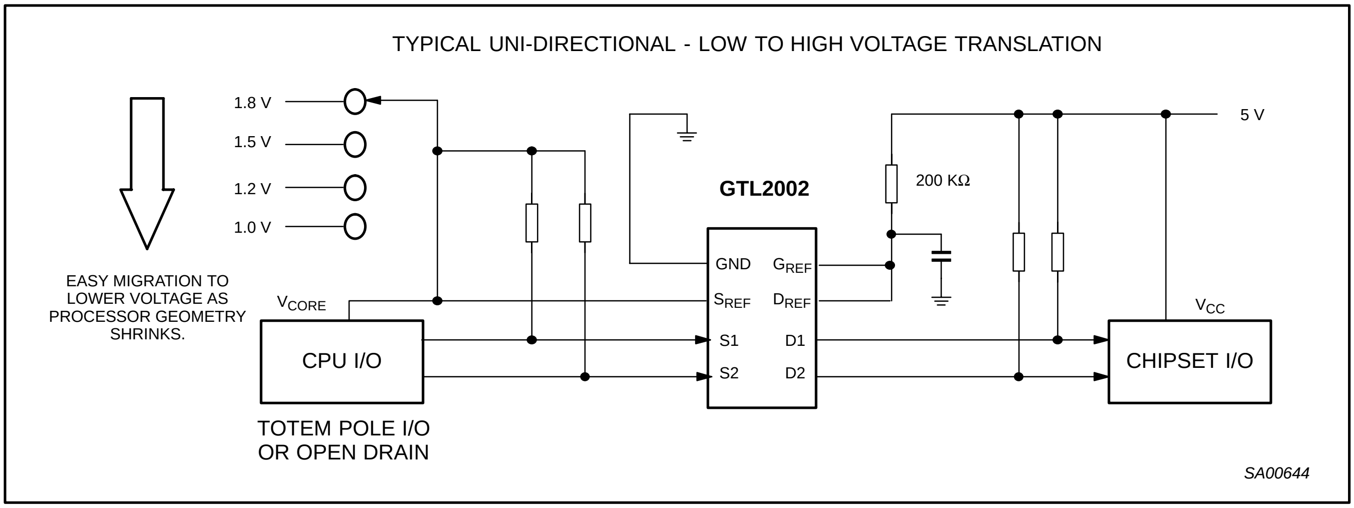


Figure 3. Uni-directional up translation, to higher voltage chip sets

Sizing pull-up resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the “on” state to about 15 mA. This will guarantee a pass voltage of 260 to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage will also be higher in the “on” state. To set the current through each pass transistor at 15 mA, the pull-up resistor value is calculated as follows:

$$\text{Resistor value } (\Omega) = \frac{\text{Pull-up voltage (V)} - 0.35\text{ V}}{0.015\text{ A}}$$

The table below summarizes resistor values for various reference voltages and currents at 15 mA and also at 10 mA and 3 mA. The resistor value shown in the +10% column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL-TVC device at 0.175 V, although the 15 mA only applies to current flowing through the GTL-TVC device. See Application Note *AN10145-01 Bi-Directional Voltage Translators* for more information.

PULL UP RESISTOR VALUES

VOLTAGE	PULL UP RESISTOR VALUE (OHMS)					
	15 mA		10 mA		3 mA	
	NOMINAL	+ 10 %	NOMINAL	+ 10 %	NOMINAL	+ 10 %
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

NOTES:

1. Calculated for V_{OL} = 0.35 V
2. Assumes output driver V_{OL} = 0.175 V at stated current
3. +10% to compensate for V_{DD} range and resistor tolerance.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{SREF}	DC source reference voltage		-0.5 to +7.0	V
V_{DREF}	DC drain reference voltage		-0.5 to +7.0	V
V_{GREF}	DC gate reference voltage		-0.5 to +7.0	V
V_{Sn}	DC voltage Port S_n		-0.5 to +7.0	V
V_{Dn}	DC voltage Port D_n		-0.5 to +7.0	V
I_{REFK}	DC diode current on reference pins	$V_I < 0$	-50	mA
I_{SK}	DC diode current Port S_n	$V_I < 0$	-50	mA
I_{DK}	DC diode current Port D_n	$V_I < 0$	-50	mA
I_{MAX}	DC clamp current per channel	Channel in ON-state	±128	mA
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			Min	Max	
$V_{I/O}$	Input/output voltage (Sn, Dn)		0	5.5	V
V_{SREF}	DC source reference voltage[1]		0	5.5	V
V_{DREF}	DC drain reference voltage		0	5.5	V
V_{GREF}	DC gate reference voltage		0	5.5	V
I_{PASS}	Pass transistor current		—	64	mA
T_{amb}	Operating ambient temperature range	In free air	-40	+85	°C

NOTE:

1. $V_{SREF} \leq V_{DREF}$ - 1.5 V for best results in level shifting applications.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS			UNIT
					MIN	TYP[1]	MAX	
V_{OL}	Low level output voltage	V_{DD} = 3.0 V; V_{SREF} = 1.365 V; V_{Sn} or V_{Dn} = 0.175 V; I_{clamp} = 15.2 mA			—	260	350	mV
V_{IK}	Input clamp voltage	I_I = -18 mA	V_{GREF} = 0		—	—	-1.2	V
I_{IH}	Gate input leakage	V_I = 5 V	V_{GREF} = 0		—	—	5	µA
$C_{I(GREF)}$	Gate capacitance	V_I = 3 V or 0			—	97.4	—	pF
$C_{IO(OFF)}$	Off capacitance	V_O = 3 V or 0	V_{GREF} = 0		—	7.4	—	pF
$C_{IO(ON)}$	On capacitance	V_O = 3 V or 0	V_{GREF} = 3 V		—	18.6	—	pF
r_{on}[2]	On-resistance	V_I = 0	V_{GREF} = 4.5 V	I_O = 64 mA	—	3.5	5	Ω
			V_{GREF} = 3 V		—	4.4	7	
			V_{GREF} = 2.3 V		—	5.5	9	
			V_{GREF} = 1.5 V		—	67	105	
			V_{GREF} = 1.5 V	I_O = 30 mA	—	9	15	Ω
		V_I = 2.4 V	V_{GREF} = 4.5 V	I_O = 15 mA	—	7	10	Ω
			V_{GREF} = 3 V		—	58	80	
		V_I = 1.7 V	V_{GREF} = 2.3 V		—	50	70	

NOTES:

1. All typical values are measured at T_{amb} = 25 °C
2. Measured by the voltage drop between the Sn and the Dn terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (Sn or Dn) terminals.

AC CHARACTERISTICS FOR TRANSLATOR TYPE APPLICATIONS

V_{REF} = 1.365 to 1.635 V; V_{DD1} = 3.0 to 3.6 V; V_{DD2} = 2.36 to 2.64 V; GND = 0 V; $t_r = t_f \leq 3.0$ ns. Refer to the Test Circuit diagram.

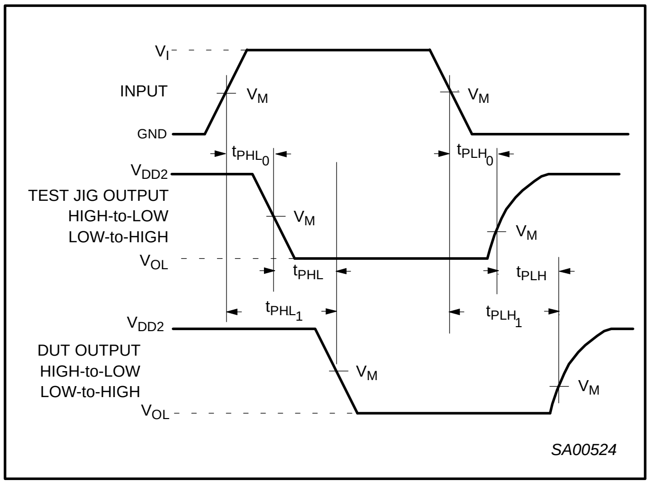
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C			
			MIN	TYP[1]	MAX	
t_{PLH}[2]	Propagation delay Sn to Dn; Dn to Sn		0.5	1.5	5.5	ns

NOTES:

1. All typical values are measured at V_{DD1} = 3.3 V, V_{DD2} = 2.5 V, V_{REF} = 1.5 V and T_{amb} = 25°C.
2. Propagation delay guaranteed by characterization.
3. $C_{ON(max)}$ of 30 pF and a $C_{OFF(max)}$ of 15 pF is guaranteed by design.

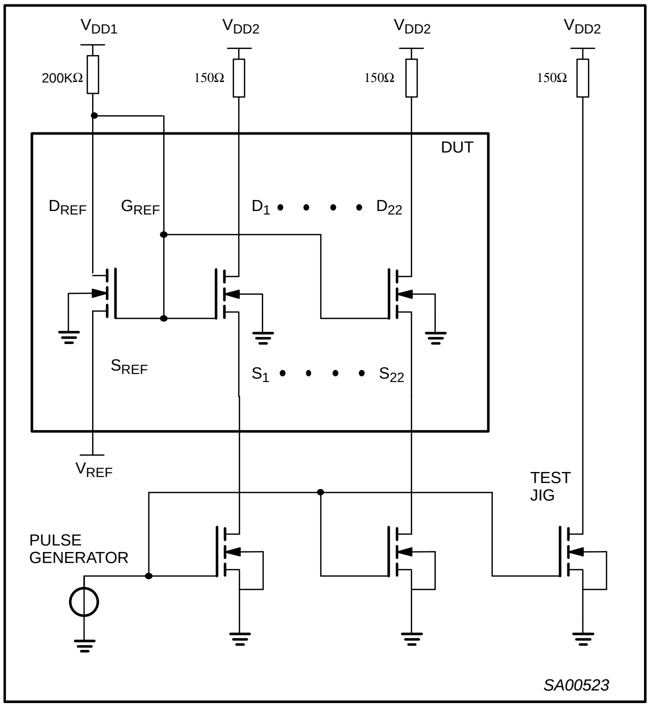
AC WAVEFORMS

V_m = 1.5 V; V_{IN} = GND to 3.0 V



Waveform 1. The Input (S_n) to Output (D_n) Propagation Delays

TEST CIRCUIT



Waveform 2. Load circuit

AC CHARACTERISTICS FOR CBT TYPE APPLICATION

GND = 0 V; $t_{R;}$ C_L = 50 pF

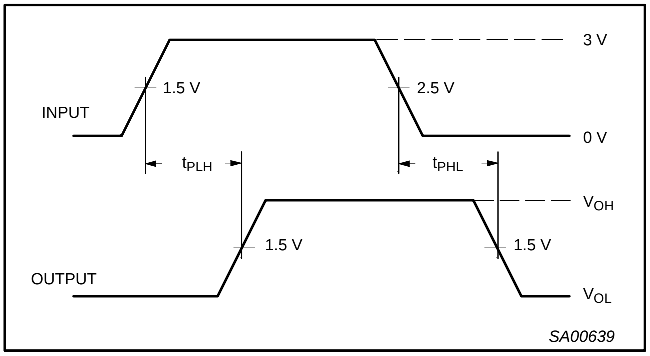
SYMBOL	PARAMETER DESCRIPTION	LIMITS -40 °C to +85°C G_{REF} = 5 V ± 0.5 V			UNITS
		Min	Mean	Max	
t_{pd}	Propagation delay[1]	—	—	250	ps

NOTES:

1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

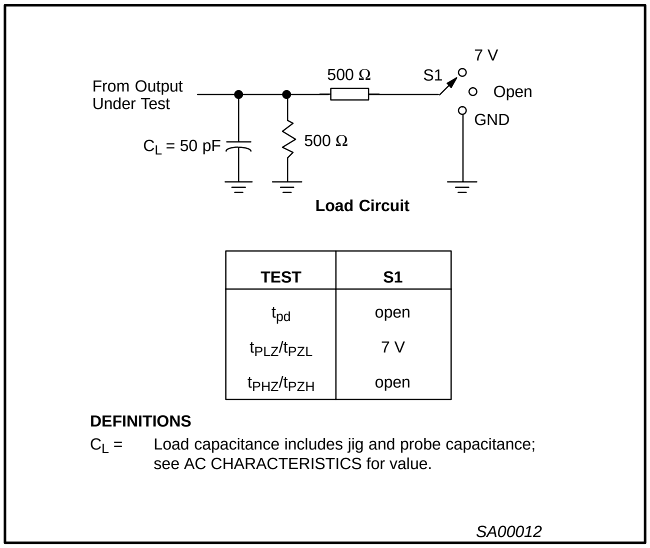
AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V



Waveform 1. Input (Sn) to Output (Dn) Propagation Delays

TEST CIRCUIT AND WAVEFORMS



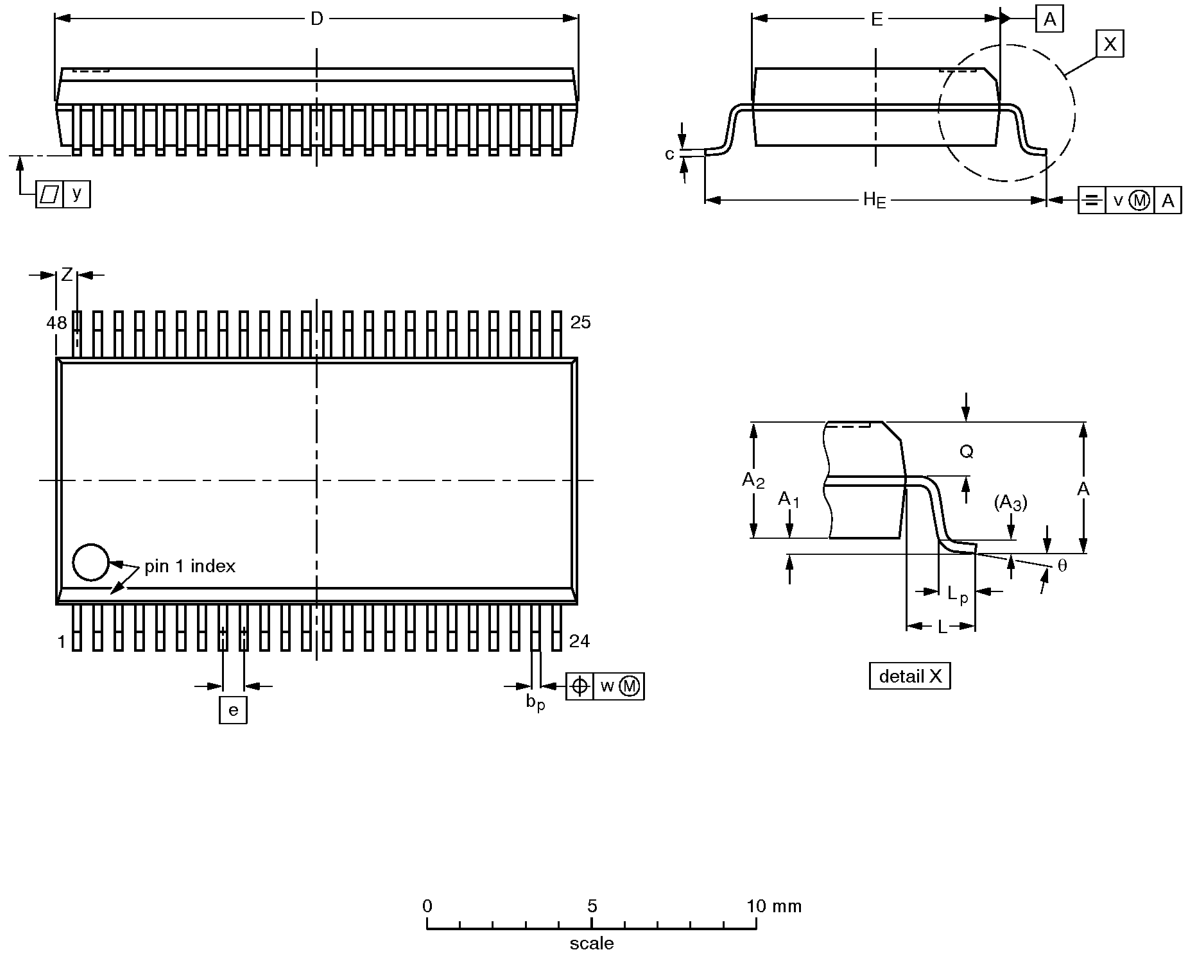
TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

Waveform 2. Load circuit

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

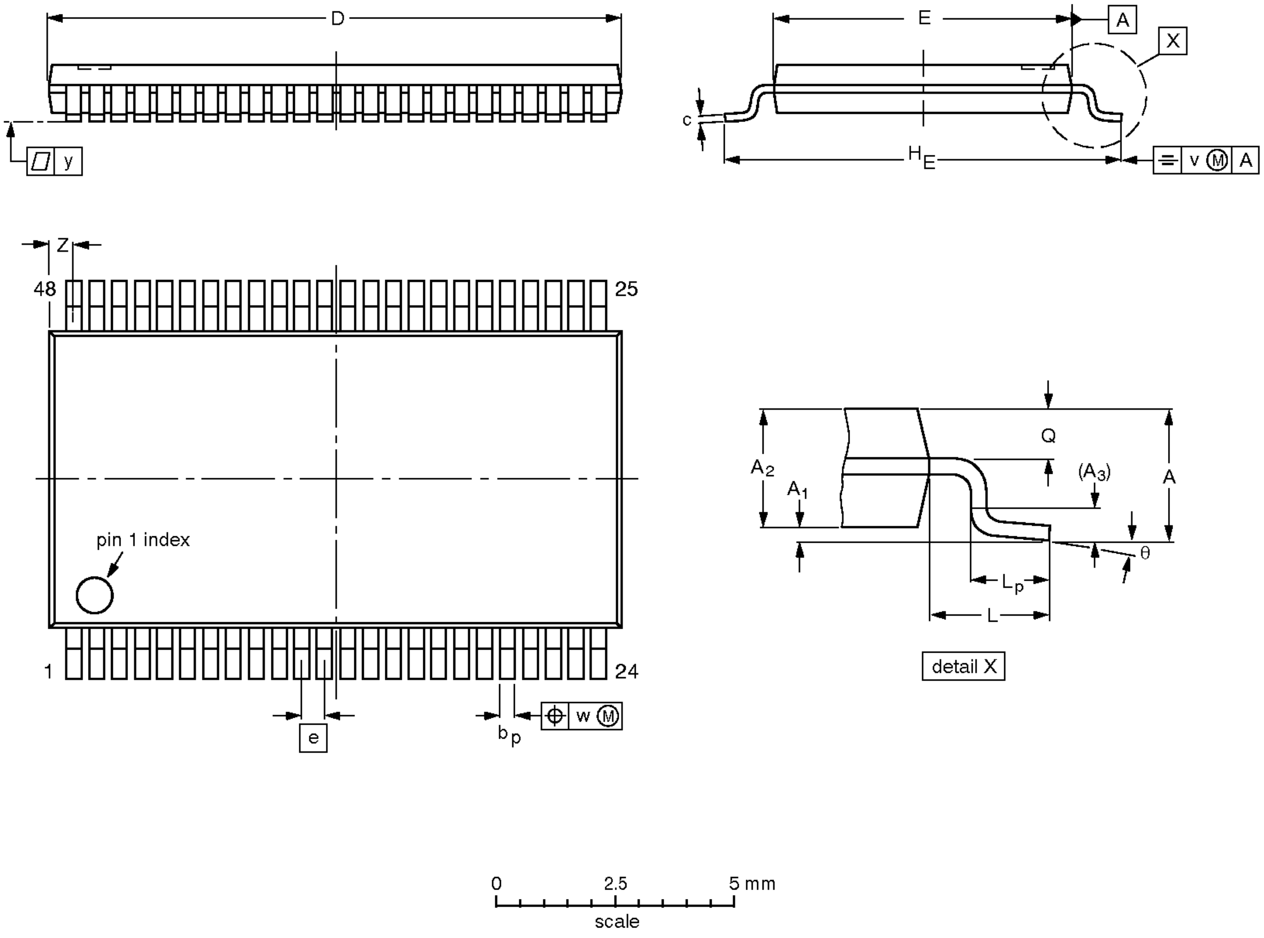
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

GTL2000DGG,118 NXP Semiconductors IC TRANSLATOR BIDIR 48TSSOP

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153					~~95-02-10~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_3	20030401	**Product data (9397 750 11347); ECN 853-2154 29441 Dated 30 January 2003. Supersedes data dated 2000 Jan 25 (9397 750 06818).** Modifications: • New package release (TSSOP). The die was not changed. • Added and modified specifications as data sheet was updated.
_2	20000125	Product data (9397 750 06818); ECN 853-2153 23030 dated 2000 Jan 25.

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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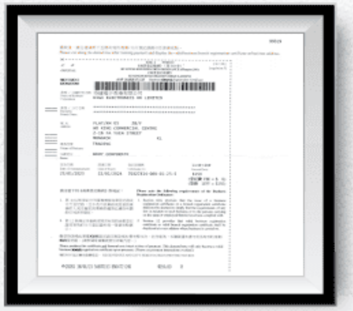

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