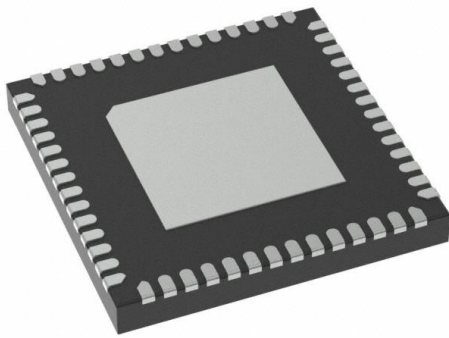


# MC32PF4210A3ESR2 Datasheet

[www.digi-electronics.com](http://www.digi-electronics.com)



<https://www.DiGi-Electronics.com>

|                              |                                   |
|------------------------------|-----------------------------------|
| DiGi Electronics Part Number | MC32PF4210A3ESR2-DG               |
| Manufacturer                 | <a href="#">NXP USA Inc.</a>      |
| Manufacturer Product Number  | MC32PF4210A3ESR2                  |
| Description                  | PF4210                            |
| Detailed Description         | Audio, Video PMIC 56-QFN-EP (8x8) |

This model MC32PF4210A3ESR2 is available at DiGi Electronics.

DiGi Electronics offers a global database of semiconductor and electronic component datasheets.

We welcome your inquiries regarding pricing, lead time, or other product-related questions.

 [Request a Quote](#)

 [Datasheet Search](#)



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.

## Purchase and inquiry

Manufacturer Product Number:

MC32PF4210A3ESR2

Series:

-

Applications:

Audio, Video

Voltage - Supply:

2.8V ~ 4.5V

Mounting Type:

Surface Mount, Wettable Flank

Supplier Device Package:

56-QFN-EP (8x8)

Manufacturer:

NXP USA Inc.

Product Status:

Active

Current - Supply:

-

Operating Temperature:

0°C ~ 85°C (TA)

Package / Case:

56-VFQFN Exposed Pad

Base Product Number:

MC32PF4210

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

EAR99



# PF4210

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Rev. 2.0 — 14 November 2018

Data sheet: technical data

## 1 General description

---

The PF4210 high performance power management integrated circuit (PMIC) provides a highly programmable/configurable architecture with fully integrated power devices and minimal external components. With up to six buck converters, six linear regulators, an RTC supply, and a coin cell charger, the PF4210 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications.

With on-chip one-time programmable (OTP) memory, the PF4210 is available in preprogrammed standard version or nonprogrammed to support custom programming. The PF4210 is defined to power low-cost audio/video applications using the i.MX 8M family of applications processors.

## 2 Features and benefits

---

- Four to six buck converters, depending on configuration
  - Single/dual phase/parallel options
  - DDR termination tracking mode option
- Boost regulator to 5.0 V output
- Six general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (one-time programmable) memory for device configuration
- Coin cell charger and RTC supply
- DDR termination reference voltage
- Power control logic with processor interface and event detection
- I<sup>2</sup>C control
- Individually programmable on, off, and standby modes



### 3 Simplified application diagram

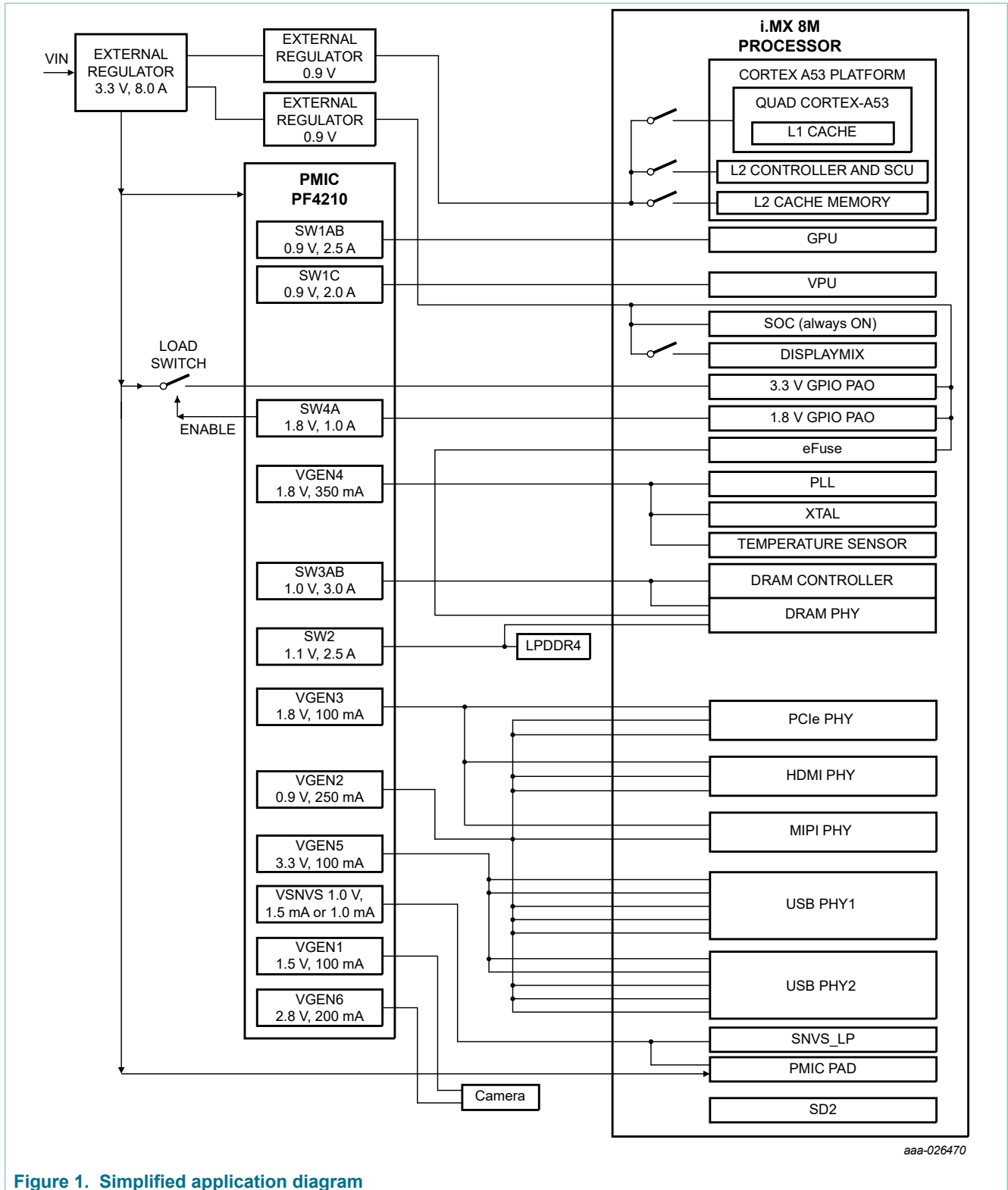


Figure 1. Simplified application diagram

## 4 Applications

- OTT STB
- Wireless audio
- Voice recognition assistant
- A/V receivers
- Sound bars
- General embedded

## 5 Orderable parts

The PF4210 is available with both preprogrammed and nonprogrammed OTP memory configurations. The nonprogrammed device uses A0 as the programming code. The preprogrammed devices are identified using the program codes from [Table 1](#), which also list the associated NXP reference designs where applicable.

Details of the OTP programming for each device can be found in [Table 8](#).

**Table 1. Orderable part variations**

| Part number <sup>[1]</sup> | Temperature (T <sub>A</sub> )                         | Package  | Programming <sup>[2]</sup> | Reference designs |
|----------------------------|---|--|----------------------------|-------------------|
| MC32PF4210A0ES             | 0 °C to 85 °C (for use in consumer applications)      | 56 QFN 8x8 mm - 0.5 mm pitch WF-type QFN (wetable flank) | A0 (Nonprogrammed)         | N/A               |
| MC32PF4210A1ES             |   |  | A1                         | MCIMX8M-EVK       |
| MC32PF4210A2ES             |   |  | A2                         | N/A               |
| MC32PF4210A3ES             |   |  | A3                         | N/A               |
| MC32PF4210A4ES             |   |  | A4                         | N/A               |
| MC34PF4210A0ES             | -40 °C to 105 °C (for use in industrial applications) |  | A0 (Nonprogrammed)         | N/A               |
| MC34PF4210A1ES             |   |  | A1                         | MCIMX8M-EVK       |
| MC34PF4210A2ES             |   |  | A2                         | N/A               |
| MC34PF4210A3ES             |   |  | A3                         | N/A               |
| MC34PF4210A4ES             |   | A4   | N/A                        |                   |

[1] For tape and reel, add an R2 suffix to the part number.

[2] For programming details see [Table 8](#). The available OTP options are not restricted to the listed reference designs. They can be used in any application where the listed voltage and sequence details are acceptable.

## 6 Internal block diagram

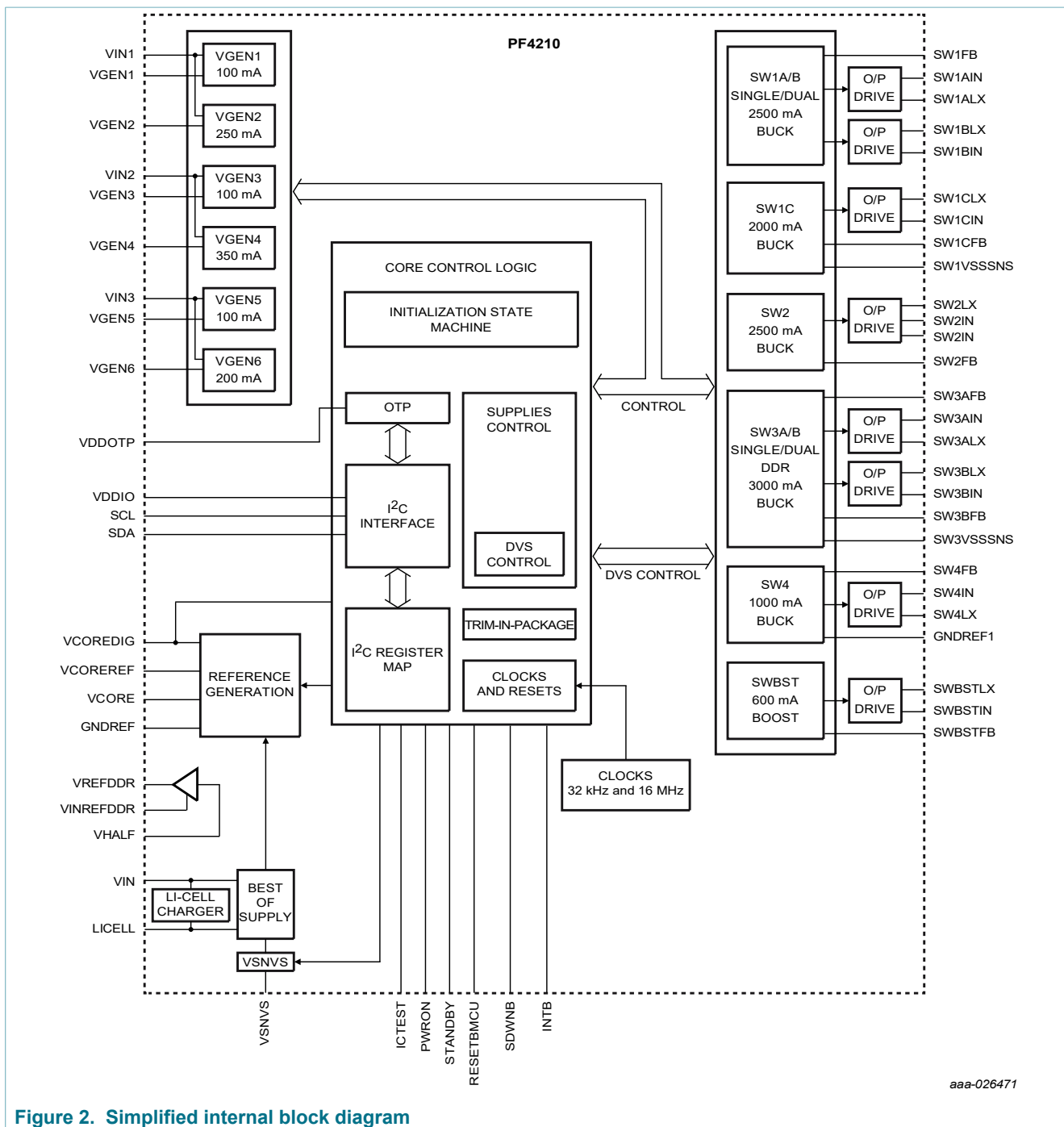


Figure 2. Simplified internal block diagram

## 7 Pinning information

### 7.1 Pinning

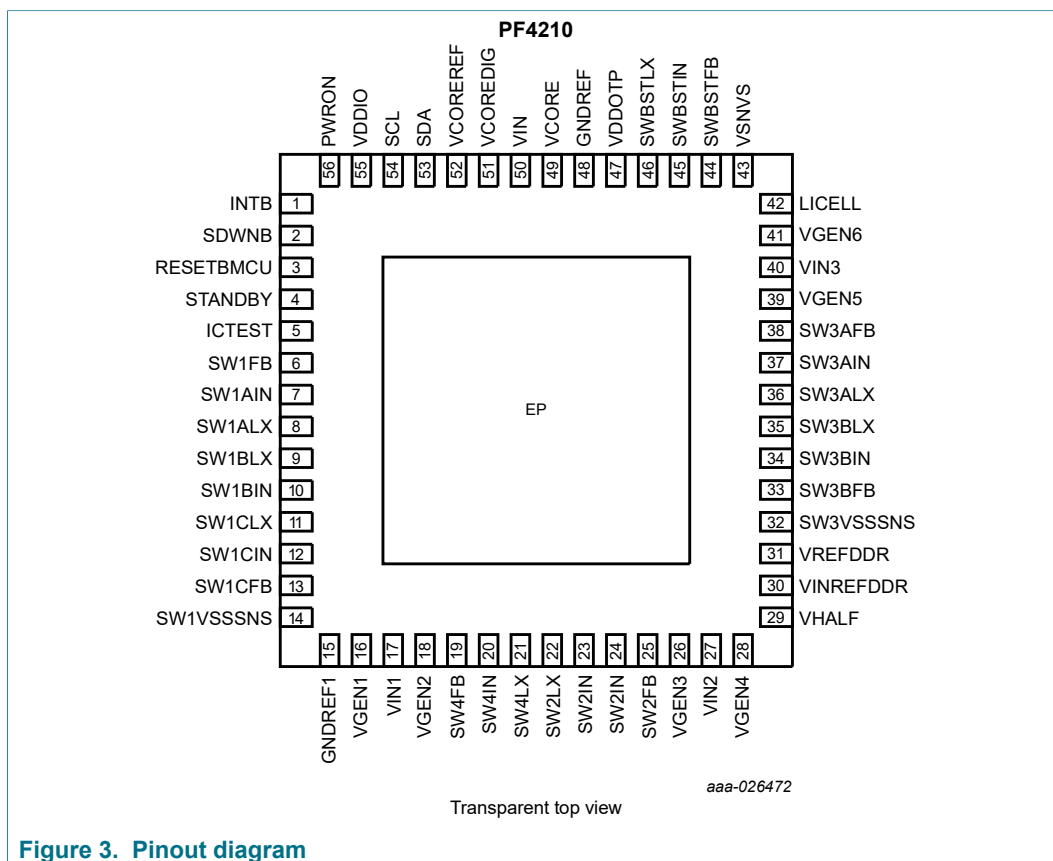


Figure 3. Pinout diagram

### 7.2 Pin definitions

Table 2. Pin definitions

| Number | Name                  | Function | Max rating | Type               | Definition  |
|--------|-----------------------|----------|------------|--------------------|---|
| 1      | INTB                  | Output   | 3.6 V      | Digital            | Open drain interrupt signal to processor  |
| 2      | SDWNB                 | Output   | 3.6 V      | Digital            | Open drain signal to indicate an imminent system shutdown   |
| 3      | RESETBMCU             | Output   | 3.6 V      | Digital            | Open drain reset output to processor. Alternatively can be used as a power output.  |
| 4      | STANDBY               | Input    | 3.6 V      | Digital            | Standby input signal from processor   |
| 5      | ICTEST                | Input    | 7.5 V      | Digital/<br>Analog | Reserved pin. Connect to GND in application.  |
| 6      | SW1FB <sup>[1]</sup>  | Input    | 3.6 V      | Analog             | Output voltage feedback for SW1A/B. Route this trace separately from the high current path and terminate at the output capacitance.                   |
| 7      | SW1AIN <sup>[1]</sup> | Input    | 4.8 V      | Analog             | Input to SW1A regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible. |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Number | Name                  | Function | Max rating | Type   | Definition  |
|--------|-----------------------|----------|------------|--------|---|
| 8      | SW1ALX <sup>[1]</sup> | Output   | 4.8 V      | Analog | Regulator 1A switch node connection   |
| 9      | SW1BLX <sup>[1]</sup> | Output   | 4.8 V      | Analog | Regulator 1B switch node connection   |
| 10     | SW1BIN <sup>[1]</sup> | Input    | 4.8 V      | Analog | Input to SW1B regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.   |
| 11     | SW1CLX <sup>[1]</sup> | Output   | 4.8 V      | Analog | Regulator 1C switch node connection   |
| 12     | SW1CIN <sup>[1]</sup> | Input    | 4.8 V      | Analog | Input to SW1C regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.   |
| 13     | SW1CFB <sup>[1]</sup> | Input    | 3.6 V      | Analog | Output voltage feedback for SW1C. Route this trace separately from the high current path and terminate at the output capacitance.   |
| 14     | SW1VSSNS              | GND      | —          | GND    | Ground reference for regulators SW1ABC. It is connected externally to GNDREF through a board ground plane.  |
| 15     | GNDREF1               | GND      | —          | GND    | Ground reference for regulators SW2 and SW4. It is connected externally to GNDREF, via board ground plane.  |
| 16     | VGEN1                 | Output   | 2.5 V      | Analog | VGEN1 regulator output. Bypass with a 2.2 $\mu$ F ceramic output capacitor.   |
| 17     | VIN1                  | Input    | 3.6 V      | Analog | VGEN1, 2 input supply. Bypass with a 1.0 $\mu$ F decoupling capacitor as close to the pin as possible.  |
| 18     | VGEN2                 | Output   | 2.5 V      | Analog | VGEN2 regulator output. Bypass with a 4.7 $\mu$ F ceramic output capacitor.   |
| 19     | SW4FB <sup>[1]</sup>  | Input    | 3.6 V      | Analog | Output voltage feedback for SW4. Route this trace separately from the high current path and terminate at the output capacitance.  |
| 20     | SW4IN <sup>[1]</sup>  | Input    | 4.8 V      | Analog | Input to SW4 regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.  |
| 21     | SW4LX <sup>[1]</sup>  | Output   | 4.8 V      | Analog | Regulator 4 switch node connection  |
| 22     | SW2LX <sup>[1]</sup>  | Output   | 4.8 V      | Analog | Regulator 2 switch node connection  |
| 23     | SW2IN <sup>[1]</sup>  | Input    | 4.8 V      | Analog | Input to SW2 regulator. Connect pin 23 together with pin 24 and bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to these pins as possible. |
| 24     | SW2IN <sup>[1]</sup>  | Input    | 4.8 V      | Analog |   |
| 25     | SW2FB <sup>[1]</sup>  | Input    | 3.6 V      | Analog | Output voltage feedback for SW2. Route this trace separately from the high current path and terminate at the output capacitance.  |
| 26     | VGEN3                 | Output   | 3.6 V      | Analog | VGEN3 regulator output. Bypass with a 2.2 $\mu$ F ceramic output capacitor.   |
| 27     | VIN2                  | Input    | 3.6 V      | Analog | VGEN3, 4 input. Bypass with a 1.0 $\mu$ F decoupling capacitor as close to the pin as possible.   |
| 28     | VGEN4                 | Output   | 3.6 V      | Analog | VGEN4 regulator output. Bypass with a 4.7 $\mu$ F ceramic output capacitor.   |
| 29     | VHALF                 | Input    | 3.6 V      | Analog | Half supply reference for VREFDDR   |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Number | Name                   | Function     | Max rating          | Type               | Definition   |
|--------|------------------------|--------------|---------------------|--------------------|--|
| 30     | VINREFDDR              | Input        | 3.6 V               | Analog             | VREFDDR regulator input. Bypass with at least 1.0 $\mu$ F decoupling capacitor as close to the pin as possible.  |
| 31     | VREFDDR                | Output       | 3.6 V               | Analog             | VREFDDR regulator output   |
| 32     | SW3VSSNS               | GND          | —                   | GND                | Ground reference for the SW3 regulator. Connect to GNDREF externally via the board ground plane.   |
| 33     | SW3BFB <sup>[1]</sup>  | Input        | 3.6 V               | Analog             | Output voltage feedback for SW3B. Route this trace separately from the high current path and terminate at the output capacitance.                      |
| 34     | SW3BIN <sup>[1]</sup>  | Input        | 4.8 V               | Analog             | Input to SW3B regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.  |
| 35     | SW3BLX <sup>[1]</sup>  | Output       | 4.8 V               | Analog             | Regulator 3B switch node connection  |
| 36     | SW3ALX <sup>[1]</sup>  | Output       | 4.8 V               | Analog             | Regulator 3A switch node connection  |
| 37     | SW3AIN <sup>[1]</sup>  | Input        | 4.8 V               | Analog             | Input to SW3A regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.  |
| 38     | SW3AFB <sup>[1]</sup>  | Input        | 3.6 V               | Analog             | Output voltage feedback for SW3A. Route this trace separately from the high current path and terminate at the output capacitance.                      |
| 39     | VGEN5                  | Output       | 3.6 V               | Analog             | VGEN5 regulator output. Bypass with a 2.2 $\mu$ F ceramic output capacitor.  |
| 40     | VIN3                   | Input        | 4.8 V               | Analog             | VGEN5, 6 input. Bypass with a 1.0 $\mu$ F decoupling capacitor as close to the pin as possible.  |
| 41     | VGEN6                  | Output       | 3.6 V               | Analog             | VGEN6 regulator output. Bypass with a 2.2 $\mu$ F ceramic output capacitor.  |
| 42     | LICELL                 | Input/Output | 3.6 V               | Analog             | Coin cell supply input/output  |
| 43     | VSNVS                  | Output       | 3.6 V               | Analog             | LDO or coin cell output to processor   |
| 44     | SWBSTFB <sup>[1]</sup> | Input        | 5.5 V               | Analog             | Boost regulator feedback. Connect this pin to the output rail close to the load. Keep this trace away from other noisy traces and planes.              |
| 45     | SWBSTIN <sup>[1]</sup> | Input        | 4.8 V               | Analog             | Input to SWBST regulator. Bypass with at least a 2.2 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible. |
| 46     | SWBSTLX <sup>[1]</sup> | Output       | 7.5 V               | Analog             | SWBST switch node connection   |
| 47     | VDDOTP                 | Input        | 10 V <sup>[2]</sup> | Digital/<br>Analog | Supply to program OTP fuses  |
| 48     | GNDREF                 | GND          | —                   | GND                | Ground reference for the main band gap regulator   |
| 49     | VCORE                  | Output       | 3.6 V               | Analog             | Analog core supply   |
| 50     | VIN                    | Input        | 4.8 V               | Analog             | Main chip supply   |
| 51     | VCOREDIG               | Output       | 1.5 V               | Analog             | Digital core supply  |
| 52     | VCOREREF               | Output       | 1.5 V               | Analog             | Main band gap reference  |
| 53     | SDA                    | Input/Output | 3.6 V               | Digital            | I <sup>2</sup> C data line (open drain)  |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Number | Name  | Function | Max rating | Type    | Definition  |
|--------|-------|----------|------------|---------|---|
| 54     | SCL   | Input    | 3.6 V      | Digital | I <sup>2</sup> C clock  |
| 55     | VDDIO | Input    | 3.6 V      | Analog  | Supply for I <sup>2</sup> C bus. Bypass with 0.1 $\mu$ F ceramic capacitor  |
| 56     | PWRON | Input    | 3.6 V      | Digital | Power on/off from processor   |
| —      | EP    | GND      | —          | GND     | Expose pad. Functions as ground return for buck regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation. |

- [1] Unused switching regulators should be connected as follow: Pins SWxLX and SWxFB should be unconnected and pin SWxIN should be connected to VIN with a 0.1  $\mu$ F bypass capacitor.
- [2] 10 V maximum voltage rating during OTP fuse programming. 7.5 V maximum DC voltage rated otherwise.

## 8 General product characteristics

### 8.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. For maximum voltage rating for each pin see [Section 7.2 "Pin definitions"](#).

| Symbol                    | Description                          | Value       | Unit |
|---------------------------|--------------------------------------|-------------|------|
| <b>Electrical ratings</b> |                                      |             |      |
| V <sub>IN</sub>           | Main input supply voltage            | -0.3 to 4.8 | V    |
| V <sub>DDOTP</sub>        | OTP programming input supply voltage | -0.3 to 10  | V    |
| V <sub>LICELL</sub>       | Coin cell voltage                    | -0.3 to 3.6 | V    |
| V <sub>ESD</sub>          | ESD ratings <sup>[1]</sup>           |             |      |
|                           | Human body model                     | $\pm$ 2000  | V    |
|                           | Charge device model                  | $\pm$ 500   |      |

- [1] ESD testing is performed in accordance with the human body model (HBM) (C<sub>ZAP</sub> = 100 pF, R<sub>ZAP</sub> = 1500  $\Omega$ ), and the charge device model (CDM), robotic (C<sub>ZAP</sub> = 4.0 pF).

### 8.2 Thermal characteristics

**Table 4. Thermal ratings**

| Symbol  | Description (rating)  | Min      | Max            | Unit         |
|---|---|----------|----------------|--------------|
| <b>Thermal ratings</b>  |   |          |                |              |
| T <sub>A</sub>  | Ambient operating temperature range<br>MC32PF4210<br>MC34PF4210 | 0<br>-40 | 85<br>105      | $^{\circ}$ C |
| T <sub>J</sub>  | Operating junction temperature range <sup>[1]</sup>             | -40      | 125            | $^{\circ}$ C |
| T <sub>ST</sub>   | Storage temperature range                                       | -65      | 150            | $^{\circ}$ C |
| T <sub>PPRT</sub>   | Peak package reflow temperature <sup>[2]</sup>                  | —        | <sup>[3]</sup> | $^{\circ}$ C |
| <b>QFN56 thermal resistance and package dissipation ratings</b> |   |          |                |              |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                 | Description (rating)                                | Min | Max | Unit |
|------------------------|---|-----|-----|------|
| R <sub>ΘJA</sub>       | Junction to ambient [4] [5] [6]                     |     |     | °C/W |
|                        | Natural convection                                  | —   | 28  |      |
|                        | Four layer board (2s2p)<br>Eight layer board (2s6p) | —   | 15  |      |
| R <sub>ΘJMA</sub>      | Junction to ambient (@200 ft/min) [4] [6]           |     |     | °C/W |
|                        | Four layer board (2s2p)                             | —   | 22  |      |
| R <sub>ΘJB</sub>       | Junction to board [7]                               | —   | 10  | °C/W |
| R <sub>ΘJCBOTTOM</sub> | Junction to case bottom [8]                         | —   | 1.2 | °C/W |
| Ψ <sub>JT</sub>        | Junction to package top [9]                         |     |     | °C/W |
|                        | Natural convection                                  | —   | 2.0 |      |

- [1] Do not operate beyond 125 °C for extended period of time. Operation above 150 °C may cause permanent damage to the IC. See [Table 5](#) for thermal protection features.
- [2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
- [3] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to [www.nxp.com](http://www.nxp.com), search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts (MC33xxx enter 33xxx), and review parametrics.
- [4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- [5] The board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
- [6] Per JEDEC JESD51-6 with the board horizontal
- [7] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- [8] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- [9] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letter (Ψ) is not available, the thermal characterization parameter is written as Psi-JT.

### 8.3 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in [Table 4](#). To optimize the thermal management and to avoid overheating, the PF4210 provides thermal protection.

An internal comparator monitors the die temperature. Interrupts THERM110I, THERM120I, THERM125I, and THERM130I are generated when the respective thresholds specified in [Table 5](#) are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry shuts down the PF4210. This thermal protection acts above the thermal protection threshold listed in [Table 5](#). To avoid any unwanted power-down resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured so protection is not tripped under normal conditions.

**Table 5. Thermal protection thresholds**

| Parameter                           | Min | Typ | Max | Units |
|-------------------------------------|-----|-----|-----|-------|
| Thermal 110 °C threshold (THERM110) | 100 | 110 | 120 | °C    |
| Thermal 120 °C threshold (THERM120) | 110 | 120 | 130 | °C    |
| Thermal 125 °C threshold (THERM125) | 115 | 125 | 135 | °C    |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Parameter                           | Min | Typ | Max | Units |
|-------------------------------------|-----|-----|-----|-------|
| Thermal 130 °C threshold (THERM130) | 120 | 130 | 140 | °C    |
| Thermal warning hysteresis          | 2.0 | —   | 4.0 | °C    |
| Thermal protection threshold        | 130 | 140 | 150 | °C    |

## 8.4 Electrical characteristics

### 8.4.1 General specifications

**Table 6. General PMIC static characteristics**

$T_{MIN}$  to  $T_{MAX}$  (see [Table 4](#)),  $V_{IN} = 2.8$  to  $4.5$  V,  $V_{DDIO} = 1.7$  to  $3.6$  V, typical external component values and full load current range, unless otherwise noted.

| Pin name  | Parameter | Load condition | Min              | Max              | Unit |
|-----------|-----------|----------------|------------------|------------------|------|
| PWRON     | $V_{IL}$  | —              | 0                | $0.2 * V_{SNVS}$ | V    |
|           | $V_{IH}$  | —              | $0.8 * V_{SNVS}$ | 3.6              | V    |
| RESETBMCU | $V_{OL}$  | -2.0 mA        | 0.0              | 0.4              | V    |
|           | $V_{OH}$  | Open drain     | $0.7 * V_{IN}$   | $V_{IN}$         | V    |
| SCL       | $V_{IL}$  | —              | 0.0              | $0.2 * V_{DDIO}$ | V    |
|           | $V_{IH}$  | —              | $0.8 * V_{DDIO}$ | 3.6              | V    |
| SDA       | $V_{IL}$  | —              | 0                | $0.2 * V_{DDIO}$ | V    |
|           | $V_{IH}$  | —              | $0.8 * V_{DDIO}$ | 3.6              | V    |
|           | $V_{OL}$  | -2.0 mA        | 0.0              | 0.4              | V    |
|           | $V_{OH}$  | Open drain     | $0.7 * V_{DDIO}$ | $V_{DDIO}$       | V    |
| INTB      | $V_{OL}$  | -2.0 mA        | 0.0              | 0.4              | V    |
|           | $V_{OH}$  | Open drain     | $0.7 * V_{IN}$   | $V_{IN}$         | V    |
| SDWNB     | $V_{OL}$  | -2.0 mA        | 0.0              | 0.4              | V    |
|           | $V_{OH}$  | Open drain     | $0.7 * V_{IN}$   | $V_{IN}$         | V    |
| STANDBY   | $V_{IL}$  | —              | 0                | $0.2 * V_{SNVS}$ | V    |
|           | $V_{IH}$  | —              | $0.8 * V_{SNVS}$ | 3.6              | V    |
| VDDOTP    | $V_{IL}$  | —              | 0                | 0.3              | V    |
|           | $V_{IH}$  | —              | 1.1              | 1.7              | V    |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

## 8.4.2 Current consumption

Table 7. Current consumption summary

$T_{MIN}$  to  $T_{MAX}$  (see Table 4),  $V_{IN} = 3.6$  V,  $V_{DDIO} = 1.7$  V to 3.6 V,  $LICELL = 1.8$  V to 3.3 V,  $V_{SNVS} = 3.0$  V, typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6$  V,  $V_{DDIO} = 3.3$  V,  $LICELL = 3.0$  V,  $V_{SNVS} = 3.0$  V and 25 °C, unless otherwise noted.

| Mode      | PF4210 conditions   | System conditions  | Typ        | Max                                      | Unit |
|-----------|---|--|------------|--|------|
| Coin cell | VSNVS from LICELL<br>All other blocks off<br>$V_{IN} = 0.0$ V<br>$V_{SNVSVOLT}[2:0] = 110$  | No load on VSNVS <sup>[1] [2]</sup>  | 4.0        | 7.0                                      | μA   |
| Off       | VSNVS from VIN or LICELL<br>Wake-up from PWRON active<br>32 kHz RC on<br>All other blocks off<br>$V_{IN} \geq UVDET$  | No load on VSNVS, PMIC able to wake-up <sup>[1] [3]</sup>  | 17         | 25                                       | μA   |
| Sleep     | VSNVS from VIN<br>Wake-up from PWRON active<br>Trimmed reference active<br>SW3A/B PFM<br>Trimmed 16 MHz RC off<br>32 kHz RC on<br>VREFDDR disabled  | No load on VSNVS. DDR memories in self refresh <sup>[1]</sup>  | 122<br>122 | 220 <sup>[4]</sup><br>250 <sup>[5]</sup> | μA   |
| Standby   | VSNVS from either VIN or LICELL<br>SW1A/B combined in PFM<br>SW1C in PFM<br>SW2 in PFM<br>SW3A/B combined in PFM<br>SW4 in PFM<br>SWBST off<br>Trimmed 16 MHz RC enabled<br>Trimmed reference active<br>VGEN1 to 6 enabled<br>VREFDDR enabled | No load on VSNVS. Processor enabled in lowpower mode. All rails powered on except boost (load = 0 mA) <sup>[1]</sup> | 297<br>297 | 450 <sup>[4]</sup><br>550 <sup>[5]</sup> | μA   |

[1] For PFM operation, headroom should be 300 mV or greater.

[2] Additional current may be drawn in the coin cell mode when RESETBMCU is pulled up to VSNVS due to an internal path from RESETBMCU to  $V_{IN}$ . The additional current is < 30 μA with a pullup resistor of 100 kΩ.

[3] When  $V_{IN}$  is below the UVDET threshold, in the range of 1.8 V  $\leq V_{IN}$  < 2.65 V, the quiescent current increases by 50 μA, typically.

[4] From -40 °C to 85 °C

[5] From -40 °C to 105 °C

## 9 Detailed description

The PF4210 is the power management integrated circuit (PMIC) designed primarily for use with NXP's i.MX 8M family of applications processors.

### 9.1 Features

This section summarizes the PF4210 features.

- Input voltage range to PMIC: 2.8 V to 4.5 V

## 14-channel power management integrated circuit (PMIC) for audio/video applications

- Buck regulators
  - Four to six channel configurable
    - SW1A/B/C, 4.5 A (single); 0.3 V to 1.875 V
    - SW1A/B, 2.5 A (single/dual); SW1C 2.0 A (independent); 0.3 V to 1.875 V
    - SW2, 2.5 A; 0.4 V to 3.3 V
    - SW3A/B, 3.0 A (single/dual); 0.4 V to 3.3 V
    - SW3A, 1.5 A (independent); SW3B, 1.5 A (independent); 0.4 V to 3.3 V
    - SW4, 1.0 A; 0.4 V to 3.3 V
    - SW4, VTT mode provide DDR termination at 50 % of SW3A
  - Dynamic voltage scaling
  - Modes: PWM, PFM, APS
  - Programmable output voltage
  - Programmable current limit
  - Programmable soft start
  - Programmable PWM switching frequency
  - Programmable OCP with fault interrupt
- Boost regulator
  - SWBST, 5.0 V to 5.15 V, 0.6 A, OTG support
  - Modes: PFM and auto
  - OCP fault interrupt
- LDOs
  - Six user-programmable LDOs
    - VGEN1, 0.80 V to 1.55 V, 100 mA
    - VGEN2, 0.80 V to 1.55 V, 250 mA
    - VGEN3, 1.8 V to 3.3 V, 100 mA
    - VGEN4, 1.8 V to 3.3 V, 350 mA
    - VGEN5, 1.8 V to 3.3 V, 100 mA
    - VGEN6, 1.8 V to 3.3 V, 200 mA
- Soft start
- LDO/switch supply
  - VSNVS (1.0/1.1/1.2/1.3/1.5/1.8/3.0 V), 1.5 mA (consumer version), 1.0 mA (industrial version)
- DDR memory reference voltage
  - VREFDDR, 0.6 V to 0.9 V, 10 mA
- 16 MHz internal master clock
- OTP (one time programmable) memory for device configuration
  - User programmable start-up sequence and timing
- Battery backed memory including coin cell charger
- I<sup>2</sup>C interface
- User programmable standby, sleep, and off modes

## 9.2 Functional block diagram

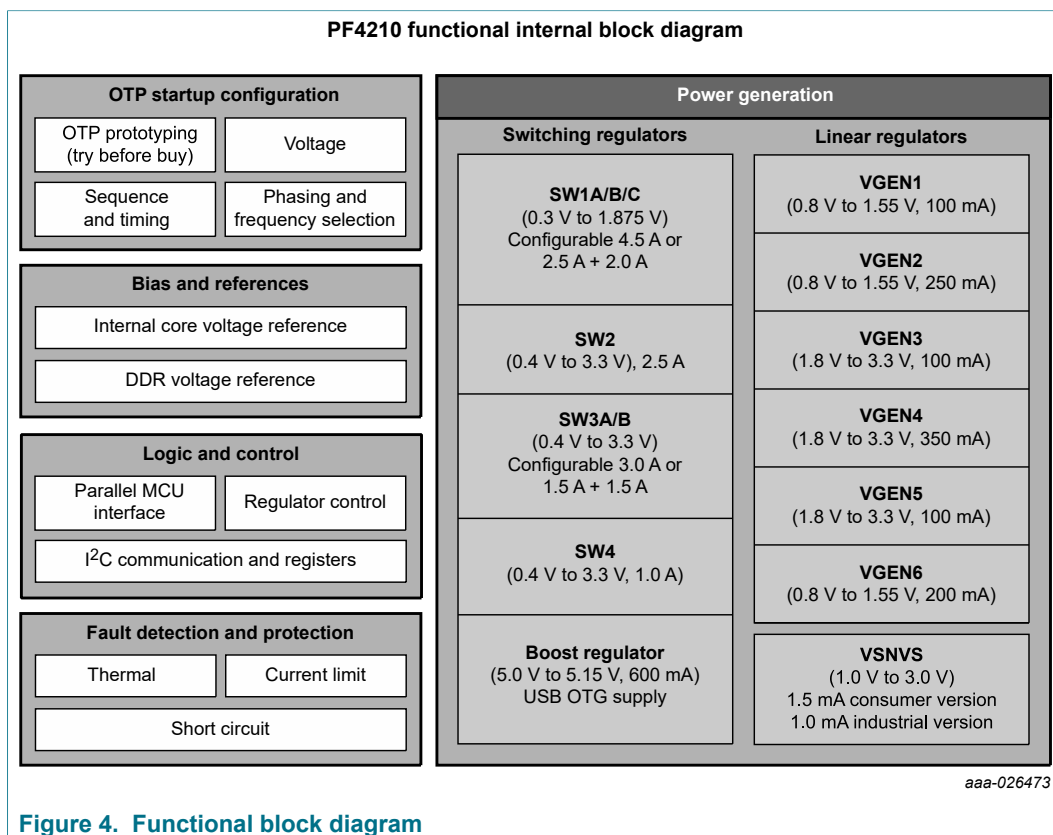


Figure 4. Functional block diagram

## 9.3 Functional description

### 9.3.1 Power generation

The PF4210 PMIC features four buck regulators (up to six independent outputs), one boost regulator, six general purpose LDOs, one switch/LDO combination and a DDR voltage reference to supply voltage for the application processor and peripheral devices.

The number of independent buck regulator outputs can be configured from four to six, thereby providing flexibility to operate with higher current capability, or to operate as independent outputs for applications requiring more voltage rails with lower current demands. SW1 and SW3 regulators can be configured as single/dual phase and/or independent converters. One of the buck regulators, SW4, can also operate as a tracking regulator when used for memory termination.

The buck regulators provide supply to processor cores and to other low voltage circuits such as IO and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and/or other circuitry.

Depending on the system power path configuration, the six general purpose LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, bluetooth, and wireless LAN. A specific VREFDDR voltage reference is included to provide an accurate reference voltage for DDR memories operating with or without VTT termination. The VSNVS block

## 14-channel power management integrated circuit (PMIC) for audio/video applications

behaves as an LDO, or as a bypass switch to supply the SNVS/SRTC circuitry in the i.MX processors; VSNVS may be powered from VIN, or from a coin cell.

### 9.3.2 Control logic

The PF4210 PMIC is fully programmable via the I<sup>2</sup>C interface. Additional communication is provided by direct logic interfacing including interrupt and reset. Startup sequence of the device is selected based on the initial OTP configuration explained in the [Section 10.1 "Startup"](#), or by configuring the Try Before Buy feature to test different power up sequences before choosing the final OTP configuration.

The PF4210 PMIC has interfaces for the power buttons and a dedicated signaling interface with the processor. It also ensures supply of critical internal logic and other circuits from the coin cell, in case of brief interruptions from the main battery. A charger for the coin cell is included as well.

#### 9.3.2.1 Interface signals

##### 9.3.2.1.1 PWRON

PWRON is an input signal to the IC generating a turn on event. It can be configured to detect a level, or an edge using the PWRON\_CFG bit. See [Section 10.4.2.1 "Turn on events"](#) for more details.

##### 9.3.2.1.2 STANDBY

STANDBY is an input signal to the IC. When it is asserted, the part enters standby mode and when deasserted, the part exits standby mode. STANDBY can be configured as active high or active low using the STANDBYINV bit. See [Section 10.4.1.3 "Standby mode"](#) for more details.

**Note:** When operating the PMIC at  $V_{IN} \leq 2.85\text{ V}$  and VSNVS is programmed for a 3.0 V output, a coin cell must be present to provide VSNVS, or the PMIC does not reliably enter and exit the standby mode.

##### 9.3.2.1.3 RESETBMCU

RESETBMCU is an open drain, active low output configurable for two modes of operation. In default mode, it is deasserted 2.0 ms to 4.0 ms after the last regulator if the startup sequence is enabled (see [Figure 5](#)). In this mode, the signal can be used to bring the processor out of reset, or as an indicator that all supplies have been enabled; it is only asserted for a turn off event.

When configured for fault mode, RESETBMCU is deasserted after the startup sequence is completed only if no faults occurred during startup. At anytime, if a fault occurs and persists for 1.8 ms typically, RESETBMCU is asserted, LOW. The PF4210 is turned off if the fault persists for more than 100 ms typically.

The PWRON signal restarts the part, though if the fault persists, the sequence described above is repeated. To enter the fault mode, set bit OTP\_PG\_EN of register OTP PWRGD EN to 1. This register, 0xE8, is located in [Table 135](#) of the register map. To test the fault mode, the bit may be set during TBB prototyping, or the mode may be permanently chosen by programming OTP fuses.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

## 9.3.2.1.4 SDWNB

SDWNB is an open drain, active low output notifying the processor of an imminent PMIC shut down. It is asserted low for one 32 kHz clock cycle before powering down and is then deasserted in the OFF state.

## 9.3.2.1.5 INTB

INTB is an open drain, active low output. It is asserted when any fault occurs, provided the fault interrupt is unmasked. INTB is deasserted after the fault interrupt is cleared by software, which requires writing a 1 to the fault interrupt bit.

## 10 Functional block requirements and behaviors

### 10.1 Startup

The PF4210 can be configured to start up from either the internal OTP configuration, or with a hard coded configuration built into the device. The internal hard coded configuration is enabled by connecting the VDDOTP pin to VCOREDIG through a 100 k $\Omega$  resistor. The OTP configuration is enabled by connecting VDDOTP to GND.

For NP (nonprogrammed) devices, selecting the OTP configuration causes the PF4210 to not start up. However, the PF4210 can be controlled through the I<sup>2</sup>C port for prototyping and programming. Once programmed, the NP device starts up with the customer programmed configuration.

#### 10.1.1 Device startup configuration

[Table 8](#) shows the default configuration for all devices and the preprogrammed OTP configurations.

**Table 8. Startup configuration**

| Registers        | Default configuration | Preprogrammed OTP configuration |       |        |       |
|------------------|-----------------------|---------------------------------|-------|--------|-------|
|                  | A0                    | A1                              | A2    | A3     | A4    |
| Default I2C addr | 0x08                  |                                 |       |        |       |
| VSNVS_VOLT       | 3.0 V                 | 1.0 V                           | 1.0 V | 1.0 V  | 1.0 V |
| SW1AB_VOLT       | 1.375 V               | 0.9 V                           | 0.9 V | 0.9 V  | 0.9 V |
| SW1AB_SEQ        | 1                     | 4                               | 4     | 4      | 3     |
| SW1C_VOLT        | 1.375 V               | 0.9 V                           | 0.9 V | 0.9 V  | 0.9 V |
| SW1C_SEQ         | 1                     | 4                               | 4     | 4      | 4     |
| SW2_VOLT         | 3.0 V                 | 1.1 V                           | 1.2 V | 1.35 V | 1.2 V |
| SW2_SEQ          | 2                     | 6                               | 6     | 6      | 6     |
| SW3A_VOLT        | 1.5 V                 | 1.0 V                           | 1.0 V | 1.0 V  | 0.9 V |
| SW3A_SEQ         | 3                     | 4                               | 4     | 4      | 4     |
| SW3B_VOLT        | 1.5 V                 | 1.0 V                           | 1.0 V | 1.0 V  | 0.9 V |
| SW3B_SEQ         | 3                     | 4                               | 4     | 4      | 4     |
| SW4_VOLT         | 1.8 V                 | 1.8 V                           | 1.8 V | 1.8 V  | 1.8 V |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Registers                | Default configuration                              | Preprogrammed OTP configuration |              |              |              |
|--------------------------|--|---------------------------------|--------------|--------------|--------------|
|                          | A0   | A1                              | A2           | A3           | A4           |
| SW4_SEQ                  | 3  | 6                               | 6            | 6            | 6            |
| SWBST_VOLT               | —  | —                               | —            | —            | —            |
| SWBST_SEQ                | —  | —                               | —            | —            | —            |
| VREFDDR_SEQ              | 3  | 6                               | 6            | 6            | 6            |
| VGEN1_VOLT               | —  | 1.5 V                           | 1.5 V        | 1.5 V        | —            |
| VGEN1_SEQ                | —  | 31                              | 31           | 31           | —            |
| VGEN2_VOLT               | 1.5 V  | 0.9 V                           | 0.9 V        | 0.9 V        | 0.9 V        |
| VGEN2_SEQ                | 2  | 7                               | 7            | 7            | 8            |
| VGEN3_VOLT               | —  | 1.8 V                           | 1.8 V        | 1.8 V        | —            |
| VGEN3_SEQ                | —  | 7                               | 7            | 7            | —            |
| VGEN4_VOLT               | 1.8 V  | 1.8 V                           | 1.8 V        | 1.8 V        | 1.8 V        |
| VGEN4_SEQ                | 3  | 5                               | 5            | 5            | 5            |
| VGEN5_VOLT               | 2.5 V  | 3.3 V                           | 3.3 V        | 3.3 V        | —            |
| VGEN5_SEQ                | 3  | 7                               | 7            | 7            | —            |
| VGEN6_VOLT               | 2.8 V  | 2.8 V                           | 2.8 V        | 2.8 V        | —            |
| VGEN6_SEQ                | 3  | 31                              | 31           | 31           | —            |
| PU CONFIG, SEQ_CLK_SPEED | 1.0 ms   | 2.0 ms                          | 2.0 ms       | 2.0 ms       | 2.0 ms       |
| PU CONFIG, SWDVS_CLK     | 6.25 mV/μs   | 1.5625 mV/μs                    | 1.5625 mV/μs | 1.5625 mV/μs | 1.5625 mV/μs |
| PU CONFIG, PWRON         | Level sensitive                                    |                                 |              |              |              |
| SW1AB CONFIG             | SW1AB single phase, SW1C independent mode, 2.0 MHz |                                 |              |              |              |
| SW1C CONFIG              | 2.0 MHz  |                                 |              |              |              |
| SW2 CONFIG               | 2.0 MHz  |                                 |              |              |              |
| SW3A CONFIG              | SW3AB single phase mode, 2.0 MHz                   |                                 |              |              |              |
| SW3B CONFIG              | 2.0 MHz  |                                 |              |              |              |
| SW4 CONFIG               | No VTT, 2.0 MHz                                    |                                 |              |              |              |
| PG EN                    | RESETBMCU in default mode                          |                                 |              |              |              |

**Notes:**

- Keep bit SW2ILIM = 0 for A1, A2, A3 and A4 for max. rated output load current.
- Keep bit SW3xILIM = 0 for A1, A2, A3 and A4 for max. rated output load current.

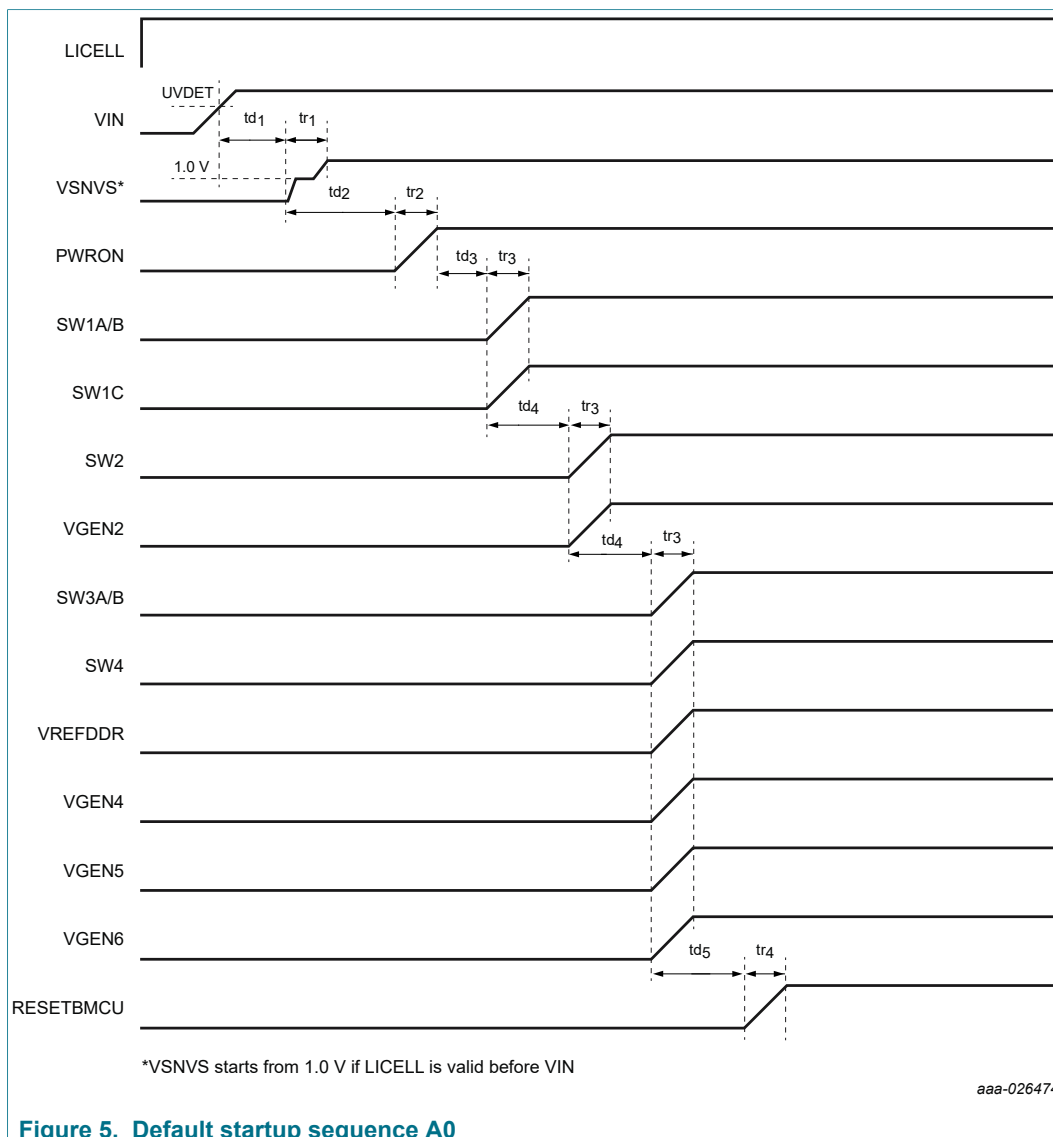


Figure 5. Default startup sequence A0

Table 9. Default startup sequence timing

| Parameter | Description   | Min | Typ                      | Max | Unit |
|-----------|---|-----|--------------------------|-----|------|
| $t_{D1}$  | Turn-on delay of VSNVS <sup>[1]</sup>   | —   | 5.0                      | —   | ms   |
| $t_{R1}$  | Rise time of VSNVS  | —   | 3.0                      | —   | ms   |
| $t_{D2}$  | User determined delay   | —   | 1.0                      | —   | ms   |
| $t_{R2}$  | Rise time of PWRON  | —   | <sup>[2]</sup>           | —   | ms   |
| $t_{D3}$  | Turn-on delay of first regulator<br>SEQ_CLK_SPEED[1:0] = 00<br>SEQ_CLK_SPEED[1:0] = 01 <sup>[3]</sup><br>SEQ_CLK_SPEED[1:0] = 10<br>SEQ_CLK_SPEED[1:0] = 11 | —   | 2.0<br>2.5<br>4.0<br>7.0 | —   | ms   |
| $t_{R3}$  | Rise time of regulators <sup>[4]</sup>  | —   | 0.2                      | —   | ms   |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Parameter       | Description  | Min | Typ                      | Max | Unit |
|-----------------|--|-----|--------------------------|-----|------|
| t <sub>D4</sub> | Delay between regulators<br>SEQ_CLK_SPEED[1:0] = 00<br>SEQ_CLK_SPEED[1:0] = 01<br>SEQ_CLK_SPEED[1:0] = 10<br>SEQ_CLK_SPEED[1:0] = 11 | —   | 0.5<br>1.0<br>2.0<br>4.0 | —   | ms   |
| t <sub>R4</sub> | Rise time of RESETBMCU   | —   | 0.2                      | —   | ms   |
| t <sub>D5</sub> | Turn-on delay of RESETBMCU   | —   | 2.0                      | —   | ms   |

- [1] Assume LICELL voltage is valid before VIN is applied. If LICELL is not valid before VIN is applied, then VSNVS turn on delay may extend to a maximum of 24 ms.
- [2] Depends on the external signal driving PWRON.
- [3] Default configuration
- [4] Rise time is a function of slew rate of regulators and nominal voltage selected.

### 10.1.2 One time programmability (OTP)

OTP allows the programming of startup configurations for a variety of applications. Before permanently programming the IC by programming fuses, a configuration may be prototyped by using the Try Before Buy (TBB) feature. An error correction code (ECC) algorithm is available to correct a single bit error and to detect multiple bit errors when fuses are programmed.

The parameters which can be configured by OTP are listed below.

- General: I<sup>2</sup>C slave address, PWRON pin configuration, startup sequence and timing
- Output voltage, dual/single phase or independent mode configuration, switching frequency, and soft start ramp rate
- Boost regulator and LDOs: output voltage

**Note:** When prototyping or programming fuses, ensure register settings are consistent with the hardware configuration. This is important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single/ dual phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it is gated by the buck regulator in the startup sequence.

#### 10.1.2.1 Startup sequence and timing

Each regulator has 5-bit allocated to program its startup time slot from a turn on event; therefore, each can be placed from position one to thirty-one in the startup sequence.

The all zeros code indicates a regulator is not part of the startup sequence and remains off (see [Table 10](#)). The delay between each position is equal; however, four delay options are available (see [Table 11](#)). The startup sequence terminates at the last programmed regulator.

**Table 10. Startup sequence**

| SWxx_SEQ[4:0]/ VGENx_SEQ[4:0]/ VREFDDR_SEQ[4:0] | Sequence               |
|---|------------------------|
| 00000   | Off                    |
| 00001   | SEQ_CLK_SPEED[1:0] * 1 |
| 00010   | SEQ_CLK_SPEED[1:0] * 2 |
| *   | *                      |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| SW <sub>xx</sub> _SEQ[4:0]/ VGEN <sub>x</sub> _SEQ[4:0]/ VREFDDR_SEQ[4:0] | Sequence                |
|---|-------------------------|
| *   | *                       |
| *   | *                       |
| *   | *                       |
| 11111   | SEQ_CLK_SPEED[1:0] * 31 |

Table 11. Startup sequence clock speed

| SEQ_CLK_SPEED[1:0] | Time (μs) |
|--------------------|-----------|
| 00                 | 500       |
| 01                 | 1000      |
| 10                 | 2000      |
| 11                 | 4000      |

## 10.1.2.2 PWRON pin configuration

The PWRON pin can be configured as either a level sensitive input (PWRON\_CFG = 0), or as an edge sensitive input (PWRON\_CFG = 1). As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into sleep mode.

As an edge sensitive input, such as when connected to a mechanical switch, a falling edge turns on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part turns off or enters sleep mode.

Table 12. PWRON configuration

| PWRON_CFG | Mode   |
|-----------|--|
| 0         | PWRON pin HIGH = ON<br>PWRON pin LOW = OFF or sleep mode                                   |
| 1         | PWRON pin pulled LOW momentarily = ON<br>PWRON pin LOW for 4.0 seconds = OFF or sleep mode |

10.1.2.3 I<sup>2</sup>C address configuration

The I<sup>2</sup>C device address can be programmed from 0x08 to 0x0F. This allows flexibility to change the I<sup>2</sup>C address to avoid bus conflicts.

Address bit, I2C\_SLV\_ADDR[3] in OTP\_I2C\_ADDR register is hard coded to 1 while the lower three LSBs of the I<sup>2</sup>C address (I2C\_SLV\_ADDR[2:0]) are programmable as shown in [Table 13](#).

Table 13. I<sup>2</sup>C address configuration

| I2C_SLV_ADDR[3] hard coded | I2C_SLV_ADDR[2:0] | I <sup>2</sup> C device address (Hex) |
|----------------------------|-------------------|---------------------------------------|
| 1                          | 000               | 0x08                                  |
| 1                          | 001               | 0x09                                  |
| 1                          | 010               | 0x0A                                  |

| I2C_SLV_ADDR[3] hard coded | I2C_SLV_ADDR[2:0] | I <sup>2</sup> C device address (Hex) |
|----------------------------|-------------------|---------------------------------------|
| 1                          | 011               | 0x0B                                  |
| 1                          | 100               | 0x0C                                  |
| 1                          | 101               | 0x0D                                  |
| 1                          | 110               | 0x0E                                  |
| 1                          | 111               | 0x0F                                  |

#### 10.1.2.4 Soft start ramp rate

The startup ramp rate or soft start ramp rate can be selected from the options shown in [Section 10.4.4.2.1 "Dynamic voltage scaling"](#).

#### 10.1.3 OTP prototyping

Before permanently programming fuses, it is possible to test the desired configuration by using the Try Before Buy feature. With this feature, the configuration is loaded from the OTP registers. These registers serve as temporary storage for the values to be written to the fuses, for the values read from the fuses, or for the values read from the default configuration. To avoid confusion, these registers are referred to as the TBBOTP registers. The portion of the register map concerned with OTP is shown in [Table 135](#) and [Table 136](#).

The contents of the TBBOTP registers are initialized to zero when a valid  $V_{IN}$  is first applied. The values loaded into the TBBOTP registers depend on the setting of the VDDOTP pin and on the value of the TBB\_POR and FUSE\_POR\_XOR bits (see [Table 14](#)).

- If VDDOTP = VCOREDIG (1.5 V), the values are loaded from the default configuration.
- If VDDOTP = 0.0 V, TBB\_POR = 0 and FUSE\_POR\_XOR = 1, the values are loaded from the fuses. In the PF4210, FUSE\_POR1, FUSE\_POR2, and FUSE\_POR3 are XOR'ed into the FUSE\_POR\_XOR bit. The FUSE\_POR\_XOR has to be 1 for fuses to be loaded. This can be achieved by setting any one or all of the FUSE\_PORx bits. It is required to set all of the FUSE\_PORx bits to be able to load the fuses.
- If VDDOTP = 0.0 V, TBB\_POR = 0 and FUSE\_POR\_XOR = 0, the TBBOTP registers remain initialized at zero.

The initial value of TBB\_POR is always 0; only when VDDOTP = 0.0 V and TBB\_POR is set to 1 and the values from the TBBOTP registers maintained and not loaded from a different source.

The contents of the TBBOTP registers are modified by I<sup>2</sup>C. To communicate with I<sup>2</sup>C,  $V_{IN}$  must be valid and VDDIO to which SDA and SCL are pulled up, must be powered by a 1.7 V to 3.6 V supply.  $V_{IN}$  or the coin cell voltage must be valid to maintain the contents of the registers. To power on with the contents of the TBBOTP registers, the following conditions must exist:

- $V_{IN}$  is valid
- VDDOTP = 0.0 V
- TBB\_POR = 1
- Valid turn on event

### 10.1.4 Reading OTP fuses

As described in the previous section, the contents of the fuses are loaded to the TBBOTP registers when the following conditions are met:

- VIN is valid
- VDDOTP = 0.0 V
- TBB\_POR = 0
- FUSE\_POR\_XOR = 1

If ECC were enabled at the time the fuses were programmed, the error corrected values can be loaded into the TBBOTP registers if desired. Once the fuses are loaded and a turn on event occurs, the PMIC powers on with the configuration programmed in the fuses.

### 10.1.5 Programming OTP fuses

The parameters which can be programmed are shown in the TBBOTP registers in [Table 135](#) of the register map. The PF4210 offers ECC, the control registers for which functions are located in [Table 136](#) of the register map.

There are ten banks of twenty-six fuses each that can be programmed. Programming the fuses requires an 8.25 V, 100 mA supply powering the VDDOTP pin, bypassed with 10 to 20  $\mu$ F of capacitance.

**Table 14. Source of startup sequence**

| VDDOTP (V) | TBB_POR | FUSE_POR_XOR | Startup sequence      |
|------------|---------|--------------|-----------------------|
| 0          | 0       | 0            | None                  |
| 0          | 0       | 1            | OTP fuses             |
| 0          | 1       | x            | TBBOTP registers      |
| 1.5        | x       | x            | Default configuration |

## 10.2 16 MHz and 32 kHz clocks

There are two clocks: a trimmed 16 MHz, RC oscillator, and an untrimmed 32 kHz, RC oscillator. The 16 MHz oscillator is specified within  $-8.0/+8.0$  %.

The 32 kHz untrimmed clock is only used in the following conditions:

- VIN < UVDET
- All regulators are in sleep mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start up, VIN > UVDET
- PWRON\_CFG = 1, for power button debounce timing

In addition, when the 16 MHz is active in the ON mode, the debounce time in [Table 25](#) are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and PWRONI interrupts, which are referenced to the 32 kHz untrimmed clock.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

**Table 15. 16 MHz clock specifications**

$T_{MIN}$  to  $T_{MAX}$  (see Table 4),  $V_{IN} = 2.8\text{ V to }4.5\text{ V}$ ,  $LICELL = 1.8\text{ V to }3.3\text{ V}$  and typical external component values. Typical values are characterized at  $V_{IN} = 3.6\text{ V}$ ,  $LICELL = 3.0\text{ V}$ , and  $25\text{ }^{\circ}\text{C}$ , unless otherwise noted.

| Symbol               | Parameters                             | Min  | Typ | Max  | Units |
|----------------------|--|------|-----|------|-------|
| $V_{IN16\text{MHz}}$ | Operating voltage from VIN             | 2.8  | —   | 4.5  | V     |
| $f_{16\text{MHz}}$   | 16 MHz clock frequency                 | 14.7 | 16  | 17.2 | MHz   |
| $f_{2\text{MHz}}$    | 2.0 MHz clock frequency <sup>[1]</sup> | 1.84 | —   | 2.15 | MHz   |

[1] 2.0 MHz clock is derived from the 16 MHz clock.

### 10.2.1 Clock adjustment

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as  $\pm 3.0\%$  of the nominal frequency. Contact your NXP representative for detailed information on this feature.

## 10.3 Bias and references block description

### 10.3.1 Internal core voltage references

All regulators use the main band gap as the reference. The main band gap is bypassed with a capacitor at VCOREREF. The band gap and the rest of the core circuitry are supplied from VCORE.

The performance of the regulator is directly dependent on the performance of the band gap. No external DC loading is allowed on VCORE, VCOREDIG, or VCOREREF. VCOREDIG is powered as long as there is a valid supply and/or valid coin cell. Table 16 shows the main characteristics of the core circuitry.

**Table 16. Core voltages electrical specifications**

$T_{MIN}$  to  $T_{MAX}$  (see Table 4),  $V_{IN} = 2.8\text{ V to }4.5\text{ V}$ ,  $LICELL = 1.8\text{ V to }3.3\text{ V}$ , and typical external component values. Typical values are characterized at  $V_{IN} = 3.6\text{ V}$ ,  $LICELL = 3.0\text{ V}$ , and  $25\text{ }^{\circ}\text{C}$ , unless otherwise noted.<sup>[1]</sup>

| Symbol   | Parameters                    | Min | Typ   | Max | Units |
|--|-------------------------------|-----|-------|-----|-------|
| <b>VCOREDIG (digital core supply)</b>            |                               |     |       |     |       |
| $V_{\text{COREDIG}}$                             | Output voltage <sup>[2]</sup> |     |       |     | V     |
|  | ON mode                       | —   | 1.5   | —   |       |
|  | Coin cell mode and OFF        | —   | 1.3   | —   |       |
| <b>VCORE (analog core supply)</b>                |                               |     |       |     |       |
| $V_{\text{CORE}}$                                | Output voltage                |     |       |     | V     |
|  | ON mode and charging          | —   | 2.775 | —   |       |
|  | OFF and coin cell mode        | —   | 0.0   | —   |       |
| <b>VCOREREF (band gap / regulator reference)</b> |                               |     |       |     |       |
| $V_{\text{COREREF}}$                             | Output voltage                | —   | 1.2   | —   | V     |
| $V_{\text{COREREFACC}}$                          | Absolute accuracy             | —   | 0.5   | —   | %     |
| $V_{\text{COREREF TACC}}$                        | Temperature drift             | —   | 0.25  | —   | %     |

[1] For information only

## 14-channel power management integrated circuit (PMIC) for audio/video applications

[2]  $3.0\text{ V} < V_{IN} < 4.5\text{ V}$ , no external loading on VCOREDIG, VCORE, or VCOREREF. Extended operation down to UVDET, but no system malfunction.

## 10.3.1.1 External components

Table 17. External components for core voltage

| Regulator | Capacitor value ( $\mu\text{F}$ ) |
|-----------|-----------------------------------|
| VCOREDIG  | 1.0                               |
| VCORE     | 1.0                               |
| VCOREREF  | 0.22                              |

## 10.3.2 VREFDDR voltage reference

VREFDDR is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. It is typically used as the reference voltage for DDR memories.

A filtered resistor divider is utilized to create a low frequency pole. This divider then utilizes a voltage follower to drive the load.

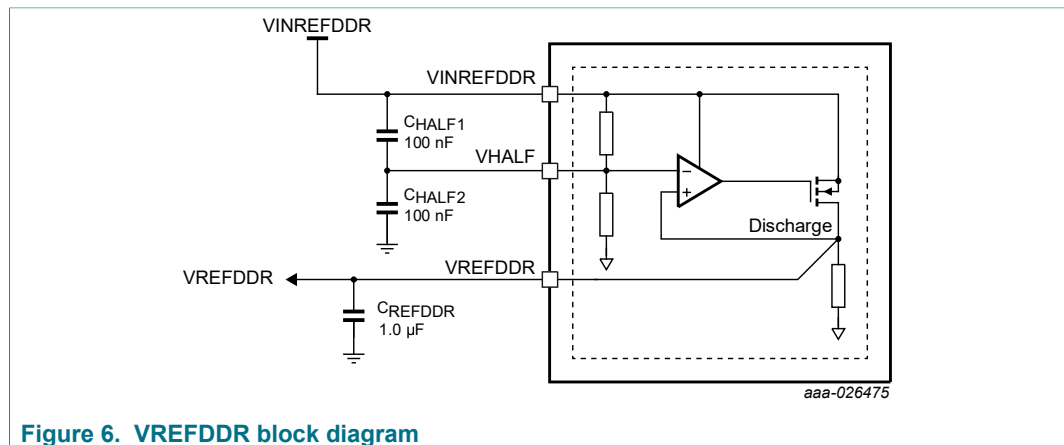


Figure 6. VREFDDR block diagram

## 10.3.2.1 VREFDDR control register

The VREFDDR voltage reference is controlled by a single bit in VREFDDCTRL register in [Table 18](#).

Table 18. Register VREFDDCTRL – ADDR 0x6A

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| UNUSED    | 3:0        | —   | 0x00    | unused   |
| VREFDDREN | 4          | R/W | 0x00    | Enables or disables VREFDDR output voltage <ul style="list-style-type: none"> <li>0 = VREFDDR disabled</li> <li>1 = VREFDDR enabled</li> </ul> |
| UNUSED    | 7:5        | —   | 0x00    | unused   |

## 10.3.2.1.1 External components

Table 19. VREFDDR external components

| Capacitor <sup>[1]</sup>          | Capacitance ( $\mu\text{F}$ ) |
|-----------------------------------|-------------------------------|
| VINREFDDR to VHALF <sup>[2]</sup> | 0.1                           |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Capacitor <sup>[1]</sup> | Capacitance (μF) |
|--------------------------|------------------|
| VHALF to GND             | 0.1              |
| VREFDDR                  | 1.0              |

[1] Use X5R or X7R capacitors.

[2] VINREFDDR to GND, 1.0 μF minimum capacitance is provided by buck regulator output.

## 10.3.2.1.2 VREFDDR specifications

**Table 20. VREFDDR electrical characteristics**

$T_{MIN}$  to  $T_{MAX}$  (see Table 4),  $V_{IN} = 3.6$  V,  $I_{REFDDR} = 0.0$  mA,  $V_{INREFDDR} = 1.5$  V and typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6$  V,  $I_{REFDDR} = 0.0$  mA,  $V_{INREFDDR} = 1.5$  V, and 25 °C, unless otherwise noted.

| Symbol                  | Parameter   | Min  | Typ              | Max | Unit  |
|-------------------------|---|------|------------------|-----|-------|
| <b>VREFDDR</b>          |   |      |                  |     |       |
| $V_{INREFDDR}$          | Operating input voltage range   | 1.1  | —                | 1.8 | V     |
| $I_{REFDDR}$            | Operating load current range  | 0.0  | —                | 10  | mA    |
| $I_{REFDRLIM}$          | Current limit<br>$I_{REFDDR}$ when $V_{REFDDR}$ is forced to $V_{INREFDDR}/4$   | 10.5 | 15               | 25  | mA    |
| $I_{REFDDRQ}$           | Quiescent current <sup>[1]</sup>  | —    | 8.0              | —   | μA    |
| <b>Active mode – DC</b> |   |      |                  |     |       |
| $V_{REFDDR}$            | Output voltage<br>$1.2$ V < $V_{INREFDDR}$ < $1.8$ V<br>$0.0$ mA < $I_{REFDDR}$ < $10$ mA<br><br>$1.1$ V ≤ $V_{INREFDDR}$ ≤ $1.2$ V<br>$0.0$ mA < $I_{REFDDR}$ ≤ $1.0$ mA   | —    | $V_{INREFDDR}/2$ | —   | V     |
| $V_{REFDRTOL}$          | Output voltage tolerance ( $T_A = 0$ °C to $85$ °C)<br>$1.2$ V < $V_{INREFDDR}$ < $1.8$ V<br>$0.6$ mA ≤ $I_{REFDDR}$ ≤ $10$ mA<br><br>$1.1$ V ≤ $V_{INREFDDR}$ ≤ $1.2$ V<br>$0.0$ mA < $I_{REFDDR}$ ≤ $1.0$ mA  | -1.0 | —                | 1.0 | %     |
| $V_{REFDRTOL}$          | Output voltage tolerance ( $T_A = -40$ °C to $105$ °C), applicable to the industrial version<br>$1.2$ V < $V_{INREFDDR}$ < $1.8$ V<br>$0.6$ mA ≤ $I_{REFDDR}$ ≤ $10$ mA<br><br>$1.1$ V ≤ $V_{INREFDDR}$ ≤ $1.2$ V<br>$0.0$ mA < $I_{REFDDR}$ ≤ $1.0$ mA | -1.2 | —                | 1.2 | %     |
| $V_{REFDRLOR}$          | Load regulation<br>$1.0$ mA < $I_{REFDDR}$ < $10$ mA<br>$1.2$ V < $V_{INREFDDR}$ < $1.8$ V<br><br>$0.1$ mA < $I_{REFDDR}$ < $1.0$ mA<br>$1.1$ V ≤ $V_{INREFDDR}$ ≤ $1.2$ V  | —    | 0.40             | —   | mV/mA |
|                         |   | —    | 1.15             | —   |       |

| Symbol                  | Parameter  | Min | Typ | Max | Unit          |
|-------------------------|--|-----|-----|-----|---------------|
| <b>Active mode – AC</b> |  |     |     |     |               |
| $t_{ONREFDDR}$          | Turn on time<br>Enable to 90 % of end value<br>$V_{INREFDDR} = 1.1\text{ V}, 1.2\text{ V}, 1.8\text{ V}$<br>$I_{REFDDR} = 0.0\text{ mA}$       | —   | —   | 100 | $\mu\text{s}$ |
| $t_{OFFREFDDR}$         | Turn off time<br>Disable to 10 % of initial value<br>$V_{INREFDDR} = 1.1\text{ V}, 1.2\text{ V}, 1.8\text{ V}$<br>$I_{REFDDR} = 0.0\text{ mA}$ | —   | —   | 10  | ms            |
| $V_{REFDDROSH}$         | Startup overshoot<br>$V_{INREFDDR} = 1.1\text{ V}, 1.2\text{ V}, 1.8\text{ V}$<br>$I_{REFDDR} = 0.0\text{ mA}$                                 | —   | 1.0 | 6.0 | %             |
| $V_{REFDDRTLRL}$        | Transient load response<br>$V_{INREFDDR} = 1.1\text{ V}, 1.2\text{ V}, 1.8\text{ V}$   | —   | 5.0 | —   | mV            |

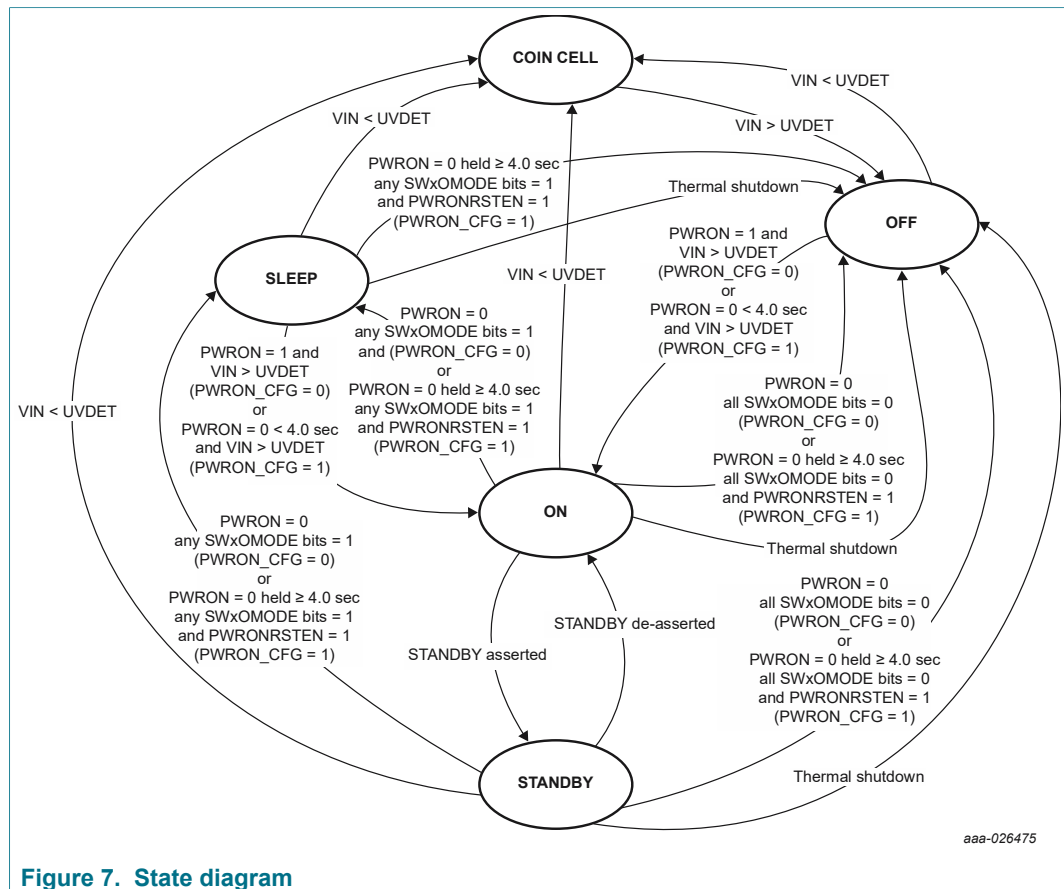
[1] When  $V_{REFDDR}$  is off there is a quiescent current of 1.5  $\mu\text{A}$  typical.

## 10.4 Power generation

### 10.4.1 Modes of operation

The operation of the PF4210 can be reduced to five states or modes: on, off, sleep, standby, and coin cell.

[Figure 7](#) shows the state diagram of the PF4210, along with the conditions to enter and exit from each state.



To complement the state diagram in [Figure 7](#), a description of the states is provided in following sections. Note that  $V_{IN}$  must exceed the rising UVDET threshold to allow a power up.

See [Table 26](#) for the UVDET thresholds. Additionally,  $I^2C$  control is not possible in the coin cell mode and the interrupt signal, INTB, is only active in sleep, standby, and on states.

#### 10.4.1.1 On mode

The PF4210 enters the on mode after a turn on event. RESETBMCU is deasserted high in this mode of operation.

#### 10.4.1.2 Off mode

The PF4210 enters the off mode after a turn off event. A thermal shutdown event also forces the PF4210 into the off mode.

Only VCOREDIG and VSNVS are powered in this mode of operation. To exit the off mode, a valid turn on event is required. RESETBMCU is asserted low in this mode.

#### 10.4.1.3 Standby mode

- Depending on STANDBY pin configuration, standby is entered when the STANDBY pin is asserted. This is typically used for low-power mode of operation.
- When STANDBY is deasserted, standby mode is exited.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

A product may be designed to go into a low-power mode after periods of inactivity. The STANDBY pin is provided for board level control of going in and out of such Deep Sleep Modes (DSM).

When a product is in DSM, it may be able to reduce the overall platform current by lowering the regulator output voltage, changing the operating mode of the regulators or disabling some regulators. The configuration of the regulators in standby is preprogrammed through the I<sup>2</sup>C interface.

Note that the STANDBY pin is programmable for active high or active low polarity, and decoding of a standby event takes into account the programmed input polarity as shown in [Table 21](#). When the PF4210 is powered up first, regulator settings for the standby mode are mirrored from the regulator settings for the on mode. To change the STANDBY pin polarity to active low, set the STANDBYINV bit via software first, and then change the regulator settings for standby mode as required. For simplicity, STANDBY generally is referred to as active high throughout this document.

**Table 21. Standby pin and polarity control**

| STANDBY (pin) <sup>[1]</sup> | STANDBYINV (I <sup>2</sup> C bit) <sup>[2]</sup> | STANDBY control <sup>[3]</sup> |
|------------------------------|--|--------------------------------|
| 0                            | 0  | 0                              |
| 0                            | 1  | 1                              |
| 1                            | 0  | 1                              |
| 1                            | 1  | 0                              |

[1] The state of the STANDBY pin only has influence in on mode.

[2] Bit 6 in power control register (ADDR – 0x1B)

[3] STANDBY = 0: system is not in standby, STANDBY = 1: system is in standby

Since STANDBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes. A programmable delay is provided to hold off the system response to a standby event. This allows the processor and peripherals some time after a standby instruction has been received to terminate processes to facilitate seamless entering into standby mode.

When enabled (STBYDLY = 01, 10, or 11) per [Table 22](#), STBYDLY delays the standby initiated response for the entire IC, until the STBYDLY counter expires.

An allowance should be made for three additional 32 kHz cycles required to synchronize the standby event.

**Table 22. STANDBY delay – initiated response**

| STBYDLY[1:0] <sup>[1]</sup> | Function                    |
|-----------------------------|-----------------------------|
| 00                          | No delay                    |
| 01                          | One 32 kHz period (default) |
| 10                          | Two 32 kHz periods          |
| 11                          | Three 32 kHz periods        |

[1] Bits [5:4] in power control register (ADDR – 0x1B)

#### 10.4.1.4 Sleep mode

- Depending on PWRON pin configuration, sleep mode is entered when PWRON is deasserted and SWxOMODE bit is set.
- To exit sleep mode, assert the PWRON pin.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

In the sleep mode, the regulator uses the set point as programmed by SW1xOFF[5:0] for SW1A/B/C and by SWxOFF[6:0] for SW2, SW3A/B, and SW4. The activated regulators maintain settings for this mode and voltage until the next turn on event. [Table 23](#) shows the control bits in sleep mode. During sleep mode, interrupts are active and the INTB pin reports any unmasked fault event.

Table 23. Regulator mode control

| SWxOMODE | Off operational mode (sleep) <sup>[1]</sup> |
|----------|---|
| 0        | Off   |
| 1        | PFM   |

[1] For sleep mode, an activated switching regulator should use the off mode set point as programmed by SW1xOFF[5:0] for SW1A/B/C and SWxOFF[6:0] for SW2, SW3A/B, and SW4.

## 10.4.1.5 Coin cell mode

In the coin cell state, the coin cell is the only valid power source ( $V_{IN} = 0.0$  V) to the PMIC. No turn on event is accepted in the coin cell state. Transition to the off state requires  $V_{IN}$  surpasses UVDET threshold. RESETBMCU is held low in this mode.

If the coin cell is depleted, a complete system reset occurs. At the next application of power and the detection of a turn on event, the system is re-initialized with all I<sup>2</sup>C bits including those reset on COINPORB, which are restored to their default states.

## 10.4.2 State machine flow summary

[Table 24](#) provides a summary matrix of the PF4210 flow diagram to show the conditions needed to transition from one state to another.

Table 24. State machine flow summary

| STATE         |           | Next state   |                  |       |         |   |
|---------------|-----------|--|------------------|-------|---------|---|
|               |           | OFF  | Coin cell        | Sleep | Standby | ON  |
| Initial state | OFF       | X  | $V_{IN} < UVDET$ | X     | X       | PWRON_CFG = 0<br>PWRON = 1 & $V_{IN} > UVDET$<br>or<br>PWRON_CFG = 1<br>PWRON = 0 < 4.0 s<br>& $V_{IN} > UVDET$ |
|               | Coin cell | $V_{IN} > UVDET$   | X                | X     | X       | X   |
|               | Sleep     | Thermal shutdown<br>PWRON_CFG = 1<br>PWRON = 0 $\geq$ 4.0 s<br>Any SWxOMODE = 1<br>&<br>PWRONRSTEN = 1 | $V_{IN} < UVDET$ | X     | X       | PWRON_CFG = 0<br>PWRON = 1 & $V_{IN} > UVDET$<br>or<br>PWRON_CFG = 1<br>PWRON = 0 < 4.0 s &<br>$V_{IN} > UVDET$ |

| STATE   |   | Next state       |  |                  |                    |    |
|---------|---|------------------|--|------------------|--------------------|----|
|         |   | OFF              | Coin cell  | Sleep            | Standby            | ON |
| Standby | Thermal shutdown  | $V_{IN} < UVDET$ | PWRON_CFG = 0<br>PWRON = 0<br>Any SWxOMODE = 1<br>or<br>PWRON_CFG = 1<br>PWRON = 0 $\geq$ 4.0 s<br>Any SWxOMODE = 1<br>&<br>PWRONRSTEN = 1 | X                | Standby deasserted |    |
|         | PWRON_CFG = 0<br>PWRON = 0<br>All SWxOMODE = 0<br>or<br>PWRON_CFG = 1<br>PWRON = 0 $\geq$ 4.0 s<br>All SWxOMODE = 0 &<br>PWRONRSTEN = 1 |                  |  |                  |                    |    |
| ON      | Thermal shutdown  | $V_{IN} < UVDET$ | PWRON_CFG = 0<br>PWRON = 0<br>Any SWxOMODE = 1<br>or<br>PWRON_CFG = 1<br>PWRON = 0 $\geq$ 4.0 s<br>Any SWxOMODE = 1<br>&<br>PWRONRSTEN = 1 | Standby asserted | X                  |    |
|         | PWRON_CFG = 0<br>PWRON = 0<br>All SWxOMODE = 0<br>or<br>PWRON_CFG = 1<br>PWRON = 0 $\geq$ 4.0 s<br>All SWxOMODE = 0 &<br>PWRONRSTEN = 1 |                  |  |                  |                    |    |

#### 10.4.2.1 Turn on events

From off and sleep modes, the PMIC is powered on by a turn on event. The type of turn on event depends on the configuration of PWRON. PWRON may be configured as an active high when PWRON\_CFG = 0, or as the input of a mechanical switch when PWRON\_CFG = 1.  $V_{IN}$  must be greater than UVDET for the PMIC to turn on.

When PWRON is configured as an active high and PWRON is high (pulled up to VSNVS) before  $V_{IN}$  is valid, a  $V_{IN}$  transition from 0.0 V to a voltage greater than UVDET is also a turn on event. See [Figure 7](#) and the [Table 24](#) for more details. Any regulator enabled in the sleep mode remains enabled when transitioning from sleep to on, the regulator does not turn off and then on again to match the startup sequence. Detailed description of the PWRON configurations are as follows:

- If PWRON\_CFG = 0, the PWRON signal is high and  $V_{IN} > UVDET$ , the PMIC turns on; the interrupt and sense bits, PWRONI and PWRONS respectively are set
- If PWRON\_CFG = 1,  $V_{IN} > UVDET$  and PWRON transitions from high to low, the PMIC turns on; the interrupt and sense bits, PWRONI and PWRONS respectively are set

The sense bit shows the real time status of the PWRON pin. In this configuration, the PWRON input can be a mechanical switch debounced through a programmable debouncer, PWRONDBNC[1:0], to avoid a response to a very short (unintentional) key press. The interrupt is generated for both the falling and the rising edge of the PWRON pin. By default, a 30 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with PWRONDBNC[1:0] as defined in [Table 25](#). The interrupt is cleared by software, or when cycling through the off mode.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 25. PWRON hardware debounce bit settings

| Bits           | State <sup>[1]</sup> | Turn on debounce (ms) | Falling edge INT debounce (ms) | Rising edge INT debounce (ms) |
|----------------|----------------------|-----------------------|--------------------------------|-------------------------------|
| PWRONDBNC[1:0] | 00                   | 0.0                   | 31.25                          | 31.25                         |
|                | 01                   | 31.25                 | 31.25                          | 31.25                         |
|                | 10                   | 125                   | 125                            | 31.25                         |
|                | 11                   | 750                   | 750                            | 31.25                         |

[1] The sense bit, PWRONS is not debounced and follows the state of the PWRON pin.

### 10.4.2.2 Turn off events

#### 10.4.2.2.1 PWRON pin

The PWRON pin is used to power off the PF4210. The PWRON pin can be configured with OTP to power off the PMIC under the following two conditions:

1. PWRON\_CFG bit = 0, SWxOMODE bit = 0 and PWRON pin is low
2. PWRON\_CFG bit = 1, SWxOMODE bit = 0, PWRONRSTEN = 1 and PWRON is held low for longer than 4.0 seconds. Alternatively, the system can be configured to restart automatically by setting the RESTARTEN bit.

#### 10.4.2.2.2 Thermal protection

If the die temperature surpasses a given threshold, the thermal protection circuit powers off the PMIC to avoid damage. A turn on event does not power on the PMIC while it is in thermal protection.

The part remains in off mode until the die temperature decreases below a given threshold. There are no specific interrupts related to this other than the warning interrupt. See [Section 8.3 "Power dissipation"](#) for more information.

#### 10.4.2.2.3 Undervoltage detection

When the voltage at VIN drops below the undervoltage falling threshold UVDET, the state machine transitions to the coin cell mode.

### 10.4.3 Power tree

The PF4210 PMIC features up to six buck regulators, one boost regulator, six general purpose LDOs, one switch/LDO combination, and a DDR voltage reference to supply voltages for the application processor and peripheral devices. The buck regulators as well as the boost regulator are supplied directly from the main input supply ( $V_{IN}$ ). The inputs to all of the buck regulators must be tied to VIN, whether they are powered on or off.

The six general use LDO regulators are directly supplied from the main input supply or from the switching regulators depending on the application requirements. Since VREFDDR is intended to provide DDR memory reference voltage, it is supplied by any rail supplying voltage to DDR memories; the typical application recommends the use of SW3 as the input supply for VREFDDR. VSNVS is supplied by either the main input supply or the coin cell. See [Table 26](#) for a summary of all power supplies provided by the PF4210.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 26. Power tree summary

| Supply  | Output voltage (V)       | Step size (mV) | Maximum load current (mA)                          |
|---------|--------------------------|----------------|--|
| SW1A/B  | 0.3 to 1.875             | 25             | 2500   |
| SW1C    | 0.3 to 1.875             | 25             | 2000   |
| SW2     | 0.4 to 3.3               | 25/50          | 2500   |
| SW3A/B  | 0.4 to 3.3               | 25/50          | 1500 <sup>[1]</sup>                                |
| SW4     | 0.5*SW3A_OUT, 0.4 to 3.3 | 25/50          | 1000   |
| SWBST   | 5.00/5.05/5.10/5.15      | 50             | 600  |
| VGEN1   | 0.80 to 1.55             | 50             | 100  |
| VGEN2   | 0.80 to 1.55             | 50             | 250  |
| VGEN3   | 1.8 to 3.3               | 100            | 100  |
| VGEN4   | 1.8 to 3.3               | 100            | 350  |
| VGEN5   | 1.8 to 3.3               | 100            | 100  |
| VGEN6   | 1.8 to 3.3               | 50             | 200  |
| VSNVS   | 1.0 to 3.0               | NA             | 1.5 (consumer version)<br>1.0 (industrial version) |
| VREFDDR | 0.5*SW3A_OUT             | NA             | 10   |

[1] Current rating per independent phase, when SW3A/B is set in single or dual phase, current capability is up to 3000 mA.

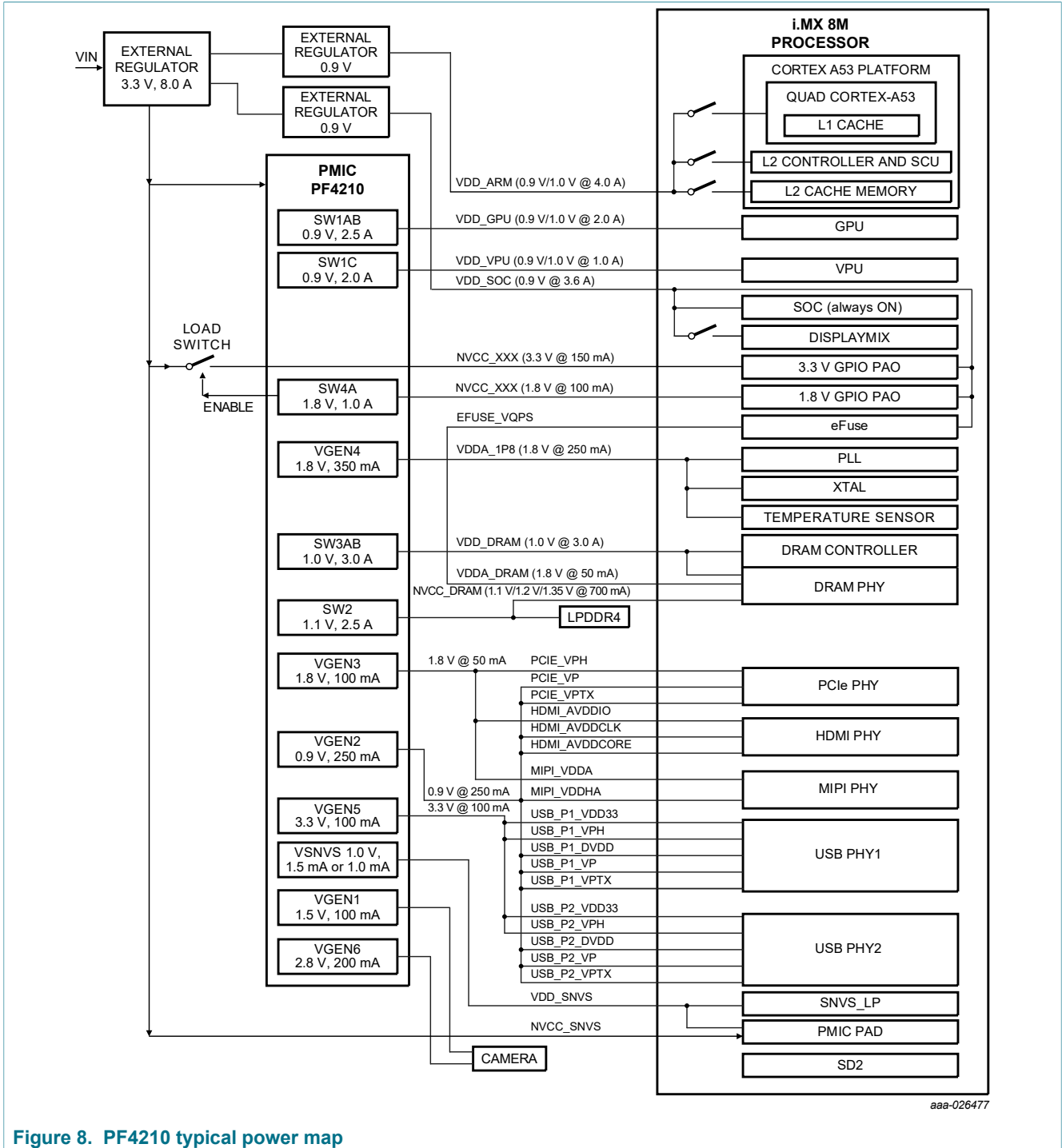
[Figure 8](#) shows a simplified power map with various recommended options to supply the different block within the PF4210, as well as the typical application voltage domain on the i.MX processor. Note that each application power tree is dependent upon the system's voltage and current requirements, therefore a proper input voltage should be selected for the regulators.

The minimum operating voltage for the main  $V_{IN}$  supply is 2.8 V, for lower voltage proper operation is not guaranteed. However at initial power up, the input voltage must surpass the rising UVDET threshold before proper operation is guaranteed. [Table 27](#) summarizes the UVDET thresholds.

Table 27. UVDET threshold

| UVDET threshold | $V_{IN}$ |
|-----------------|----------|
| Rising          | 3.1 V    |
| Falling         | 2.65 V   |

14-channel power management integrated circuit (PMIC) for audio/video applications



aaa-026477

Figure 8. PF4210 typical power map

10.4.4 Buck regulators

Each buck regulator is capable of operating in PFM, APS, and PWM switching modes.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

## 10.4.4.1 Current limit

Each buck regulator has a programmable current limit. In an overcurrent condition, the current is limited cycle-by-cycle. If the current limit condition persists for more than 8.0 ms, a fault interrupt is generated.

## 10.4.4.2 General control

To improve system efficiency the buck regulators can operate in different switching modes. Changing between switching modes can occur by any of the following means: I<sup>2</sup>C programming, exiting/entering the standby mode, exiting/entering sleep mode, and load current variation.

Available switching modes for buck regulators are presented in [Table 28](#).

Table 28. Switching mode description

| Mode | Description  |
|------|--|
| OFF  | The regulator is switched off and the output voltage is discharged.  |
| PFM  | In this mode, the regulator is always in PFM mode, which is useful at light loads for optimized efficiency.            |
| PWM  | In this mode, the regulator is always in PWM mode operation regardless of load conditions.                             |
| APS  | In this mode, the regulator moves automatically between pulse skipping mode and PWM mode depending on load conditions. |

During soft start of the buck regulators, the controller transitions through the PFM, APS, and PWM switching modes. 3.0 ms (typical) after the output voltage reaches regulation, the controller transitions to the selected switching mode. Depending on the particular switching mode selected, additional ripple is observed on the output voltage rail as the controller transitions between switching modes.

[Table 29](#) summarizes the buck regulator programmability for normal and standby modes.

Table 29. Regulator mode control

| SWxMODE[3:0]      | Normal mode | Standby mode |
|-------------------|-------------|--------------|
| 0000              | Off         | Off          |
| 0001              | PWM         | Off          |
| 0010              | Reserved    | Reserved     |
| 0011              | PFM         | Off          |
| 0100              | APS         | Off          |
| 0101              | PWM         | PWM          |
| 0110              | PWM         | APS          |
| 0111              | Reserved    | Reserved     |
| 1000 (by default) | APS         | APS          |
| 1001              | Reserved    | Reserved     |
| 1010              | Reserved    | Reserved     |
| 1011              | Reserved    | Reserved     |
| 1100              | APS         | PFM          |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| SWxMODE[3:0] | Normal mode | Standby mode |
|--------------|-------------|--------------|
| 1101         | PWM         | PFM          |
| 1110         | Reserved    | Reserved     |
| 1111         | Reserved    | Reserved     |

Transitioning between normal and standby modes can affect a change in switching modes as well as output voltage. The rate of the output voltage change is controlled by the dynamic voltage scaling (DVS), explained in [Section 10.4.4.2.1 "Dynamic voltage scaling"](#). For each regulator, the output voltage options are the same for normal and standby modes.

When in standby mode, the regulator outputs the voltage programmed in its standby voltage register and operates in the mode selected by the SWxMODE[3:0] bits. Upon exiting standby mode, the regulator returns to its normal switching mode and its output voltage programmed in its voltage register.

Any regulators whose SWxOMODE bit is set to 1 enters sleep mode if a PWRON turn off event occurs, and any regulator whose SWxOMODE bit is set to 0 turns off. In sleep mode, the regulator outputs the voltage programmed in its off (sleep) voltage register and operates in the PFM mode. The regulator exits the sleep mode when a turn on event occurs. Any regulator whose SWxOMODE bit is set to 1 remains on and change to its normal configuration settings when exiting the sleep state to the on state. Any regulator whose SWxOMODE bit is set to 0 is powered up with the same delay in the start up sequence as when powering on from off. At this point, the regulator returns to its default on state output voltage and switch mode settings.

[Table 23](#) shows the control bits in sleep mode. When sleep mode is activated by the SWxOMODE bit, the regulator uses the set point as programmed by SW1xOFF[5:0] for SW1A/B/C and by SWxOFF[6:0] for SW2, SW3A/B, and SW4.

#### 10.4.4.2.1 Dynamic voltage scaling

To reduce overall power consumption, processor core voltage can be varied depending on the mode or activity level of the processor.

1. Normal operation: The output voltage is selected by I<sup>2</sup>C bits SW1x[5:0] for SW1A/B/C and SWx[6:0] for SW2, SW3A/B, and SW4. A voltage transition initiated by I<sup>2</sup>C is governed by the DVS stepping rates shown in [Table 32](#) and [Table 33](#).
2. Standby mode: The output voltage can be higher, or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I<sup>2</sup>C bits SW1xSTBY[5:0] for SW1A/B/C and by bits SWxSTBY[6:0] for SW2, SW3A/B, and SW4. Voltage transitions initiated by a Standby event are governed by the SW1xDVSSPEED[1:0] and SWxDVSSPEED[1:0] I<sup>2</sup>C bits shown in [Table 32](#) and [Table 33](#) respectively.
3. Sleep mode: The output voltage can be higher or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I<sup>2</sup>C bits SW1xOFF[5:0] for SW1A/B/C and by bits SWxOFF[6:0] for SW2, SW3A/B, and SW4. Voltage transitions initiated by a turn off event are governed by the SW1xDVSSPEED[1:0] and SWxDVSSPEED[1:0] I<sup>2</sup>C bits shown in [Table 32](#) and [Table 33](#) respectively.

[Table 30](#), [Table 31](#), [Table 32](#), and [Table 33](#) summarize the set point control and DVS time stepping applied to all regulators.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 30. DVS control logic for SW1A/B/C

| STANDBY | Set point selected by |
|---------|-----------------------|
| 0       | SW1x[5:0]             |
| 1       | SW1xSTBY[5:0]         |

Table 31. DVS control logic for SW2, SW3A/B, and SW4

| STANDBY | Set point selected by |
|---------|-----------------------|
| 0       | SWx[6:0]              |
| 1       | SWxSTBY[6:0]          |

Table 32. DVS speed selection for SW1A/B/C

| SW1xDVSSPEED[1:0] | Function                    |
|-------------------|-----------------------------|
| 00                | 25 mV step each 2.0 $\mu$ s |
| 01 (default)      | 25 mV step each 4.0 $\mu$ s |
| 10                | 25 mV step each 8.0 $\mu$ s |
| 11                | 25 mV step each 16 $\mu$ s  |

Table 33. DVS speed selection for SW2, SW3A/B, and SW4

| SWxDVSSPEED[1:0] | Function<br>SWx[6] = 0 or SWxSTBY[6] = 0 | Function<br>SWx[6] = 1 or SWxSTBY[6] = 1 |
|------------------|--|--|
| 00               | 25 mV step each 2.0 $\mu$ s              | 50 mV step each 4.0 $\mu$ s              |
| 01 (default)     | 25 mV step each 4.0 $\mu$ s              | 50 mV step each 8.0 $\mu$ s              |
| 10               | 25 mV step each 8.0 $\mu$ s              | 50 mV step each 16 $\mu$ s               |
| 11               | 25 mV step each 16 $\mu$ s               | 50 mV step each 32 $\mu$ s               |

The regulators have a strong sourcing and sinking capability in PWM mode, therefore the fastest rising and falling slopes are determined by the regulator in PWM mode. However, if the regulators are programmed in PFM or APS mode during a DVS transition, the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

The following diagram shows the general behavior for the regulators when initiated with I<sup>2</sup>C programming, or standby control. During the DVS period the overcurrent condition of the regulator should be masked.

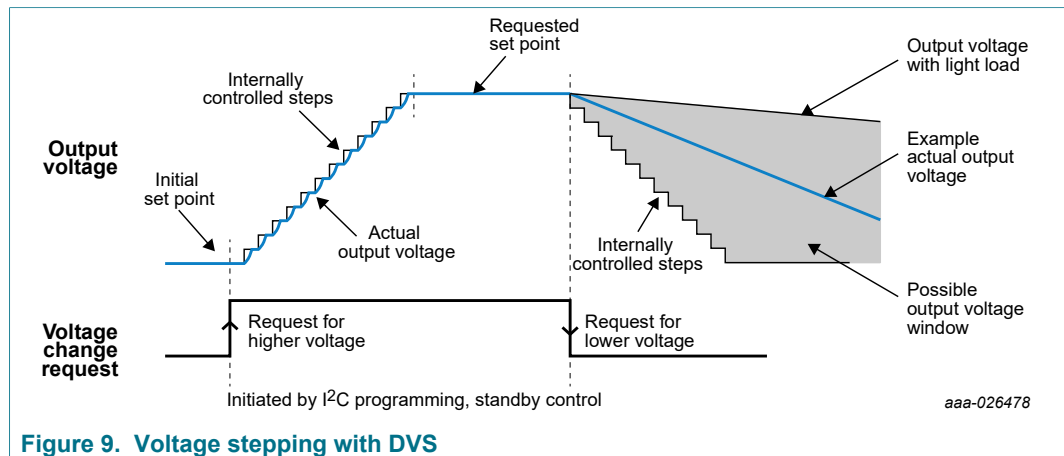


Figure 9. Voltage stepping with DVS

#### 10.4.4.2.2 Regulator phase clock

The SWxPHASE[1:0] bits select the phase of the regulator clock as shown in [Table 34](#). By default, each regulator is initialized at 90° out of phase with respect to each other. For example, SW1x is set to 0°, SW2 is set to 90°, SW3A/B is set to 180°, and SW4 is set to 270° by default at power up.

**Table 34. Regulator phase clock selection**

| SWxPHASE[1:0] | Phase of clock sent to regulator (degrees) |
|---------------|--|
| 00            | 0  |
| 01            | 90   |
| 10            | 180  |
| 11            | 270  |

The SWxFREQ[1:0] register is used to set the desired switching frequency for each one of the buck regulators. [Table 36](#) shows the selectable options for SWxFREQ[1:0]. For each frequency, all phases are available, allowing regulators operating at different frequencies to have different relative switching phases. However, not all combinations are practical. For example, 2.0 MHz, 90° and 4.0 MHz, 180° are the same in terms of phasing. [Table 35](#) shows the optimum phasing when using more than one switching frequency.

**Table 35. Optimum phasing**

| Frequencies | Optimum phasing |
|-------------|-----------------|
| 1.0 MHz     | 0°              |
| 2.0 MHz     | 180°            |
| 1.0 MHz     | 0°              |
| 4.0 MHz     | 180°            |
| 2.0 MHz     | 0°              |
| 4.0 MHz     | 180°            |
| 1.0 MHz     | 0°              |
| 2.0 MHz     | 90°             |
| 4.0 MHz     | 90°             |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 36. Regulator frequency configuration

| SWxFREQ[1:0] | Frequency |
|--------------|-----------|
| 00           | 1.0 MHz   |
| 01           | 2.0 MHz   |
| 10           | 4.0 MHz   |
| 11           | Reserved  |

## 10.4.4.2.3 Programmable maximum current

The maximum current,  $ISW_{xMAX}$ , of each buck regulator is programmable. This allows the use of smaller inductors where lower currents are required. Programmability is accomplished by choosing the number of paralleled power stages in each regulator. The SWx\_PWRSTG[2:0] bits in [Table 136](#) of the register map control the number of power stages.

See [Table 37](#) for the programmable options. Bit[0] must always be enabled to ensure the stage with the current sensor is used. The default setting, SWx\_PWRSTG[2:0] = 111, represents the highest maximum current. The current limit for each option is also scaled by the percentage of power stages enabled.

Table 37. Programmable current configuration

| Regulators | Control bits      |   |   | % of power stages enabled | Rated current (A) |
|------------|-------------------|---|---|---------------------------|-------------------|
| SW1AB      | SW1AB_PWRSTG[2:0] |   |   |                           | $ISW1AB_{MAX}$    |
|            | 0                 | 0 | 1 | 40 %                      | 1.0               |
|            | 0                 | 1 | 1 | 80 %                      | 2.0               |
|            | 1                 | 0 | 1 | 60 %                      | 1.5               |
|            | 1                 | 1 | 1 | 100 %                     | 2.5               |
| SW1C       | SW1C_PWRSTG[2:0]  |   |   |                           | $ISW1C_{MAX}$     |
|            | 0                 | 0 | 1 | 43 %                      | 0.9               |
|            | 0                 | 1 | 1 | 58 %                      | 1.2               |
|            | 1                 | 0 | 1 | 86 %                      | 1.7               |
|            | 1                 | 1 | 1 | 100 %                     | 2.0               |
| SW2        | SW2_PWRSTG[2:0]   |   |   |                           | $ISW2_{MAX}$      |
|            | 0                 | 0 | 1 | 38%                       | 0.75              |
|            | 0                 | 1 | 1 | 75%                       | 1.5               |
|            | 1                 | 0 | 1 | 63 %                      | 1.25              |
|            | 1                 | 1 | 1 | 100 %                     | 2.5               |
| SW3A       | SW3A_PWRSTG[2:0]  |   |   |                           | $ISW3A_{MAX}$     |
|            | 0                 | 0 | 1 | 40 %                      | 0.5               |
|            | 0                 | 1 | 1 | 80 %                      | 1.0               |
|            | 1                 | 0 | 1 | 60 %                      | 0.75              |
|            | 1                 | 1 | 1 | 100 %                     | 1.5               |
| SW3B       | SW3B_PWRSTG[2:0]  |   |   |                           | $ISW3B_{MAX}$     |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Regulators | Control bits    |   |   | % of power stages enabled | Rated current (A)   |
|------------|-----------------|---|---|---------------------------|---------------------|
|            |                 |   |   |                           |                     |
|            | 0               | 0 | 1 | 40 %                      | 0.5                 |
|            | 0               | 1 | 1 | 80 %                      | 1.0                 |
|            | 1               | 0 | 1 | 60 %                      | 0.75                |
|            | 1               | 1 | 1 | 100 %                     | 1.5                 |
| SW4        | SW4_PWRSTG[2:0] |   |   |                           | ISW4 <sub>MAX</sub> |
|            | 0               | 0 | 1 | 50 %                      | 0.5                 |
|            | 0               | 1 | 1 | 75 %                      | 0.75                |
|            | 1               | 0 | 1 | 75 %                      | 0.75                |
|            | 1               | 1 | 1 | 100 %                     | 1.0                 |

## 10.4.4.3 SW1A/B/C

SW1A/B/C are 2.5 A to 4.5 A buck regulators which can be configured in various phasing schemes, depending on the desired cost/ performance trade-offs. The following configurations are available:

- SW1A/B/C single phase with one inductor
- SW1A/B as a single phase with one inductor and SW1C in independent mode with one inductor
- SW1A/B as a dual phase with two inductors and SW1C in independent mode with one inductor

The desired configuration is programmed by OTP by using SW1\_CONFIG[1:0] bits in the register map [Table 135](#), as shown in [Table 38](#).

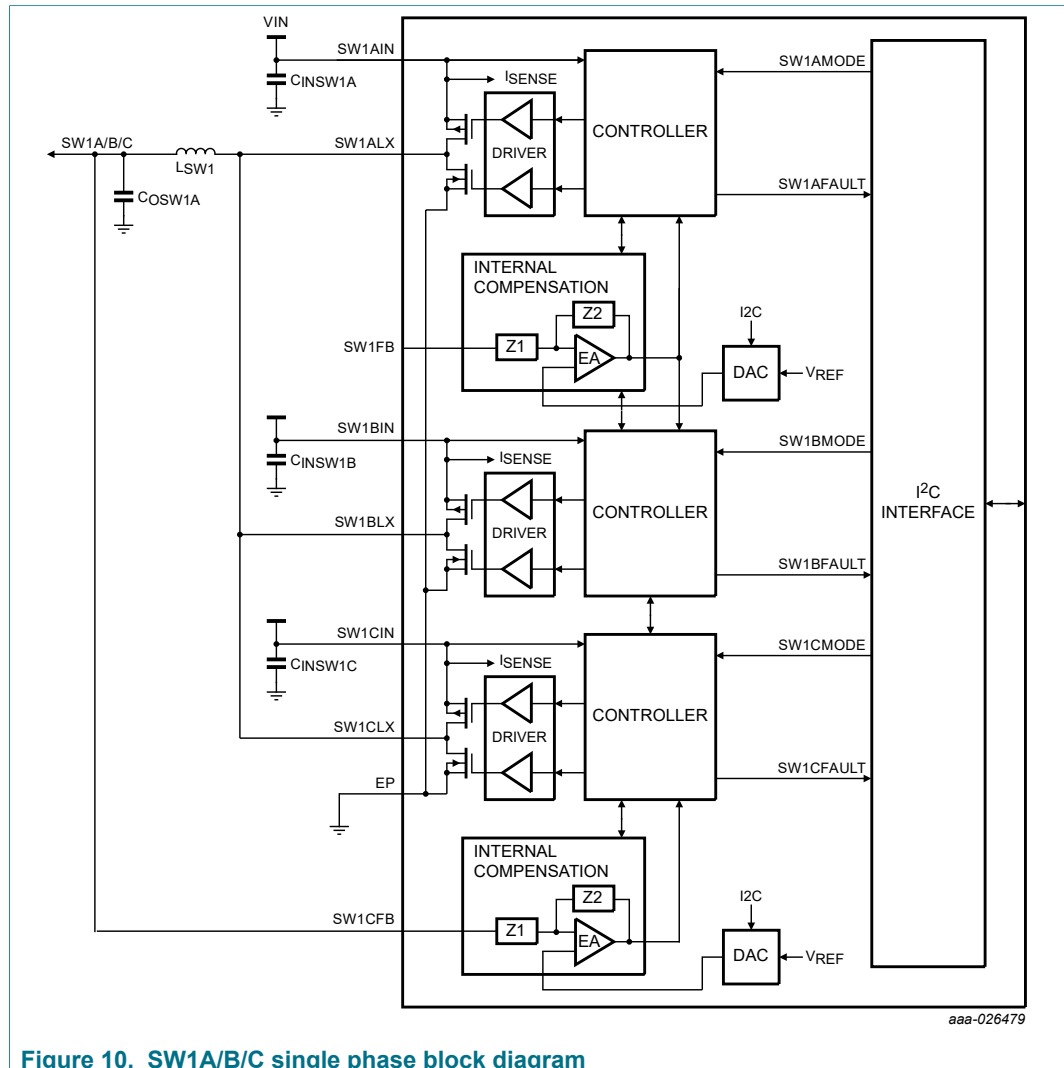
Table 38. SW1 configuration

| SW1_CONFIG[1:0] | Description                          |
|-----------------|--------------------------------------|
| 00              | A/B/C single phase                   |
| 01              | A/B single phase, C independent mode |
| 10              | A/B dual phase, C independent mode   |
| 11              | Reserved                             |

## 10.4.4.3.1 SW1A/B/C single phase

In this configuration, all phases A, B, and C are connected together to a single inductor, thus, providing up to 4.50 A current capability for high current applications. The feedback and all other controls are accomplished by use of pin SW1CFB and SW1C control registers, respectively. [Figure 10](#) shows the connection for SW1A/B/C in single phase mode.

During single phase mode operation, all three phases use the same configuration for frequency, phase, and DVS speed set in SW1CCONF register. However, the same configuration settings for frequency, phase, and DVS speed setting on SW1AB registers should be used. The SW1FB pin should be left floating in this configuration.



**Figure 10. SW1A/B/C single phase block diagram**

#### 10.4.4.3.2 SW1A/B single phase - SW1C independent mode

In this configuration, SW1A/B is connected as a single phase with a single inductor, while SW1C is used as an independent output, using its own inductor and configurations parameters. This configuration allows reduced component count by using only one inductor for SW1A/ B. As mentioned before, SW1A/B and SW1C operate independently from one another, thus, they can be operated with a different voltage set point for normal, standby, and sleep modes, as well as switching mode selection and on/off control.

[Figure 11](#) shows the physical connection for SW1A/B in single phase and SW1C as an independent output.

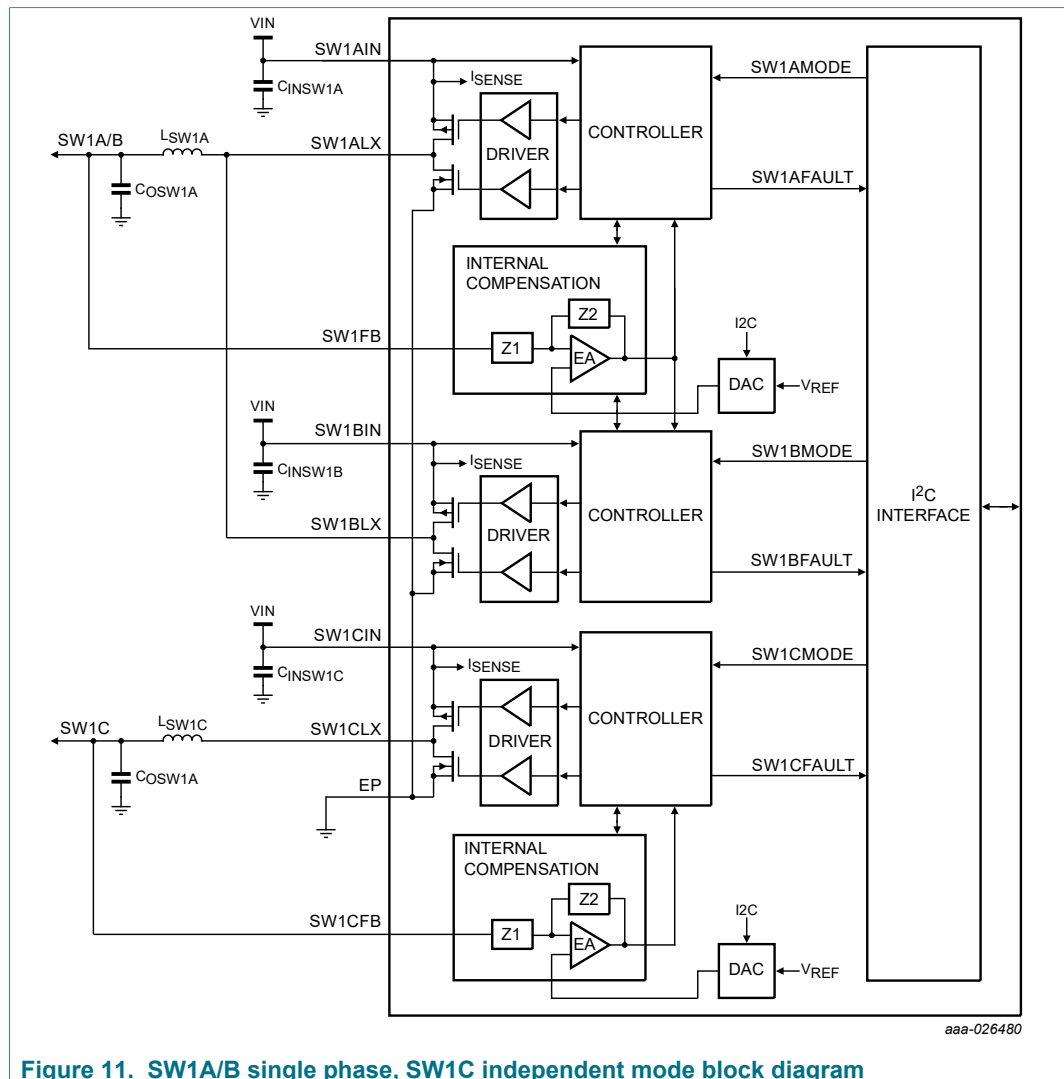


Figure 11. SW1A/B single phase, SW1C independent mode block diagram

Both SW1ALX and SW1BLX nodes operate at the same DVS, frequency, and phase configured by the SW1ABCONF register, while SW1CLX node operates independently, using the configuration in the SW1CCONF register.

#### 10.4.4.3.3 SW1A/B dual phase - SW1C independent mode

In this mode, SW1A/B is connected in dual phase mode using one inductor per switching node, while SW1C is used as an independent output using its own inductor and configuration parameters. This mode provides a smaller output voltage ripple on the SW1A/B output. SW1A/B and SW1C operate independently from one another, thus, they can be operated with a different voltage set point for normal, standby, and sleep modes, as well as switching mode selection and on/off control. Figure 12 shows the physical connection for SW1A/B in dual phase and SW1C as an independent output.

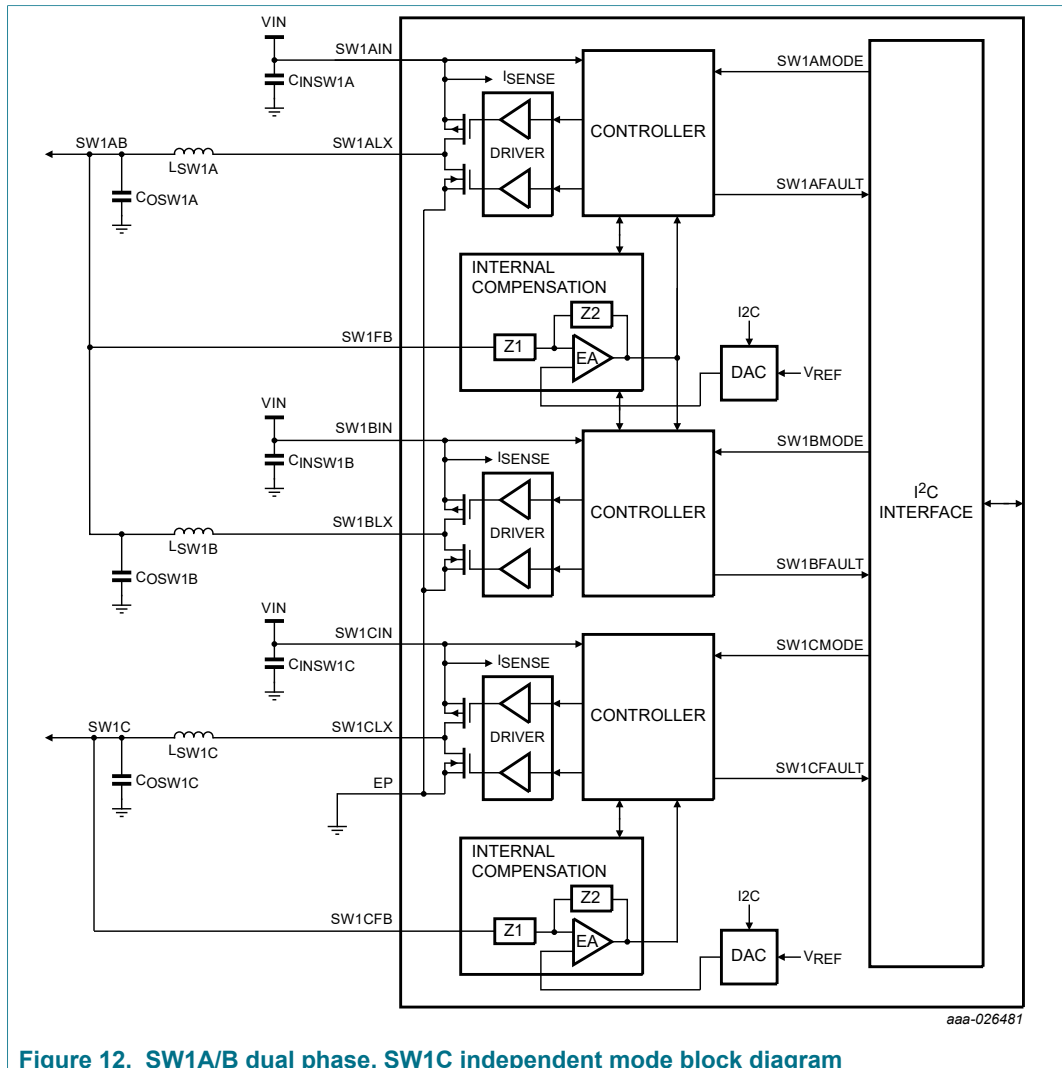


Figure 12. SW1A/B dual phase, SW1C independent mode block diagram

In this mode of operation, SW1ALX and SW1BLX nodes operate automatically at 180° phase shift from each other and use the same frequency and DVS configured by SW1ABCONF register, while SW1CLX node operate independently using the configuration in the SW1CCONF register.

#### 10.4.4.3.4 SW1A/B/C setup and control registers

SW1A/B and SW1C output voltages are programmable from 0.300 V to 1.875 V in steps of 25 mV. The output voltage set point is independently programmed for normal, standby, and sleep mode by setting the SW1x[5:0], SW1xSTBY[5:0], and SW1xOFF[5:0] bits respectively. [Table 39](#) shows the output voltage coding for SW1A/B or SW1C.

**Note:** Voltage set points of 0.6 V and below are not supported.

Table 39. SW1A/B/C output voltage configuration

| Set point | SW1x[5:0]<br>SW1xSTBY[5:0]<br>SW1xOFF[5:0] | SW1x output (V) | Set point | SW1x[5:0]<br>SW1xSTBY[5:0]<br>SW1xOFF[5:0] | SW1x output (V) |
|-----------|--|-----------------|-----------|--|-----------------|
| 0         | 000000                                     | 0.3000          | 32        | 100000                                     | 1.1000          |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Set point | SW1x[5:0]<br>SW1xSTBY[5:0]<br>SW1xOFF[5:0] | SW1x output (V) | Set point | SW1x[5:0]<br>SW1xSTBY[5:0]<br>SW1xOFF[5:0] | SW1x output (V) |
|-----------|--|-----------------|-----------|--|-----------------|
| 1         | 000001                                     | 0.3250          | 33        | 100001                                     | 1.1250          |
| 2         | 000010                                     | 0.3500          | 34        | 100010                                     | 1.1500          |
| 3         | 000011                                     | 0.3750          | 35        | 100011                                     | 1.1750          |
| 4         | 000100                                     | 0.4000          | 36        | 100100                                     | 1.2000          |
| 5         | 000101                                     | 0.4250          | 37        | 100101                                     | 1.2250          |
| 6         | 000110                                     | 0.4500          | 38        | 100110                                     | 1.2500          |
| 7         | 000111                                     | 0.4750          | 39        | 100111                                     | 1.2750          |
| 8         | 001000                                     | 0.5000          | 40        | 101000                                     | 1.3000          |
| 9         | 001001                                     | 0.5250          | 41        | 101001                                     | 1.3250          |
| 10        | 001010                                     | 0.5500          | 42        | 101010                                     | 1.3500          |
| 11        | 001011                                     | 0.5750          | 43        | 101011                                     | 1.3750          |
| 12        | 001100                                     | 0.6000          | 44        | 101100                                     | 1.4000          |
| 13        | 001101                                     | 0.6250          | 45        | 101101                                     | 1.4250          |
| 14        | 001110                                     | 0.6500          | 46        | 101110                                     | 1.4500          |
| 15        | 001111                                     | 0.6750          | 47        | 101111                                     | 1.4750          |
| 16        | 010000                                     | 0.7000          | 48        | 110000                                     | 1.5000          |
| 17        | 010001                                     | 0.7250          | 49        | 110001                                     | 1.5250          |
| 18        | 010010                                     | 0.7500          | 50        | 110010                                     | 1.5500          |
| 19        | 010011                                     | 0.7750          | 51        | 110011                                     | 1.5750          |
| 20        | 010100                                     | 0.8000          | 52        | 110100                                     | 1.6000          |
| 21        | 010101                                     | 0.8250          | 53        | 110101                                     | 1.6250          |
| 22        | 010110                                     | 0.8500          | 54        | 110110                                     | 1.6500          |
| 23        | 010111                                     | 0.8750          | 55        | 110111                                     | 1.6750          |
| 24        | 011000                                     | 0.9000          | 56        | 111000                                     | 1.7000          |
| 25        | 011001                                     | 0.9250          | 57        | 111001                                     | 1.7250          |
| 26        | 011010                                     | 0.9500          | 58        | 111010                                     | 1.7500          |
| 27        | 011011                                     | 0.9750          | 59        | 111011                                     | 1.7750          |
| 28        | 011100                                     | 1.0000          | 60        | 111100                                     | 1.8000          |
| 29        | 011101                                     | 1.0250          | 61        | 111101                                     | 1.8250          |
| 30        | 011110                                     | 1.0500          | 62        | 111110                                     | 1.8500          |
| 31        | 011111                                     | 1.0750          | 63        | 111111                                     | 1.8750          |

[Table 40](#) provides a list of registers used to configure and operate SW1A/B/C and a detailed description on each one of these register is provided in [Table 41](#) to [Table 50](#).

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 40. SW1A/B/C register summary

| Register  | Address | Output   |
|-----------|---------|--|
| SW1ABVOLT | 0x20    | SW1AB output voltage set point in normal operation |
| SW1ABSTBY | 0x21    | SW1AB output voltage set point on standby          |
| SW1ABOFF  | 0x22    | SW1AB output voltage set point on sleep            |
| SW1ABMODE | 0x23    | SW1AB switching mode selector register             |
| SW1ABCONF | 0x24    | SW1AB DVS, phase, frequency and ILIM configuration |
| SW1CVOLT  | 0x2E    | SW1C output voltage set point in normal operation  |
| SW1CSTBY  | 0x2F    | SW1C output voltage set point in standby           |
| SW1COFF   | 0x30    | SW1C output voltage set point in sleep             |
| SW1CMODE  | 0x31    | SW1C switching mode selector register              |
| SW1CCONF  | 0x32    | SW1C DVS, phase, frequency and ILIM configuration  |

Table 41. Register SW1ABVOLT - ADDR 0x20

| Name   | Bit number | R/W | Default | Description   |
|--------|------------|-----|---------|---|
| SW1AB  | 5:0        | R/W | 0x00    | Sets the SW1AB output voltage during normal operation mode. See <a href="#">Table 39</a> for all possible configurations. |
| UNUSED | 7:6        | —   | 0x00    | unused  |

Table 42. Register SW1ABSTBY – ADDR 0x21

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| SW1ABSTBY | 5:0        | R/W | 0x00    | Sets the SW1AB output voltage during standby mode. See <a href="#">Table 39</a> for all possible configurations. |
| UNUSED    | 7:6        | —   | 0x00    | unused   |

Table 43. Register SW1ABOFF – ADDR 0x22

| Name     | Bit number | R/W | Default | Description  |
|----------|------------|-----|---------|--|
| SW1ABOFF | 5:0        | R/W | 0x00    | Sets the SW1AB output voltage during sleep mode. See <a href="#">Table 39</a> for all possible configurations. |
| UNUSED   | 7:6        | —   | 0x00    | unused   |

Table 44. Register SW1ABMODE – ADDR 0x23

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| SW1ABMODE | 3:0        | R/W | 0x08    | Sets the SW1AB switching operation mode. See <a href="#">Table 29</a> for all possible configurations. |
| UNUSED    | 4          | —   | 0x00    | unused   |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name       | Bit number | R/W | Default | Description   |
|------------|------------|-----|---------|---|
| SW1ABOMODE | 5          | R/W | 0x00    | Set status of SW1AB when in sleep mode <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = PFM</li> </ul> |
| UNUSED     | 7:6        | —   | 0x00    | unused  |

Table 45. Register SW1ABCONF – ADDR 0x24

| Name          | Bit number | R/W | Default | Description   |
|---------------|------------|-----|---------|---|
| SW1ABILIM     | 0          | R/W | 0x00    | SW1AB current limit level selection <ul style="list-style-type: none"> <li>• 0 = High-level current limit</li> <li>• 1 = Low-level current limit</li> </ul> |
| UNUSED        | 1          | R/W | 0x00    | unused  |
| SW1ABFREQ     | 3:2        | R/W | 0x00    | SW1A/B switching frequency selector. See <a href="#">Table 36</a> .   |
| SW1ABPHASE    | 5:4        | R/W | 0x00    | SW1A/B phase clock selection. See <a href="#">Table 34</a> .  |
| SW1ABDVSSPEED | 7:6        | R/W | 0x00    | SW1A/B DVS speed selection. See <a href="#">Table 33</a> .  |

Table 46. Register SW1CVOLT – ADDR 0x2E

| Name   | Bit number | R/W | Default | Description  |
|--------|------------|-----|---------|--|
| SW1C   | 5:0        | R/W | 0x00    | Sets the SW1C output voltage during normal operation mode. See <a href="#">Table 39</a> for all possible configurations. |
| UNUSED | 7:6        | —   | 0x00    | unused   |

Table 47. Register SW1CSTBY – ADDR 0x2F

| Name     | Bit number | R/W | Default | Description   |
|----------|------------|-----|---------|---|
| SW1CSTBY | 5:0        | R/W | 0x00    | Sets the SW1C output voltage during standby mode. See <a href="#">Table 39</a> for all possible configurations. |
| UNUSED   | 7:6        | —   | 0x00    | unused  |

Table 48. Register SW1COFF – ADDR 0x30

| Name    | Bit number | R/W | Default | Description   |
|---------|------------|-----|---------|---|
| SW1COFF | 5:0        | R/W | 0x00    | Sets the SW1C output voltage during sleep mode. See <a href="#">Table 39</a> for all possible configurations. |
| UNUSED  | 7:6        | —   | 0x00    | unused  |

Table 49. Register SW1CMODE – ADDR 0x31

| Name     | Bit number | R/W | Default | Description   |
|----------|------------|-----|---------|---|
| SW1CMODE | 3:0        | R/W | 0x08    | Sets the SW1C switching operation mode. See <a href="#">Table 29</a> for all possible configurations. |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| UNUSED    | 4          | —   | 0x00    | unused   |
| SW1COMODE | 5          | R/W | 0x00    | Set status of SW1C when in sleep mode <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = PFM</li> </ul> |
| UNUSED    | 7:6        | —   | 0x00    | unused   |

Table 50. Register SW1CCONF – ADDR 0x32

| Name         | Bit number | R/W | Default | Description  |
|--------------|------------|-----|---------|--|
| SW1CILIM     | 0          | R/W | 0x00    | SW1C current limit level selection <ul style="list-style-type: none"> <li>• 0 = High-level current limit</li> <li>• 1 = Low-level current limit</li> </ul> |
| UNUSED       | 1          | R/W | 0x00    | unused   |
| SW1CFREQ     | 3:2        | R/W | 0x00    | SW1C switching frequency selector. See <a href="#">Table 36</a> .  |
| SW1CPHASE    | 5:4        | R/W | 0x00    | SW1C phase clock selection. See <a href="#">Table 34</a> .   |
| SW1CDVSSPEED | 7:6        | R/W | 0x00    | SW1C DVS speed selection. See <a href="#">Table 32</a> .   |

## 10.4.4.3.5 SW1A/B/C external components

Table 51. SW1A/B/C external component recommendations

| Components                         | Description                     | Mode               |                                 |                               |
|------------------------------------|---------------------------------|--------------------|---------------------------------|-------------------------------|
|                                    |                                 | A/B/C single phase | A/B single - C independent mode | A/B dual - C independent mode |
| C <sub>INSW1A</sub> <sup>[1]</sup> | SW1A input capacitor            | 4.7 µF             | 4.7 µF                          | 4.7 µF                        |
| C <sub>IN1AHF</sub> <sup>[1]</sup> | SW1A decoupling input capacitor | 0.1 µF             | 0.1 µF                          | 0.1 µF                        |
| C <sub>INSW1B</sub> <sup>[1]</sup> | SW1B input capacitor            | 4.7 µF             | 4.7 µF                          | 4.7 µF                        |
| C <sub>IN1BHF</sub> <sup>[1]</sup> | SW1B decoupling input capacitor | 0.1 µF             | 0.1 µF                          | 0.1 µF                        |
| C <sub>INSW1C</sub> <sup>[1]</sup> | SW1C input capacitor            | 4.7 µF             | 4.7 µF                          | 4.7 µF                        |
| C <sub>IN1CHF</sub>                | SW1C decoupling input capacitor | 0.1 µF             | 0.1 µF                          | 0.1 µF                        |
| C <sub>OSW1AB</sub> <sup>[1]</sup> | SW1A/B output capacitor         | 6 x 22 µF          | 2 x 22 µF                       | 4 x 22 µF                     |
| C <sub>OSW1C</sub> <sup>[1]</sup>  | SW1C output capacitor           | —                  | 3 x 22 µF                       | 3 x 22 µF                     |
| L <sub>SW1A</sub>                  | SW1A inductor                   | 1.0 µH             | 1.0 µH                          | 1.0 µH                        |
| L <sub>SW1B</sub>                  | SW1B inductor                   | —                  | —                               | 1.0 µH                        |
| L <sub>SW1C</sub>                  | SW1C inductor                   | —                  | 1.0 µH                          | 1.0 µH                        |

[1] Use X5R or X7R capacitors.

## 10.4.4.3.6 SW1A/B/C specifications

**Table 52. SW1A/B/C electrical characteristics**

All parameters are specified at  $T_{MIN}$  to  $T_{MAX}$  (see Table 4),  $V_{IN} = V_{IN_{SW1x}} = 3.6\text{ V}$ ,  $V_{SW1x} = 1.2\text{ V}$ ,  $I_{SW1x} = 100\text{ mA}$ ,  $SW1x\_PWRSTG[2:0] = [111]$ , typical external component values,  $f_{SW1x} = 2.0\text{ MHz}$ , unless otherwise noted. Typical values are characterized at  $V_{IN} = V_{IN_{SW1x}} = 3.6\text{ V}$ ,  $V_{SW1x} = 1.2\text{ V}$ ,  $I_{SW1x} = 100\text{ mA}$ ,  $SW1x\_PWRSTG[2:0] = [111]$ , and  $25\text{ }^\circ\text{C}$ , unless otherwise noted.

| Symbol  | Parameter  | Min           | Typ               | Max          | Unit          |
|---|--|---------------|-------------------|--------------|---------------|
| <b>SW1A/B/C (Single phase)</b>                        |  |               |                   |              |               |
| $V_{IN_{SW1A}}$<br>$V_{IN_{SW1B}}$<br>$V_{IN_{SW1C}}$ | Operating input voltage  | 2.8           | —                 | 4.5          | V             |
| $V_{SW1ABC}$  | Nominal output voltage   | —             | Table 39          | —            | V             |
| $V_{SW1ABCACC}$                                       | Output voltage accuracy<br>PWM, APS, $2.8\text{ V} < V_{IN} < 4.5\text{ V}$ , $0 < I_{SW1ABC} < 4.5\text{ A}$<br>$0.625\text{ V} \leq V_{SW1ABC} \leq 1.450\text{ V}$<br>$1.475\text{ V} \leq V_{SW1ABC} \leq 1.875\text{ V}$<br>PFM, steady state, $2.8\text{ V} < V_{IN} < 4.5\text{ V}$ , $0 < I_{SW1ABC} < 150\text{ mA}$<br>$0.625\text{ V} < V_{SW1ABC} < 0.675\text{ V}$<br>$0.7\text{ V} < V_{SW1ABC} < 0.85\text{ V}$<br>$0.875\text{ V} < V_{SW1ABC} < 1.875\text{ V}$ | -25<br>-3.0 % | —<br>—            | 25<br>3.0 %  | mV<br>%       |
| $I_{SW1ABC}$  | Rated output load current<br>$2.8\text{ V} < V_{IN} < 4.5\text{ V}$ , $0.625\text{ V} < V_{SW1ABC} < 1.875\text{ V}$   | —             | —                 | 4500         | mA            |
| $I_{SW1ABCLIM}$                                       | Current limiter peak current detection<br>Current through inductor<br>SW1ABILIM = 0<br>SW1ABILIM = 1   | 7.1<br>5.3    | 10.5<br>7.9       | 13.7<br>10.3 | A             |
| $V_{SW1ABCOSH}$                                       | Startup overshoot<br>$I_{SW1ABC} = 0\text{ mA}$<br>DVS clk = $25\text{ mV}/4\text{ }\mu\text{s}$ , $V_{IN} = V_{IN_{SW1x}} = 4.5\text{ V}$ , $V_{SW1ABC} = 1.875\text{ V}$   | —             | —                 | 66           | mV            |
| $t_{ON_{SW1ABC}}$                                     | Turn on time<br>Enable to 90 % of end value<br>$I_{SW1x} = 0\text{ mA}$<br>DVS clk = $25\text{ mV}/4.0\text{ }\mu\text{s}$ , $V_{IN} = V_{IN_{SW1x}} = 4.5\text{ V}$ , $V_{SW1ABC} = 1.875\text{ V}$   | —             | —                 | 500          | $\mu\text{s}$ |
| $f_{SW1ABC}$  | Switching frequency<br>SW1xFREQ[1:0] = 00<br>SW1xFREQ[1:0] = 01<br>SW1xFREQ[1:0] = 10  | —<br>—<br>—   | 1.0<br>2.0<br>4.0 | —<br>—<br>—  | MHz           |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                             | Parameter   | Min                                   | Typ                              | Max                              | Unit                     |
|------------------------------------|---|---------------------------------------|----------------------------------|----------------------------------|--------------------------|
| $\eta_{SW1ABC}$                    | Efficiency<br>$V_{IN} = 3.6\text{ V}$ , $f_{SW1ABC} = 2.0\text{ MHz}$ ,<br>$L_{SW1ABC} = 1.0\text{ }\mu\text{H}$<br>PFM, 0.9 V, 1.0 mA<br>PFM, 1.2 V, 50 mA<br>APS, PWM, 1.2 V, 850 mA<br>APS, PWM, 1.2 V, 1275 mA<br>APS, PWM, 1.2 V, 2125 mA<br>APS, PWM, 1.2 V, 4500 mA  | —<br>—<br>—<br>—<br>—<br>—            | 77<br>82<br>86<br>84<br>80<br>68 | —<br>—<br>—<br>—<br>—<br>—       | %                        |
| $\Delta V_{SW1ABC}$                | Output ripple   | —                                     | 10                               | —                                | mV                       |
| $V_{SW1ABCLIR}$                    | Line regulation (APS, PWM)  | —                                     | —                                | 20                               | mV                       |
| $V_{SW1ABCCLOR}$                   | DC load regulation (APS, PWM)   | —                                     | —                                | 20                               | mV                       |
| $V_{SW1ABCLOTR}$                   | Transient load regulation<br>Transient load = 0 to 2.25 A, $di/dt = 100\text{ mA}/\mu\text{s}$<br>Overshoot<br>Undershoot   | —<br>—                                | —<br>—                           | 50<br>50                         | mV                       |
| $I_{SW1ABCQ}$                      | Quiescent current<br>PFM mode<br>APS mode   | —<br>—                                | 18<br>145                        | —<br>—                           | $\mu\text{A}$            |
| $R_{SW1ABCDIS}$                    | Discharge resistance  | —                                     | 600                              | —                                | $\Omega$                 |
| <b>SW1A/B (Single/ dual phase)</b> |   |                                       |                                  |                                  |                          |
| $V_{INSW1A}$<br>$V_{INSW1B}$       | Operating input voltage   | 2.8                                   | —                                | 4.5                              | V                        |
| $V_{SW1AB}$                        | Nominal output voltage  | —                                     | <a href="#">Table 39</a>         | —                                | V                        |
| $V_{SW1ABACC}$                     | Output voltage accuracy<br>PWM, APS, $2.8\text{ V} < V_{IN} < 4.5\text{ V}$ , $0 < I_{SW1AB} < 2.5\text{ A}$<br>$0.625\text{ V} \leq V_{SW1AB} \leq 1.450\text{ V}$<br>$1.475\text{ V} \leq V_{SW1AB} \leq 1.875\text{ V}$<br>PFM, steady state, $2.8\text{ V} < V_{IN} < 4.5\text{ V}$ , $0 < I_{SW1AB} < 150\text{ mA}$<br>$0.625\text{ V} < V_{SW1AB} < 0.675\text{ V}$<br>$0.7\text{ V} < V_{SW1AB} < 0.85\text{ V}$<br>$0.875\text{ V} < V_{SW1AB} < 1.875\text{ V}$ | -25<br>-3.0 %<br>-65<br>-45<br>-3.0 % | —<br>—<br>—<br>—<br>—            | 25<br>3.0 %<br>65<br>45<br>3.0 % | mV<br>%<br>mV<br>mV<br>% |
| $I_{SW1AB}$                        | Rated output load current,<br>$2.8\text{ V} < V_{IN} < 4.5\text{ V}$ , $0.625\text{ V} < V_{SW1AB} < 1.875\text{ V}$  | —                                     | —                                | 2500                             | mA                       |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                   | Parameter   | Min | Typ | Max | Unit |
|--------------------------|---|-----|-----|-----|------|
| I <sub>SW1ABLIM</sub>    | Current limiter peak current detection                    |     |     |     | A    |
|                          | SW1A/B single phase (current through inductor)            | 4.5 | 6.5 | 8.5 |      |
|                          | SW1ABILIM = 0   | 3.3 | 4.9 | 6.4 |      |
|                          | SW1ABILIM = 1   | 2.2 | 3.2 | 4.3 |      |
| V <sub>SW1ABOSH</sub>    | Start-up overshoot  |     |     |     | mV   |
|                          | I <sub>SW1AB</sub> = 0.0 mA                               |     |     | 66  |      |
|                          | DVS clk = 25 mV/4 μs, V <sub>IN</sub> =                   | —   | —   |     |      |
|                          | V <sub>INSW1X</sub> = 4.5 V, V <sub>SW1AB</sub> = 1.875 V |     |     |     |      |
| t <sub>ONSW1AB</sub>     | Turn-on time  |     |     |     | μs   |
|                          | Enable to 90 % of end value                               | —   | —   | 500 |      |
|                          | I <sub>SW1AB</sub> = 0.0 mA                               |     |     |     |      |
|                          | DVS clk = 25 mV/4 μs, V <sub>IN</sub> =                   |     |     |     |      |
| f <sub>SW1AB</sub>       | Switching frequency                                       |     |     |     | MHz  |
|                          | SW1ABFREQ[1:0] = 00                                       | —   | 1.0 | —   |      |
|                          | SW1ABFREQ[1:0] = 01                                       | —   | 2.0 | —   |      |
|                          | SW1ABFREQ[1:0] = 10                                       | —   | 4.0 | —   |      |
| η <sub>SW1AB</sub>       | Efficiency (single phase)                                 |     |     |     | %    |
|                          | V <sub>IN</sub> = 3.6 V, f <sub>SW1AB</sub> = 2.0 MHz,    |     | 82  | —   |      |
|                          | L <sub>SW1AB</sub> = 1.0 μH                               |     |     |     |      |
|                          | PFM, 0.9 V, 1.0 mA  | —   | 84  | —   |      |
|                          | PFM, 1.2 V, 50 mA   | —   | 86  | —   |      |
|                          | APS, PWM, 1.2 V, 500 mA                                   | —   | 87  | —   |      |
|                          | APS, PWM, 1.2 V, 750 mA                                   | —   | 82  | —   |      |
|                          | APS, PWM, 1.2 V, 1250 mA                                  | —   | 71  | —   |      |
| APS, PWM, 1.2 V, 2500 mA | —   |     |     |     |      |
| ΔV <sub>SW1AB</sub>      | Output ripple   | —   | 10  | —   | mV   |
| V <sub>SW1ABLIR</sub>    | Line regulation (APS, PWM)                                | —   | —   | 20  | mV   |
| V <sub>SW1ABLOR</sub>    | DC load regulation (APS, PWM)                             | —   | —   | 20  | mV   |
| V <sub>SW1ABLOTR</sub>   | Transient load regulation                                 |     |     |     | mV   |
|                          | Transient load = 0 to 1.25 A, di/dt = 100 μs              | —   | —   | 50  |      |
|                          | Overshoot   | —   | —   | 50  |      |
| I <sub>SW1ABQ</sub>      | Quiescent current   |     |     |     | μA   |
|                          | PFM mode  | —   | 18  | —   |      |
|                          | APS mode  | —   | 235 | —   |      |
| R <sub>ONSW1AP</sub>     | SW1A P-MOSFET R <sub>DS(on)</sub>                         |     |     |     | mΩ   |
|                          | V <sub>INSW1A</sub> = 3.3 V                               | —   | 215 | 245 |      |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                    | Parameter   | Min           | Typ        | Max         | Unit    |
|---------------------------|---|---------------|------------|-------------|---------|
| R <sub>ONSW1AN</sub>      | SW1A N-MOSFET R <sub>DS(on)</sub><br>V <sub>INSW1A</sub> = 3.3 V  | —             | 258        | 326         | mΩ      |
| I <sub>SW1APQ</sub>       | SW1A P-MOSFET leakage current<br>V <sub>INSW1A</sub> = 4.5 V  | —             | —          | 7.5         | μA      |
| I <sub>SW1ANQ</sub>       | SW1A N-MOSFET leakage current<br>V <sub>INSW1A</sub> = 4.5 V  | —             | —          | 2.5         | μA      |
| R <sub>ONSW1BP</sub>      | SW1B P-MOSFET R <sub>DS(on)</sub><br>V <sub>INSW1B</sub> = 3.3 V  | —             | 215        | 245         | mΩ      |
| R <sub>ONSW1BN</sub>      | SW1B N-MOSFET R <sub>DS(on)</sub><br>V <sub>INSW1B</sub> = 3.3 V  | —             | 258        | 326         | mΩ      |
| I <sub>SW1BPQ</sub>       | SW1B P-MOSFET leakage current<br>V <sub>INSW1B</sub> = 4.5 V  | —             | —          | 7.5         | μA      |
| I <sub>SW1BNQ</sub>       | SW1B N-MOSFET leakage current<br>V <sub>INSW1B</sub> = 4.5 V  | —             | —          | 2.5         | μA      |
| R <sub>SW1ABDIS</sub>     | Discharge resistance  | —             | 600        | —           | Ω       |
| <b>SW1C (independent)</b> |   |               |            |             |         |
| V <sub>INSW1C</sub>       | Operating input voltage   | 2.8           | —          | 4.5         | V       |
| V <sub>SW1C</sub>         | Nominal output voltage  | —             | Table 39   | —           | V       |
| V <sub>SW1CACC</sub>      | Output voltage accuracy<br>PWM, APS, 2.8 V < V <sub>IN</sub> < 4.5 V, 0 < I <sub>SW1C</sub> < 2.0 A<br>0.625 V ≤ V <sub>SW1C</sub> ≤ 1.450 V<br>1.475 V ≤ V <sub>SW1C</sub> ≤ 1.875 V<br>PFM, steady state 2.8 V < V <sub>IN</sub> < 4.5 V, 0 < I <sub>SW1C</sub> < 50 mA<br>0.625 V < V <sub>SW1C</sub> < 0.675 V<br>0.7 V < V <sub>SW1C</sub> < 0.85 V<br>0.875 V < V <sub>SW1C</sub> < 1.875 V | -25<br>-3.0 % | —<br>—     | 25<br>3.0 % | mV<br>% |
| I <sub>SW1C</sub>         | Rated output load current<br>2.8 V < V <sub>IN</sub> < 4.5 V, 0.625 V < V <sub>SW1C</sub> < 1.875 V   | —             | —          | 2000        | mA      |
| I <sub>SW1CLIM</sub>      | Current limiter peak current detection<br>Current through inductor<br>SW1CILIM = 0<br>SW1CILIM = 1  | 2.6<br>1.95   | 4.0<br>3.0 | 5.2<br>3.9  | A       |
| V <sub>SW1COSH</sub>      | Start up overshoot<br>I <sub>SW1C</sub> = 0 mA<br>DVS clk = 25 mV/4 μs, V <sub>IN</sub> = V <sub>INSW1C</sub> = 4.5 V, V <sub>SW1C</sub> = 1.875 V  | —             | —          | 66          | mV      |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol            | Parameter  | Min                        | Typ                              | Max                        | Unit       |
|-------------------|--|----------------------------|----------------------------------|----------------------------|------------|
| $t_{ON_{SW1C}}$   | Turn on time<br>Enable to 90 % of end value<br>$I_{SW1C} = 0$ mA<br>DVS clk = 25 mV/4 $\mu$ s, $V_{IN}$<br>= $V_{IN_{SW1C}} = 4.5$ V, $V_{SW1C} =$<br>1.875 V  | —                          | —                                | 500                        | $\mu$ s    |
| $f_{SW1C}$        | Switching frequency<br>SW1CFREQ[1:0] = 00<br>SW1CFREQ[1:0] = 01<br>SW1CFREQ[1:0] = 10  | —<br>—<br>—                | 1.0<br>2.0<br>4.0                | —<br>—<br>—                | MHz        |
| $\eta_{SW1C}$     | Efficiency<br>$V_{IN} = 3.6$ V, $f_{SW1C} = 2.0$ MHz,<br>$L_{SW1C} = 1.0$ $\mu$ H<br>PFM, 0.9 V, 1.0 mA<br>PFM, 1.2 V, 50 mA<br>APS, PWM, 1.2 V, 400 mA<br>APS, PWM, 1.2 V, 600 mA<br>APS, PWM, 1.2 V, 1000 mA<br>APS, PWM, 1.2 V, 2000 mA | —<br>—<br>—<br>—<br>—<br>— | 77<br>78<br>86<br>84<br>78<br>65 | —<br>—<br>—<br>—<br>—<br>— | %          |
| $\Delta V_{SW1C}$ | Output ripple  | —                          | 10                               | —                          | mV         |
| $V_{SW1CLR}$      | Line regulation (APS, PWM)   | —                          | —                                | 20                         | mV         |
| $V_{SW1CLOR}$     | DC load regulation (APS, PWM)  | —                          | —                                | 20                         | mV         |
| $V_{SW1CLOTR}$    | Transient load regulation<br>Transient load = 0.0 mA to 1.0 A,<br>$di/dt = 100$ mA/ $\mu$ s<br>Overshoot<br>Undershoot   | —<br>—                     | —<br>—                           | 50<br>50                   | mV         |
| $I_{SW1CQ}$       | Quiescent current<br>PFM mode<br>APS mode  | —<br>—                     | 22<br>145                        | —<br>—                     | $\mu$ A    |
| $R_{ON_{SW1CP}}$  | SW1C P-MOSFET $R_{DS(on)}$<br>at $V_{IN_{SW1C}} = 3.3$ V   | —                          | 184                              | 206                        | m $\Omega$ |
| $R_{ON_{SW1CN}}$  | SW1C N-MOSFET $R_{DS(on)}$<br>at $V_{IN_{SW1C}} = 3.3$ V   | —                          | 211                              | 260                        | m $\Omega$ |
| $I_{SW1CPQ}$      | SW1C P-MOSFET leakage current<br>$V_{IN_{SW1C}} = 4.5$ V   | —                          | —                                | 10.5                       | $\mu$ A    |
| $I_{SW1CNQ}$      | SW1C N-MOSFET leakage current<br>$V_{IN_{SW1C}} = 4.5$ V   | —                          | —                                | 3.5                        | $\mu$ A    |
| $R_{SW1CDIS}$     | Discharge resistance   | —                          | 600                              | —                          | $\Omega$   |

14-channel power management integrated circuit (PMIC) for audio/video applications

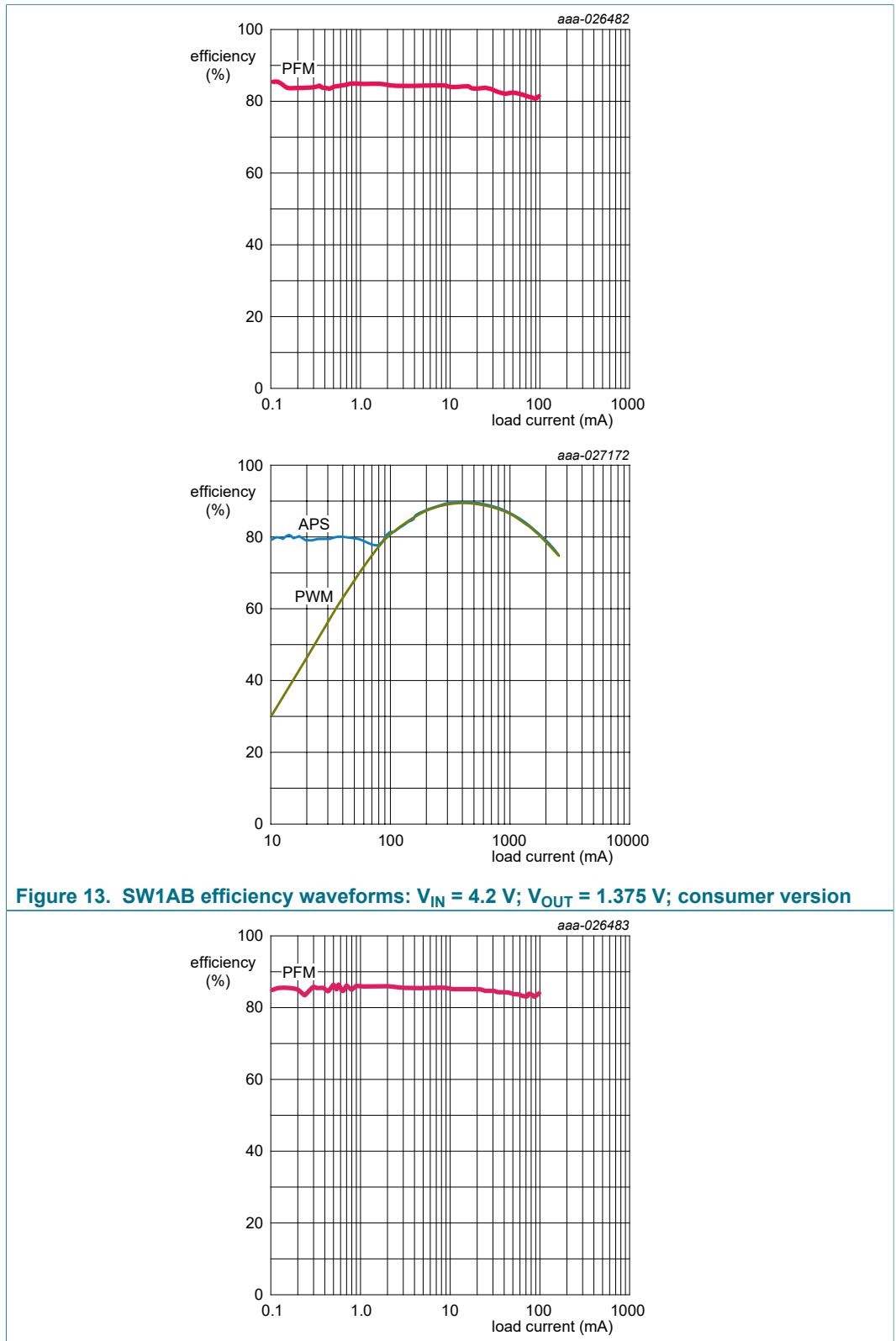


Figure 13. SW1AB efficiency waveforms:  $V_{IN} = 4.2\text{ V}$ ;  $V_{OUT} = 1.375\text{ V}$ ; consumer version

14-channel power management integrated circuit (PMIC) for audio/video applications

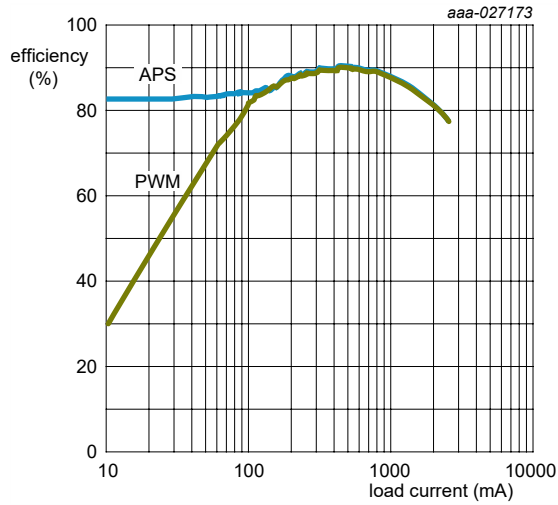


Figure 14. SW1AB efficiency waveforms:  $V_{IN} = 4.2\text{ V}$ ;  $V_{OUT} = 1.375\text{ V}$ ; industrial version

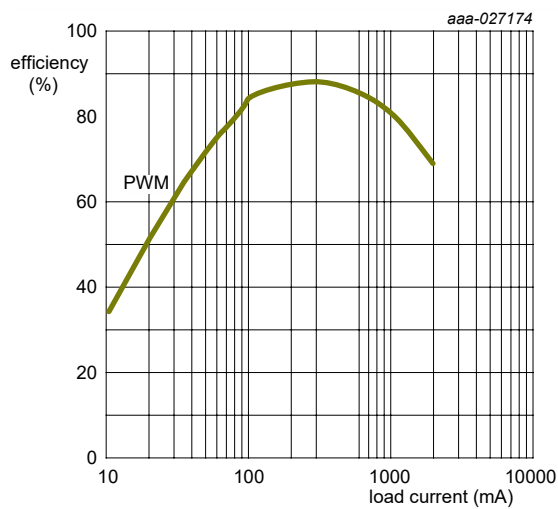
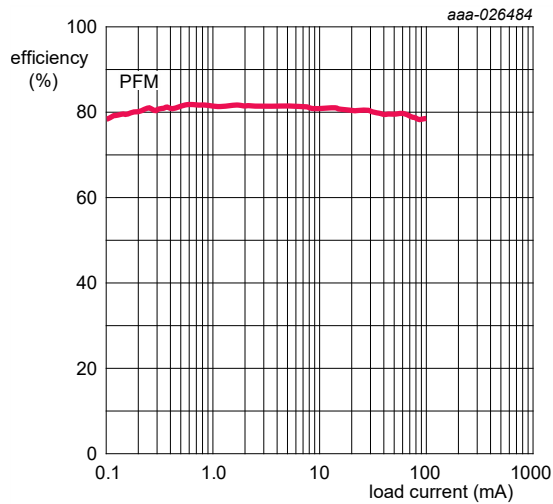
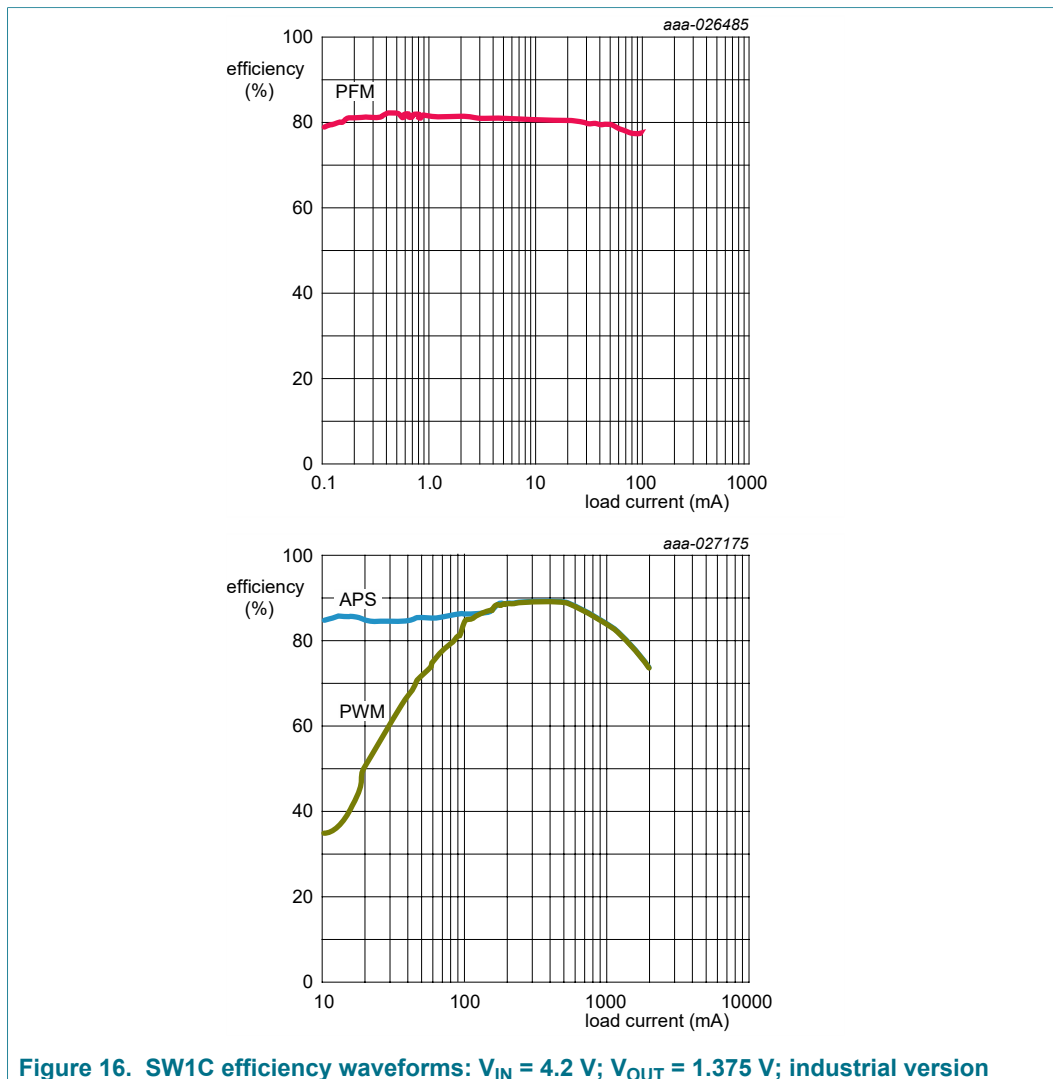


Figure 15. SW1C efficiency waveforms:  $V_{IN} = 4.2\text{ V}$ ;  $V_{OUT} = 1.375\text{ V}$ ; consumer version



#### 10.4.4.4 SW2

SW2 is a single phase, 2.5 A rated buck regulator. [Table 28](#) describes the modes, and [Table 29](#) shows the options for the SWxMODE[3:0] bits.

[Figure 17](#) shows the block diagram and the external component connections for SW2 regulator.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

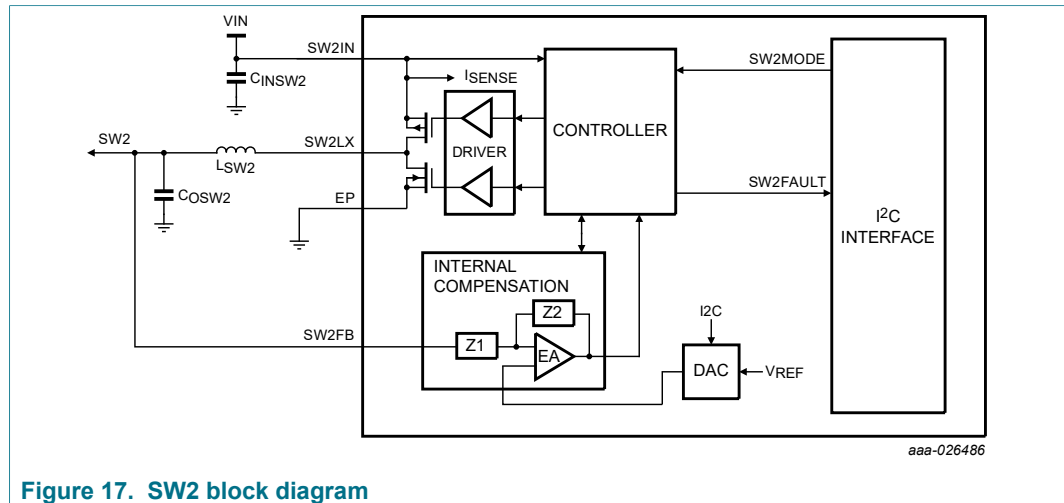


Figure 17. SW2 block diagram

## 10.4.4.4.1 SW2 setup and control registers

SW2 output voltage is programmable from 0.400 V to 3.300 V; however, bit SW2[6] in register SW2VOLT is read-only during normal operation. Its value is determined by the default configuration, or may be changed by using the OTP registers. Therefore, once SW2[6] is set to 0, the output is limited to the lower output voltage range from 0.400 V to 1.975 V with 25 mV increments, as determined by bits SW2[5:0]. Likewise, once bit SW2[6] is set to 1, the output voltage is limited to the higher output voltage range from 0.800 V to 3.300 V with 50 mV increments, as determined by bits SW2[5:0].

In order to optimize the performance of the regulator, it is recommended only voltage from 2.000 V to 3.300 V be used in the high range, and the lower range be used for voltage from 0.400 V to 1.975 V.

The output voltage set point is independently programmed for normal, standby, and sleep mode by setting the SW2[5:0], SW2STBY[5:0] and SW2OFF[5:0] bits, respectively. However, the initial state of bit SW2[6] are copied into bits SW2STBY[6], and SW2OFF[6] bits. Therefore, the output voltage range remains the same in all three operating modes. [Table 53](#) shows the output voltage coding valid for SW2.

**Note:** Voltage set points of 0.6 V and below are not supported.

Table 53. SW2 output voltage configuration

| Low output voltage range <sup>[1]</sup> |          |            | High output voltage range |          |            |
|---|----------|------------|---------------------------|----------|------------|
| Set point                               | SW2[6:0] | SW2 output | Set point                 | SW2[6:0] | SW2 output |
| 0                                       | 0000000  | 0.4000     | 64                        | 1000000  | 0.8000     |
| 1                                       | 0000001  | 0.4250     | 65                        | 1000001  | 0.8500     |
| 2                                       | 0000010  | 0.4500     | 66                        | 1000010  | 0.9000     |
| 3                                       | 0000011  | 0.4750     | 67                        | 1000011  | 0.9500     |
| 4                                       | 0000100  | 0.5000     | 68                        | 1000100  | 1.0000     |
| 5                                       | 0000101  | 0.5250     | 69                        | 1000101  | 1.0500     |
| 6                                       | 0000110  | 0.5500     | 70                        | 1000110  | 1.1000     |
| 7                                       | 0000111  | 0.5750     | 71                        | 1000111  | 1.1500     |
| 8                                       | 0001000  | 0.6000     | 72                        | 1001000  | 1.2000     |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Low output voltage range <sup>[1]</sup> |          |            | High output voltage range |          |            |
|---|----------|------------|---------------------------|----------|------------|
| Set point                               | SW2[6:0] | SW2 output | Set point                 | SW2[6:0] | SW2 output |
| 9                                       | 0001001  | 0.6250     | 73                        | 1001001  | 1.2500     |
| 10                                      | 0001010  | 0.6500     | 74                        | 1001010  | 1.3000     |
| 11                                      | 0001011  | 0.6750     | 75                        | 1001011  | 1.3500     |
| 12                                      | 0001100  | 0.7000     | 76                        | 1001100  | 1.4000     |
| 13                                      | 0001101  | 0.7250     | 77                        | 1001101  | 1.4500     |
| 14                                      | 0001110  | 0.7500     | 78                        | 1001110  | 1.5000     |
| 15                                      | 0001111  | 0.7750     | 79                        | 1001111  | 1.5500     |
| 16                                      | 0010000  | 0.8000     | 80                        | 1010000  | 1.6000     |
| 17                                      | 0010001  | 0.8250     | 81                        | 1010001  | 1.6500     |
| 18                                      | 0010010  | 0.8500     | 82                        | 1010010  | 1.7000     |
| 19                                      | 0010011  | 0.8750     | 83                        | 1010011  | 1.7500     |
| 20                                      | 0010100  | 0.9000     | 84                        | 1010100  | 1.8000     |
| 21                                      | 0010101  | 0.9250     | 85                        | 1010101  | 1.8500     |
| 22                                      | 0010110  | 0.9500     | 86                        | 1010110  | 1.9000     |
| 23                                      | 0010111  | 0.9750     | 87                        | 1010111  | 1.9500     |
| 24                                      | 0011000  | 1.0000     | 88                        | 1011000  | 2.0000     |
| 25                                      | 0011001  | 1.0250     | 89                        | 1011001  | 2.0500     |
| 26                                      | 0011010  | 1.0500     | 90                        | 1011010  | 2.1000     |
| 27                                      | 0011011  | 1.0750     | 91                        | 1011011  | 2.1500     |
| 28                                      | 0011100  | 1.1000     | 92                        | 1011100  | 2.2000     |
| 29                                      | 0011101  | 1.1250     | 93                        | 1011101  | 2.2500     |
| 30                                      | 0011110  | 1.1500     | 94                        | 1011110  | 2.3000     |
| 31                                      | 0011111  | 1.1750     | 95                        | 1011111  | 2.3500     |
| 32                                      | 0100000  | 1.2000     | 96                        | 1100000  | 2.4000     |
| 33                                      | 0100001  | 1.2250     | 97                        | 1100001  | 2.4500     |
| 34                                      | 0100010  | 1.2500     | 98                        | 1100010  | 2.5000     |
| 35                                      | 0100011  | 1.2750     | 99                        | 1100011  | 2.5500     |
| 36                                      | 0100100  | 1.3000     | 100                       | 1100100  | 2.6000     |
| 37                                      | 0100101  | 1.3250     | 101                       | 1100101  | 2.6500     |
| 38                                      | 0100110  | 1.3500     | 102                       | 1100110  | 2.7000     |
| 39                                      | 0100111  | 1.3750     | 103                       | 1100111  | 2.7500     |
| 40                                      | 0101000  | 1.4000     | 104                       | 1101000  | 2.8000     |
| 41                                      | 0101001  | 1.4250     | 105                       | 1101001  | 2.8500     |
| 42                                      | 0101010  | 1.4500     | 106                       | 1101010  | 2.9000     |
| 43                                      | 0101011  | 1.4750     | 107                       | 1101011  | 2.9500     |
| 44                                      | 0101100  | 1.5000     | 108                       | 1101100  | 3.0000     |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Low output voltage range <sup>[1]</sup> |          |            | High output voltage range |          |            |
|---|----------|------------|---------------------------|----------|------------|
| Set point                               | SW2[6:0] | SW2 output | Set point                 | SW2[6:0] | SW2 output |
| 45                                      | 0101101  | 1.5250     | 109                       | 1101101  | 3.0500     |
| 46                                      | 0101110  | 1.5500     | 110                       | 1101110  | 3.1000     |
| 47                                      | 0101111  | 1.5750     | 111                       | 1101111  | 3.1500     |
| 48                                      | 0110000  | 1.6000     | 112                       | 1110000  | 3.2000     |
| 49                                      | 0110001  | 1.6250     | 113                       | 1110001  | 3.2500     |
| 50                                      | 0110010  | 1.6500     | 114                       | 1110010  | 3.3000     |
| 51                                      | 0110011  | 1.6750     | 115                       | 1110011  | Reserved   |
| 52                                      | 0110100  | 1.7000     | 116                       | 1110100  | Reserved   |
| 53                                      | 0110101  | 1.7250     | 117                       | 1110101  | Reserved   |
| 54                                      | 0110110  | 1.7500     | 118                       | 1110110  | Reserved   |
| 55                                      | 0110111  | 1.7750     | 119                       | 1110111  | Reserved   |
| 56                                      | 0111000  | 1.8000     | 120                       | 1111000  | Reserved   |
| 57                                      | 0111001  | 1.8250     | 121                       | 1111001  | Reserved   |
| 58                                      | 0111010  | 1.8500     | 122                       | 1111010  | Reserved   |
| 59                                      | 0111011  | 1.8750     | 123                       | 1111011  | Reserved   |
| 60                                      | 0111100  | 1.9000     | 124                       | 1111100  | Reserved   |
| 61                                      | 0111101  | 1.9250     | 125                       | 1111101  | Reserved   |
| 62                                      | 0111110  | 1.9500     | 126                       | 1111110  | Reserved   |
| 63                                      | 0111111  | 1.9750     | 127                       | 1111111  | Reserved   |

[1] For voltage less than 2.0 V, use set points 0 to 63.

Setup and control of SW2 is done through I<sup>2</sup>C registers listed in [Table 54](#), and a detailed description of each one of the registers is provided in [Table 55](#) to [Table 59](#).

**Table 54. SW2 register summary**

| Register | Address | Description                                   |
|----------|---------|---|
| SW2VOLT  | 0x35    | Output voltage set point in normal operation  |
| SW2STBY  | 0x36    | Output voltage set point in standby           |
| SW2OFF   | 0x37    | Output voltage set point in sleep             |
| SW2MODE  | 0x38    | Switching mode selector register              |
| SW2CONF  | 0x39    | DVS, phase, frequency, and ILIM configuration |

**Table 55. Register SW2VOLT - ADDR 0x35**

| Name | Bit number | R/W | Default | Description   |
|------|------------|-----|---------|---|
| SW2  | 5:0        | R/W | 0x00    | Sets the SW2 output voltage during normal operation mode. See <a href="#">Table 53</a> for all possible configurations. |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name   | Bit number | R/W | Default | Description  |
|--------|------------|-----|---------|--|
| SW2    | 6          | R   | 0x00    | Sets the operating output voltage range for SW2. Set during OTP or TBB configuration only. See <a href="#">Table 53</a> for all possible configurations. |
| UNUSED | 7          | —   | 0x00    | unused   |

Table 56. Register SW2STBY - ADDR 0x36

| Name    | Bit number | R/W | Default | Description  |
|---------|------------|-----|---------|--|
| SW2STBY | 5:0        | R/W | 0x00    | Sets the SW2 output voltage during standby mode. See <a href="#">Table 53</a> for all possible configurations.   |
| SW2STBY | 6          | R   | 0x00    | Sets the operating output voltage range for SW2 in standby mode. This bit inherits the value configured on bit SW2[6] during OTP or TBB configuration. See <a href="#">Table 53</a> for all possible configurations. |
| UNUSED  | 7          | —   | 0x00    | unused   |

Table 57. Register SW2OFF - ADDR 0x37

| Name   | Bit number | R/W | Default | Description  |
|--------|------------|-----|---------|--|
| SW2OFF | 5:0        | R/W | 0x00    | Sets the SW2 output voltage during sleep mode. See <a href="#">Table 53</a> for all possible configurations.   |
| SW2OFF | 6          | R   | 0x00    | Sets the operating output voltage range for SW2 in sleep mode. This bit inherits the value configured on bit SW2[6] during OTP or TBB configuration. See <a href="#">Table 53</a> for all possible configurations. |
| UNUSED | 7          | —   | 0x00    | unused   |

Table 58. Register SW2MODE - ADDR 0x38

| Name     | Bit number | R/W | Default | Description   |
|----------|------------|-----|---------|---|
| SW2MODE  | 3:0        | R/W | 0x08    | Sets the SW2 switching operation mode. See <a href="#">Table 29</a> for all possible configurations.                |
| UNUSED   | 4          | —   | 0x00    | unused  |
| SW2OMODE | 5          | R/W | 0x00    | Set status of SW2 when in sleep mode <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = PFM</li> </ul> |
| UNUSED   | 7:6        | —   | 0x00    | unused  |

Table 59. Register SW2CONF - ADDR 0x39

| Name    | Bit number | R/W | Default | Description  |
|---------|------------|-----|---------|--|
| SW2ILIM | 0          | R/W | 0x00    | SW2 current limit level selection <sup>[1]</sup> <ul style="list-style-type: none"> <li>• 0 = High-level current limit</li> <li>• 1 = Low-level current limit</li> </ul> |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name        | Bit number | R/W | Default | Description  |
|-------------|------------|-----|---------|--|
| UNUSED      | 1          | R/W | 0x00    | unused   |
| SW2FREQ     | 3:2        | R/W | 0x00    | SW2 switching frequency selector. See <a href="#">Table 36</a> . |
| SW2PHASE    | 5:4        | R/W | 0x00    | SW2 phase clock selection. See <a href="#">Table 34</a> .        |
| SW2DVSSPEED | 7:6        | R/W | 0x00    | SW2 DVS speed selection. See <a href="#">Table 33</a> .          |

[1] SW2ILIM = 0 must be used if 2.5 A output load current is desired

## 10.4.4.4.2 SW2 external components

Table 60. SW2 external component recommendations

| Components      | Description                    | Values         |
|-----------------|--------------------------------|----------------|
| $C_{INSW2}$ [1] | SW2 input capacitor            | 4.7 $\mu$ F    |
| $C_{IN2HF}$ [1] | SW2 decoupling input capacitor | 0.1 $\mu$ F    |
| $C_{OSW2}$ [1]  | SW2 output capacitor           | 3 x 22 $\mu$ F |
| $L_{SW2}$       | SW2 inductor                   | 1.0 $\mu$ H    |

[1] Use X5R or X7R capacitors.

## 10.4.4.4.3 SW2 Specifications

Table 61. SW2 electrical characteristics

All parameters are specified at  $T_{MIN}$  to  $T_{MAX}$  (see [Table 4](#)),  $V_{IN} = V_{INSW2} = 3.6$  V,  $V_{SW2} = 3.15$  V,  $I_{SW2} = 100$  mA,  $SW2\_PWRSTG[2:0] = [111]$ , typical external component values,  $f_{SW2} = 2.0$  MHz, unless otherwise noted. Typical values are characterized at  $V_{IN} = V_{INSW2} = 3.6$  V,  $V_{SW2} = 3.15$  V,  $I_{SW2} = 100$  mA,  $SW2\_PWRSTG[2:0] = [111]$ , and 25 °C, unless otherwise noted.

| Symbol                        | Parameter  | Min    | Typ                      | Max   | Unit |
|-------------------------------|--|--------|--------------------------|-------|------|
| <b>SWITCH MODE SUPPLY SW2</b> |  |        |                          |       |      |
| $V_{INSW2}$                   | Operating input voltage [1]  | 2.8    | —                        | 4.5   | V    |
| $V_{SW2}$                     | Nominal output voltage   | —      | <a href="#">Table 53</a> | —     | V    |
| $V_{SW2ACC}$                  | Output voltage accuracy<br>PWM, APS, $2.8$ V < $V_{IN}$ < $4.5$ V, $0$ < $I_{SW2}$ < $2.5$ A | -25    | —                        | 25    | mV   |
|                               | $0.625$ V < $V_{SW2}$ < $0.85$ V   | -3.0 % | —                        | 3.0 % | %    |
|                               | $0.875$ V < $V_{SW2}$ < $1.975$  | -6.0 % | —                        | 6.0 % | %    |
|                               | $2.0$ V < $V_{SW2}$ < $3.3$ V  | —      | —                        | —     | —    |
|                               | PFM, $2.8$ V < $V_{IN}$ < $4.5$ V, $0$ < $I_{SW2} \leq 50$ mA                                | -65    | —                        | 65    | mV   |
|                               | $0.625$ V < $V_{SW2}$ < $0.675$ V  | -45    | —                        | 45    | mV   |
|                               | $0.7$ V < $V_{SW2}$ < $0.85$ V   | -3.0 % | —                        | 3.0 % | %    |
| $I_{SW2}$                     | Rated output load current [2]  | —      | —                        | 2500  | mA   |
|                               | $2.8$ V < $V_{IN}$ < $4.5$ V, $0.625$ V < $V_{SW2}$ < $3.3$ V                                | —      | —                        | —     | —    |
|                               | $2.8$ V < $V_{IN}$ < $4.5$ V, $1.2$ V < $V_{SW2}$ < $3.3$ V, $SW2LIM = 0$                    | —      | —                        | —     | —    |
|                               | —  | —      | —                        | —     | —    |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol               | Parameter  | Min        | Typ        | Max        | Unit |
|----------------------|--|------------|------------|------------|------|
| I <sub>SW2LIM</sub>  | Current limiter peak current detection   |            |            |            | A    |
|                      | Current through inductor<br>SW2ILIM = 0<br>SW2ILIM = 1   | 2.8<br>2.1 | 4.0<br>3.0 | 5.2<br>3.9 |      |
| V <sub>SW2OSH</sub>  | Startup overshoot<br>I <sub>SW2</sub> = 0.0 mA<br>DVS clk = 25 mV/4 μs, V <sub>IN</sub> = V <sub>INSW2</sub> = 4.5 V                           | —          | —          | 66         | mV   |
| t <sub>ONSW2</sub>   | Turn on time<br>Enable to 90 % of end value<br>I <sub>SW2</sub> = 0.0 mA<br>DVS clk = 50 mV/8 μs, V <sub>IN</sub> = V <sub>INSW2</sub> = 4.5 V | —          | —          | 550        | μs   |
| f <sub>SW2</sub>     | Switching frequency  |            |            |            | MHz  |
|                      | SW2FREQ[1:0] = 00  | —          | 1.0        | —          |      |
|                      | SW2FREQ[1:0] = 01<br>SW2FREQ[1:0] = 10   | —<br>—     | 2.0<br>4.0 | —<br>—     |      |
| η <sub>SW2</sub>     | Efficiency   |            |            |            | %    |
|                      | V <sub>IN</sub> = 3.6 V, f <sub>SW2</sub> = 2.0 MHz, L <sub>SW2</sub> = 1.0 μH   |            |            |            |      |
|                      | PFM, 3.15 V, 1.0 mA  | —          | 94         | —          |      |
|                      | PFM, 3.15 V, 50 mA   | —          | 95         | —          |      |
|                      | APS, PWM, 3.15 V, 400 mA   | —          | 96         | —          |      |
|                      | APS, PWM, 3.15 V, 600 mA   | —          | 94         | —          |      |
|                      | APS, PWM, 3.15 V, 1000 mA  | —          | 92         | —          |      |
|                      | APS, PWM, 3.15 V, 2000 mA<br>APS, PWM, 3.15 V, 2500 mA   | —<br>—     | 86<br>81   | —<br>—     |      |
| ΔV <sub>SW2</sub>    | Output ripple  | —          | 10         | —          | mV   |
| V <sub>SW2LIR</sub>  | Line regulation (APS, PWM)   | —          | —          | 20         | mV   |
| V <sub>SW2LOR</sub>  | DC load regulation (APS, PWM)  | —          | —          | 20         | mV   |
| V <sub>SW2LOTR</sub> | Transient load regulation  |            |            |            | mV   |
|                      | Transient load = 0.0 mA to 1.0 A, di/dt = 100 mA/μs  | —          | —          | 50         |      |
|                      | Overshoot<br>Undershoot  | —<br>—     | —<br>—     | 50<br>50   |      |
| I <sub>SW2Q</sub>    | Quiescent current  |            |            |            | μA   |
|                      | PFM mode   | —          | 23         | —          |      |
|                      | APS mode (low output voltage settings)<br>APS mode (high output voltage settings)  | —<br>—     | 145<br>305 | —<br>—     |      |
| R <sub>ONSW2P</sub>  | SW2 P-MOSFET R <sub>DS(on)</sub><br>at V <sub>IN</sub> = V <sub>INSW2</sub> = 3.3 V  | —          | 190        | 209        | mΩ   |
| R <sub>ONSW2N</sub>  | SW2 N-MOSFET R <sub>DS(on)</sub><br>at V <sub>IN</sub> = V <sub>INSW2</sub> = 3.3 V  | —          | 212        | 255        | mΩ   |
| I <sub>SW2PQ</sub>   | SW2 P-MOSFET leakage current<br>V <sub>IN</sub> = V <sub>INSW2</sub> = 4.5 V   | —          | —          | 12         | μA   |
| I <sub>SW2NQ</sub>   | SW2 N-MOSFET leakage current<br>V <sub>IN</sub> = V <sub>INSW2</sub> = 4.5 V   | —          | —          | 4.0        | μA   |
| R <sub>SW2DIS</sub>  | Discharge resistance   | —          | 600        | —          | Ω    |

14-channel power management integrated circuit (PMIC) for audio/video applications

- [1] When output is set to > 2.6 V, the output follows the input down when  $V_{IN}$  gets near 2.8 V.
- [2] The higher output voltage available depends on the voltage drop in the conduction path as given by the following equation:  $(V_{IN_{SW2}} - V_{SW2}) = I_{SW2} * (DCR \text{ of Inductor} + R_{ON_{SW2P}} + PCB \text{ trace resistance})$ .

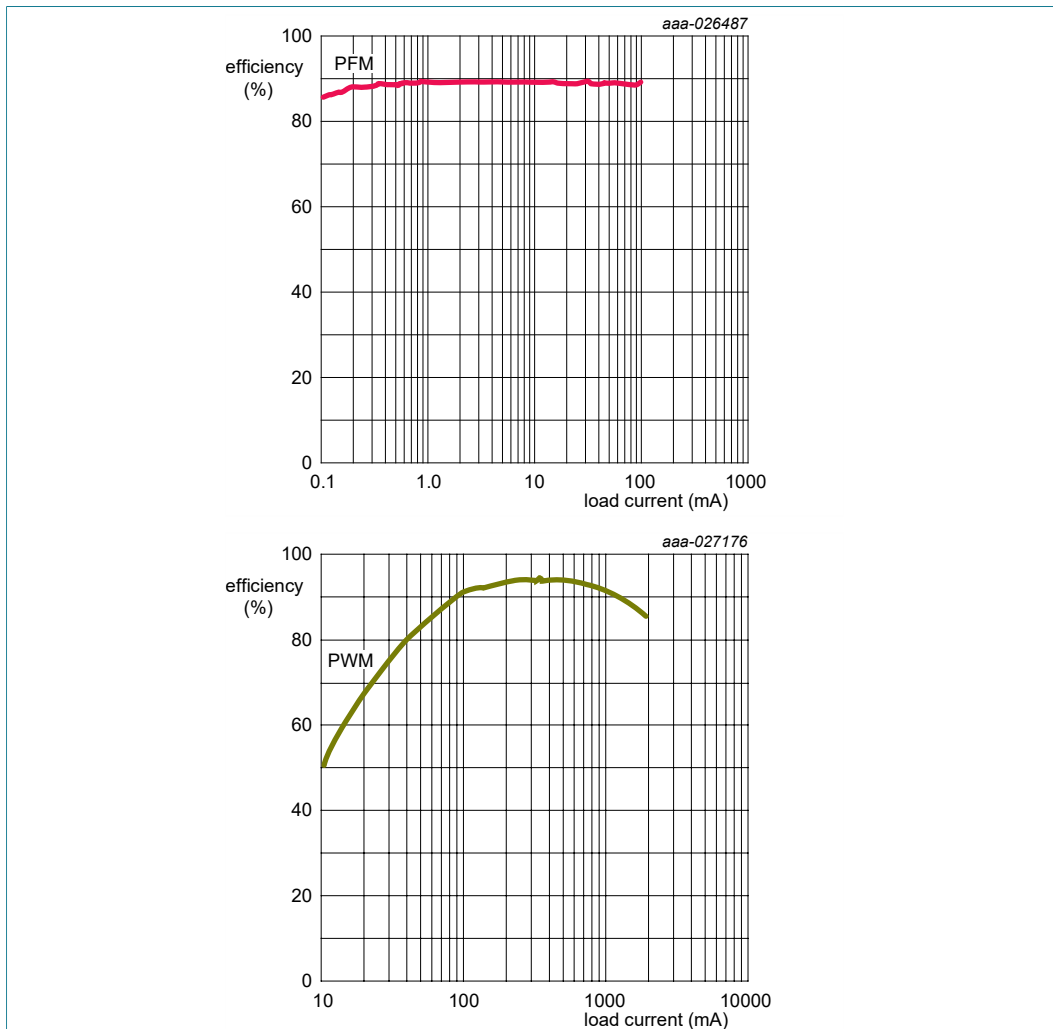
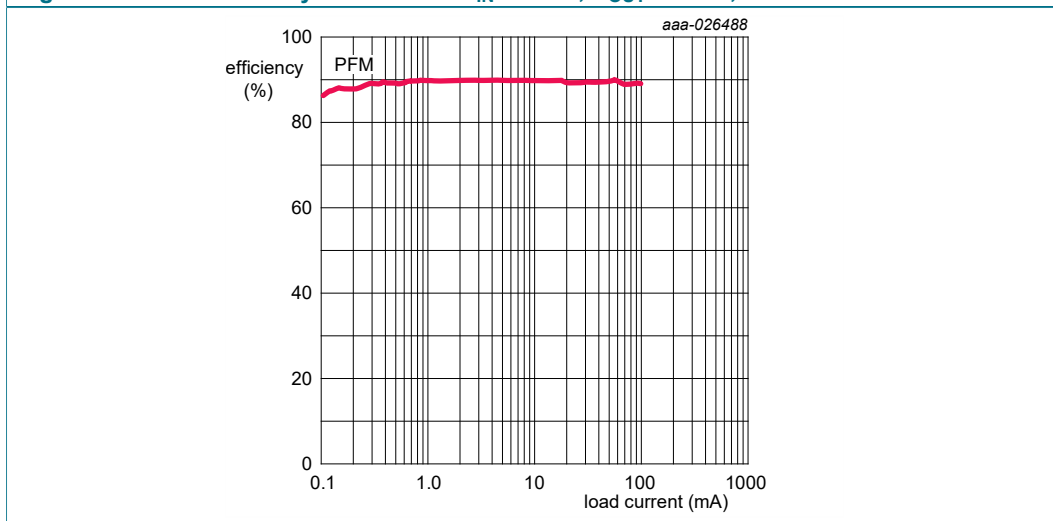
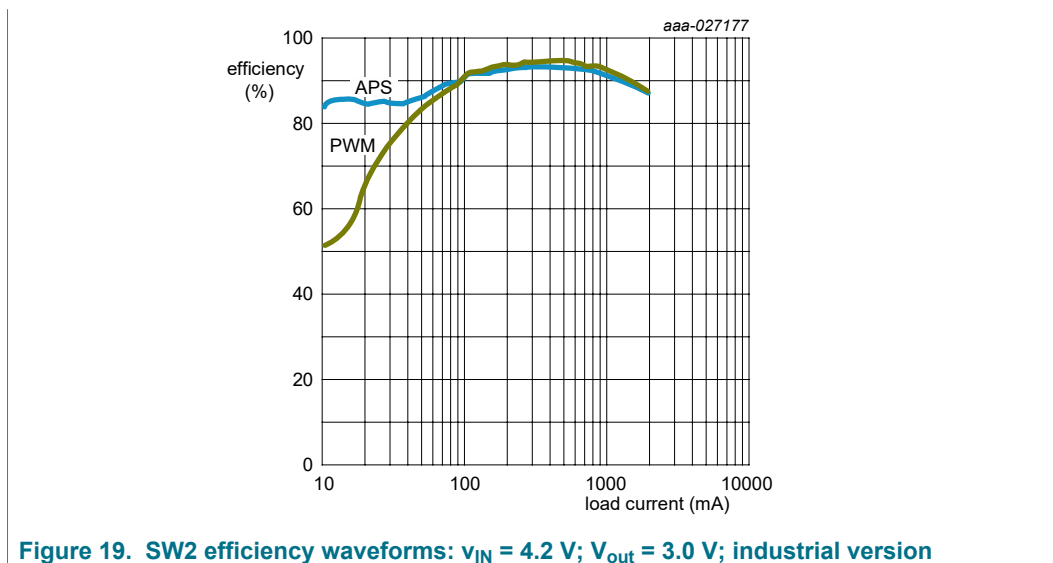


Figure 18. SW2 efficiency waveforms:  $V_{IN} = 4.2 \text{ V}$ ;  $V_{OUT} = 3.0 \text{ V}$ ; consumer version





#### 10.4.4.5 SW3A/B

SW3A/B are 1.5 to 3.0 A rated buck regulators, depending on the configuration. [Table 28](#) describes the available switching modes and [Table 29](#) shows the actual configuration options for the SW3xMODE[3:0] bits. SW3A/B can be configured in various phasing schemes, depending on the desired cost/performance trade-offs. The following configurations are available:

- A single phase
- A dual phase
- Independent regulators

The desired configuration is programmed in OTP by using the SW3\_CONFIG[1:0] bits. [Table 62](#) shows the options for the SW3CFG[1:0] bits.

**Table 62. SW3 configuration**

| SW3_CONFIG[1:0] | Description      |
|-----------------|------------------|
| 00              | A/B single phase |
| 01              | A/B single phase |
| 10              | A/B dual phase   |
| 11              | A/B independent  |

##### 10.4.4.5.1 SW3A/B single phase

In this configuration, SW3ALX and SW3BLX are connected in single phase with a single inductor as shown in [Figure 20](#). This configuration reduces cost and component count. Feedback is taken from the SW3AFB pin and the SW3BFB pin must be left open. Although control is from SW3A, registers of both regulators, SW3A and SW3B, must be identically set.

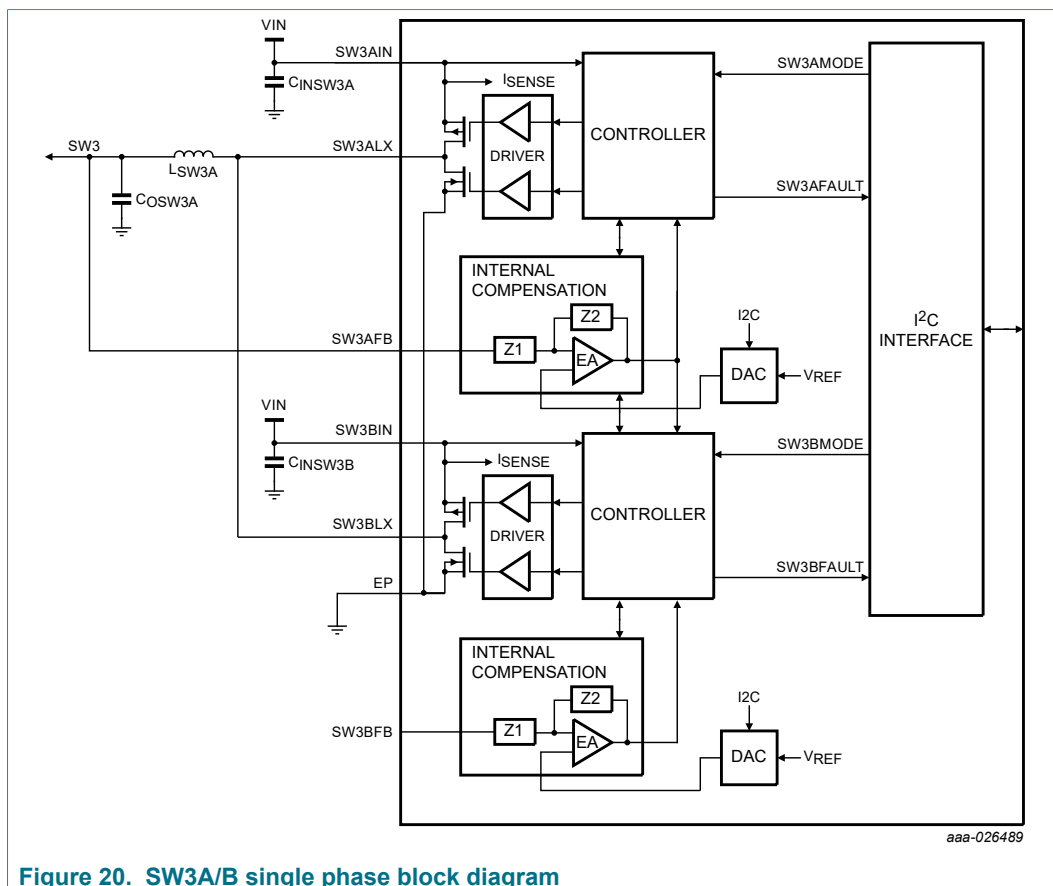


Figure 20. SW3A/B single phase block diagram

#### 10.4.4.5.2 SW3A/B dual phase

SW3A/B can be connected in dual phase configuration using one inductor per switching node, as shown in [Figure 21](#). This mode allows a smaller output voltage ripple. Feedback is taken from pin SW3AFB and pin SW3BFB must be left open. Although control is from SW3A, registers of both regulators, SW3A and SW3B, must be identically set. In this configuration, the regulators switch 180 degrees apart.

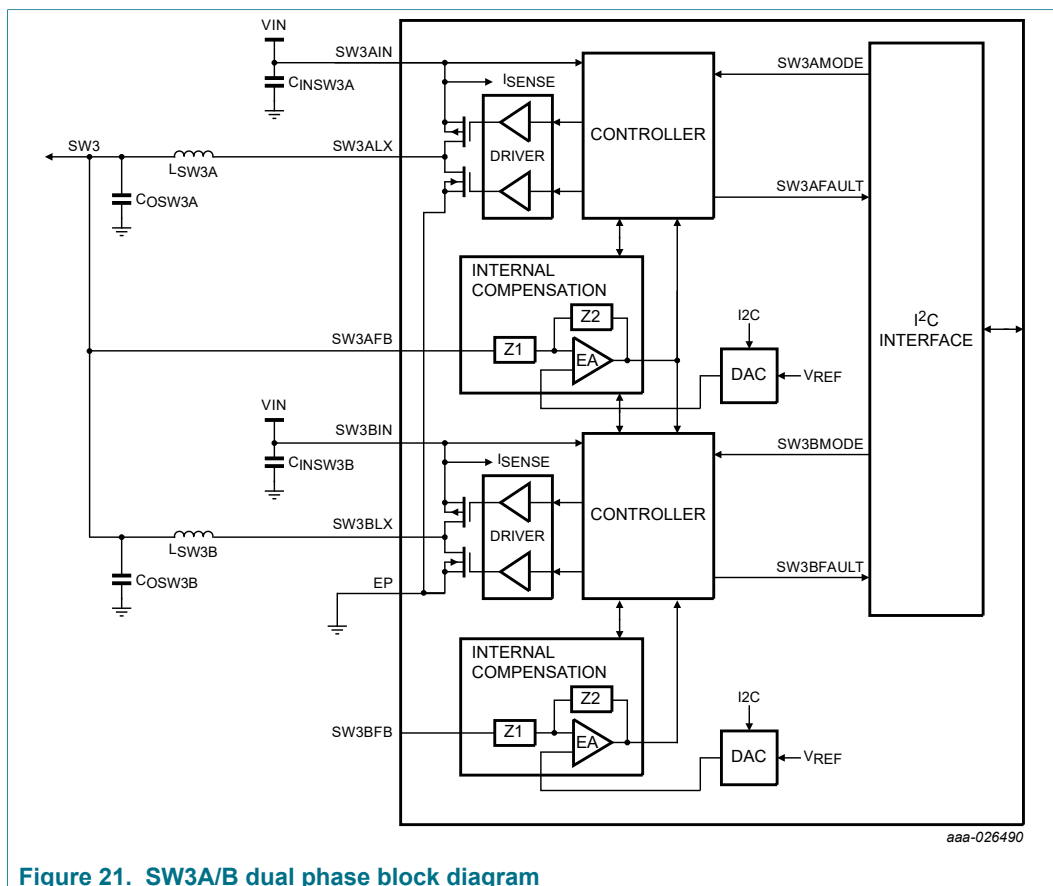


Figure 21. SW3A/B dual phase block diagram

#### 10.4.4.5.3 SW3A – SW3B independent outputs

SW3A and SW3B can be configured as independent outputs as shown in [Figure 22](#), providing flexibility for applications requiring more voltage rails with less current capability. Each output is configured and controlled independently by its respective I<sup>2</sup>C registers as shown in [Table 64](#).

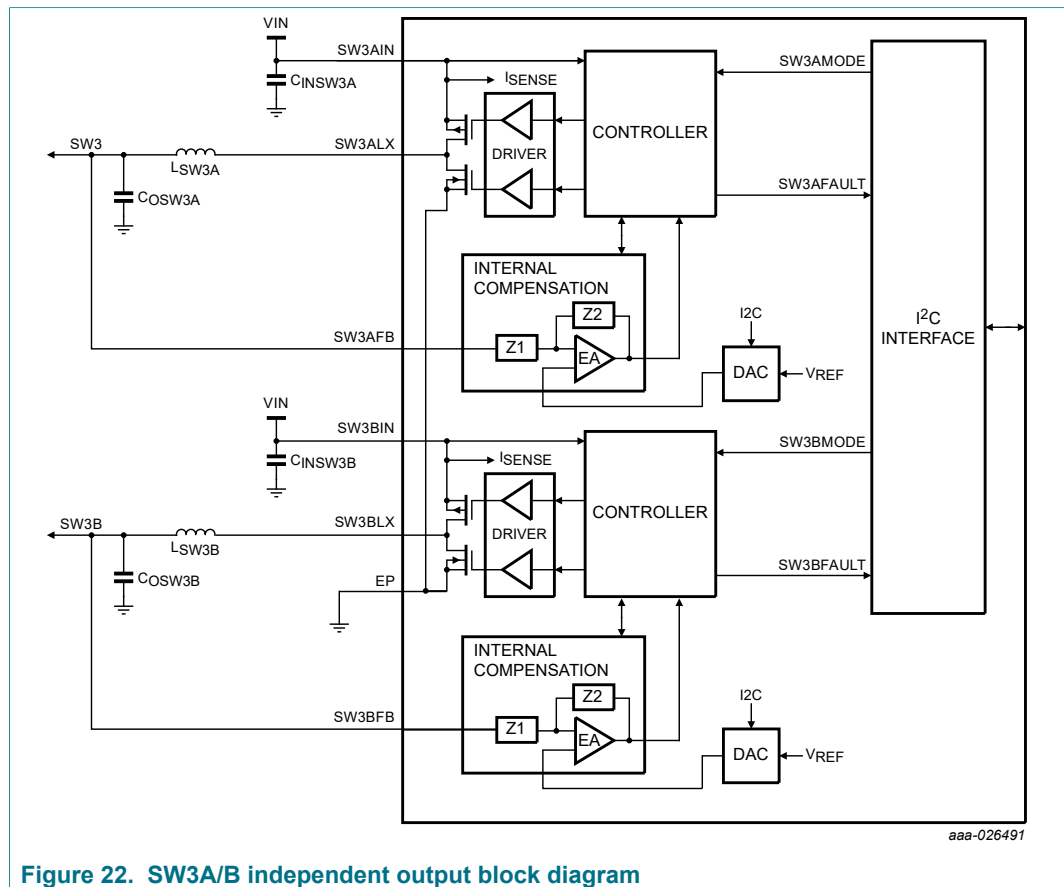


Figure 22. SW3A/B independent output block diagram

#### 10.4.4.5.4 SW3A/B setup and control registers

SW3A/B output voltage is programmable from 0.400 V to 3.300 V; however, bit SW3x[6] in register SW3xVOLT is read-only during normal operation. Its value is determined by the default configuration, or may be changed by using the OTP registers. Therefore, once SW3x[6] is set to 0, the output is limited to the lower output voltage range from 0.40 V to 1.975 V with 25 mV increments, as determined by bits SW3x[5:0]. Likewise, once bit SW3x[6] is set to 1, the output voltage is limited to the higher output voltage range from 0.800 V to 3.300 V with 50 mV increments, as determined by bits SW3x[5:0].

In order to optimize the performance of the regulator, it is recommended only voltage from 2.00 V to 3.300 V be used in the high range and the lower range be used for voltage from 0.400 V to 1.975 V.

The output voltage set point is independently programmed for normal, standby, and sleep mode by setting the SW3x[5:0], SW3xSTBY[5:0], and SW3xOFF[5:0] bits respectively; however, the initial state of the SW3x[6] bit is copied into the SW3xSTBY[6] and SW3xOFF[6] bits. Therefore, the output voltage range remains the same on all three operating modes. [Table 63](#) shows the output voltage coding valid for SW3x.

**Note:** Voltage set points of 0.6 V and below are not supported.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 63. SW3A/B output voltage configuration

| Low output voltage range <sup>[1]</sup> |           |             | High output voltage range |           |             |
|---|-----------|-------------|---------------------------|-----------|-------------|
| Set point                               | SW3x[6:0] | SW3x output | Set point                 | SW3x[6:0] | SW3x output |
| 0                                       | 0000000   | 0.4000      | 64                        | 1000000   | 0.8000      |
| 1                                       | 0000001   | 0.4250      | 65                        | 1000001   | 0.8500      |
| 2                                       | 0000010   | 0.4500      | 66                        | 1000010   | 0.9000      |
| 3                                       | 0000011   | 0.4750      | 67                        | 1000011   | 0.9500      |
| 4                                       | 0000100   | 0.5000      | 68                        | 1000100   | 1.0000      |
| 5                                       | 0000101   | 0.5250      | 69                        | 1000101   | 1.0500      |
| 6                                       | 0000110   | 0.5500      | 70                        | 1000110   | 1.1000      |
| 7                                       | 0000111   | 0.5750      | 71                        | 1000111   | 1.1500      |
| 8                                       | 0001000   | 0.6000      | 72                        | 1001000   | 1.2000      |
| 9                                       | 0001001   | 0.6250      | 73                        | 1001001   | 1.2500      |
| 10                                      | 0001010   | 0.6500      | 74                        | 1001010   | 1.3000      |
| 11                                      | 0001011   | 0.6750      | 75                        | 1001011   | 1.3500      |
| 12                                      | 0001100   | 0.7000      | 76                        | 1001100   | 1.4000      |
| 13                                      | 0001101   | 0.7250      | 77                        | 1001101   | 1.4500      |
| 14                                      | 0001110   | 0.7500      | 78                        | 1001110   | 1.5000      |
| 15                                      | 0001111   | 0.7750      | 79                        | 1001111   | 1.5500      |
| 16                                      | 0010000   | 0.8000      | 80                        | 1010000   | 1.6000      |
| 17                                      | 0010001   | 0.8250      | 81                        | 1010001   | 1.6500      |
| 18                                      | 0010010   | 0.8500      | 82                        | 1010010   | 1.7000      |
| 19                                      | 0010011   | 0.8750      | 83                        | 1010011   | 1.7500      |
| 20                                      | 0010100   | 0.9000      | 84                        | 1010100   | 1.8000      |
| 21                                      | 0010101   | 0.9250      | 85                        | 1010101   | 1.8500      |
| 22                                      | 0010110   | 0.9500      | 86                        | 1010110   | 1.9000      |
| 23                                      | 0010111   | 0.9750      | 87                        | 1010111   | 1.9500      |
| 24                                      | 0011000   | 1.0000      | 88                        | 1011000   | 2.0000      |
| 25                                      | 0011001   | 1.0250      | 89                        | 1011001   | 2.0500      |
| 26                                      | 0011010   | 1.0500      | 90                        | 1011010   | 2.1000      |
| 27                                      | 0011011   | 1.0750      | 91                        | 1011011   | 2.1500      |
| 28                                      | 0011100   | 1.1000      | 92                        | 1011100   | 2.2000      |
| 29                                      | 0011101   | 1.1250      | 93                        | 1011101   | 2.2500      |
| 30                                      | 0011110   | 1.1500      | 94                        | 1011110   | 2.3000      |
| 31                                      | 0011111   | 1.1750      | 95                        | 1011111   | 2.3500      |
| 32                                      | 0100000   | 1.2000      | 96                        | 1100000   | 2.4000      |
| 33                                      | 0100001   | 1.2250      | 97                        | 1100001   | 2.4500      |
| 34                                      | 0100010   | 1.2500      | 98                        | 1100010   | 2.5000      |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Low output voltage range <sup>[1]</sup> |           |             | High output voltage range |           |             |
|---|-----------|-------------|---------------------------|-----------|-------------|
| Set point                               | SW3x[6:0] | SW3x output | Set point                 | SW3x[6:0] | SW3x output |
| 35                                      | 0100011   | 1.2750      | 99                        | 1100011   | 2.5500      |
| 36                                      | 0100100   | 1.3000      | 100                       | 1100100   | 2.6000      |
| 37                                      | 0100101   | 1.3250      | 101                       | 1100101   | 2.6500      |
| 38                                      | 0100110   | 1.3500      | 102                       | 1100110   | 2.7000      |
| 39                                      | 0100111   | 1.3750      | 103                       | 1100111   | 2.7500      |
| 40                                      | 0101000   | 1.4000      | 104                       | 1101000   | 2.8000      |
| 41                                      | 0101001   | 1.4250      | 105                       | 1101001   | 2.8500      |
| 42                                      | 0101010   | 1.4500      | 106                       | 1101010   | 2.9000      |
| 43                                      | 0101011   | 1.4750      | 107                       | 1101011   | 2.9500      |
| 44                                      | 0101100   | 1.5000      | 108                       | 1101100   | 3.0000      |
| 45                                      | 0101101   | 1.5250      | 109                       | 1101101   | 3.0500      |
| 46                                      | 0101110   | 1.5500      | 110                       | 1101110   | 3.1000      |
| 47                                      | 0101111   | 1.5750      | 111                       | 1101111   | 3.1500      |
| 48                                      | 0110000   | 1.6000      | 112                       | 1110000   | 3.2000      |
| 49                                      | 0110001   | 1.6250      | 113                       | 1110001   | 3.2500      |
| 50                                      | 0110010   | 1.6500      | 114                       | 1110010   | 3.3000      |
| 51                                      | 0110011   | 1.6750      | 115                       | 1110011   | Reserved    |
| 52                                      | 0110100   | 1.7000      | 116                       | 1110100   | Reserved    |
| 53                                      | 0110101   | 1.7250      | 117                       | 1110101   | Reserved    |
| 54                                      | 0110110   | 1.7500      | 118                       | 1110110   | Reserved    |
| 55                                      | 0110111   | 1.7750      | 119                       | 1110111   | Reserved    |
| 56                                      | 0111000   | 1.8000      | 120                       | 1111000   | Reserved    |
| 57                                      | 0111001   | 1.8250      | 121                       | 1111001   | Reserved    |
| 58                                      | 0111010   | 1.8500      | 122                       | 1111010   | Reserved    |
| 59                                      | 0111011   | 1.8750      | 123                       | 1111011   | Reserved    |
| 60                                      | 0111100   | 1.9000      | 124                       | 1111100   | Reserved    |
| 61                                      | 0111101   | 1.9250      | 125                       | 1111101   | Reserved    |
| 62                                      | 0111110   | 1.9500      | 126                       | 1111110   | Reserved    |
| 63                                      | 0111111   | 1.9750      | 127                       | 1111111   | Reserved    |

[1] For voltage less than 2.0 V, use set points 0 to 63.

[Table 64](#) provides a list of registers used to configure and operate SW3A/B. A detailed description on each of these registers is provided in [Table 65](#) to [Table 74](#).

**Table 64. SW3AB register summary**

| Register | Address | Output  |
|----------|---------|---|
| SW3AVOLT | 0x3C    | SW3A output voltage set point on normal operation |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Register | Address | Output  |
|----------|---------|---|
| SW3ASTBY | 0x3D    | SW3A output voltage set point on standby          |
| SW3AOFF  | 0x3E    | SW3A output voltage set point on sleep            |
| SW3AMODE | 0x3F    | SW3A switching mode selector register             |
| SW3ACONF | 0x40    | SW3A DVS, phase, frequency and ILIM configuration |
| SW3BVOLT | 0x43    | SW3B output voltage set point on normal operation |
| SW3BSTBY | 0x44    | SW3B output voltage set point on standby          |
| SW3BOFF  | 0x45    | SW3B output voltage set point on sleep            |
| SW3BMODE | 0x46    | SW3B switching mode selector register             |
| SW3BCONF | 0x47    | SW3B DVS, phase, frequency and ILIM configuration |

Table 65. Register SW3AVOLT - ADDR 0x3C

| Name   | Bit number | R/W | Default | Description   |
|--------|------------|-----|---------|---|
| SW3A   | 5:0        | R/W | 0x00    | Sets the SW3A output voltage (independent) or SW3A/B output voltage (single/dual phase), during normal operation mode. See <a href="#">Table 63</a> for all possible configurations.                  |
| SW3A   | 6          | R   | 0x00    | Sets the operating output voltage range for SW3A (independent) or SW3A/B (single/dual phase). Set during OTP or TBB configuration only. See <a href="#">Table 63</a> for all possible configurations. |
| UNUSED | 7          | —   | 0x00    | unused  |

Table 66. Register SW3ASTBY - ADDR 0x3D

| Name     | Bit number | R/W | Default | Description  |
|----------|------------|-----|---------|--|
| SW3ASTBY | 5:0        | R/W | 0x00    | Sets the SW3A output voltage (independent) or SW3A/B output voltage (single/dual phase), during standby mode. See <a href="#">Table 63</a> for all possible configurations.  |
| SW3ASTBY | 6          | R   | 0x00    | Sets the operating output voltage range for SW3A (independent) or SW3A/B (single/dual phase) in standby mode. This bit inherits the value configured on bit SW3A[6] during OTP or TBB configuration. See <a href="#">Table 63</a> for all possible configurations. |
| UNUSED   | 7          | —   | 0x00    | unused   |

Table 67. Register SW3AOFF - ADDR 0x3E

| Name    | Bit number | R/W | Default | Description   |
|---------|------------|-----|---------|---|
| SW3AOFF | 5:0        | R/W | 0x00    | Sets the SW3A output voltage (independent) or SW3A/B output voltage (single/dual phase), during sleep mode. See <a href="#">Table 63</a> for all possible configurations. |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name    | Bit number | R/W | Default | Description  |
|---------|------------|-----|---------|--|
| SW3AOFF | 6          | R   | 0x00    | Sets the operating output voltage range for SW3A (independent) or SW3A/B (single/dual phase) in sleep mode. This bit inherits the value configured on bit SW3A[6] during OTP or TBB configuration. See <a href="#">Table 63</a> for all possible configurations. |
| UNUSED  | 7          | —   | 0x00    | unused   |

Table 68. Register SW3AMODE - ADDR 0x3F

| Name      | Bit number | R/W | Default | Description   |
|-----------|------------|-----|---------|---|
| SW3AMODE  | 3:0        | R/W | 0x08    | Sets the SW3A (independent) or SW3A/B (single/dual phase) switching operation mode. See <a href="#">Table 29</a> for all possible configurations.                 |
| UNUSED    | 4          | —   | 0x00    | unused  |
| SW3AOMODE | 5          | R/W | 0x00    | Set status of SW3A (independent) or SW3A/B (single/dual phase) when in sleep mode. <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = PFM</li> </ul> |
| UNUSED    | 7:6        | —   | 0x00    | unused  |

Table 69. Register SW3ACONF - ADDR 0x40

| Name         | Bit number | R/W | Default | Description  |
|--------------|------------|-----|---------|--|
| SW3AILIM     | 0          | R/W | 0x00    | SW3A current limit level selection <ul style="list-style-type: none"> <li>• 0 = High-level current limit</li> <li>• 1 = Low-level current limit</li> </ul> |
| UNUSED       | 1          | R/W | 0x00    | unused   |
| SW3AFREQ     | 3:2        | R/W | 0x00    | SW3A switching frequency selector. See <a href="#">Table 36</a> .  |
| SW3APHASE    | 5:4        | R/W | 0x00    | SW3A phase clock selection. See <a href="#">Table 34</a> .   |
| SW3ADVSSPEED | 7:6        | R/W | 0x00    | SW3A DVS speed selection. See <a href="#">Table 33</a> .   |

Table 70. Register SW3BVOLT - ADDR 0x43

| Name   | Bit number | R/W | Default | Description   |
|--------|------------|-----|---------|---|
| SW3B   | 5:0        | R/W | 0x00    | Sets the SW3B output voltage (independent) during normal operation mode. See <a href="#">Table 63</a> for all possible configurations.                                  |
| SW3B   | 6          | R   | 0x00    | Sets the operating output voltage range for SW3B (independent). Set during OTP or TBB configuration only. See <a href="#">Table 63</a> for all possible configurations. |
| UNUSED | 7          | —   | 0x00    | unused  |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 71. Register SW3BSTBY - ADDR 0x44

| Name     | Bit number | R/W | Default | Description  |
|----------|------------|-----|---------|--|
| SW3BSTBY | 5:0        | R/W | 0x00    | Sets the SW3B output voltage (independent) during standby mode. See <a href="#">Table 63</a> for all possible configurations.  |
| SW3BSTBY | 6          | R   | 0x00    | Sets the operating output voltage range for SW3B (independent) in standby mode. This bit inherits the value configured on bit SW3B[6] during OTP or TBB configuration. See <a href="#">Table 63</a> for all possible configurations. |
| UNUSED   | 7          | —   | 0x00    | unused   |

Table 72. Register SW3BOFF - ADDR 0x45

| Name    | Bit number | R/W | Default | Description  |
|---------|------------|-----|---------|--|
| SW3BOFF | 5:0        | R/W | 0x00    | Sets the SW3B output voltage (independent) during sleep mode. See <a href="#">Table 63</a> for all possible configurations.  |
| SW3BOFF | 6          | R   | 0x00    | Sets the operating output voltage range for SW3B (independent) in sleep mode. This bit inherits the value configured on bit SW3B[6] during OTP or TBB configuration. See <a href="#">Table 63</a> for all possible configurations. |
| UNUSED  | 7          | —   | 0x00    | unused   |

Table 73. Register SW3BMODE - ADDR 0x46

| Name      | Bit number | R/W | Default | Description   |
|-----------|------------|-----|---------|---|
| SW3BMODE  | 3:0        | R/W | 0x08    | Sets the SW3B (independent) switching operation mode. See <a href="#">Table 29</a> for all possible configurations.             |
| UNUSED    | 4          | —   | 0x00    | unused  |
| SW3BOMODE | 5          | R/W | 0x00    | Set status of SW3B (independent) when in sleep mode. <ul style="list-style-type: none"> <li>0 = OFF</li> <li>1 = PFM</li> </ul> |
| UNUSED    | 7:6        | —   | 0x00    | unused  |

Table 74. Register SW3BCONF - ADDR 0x47

| Name         | Bit number | R/W | Default | Description  |
|--------------|------------|-----|---------|--|
| SW3BILIM     | 0          | R/W | 0x00    | SW3B current limit level selection <ul style="list-style-type: none"> <li>0 = High-level Current limit</li> <li>1 = Low-level Current limit</li> </ul> |
| UNUSED       | 1          | R/W | 0x00    | unused   |
| SW3BFREQ     | 3:2        | R/W | 0x00    | SW3B switching frequency selector. See <a href="#">Table 36</a> .  |
| SW3BPHASE    | 5:4        | R/W | 0x00    | SW3B phase clock selection. See <a href="#">Table 34</a> .   |
| SW3BDVSSPEED | 7:6        | R/W | 0x00    | SW3B DVS speed selection. See <a href="#">Table 33</a> .   |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

## 10.4.4.5.5 SW3A/B external components

Table 75. SW3A/B external component requirements

| Components                                | Description                     | Mode                 |                      |                                      |
|---|---------------------------------|----------------------|----------------------|--------------------------------------|
|   |                                 | SW3A/B single phase  | SW3A/B dual phase    | SW3A independent<br>SW3B independent |
| $C_{IN\text{SW}3\text{A}}$ <sup>[1]</sup> | SW3A input capacitor            | 4.7 $\mu\text{F}$    | 4.7 $\mu\text{F}$    | 4.7 $\mu\text{F}$                    |
| $C_{IN3\text{AHF}}$ <sup>[1]</sup>        | SW3A decoupling input capacitor | 0.1 $\mu\text{F}$    | 0.1 $\mu\text{F}$    | 0.1 $\mu\text{F}$                    |
| $C_{IN\text{SW}3\text{B}}$ <sup>[1]</sup> | SW3B input capacitor            | 4.7 $\mu\text{F}$    | 4.7 $\mu\text{F}$    | 4.7 $\mu\text{F}$                    |
| $C_{IN3\text{BHF}}$ <sup>[1]</sup>        | SW3B decoupling input capacitor | 0.1 $\mu\text{F}$    | 0.1 $\mu\text{F}$    | 0.1 $\mu\text{F}$                    |
| $C_{OS\text{W}3\text{A}}$ <sup>[1]</sup>  | SW3A output capacitor           | 3 x 22 $\mu\text{F}$ | 2 x 22 $\mu\text{F}$ | 2 x 22 $\mu\text{F}$                 |
| $C_{OS\text{W}3\text{B}}$ <sup>[1]</sup>  | SW3B output capacitor           | —                    | 2 x 22 $\mu\text{F}$ | 2 x 22 $\mu\text{F}$                 |
| $L_{\text{SW}3\text{A}}$                  | SW3A inductor                   | 1.0 $\mu\text{H}$    | 1.0 $\mu\text{H}$    | 1.0 $\mu\text{H}$                    |
| $L_{\text{SW}3\text{B}}$                  | SW3B inductor                   | —                    | 1.0 $\mu\text{H}$    | 1.0 $\mu\text{H}$                    |

[1] Use X5R or X7R capacitors.

## 10.4.4.5.6 SW3A/B specifications

Table 76. SW3A/B electrical characteristics

All parameters are specified at  $T_{\text{MIN}}$  to  $T_{\text{MAX}}$  (see Table 4),  $V_{\text{IN}} = V_{\text{IN}\text{SW}3\text{x}} = 3.6\text{ V}$ ,  $V_{\text{SW}3\text{x}} = 1.5\text{ V}$ ,  $I_{\text{SW}3\text{x}} = 100\text{ mA}$ ,  $\text{SW}3\text{x\_PWRSTG}[2:0] = [111]$ , typical external component values,  $f_{\text{SW}3\text{x}} = 2.0\text{ MHz}$ , single/dual phase and independent mode unless, otherwise noted. Typical values are characterized at  $V_{\text{IN}} = V_{\text{IN}\text{SW}3\text{x}} = 3.6\text{ V}$ ,  $V_{\text{SW}3\text{x}} = 1.5\text{ V}$ ,  $I_{\text{SW}3\text{x}} = 100\text{ mA}$ ,  $\text{SW}3\text{x\_PWRSTG}[2:0] = [111]$ , and  $25\text{ }^\circ\text{C}$ , unless otherwise noted.

| Symbol   | Parameter   | Min    | Typ      | Max   | Unit |
|--|---|--------|----------|-------|------|
| <b>Switch mode supply SW3A/B</b>                           |   |        |          |       |      |
| $V_{\text{IN}\text{SW}3\text{x}}$                          | Operating input voltage <sup>[1]</sup>  | 2.8    | —        | 4.5   | V    |
| $V_{\text{SW}3\text{x}}$                                   | Nominal output voltage  | —      | Table 63 | —     | V    |
| $V_{\text{SW}3\text{xACC}}$                                | Output voltage accuracy   |        |          |       |      |
|  | PWM, APS $2.8\text{ V} < V_{\text{IN}} < 4.5\text{ V}$ , $0 < I_{\text{SW}3\text{x}} < I_{\text{SW}3\text{xMAX}}$ | -25    | —        | 25    | mV   |
|  | $0.625\text{ V} < V_{\text{SW}3\text{x}} < 0.85\text{ V}$   | -3.0 % | —        | 3.0 % | %    |
|  | $0.875\text{ V} < V_{\text{SW}3\text{x}} < 1.975\text{ V}$  | -6.0 % | —        | 6.0 % | %    |
|  | $2.0\text{ V} < V_{\text{SW}3\text{x}} < 3.3\text{ V}$  |        |          |       |      |
|  | PFM, steady state ( $2.8\text{ V} < V_{\text{IN}} < 4.5\text{ V}$ , $0 < I_{\text{SW}3\text{x}} < 50\text{ mA}$ ) | -65    | —        | 65    | mV   |
|  | $0.625\text{ V} < V_{\text{SW}3\text{x}} < 0.675\text{ V}$  | -45    | —        | 45    | mV   |
|  | $0.7\text{ V} < V_{\text{SW}3\text{x}} < 0.85\text{ V}$   | -3.0 % | —        | 3.0 % | %    |
| $0.875\text{ V} < V_{\text{SW}3\text{x}} < 1.975\text{ V}$ | -3.0 %  | —      | 3.0 %    | %     |      |
| $2.0\text{ V} < V_{\text{SW}3\text{x}} < 3.3\text{ V}$     |   |        |          |       |      |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

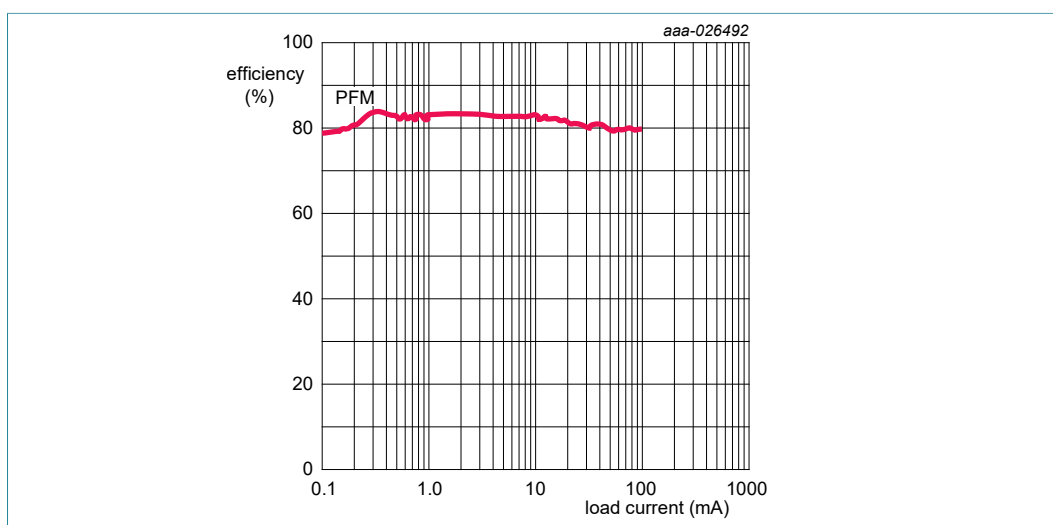
| Symbol            | Parameter  | Min                             | Typ                                    | Max                             | Unit    |
|-------------------|--|---------------------------------|--|---------------------------------|---------|
| $I_{SW3x}$        | Rated output load current [2]<br>2.8 V < $V_{IN}$ < 4.5 V, 0.625 V < $V_{SW3x}$ < 3.3 V<br>PWM, APS mode single/dual phase,<br>SW3xILIM = 0<br>PWM, APS mode independent (per phase),<br>SW3xILIM = 0  | —<br>—                          | —<br>—                                 | 3000<br>1500                    | mA      |
| $I_{SW3xLIM}$     | Current limiter peak current detection<br>Single phase (current through inductor)<br>SW3xILIM = 0<br>SW3xILIM = 1<br>Independent mode or dual phase (current through inductor per phase)<br>SW3xILIM = 0<br>SW3xILIM = 1                                   | 3.5<br>2.7<br>1.8<br>1.3        | 5.0<br>3.8<br>2.5<br>1.9               | 6.5<br>4.9<br>3.3<br>2.5        | A       |
| $V_{SW3xOSH}$     | Startup overshoot<br>$I_{SW3x} = 0.0$ mA<br>DVS clk = 25 mV/4 $\mu$ s, $V_{IN} = V_{IN_{SW3x}} = 4.5$ V  | —                               | —                                      | 66                              | mV      |
| $t_{ON_{SW3x}}$   | Turn on time<br>Enable to 90 % of end value<br>$I_{SW3x} = 0$ mA<br>DVS clk = 25 mV/4 $\mu$ s, $V_{IN} = V_{IN_{SW3x}} = 4.5$ V  | —                               | —                                      | 500                             | $\mu$ s |
| $f_{SW3x}$        | Switching frequency<br>SW3xFREQ[1:0] = 00<br>SW3xFREQ[1:0] = 01<br>SW3xFREQ[1:0] = 10  | —<br>—<br>—                     | 1.0<br>2.0<br>4.0                      | —<br>—<br>—                     | MHz     |
| $\eta_{SW3AB}$    | Efficiency (single phase)<br>$f_{SW3} = 2.0$ MHz, $L_{SW3x} = 1.0$ $\mu$ H<br>PFM, 1.5 V, 1.0 mA<br>PFM, 1.5 V, 50 mA<br>APS, PWM 1.5 V, 500 mA<br>APS, PWM 1.5 V, 750 mA<br>APS, PWM 1.5 V, 1250 mA<br>APS, PWM 1.5 V, 2500 mA<br>APS, PWM 1.5 V, 3000 mA | —<br>—<br>—<br>—<br>—<br>—<br>— | 84<br>85<br>85<br>84<br>80<br>74<br>65 | —<br>—<br>—<br>—<br>—<br>—<br>— | %       |
| $\Delta V_{SW3x}$ | Output ripple  | —                               | 10                                     | —                               | mV      |
| $V_{SW3xLIR}$     | Line regulation (APS, PWM)   | —                               | —                                      | 20                              | mV      |
| $V_{SW3xLOR}$     | DC load regulation (APS, PWM)  | —                               | —                                      | 20                              | mV      |
| $V_{SW3xLOTR}$    | Transient load regulation<br>Transient load = 0.0 mA to $I_{SW3x}/2$ , di/dt = 100 mA/ $\mu$ s<br>Overshoot<br>Undershoot  | —<br>—                          | —<br>—                                 | 50<br>50                        | mV      |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol               | Parameter   | Min | Typ | Max | Unit |
|----------------------|---|-----|-----|-----|------|
| I <sub>SW3xQ</sub>   | Quiescent current   | —   | 22  | —   | μA   |
|                      | PFM mode (single/dual phase)  | —   | 300 | —   |      |
|                      | APS mode (single/dual phase)  | —   | 50  | —   |      |
|                      | PFM mode (independent mode)   | —   | 250 | —   |      |
|                      | APS mode (SW3A independent mode)  | —   | 150 | —   |      |
| R <sub>ONSW3AP</sub> | SW3A P-MOSFET R <sub>DS(on)</sub><br>at V <sub>IN</sub> = V <sub>INSW3A</sub> = 3.3 V | —   | 215 | 245 | mΩ   |
| R <sub>ONSW3AN</sub> | SW3A N-MOSFET R <sub>DS(on)</sub><br>at V <sub>IN</sub> = V <sub>INSW3A</sub> = 3.3 V | —   | 258 | 326 | mΩ   |
| I <sub>SW3APQ</sub>  | SW3A P-MOSFET leakage current<br>V <sub>IN</sub> = V <sub>INSW3A</sub> = 4.5 V        | —   | —   | 7.5 | μA   |
| I <sub>SW3ANQ</sub>  | SW3A N-MOSFET leakage current<br>V <sub>IN</sub> = V <sub>INSW3A</sub> = 4.5 V        | —   | —   | 2.5 | μA   |
| R <sub>ONSW3BP</sub> | SW3B P-MOSFET R <sub>DS(on)</sub><br>at V <sub>IN</sub> = V <sub>INSW3B</sub> = 3.3 V | —   | 215 | 245 | mΩ   |
| R <sub>ONSW3BN</sub> | SW3B N-MOSFET R <sub>DS(on)</sub><br>at V <sub>IN</sub> = V <sub>INSW3B</sub> = 3.3 V | —   | 258 | 326 | mΩ   |
| I <sub>SW3BPQ</sub>  | SW3B P-MOSFET leakage current<br>V <sub>IN</sub> = V <sub>INSW3B</sub> = 4.5 V        | —   | —   | 7.5 | μA   |
| I <sub>SW3BNQ</sub>  | SW3B N-MOSFET leakage current<br>V <sub>IN</sub> = V <sub>INSW3B</sub> = 4.5 V        | —   | —   | 2.5 | μA   |
| R <sub>SW3xDIS</sub> | Discharge resistance  | —   | 600 | —   | Ω    |

[1] When output is set to > 2.6 V, the output follows the input down when V<sub>IN</sub> gets near 2.8 V.

[2] The higher output voltage available depends on the voltage drop in the conduction path as given by the following equation: (V<sub>INSW3x</sub> - V<sub>SW3x</sub>) = I<sub>SW3x</sub>\* (DCR of inductor + R<sub>ONSW3xP</sub> + PCB trace resistance).



14-channel power management integrated circuit (PMIC) for audio/video applications

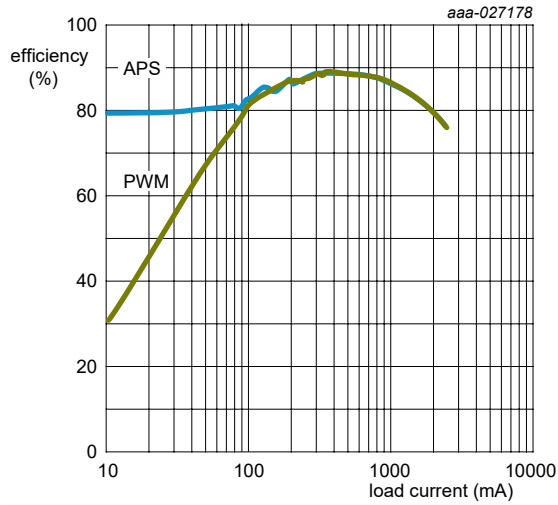


Figure 23. SW3AB efficiency waveforms:  $V_{IN} = 4.2\text{ V}$ ;  $V_{OUT} = 1.5\text{ V}$ ; consumer version

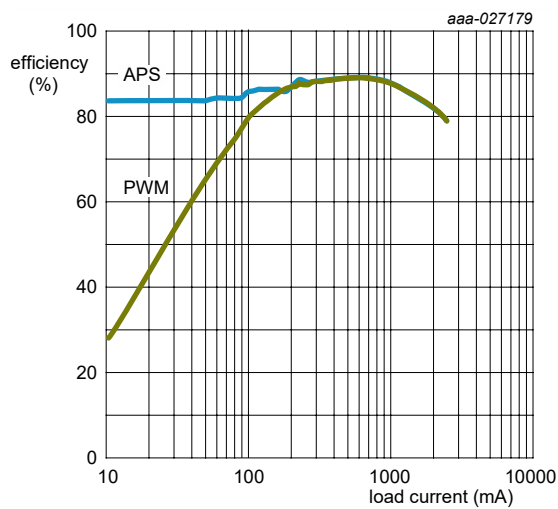
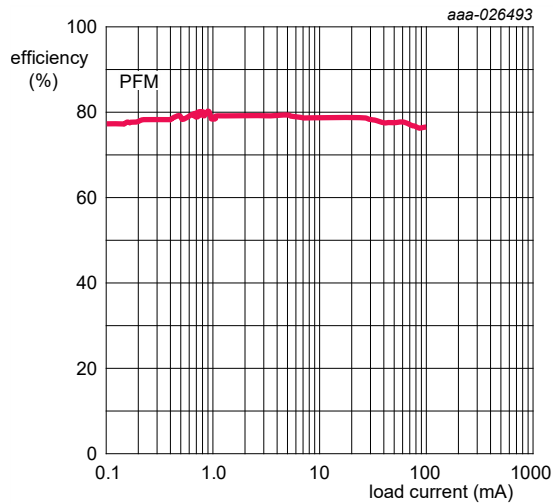


Figure 24. SW3AB efficiency waveforms:  $V_{IN} = 4.2\text{ V}$ ;  $V_{OUT} = 1.5\text{ V}$ ; industrial version

#### 10.4.4.6 SW4

SW4 is a 1.0 A rated single phase buck regulator capable of operating in two modes. In default mode, it operates as a normal buck regulator with a programmable output between 0.400 V and 3.300 V. It is capable of operating in the three available switching modes: PFM, APS, and PWM, described in [Table 28](#) and configured by the SW4MODE[3:0] bits, as shown in [Table 29](#).

If the system requires DDR memory termination, SW4 can be used in VTT mode. In the VTT mode, the reference voltage tracks the output voltage of SW3A, scaled by 0.5. In VTT mode, only the PWM switching mode is allowed. The VTT mode can be configured by use of VTT bit in the OTP\_SW4\_CONFIG register.

[Figure 25](#) shows the block diagram and the external component connections for the SW4 regulator.

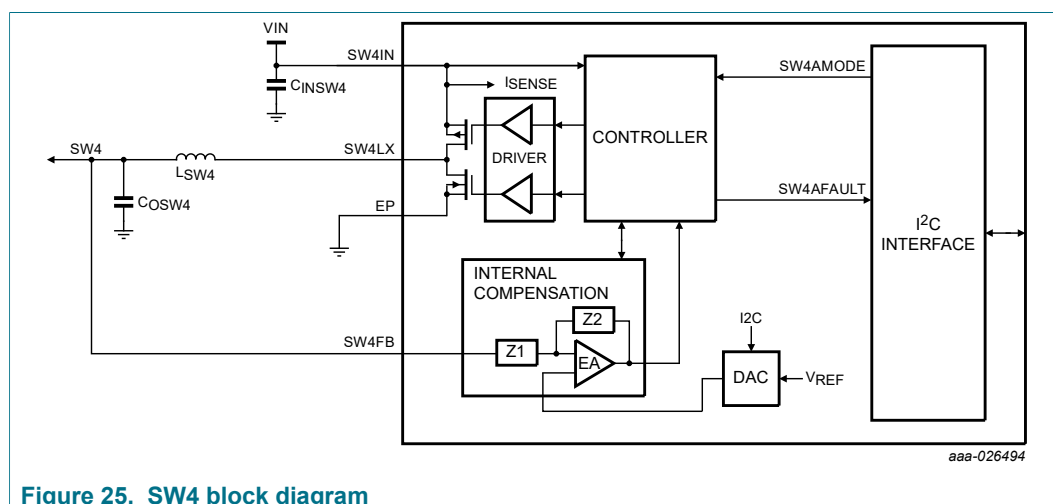


Figure 25. SW4 block diagram

##### 10.4.4.6.1 SW4 setup and control registers

To set the SW4 in regulator or VTT mode, bit VTT of the register OTP\_SW4\_CONF register in [Table 135](#) is programmed during OTP or TBB configuration; setting bit VTT to 1 enables SW4 to operate in VTT mode and 0 in regulator mode. See [Section 10.1.2 "One time programmability \(OTP\)"](#) for detailed information on OTP configuration.

In regulator mode, the SW4 output voltage is programmable from 0.400 V to 3.300 V; however, bit SW4[6] in the SW4VOLT register is read-only during normal operation. Its value is determined by the default configuration, or may be changed by using the OTP registers. Once SW4[6] is set to 0, the output is limited to the lower output voltage range from 0.400 V to 1.975 V with 25 mV increments, as determined by the SW4[5:0] bits. Likewise, once the SW4[6] bit is set to 1, the output voltage is limited to the higher output voltage range from 0.800 V to 3.300 V with 50 mV increments, as determined by the SW4[5:0] bits.

To optimize the performance of the regulator, it is recommended only voltage from 2.000 V to 3.300 V be used in the high range and the lower range be used for voltage from 0.400 V to 1.975 V.

The output voltage set point is independently programmed for normal, standby, and sleep mode by setting the SW4[5:0], SW4STBY[5:0], and SW4OFF[5:0] bits, respectively. However, the initial state of the SW4[6] bit is copied into bits SW4STBY[6], and

## 14-channel power management integrated circuit (PMIC) for audio/video applications

SW4OFF[6] bits, so the output voltage range remains the same on all three operating modes. [Table 77](#) shows the output voltage coding valid for SW4.

**Note:** Voltage set points of 0.6 V and below are supported only in the VTT mode.

Table 77. SW4 output voltage configuration

| Low output voltage range <sup>[1]</sup> |          |            | High output voltage range |          |            |
|---|----------|------------|---------------------------|----------|------------|
| Set point                               | SW4[6:0] | SW4 output | Set point                 | SW4[6:0] | SW4 output |
| 0                                       | 0000000  | 0.4000     | 64                        | 1000000  | 0.8000     |
| 1                                       | 0000001  | 0.4250     | 65                        | 1000001  | 0.8500     |
| 2                                       | 0000010  | 0.4500     | 66                        | 1000010  | 0.9000     |
| 3                                       | 0000011  | 0.4750     | 67                        | 1000011  | 0.9500     |
| 4                                       | 0000100  | 0.5000     | 68                        | 1000100  | 1.0000     |
| 5                                       | 0000101  | 0.5250     | 69                        | 1000101  | 1.0500     |
| 6                                       | 0000110  | 0.5500     | 70                        | 1000110  | 1.1000     |
| 7                                       | 0000111  | 0.5750     | 71                        | 1000111  | 1.1500     |
| 8                                       | 0001000  | 0.6000     | 72                        | 1001000  | 1.2000     |
| 9                                       | 0001001  | 0.6250     | 73                        | 1001001  | 1.2500     |
| 10                                      | 0001010  | 0.6500     | 74                        | 1001010  | 1.3000     |
| 11                                      | 0001011  | 0.6750     | 75                        | 1001011  | 1.3500     |
| 12                                      | 0001100  | 0.7000     | 76                        | 1001100  | 1.4000     |
| 13                                      | 0001101  | 0.7250     | 77                        | 1001101  | 1.4500     |
| 14                                      | 0001110  | 0.7500     | 78                        | 1001110  | 1.5000     |
| 15                                      | 0001111  | 0.7750     | 79                        | 1001111  | 1.5500     |
| 16                                      | 0010000  | 0.8000     | 80                        | 1010000  | 1.6000     |
| 17                                      | 0010001  | 0.8250     | 81                        | 1010001  | 1.6500     |
| 18                                      | 0010010  | 0.8500     | 82                        | 1010010  | 1.7000     |
| 19                                      | 0010011  | 0.8750     | 83                        | 1010011  | 1.7500     |
| 20                                      | 0010100  | 0.9000     | 84                        | 1010100  | 1.8000     |
| 21                                      | 0010101  | 0.9250     | 85                        | 1010101  | 1.8500     |
| 22                                      | 0010110  | 0.9500     | 86                        | 1010110  | 1.9000     |
| 23                                      | 0010111  | 0.9750     | 87                        | 1010111  | 1.9500     |
| 24                                      | 0011000  | 1.0000     | 88                        | 1011000  | 2.0000     |
| 25                                      | 0011001  | 1.0250     | 89                        | 1011001  | 2.0500     |
| 26                                      | 0011010  | 1.0500     | 90                        | 1011010  | 2.1000     |
| 27                                      | 0011011  | 1.0750     | 91                        | 1011011  | 2.1500     |
| 28                                      | 0011100  | 1.1000     | 92                        | 1011100  | 2.2000     |
| 29                                      | 0011101  | 1.1250     | 93                        | 1011101  | 2.2500     |
| 30                                      | 0011110  | 1.1500     | 94                        | 1011110  | 2.3000     |
| 31                                      | 0011111  | 1.1750     | 95                        | 1011111  | 2.3500     |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Low output voltage range <sup>[1]</sup> |          |            | High output voltage range |          |            |
|---|----------|------------|---------------------------|----------|------------|
| Set point                               | SW4[6:0] | SW4 output | Set point                 | SW4[6:0] | SW4 output |
| 32                                      | 0100000  | 1.2000     | 96                        | 1100000  | 2.4000     |
| 33                                      | 0100001  | 1.2250     | 97                        | 1100001  | 2.4500     |
| 34                                      | 0100010  | 1.2500     | 98                        | 1100010  | 2.5000     |
| 35                                      | 0100011  | 1.2750     | 99                        | 1100011  | 2.5500     |
| 36                                      | 0100100  | 1.3000     | 100                       | 1100100  | 2.6000     |
| 37                                      | 0100101  | 1.3250     | 101                       | 1100101  | 2.6500     |
| 38                                      | 0100110  | 1.3500     | 102                       | 1100110  | 2.7000     |
| 39                                      | 0100111  | 1.3750     | 103                       | 1100111  | 2.7500     |
| 40                                      | 0101000  | 1.4000     | 104                       | 1101000  | 2.8000     |
| 41                                      | 0101001  | 1.4250     | 105                       | 1101001  | 2.8500     |
| 42                                      | 0101010  | 1.4500     | 106                       | 1101010  | 2.9000     |
| 43                                      | 0101011  | 1.4750     | 107                       | 1101011  | 2.9500     |
| 44                                      | 0101100  | 1.5000     | 108                       | 1101100  | 3.0000     |
| 45                                      | 0101101  | 1.5250     | 109                       | 1101101  | 3.0500     |
| 46                                      | 0101110  | 1.5500     | 110                       | 1101110  | 3.1000     |
| 47                                      | 0101111  | 1.5750     | 111                       | 1101111  | 3.1500     |
| 48                                      | 0110000  | 1.6000     | 112                       | 1110000  | 3.2000     |
| 49                                      | 0110001  | 1.6250     | 113                       | 1110001  | 3.2500     |
| 50                                      | 0110010  | 1.6500     | 114                       | 1110010  | 3.3000     |
| 51                                      | 0110011  | 1.6750     | 115                       | 1110011  | Reserved   |
| 52                                      | 0110100  | 1.7000     | 116                       | 1110100  | Reserved   |
| 53                                      | 0110101  | 1.7250     | 117                       | 1110101  | Reserved   |
| 54                                      | 0110110  | 1.7500     | 118                       | 1110110  | Reserved   |
| 55                                      | 0110111  | 1.7750     | 119                       | 1110111  | Reserved   |
| 56                                      | 0111000  | 1.8000     | 120                       | 1111000  | Reserved   |
| 57                                      | 0111001  | 1.8250     | 121                       | 1111001  | Reserved   |
| 58                                      | 0111010  | 1.8500     | 122                       | 1111010  | Reserved   |
| 59                                      | 0111011  | 1.8750     | 123                       | 1111011  | Reserved   |
| 60                                      | 0111100  | 1.9000     | 124                       | 1111100  | Reserved   |
| 61                                      | 0111101  | 1.9250     | 125                       | 1111101  | Reserved   |
| 62                                      | 0111110  | 1.9500     | 126                       | 1111110  | Reserved   |
| 63                                      | 0111111  | 1.9750     | 127                       | 1111111  | Reserved   |

[1] For voltage less than 2.0 V, use set points 0 to 63.

Full setup and control of SW4 is done through the I<sup>2</sup>C registers listed in [Table 77](#). A detailed description of each of the registers is provided in [Table 79](#) to [Table 83](#).

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 78. SW4 register summary

| Register | Address | Description                                  |
|----------|---------|--|
| SW4VOLT  | 0x4A    | Output voltage set point on normal operation |
| SW4STBY  | 0x4B    | Output voltage set point on standby          |
| SW4OFF   | 0x4C    | Output voltage set point on sleep            |
| SW4MODE  | 0x4D    | Switching mode selector register             |
| SW4CONF  | 0x4E    | DVS, phase, frequency and ILIM configuration |

Table 79. Register SW4VOLT - ADDR 0x4A

| Name   | Bit number | R/W | Default | Description  |
|--------|------------|-----|---------|--|
| SW4    | 5:0        | R/W | 0x00    | Sets the SW4 output voltage during normal operation mode. See <a href="#">Table 77</a> for all possible configurations.                                  |
| SW4    | 6          | R   | 0x00    | Sets the operating output voltage range for SW4. Set during OTP or TBB configuration only. See <a href="#">Table 77</a> for all possible configurations. |
| UNUSED | 7          | —   | 0x00    | unused   |

Table 80. Register SW4STBY - ADDR 0x4B

| Name    | Bit number | R/W | Default | Description  |
|---------|------------|-----|---------|--|
| SW4STBY | 5:0        | R/W | 0x00    | Sets the SW4 output voltage during standby mode. See <a href="#">Table 77</a> for all possible configurations.   |
| SW4STBY | 6          | R   | 0x00    | Sets the operating output voltage range for SW4 in standby mode. This bit inherits the value configured on bit SW4[6] during OTP or TBB configuration. See <a href="#">Table 77</a> for all possible configurations. |
| UNUSED  | 7          | —   | 0x00    | unused   |

Table 81. Register SW4OFF - ADDR 0x4C

| Name   | Bit number | R/W | Default | Description  |
|--------|------------|-----|---------|--|
| SW4OFF | 5:0        | R/W | 0x00    | Sets the SW4 output voltage during sleep mode. See <a href="#">Table 77</a> for all possible configurations.   |
| SW4OFF | 6          | R   | 0x00    | Sets the operating output voltage range for SW4 in sleep mode. This bit inherits the value configured in bit SW4[6] during OTP or TBB configuration. See <a href="#">Table 77</a> for all possible configurations. |
| UNUSED | 7          | —   | 0x00    | unused   |

Table 82. Register SW4MODE - ADDR 0x4D

| Name    | Bit number | R/W | Default | Description  |
|---------|------------|-----|---------|--|
| SW4MODE | 3:0        | R/W | 0x08    | Sets the SW4 switching operation mode. See <a href="#">Table 29</a> for all possible configurations. |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name     | Bit number | R/W | Default | Description   |
|----------|------------|-----|---------|---|
| UNUSED   | 4          | —   | 0x00    | unused  |
| SW4OMODE | 5          | R/W | 0x00    | Set status of SW4 when in sleep mode <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = PFM</li> </ul> |
| UNUSED   | 7:6        | —   | 0x00    | unused  |

Table 83. Register SW4CONF - ADDR 0x4E

| Name        | Bit number | R/W | Default | Description   |
|-------------|------------|-----|---------|---|
| SW4ILIM     | 0          | R/W | 0x00    | SW4 current limit level selection <ul style="list-style-type: none"> <li>• 0 = High-level current limit</li> <li>• 1 = Low-level current limit</li> </ul> |
| UNUSED      | 1          | R/W | 0x00    | unused  |
| SW4FREQ     | 3:2        | R/W | 0x00    | SW4 switching frequency selector. See <a href="#">Table 36</a> .  |
| SW4PHASE    | 5:4        | R/W | 0x00    | SW4 phase clock selection. See <a href="#">Table 34</a> .   |
| SW4DVSSPEED | 7:6        | R/W | 0x00    | SW4 DVS speed selection. See <a href="#">Table 33</a> .   |

## 10.4.4.6.2 SW4 external components

Table 84. SW4 external component requirements

| Components                 | Description                    | Values         |
|----------------------------|--------------------------------|----------------|
| $C_{INSW4}$ <sup>[1]</sup> | SW4 input capacitor            | 4.7 $\mu$ F    |
| $C_{IN4HF}$ <sup>[1]</sup> | SW4 decoupling input capacitor | 0.1 $\mu$ F    |
| $C_{OSW4}$ <sup>[1]</sup>  | SW4 output capacitor           | 3 x 22 $\mu$ F |
| $L_{SW4}$                  | SW4 inductor                   | 1.0 $\mu$ H    |

[1] Use X5R or X7R capacitors.

## 10.4.4.6.3 SW4 specifications

Table 85. SW4 electrical characteristics

All parameters are specified at  $T_{MIN}$  to  $T_{MAX}$  (see [Table 4](#)),  $V_{IN} = VIN_{SW4} = 3.6$  V,  $V_{SW4} = 1.8$  V,  $I_{SW4} = 100$  mA,  $SW4\_PWRSTG[2:0] = [101]$ , typical external component values,  $f_{SW4} = 2.0$  MHz, single/dual phase and independent mode unless, otherwise noted. Typical values are characterized at  $V_{IN} = VIN_{SW4} = 3.6$  V,  $V_{SW4} = 1.8$  V,  $I_{SW4} = 100$  mA,  $SW4\_PWRSTG[2:0] = [101]$ , and 25 °C, unless otherwise noted.

| Symbol                        | Parameter                              | Min | Typ                      | Max | Unit |
|-------------------------------|--|-----|--------------------------|-----|------|
| <b>SWITCH MODE SUPPLY SW4</b> |  |     |                          |     |      |
| $V_{INSW4}$                   | Operating input voltage <sup>[1]</sup> | 2.8 | —                        | 4.5 | V    |
| $V_{SW4}$                     | Nominal output voltage                 | —   | <a href="#">Table 77</a> | —   | V    |
|                               | Normal operation<br>VTT mode           | —   | $V_{SW3AFB}/2$           | —   |      |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

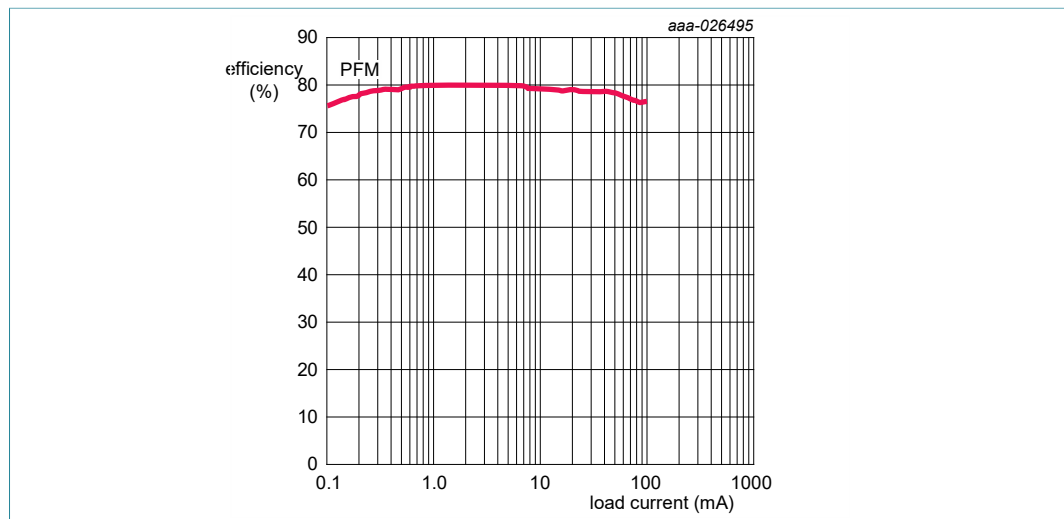
| Symbol  | Parameter  | Min  | Typ | Max  | Unit |
|---|--|------|-----|------|------|
| V <sub>SW4ACC</sub>   | Output voltage accuracy  |      |     |      |      |
|   | PWM, APS, 2.8 V < V <sub>IN</sub> < 4.5 V, 0 < I <sub>SW4</sub> < 1.0 A                              |      |     |      |      |
|   | 0.625 V < V <sub>SW4</sub> < 0.85 V  | -25  | —   | 25   | mV   |
|   | 0.875 V < V <sub>SW4</sub> < 1.975 V   | -3.0 | —   | 3.0  | %    |
|   | 2.0 V < V <sub>SW4</sub> < 3.3 V   | -6.0 | —   | 6.0  | %    |
|   | PFM, steady state, 2.8 V < V <sub>IN</sub> < 4.5 V, 0 < I <sub>SW4</sub> < 50 mA                     |      |     |      |      |
|   | 0.625 V < V <sub>SW4</sub> < 0.675 V   | -65  | —   | 65   | mV   |
|   | 0.7 V < V <sub>SW4</sub> < 0.85 V  | -45  | —   | 45   | mV   |
|   | 0.875 V < V <sub>SW4</sub> < 1.975 V   | -3.0 | —   | 3.0  | %    |
|   | 2.0 V < V <sub>SW4</sub> < 3.3 V   | -3.0 | —   | 3.0  | %    |
| VTT Mode, 2.8 V < V <sub>IN</sub> < 4.5 V, 0 < I <sub>SW4</sub> < 1.0 A |  |      |     |      |      |
|   |  |      |     |      |      |
| I <sub>SW4</sub>  | Rated output load current [2]<br>2.8 V < V <sub>IN</sub> < 4.5 V, 0.625 V < V <sub>SW4</sub> < 3.3 V | —    | —   | 1000 | mA   |
| I <sub>SW4LIM</sub>   | Current limiter peak current detection   |      |     |      | A    |
|   | Current through inductor   |      |     |      |      |
|   | SW4ILIM = 0  | 1.4  | 2.0 | 3.0  |      |
|   | SW4ILIM = 1  | 1.0  | 1.5 | 2.4  |      |
| V <sub>SW4OSH</sub>   | Startup overshoot  |      |     |      | mV   |
|   | I <sub>SW4</sub> = 0.0 mA<br>DVS clk = 25 mV/4 μs, V <sub>IN</sub> = V <sub>INSW4</sub> = 4.5 V      | —    | —   | 66   |      |
| t <sub>ONSW4</sub>  | Turn on time   |      |     |      | μs   |
|   | Enable to 90 % of end value  |      |     |      |      |
|   | I <sub>SW4</sub> = 0.0 mA<br>DVS clk = 25 mV/4 μs, V <sub>IN</sub> = V <sub>INSW4</sub> = 4.5 V      | —    | —   | 500  |      |
| f <sub>SW4</sub>  | Switching frequency  |      |     |      | MHz  |
|   | SW4FREQ[1:0] = 00  | —    | 1.0 | —    |      |
|   | SW4FREQ[1:0] = 01  | —    | 2.0 | —    |      |
|   | SW4FREQ[1:0] = 10  | —    | 4.0 | —    |      |
| η <sub>SW4</sub>  | Efficiency   |      |     |      | %    |
|   | f <sub>SW4</sub> = 2.0 MHz, L <sub>SW4</sub> = 1.0 μH  |      |     |      |      |
|   | PFM, 1.8 V, 1.0 mA   | —    | 81  | —    |      |
|   | PFM, 1.8 V, 50 mA  | —    | 78  | —    |      |
|   | APS, PWM 1.8 V, 200 mA   | —    | 87  | —    |      |
|   | APS, PWM 1.8 V, 500 mA   | —    | 88  | —    |      |
|   | APS, PWM 1.8 V, 1000 mA  | —    | 83  | —    |      |
|   | PWM 0.75 V, 200 mA   | —    | 78  | —    |      |
|   | PWM 0.75 V, 500 mA   | —    | 76  | —    |      |
| PWM 0.75 V, 1000 mA   | —  | 66   | —   |      |      |
| ΔV <sub>SW4</sub>   | Output ripple  | —    | 10  | —    | mV   |
| V <sub>SW4LIR</sub>   | Line regulation (APS, PWM)   | —    | —   | 20   | mV   |
| V <sub>SW4LOR</sub>   | DC load regulation (APS, PWM)  | —    | —   | 20   | mV   |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

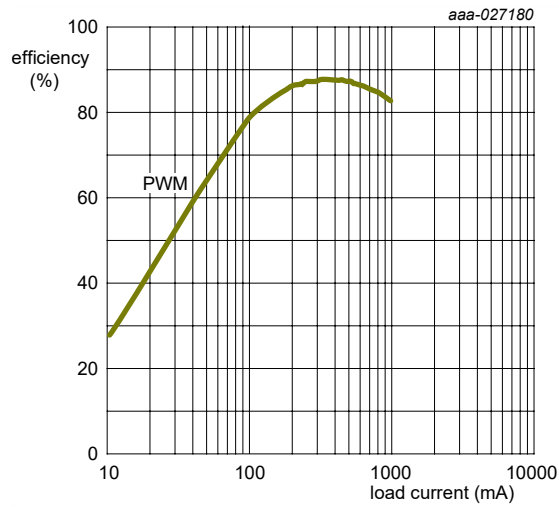
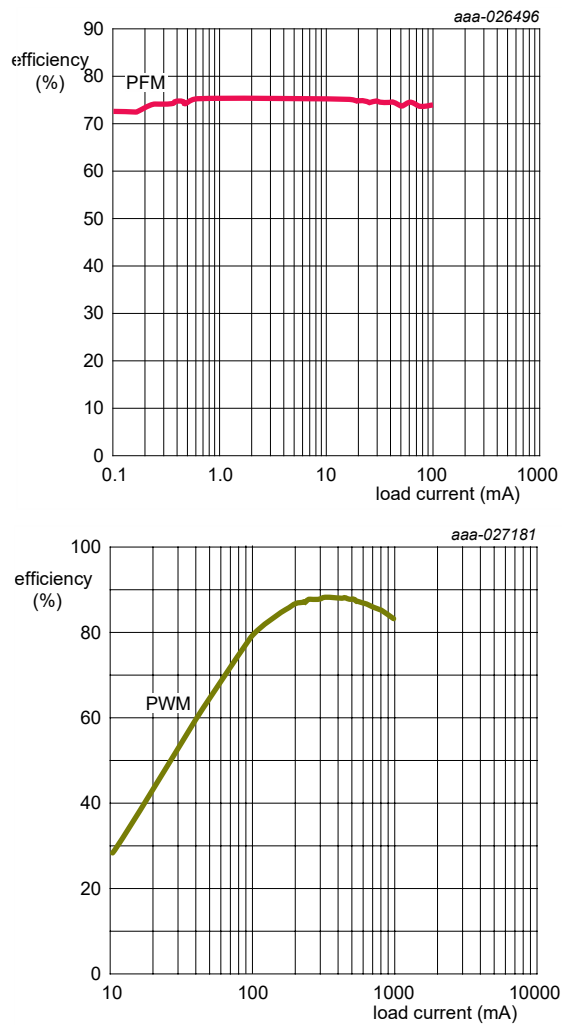
| Symbol        | Parameter  | Min | Typ       | Max | Unit             |
|---------------|--|-----|-----------|-----|------------------|
| $V_{SW4LOTR}$ | Transient load regulation<br>Transient load = 0.0 mA to 500 mA,<br>$di/dt = 100 \text{ mA}/\mu\text{s}$<br>Overshoot<br>Undershoot | —   | —         | 50  | mV               |
| $I_{SW4Q}$    | Quiescent current<br>PFM mode<br>APS mode  | —   | 22<br>145 | —   | $\mu\text{A}$    |
| $R_{ONSW4P}$  | SW4 P-MOSFET $R_{DS(on)}$<br>at $V_{IN} = V_{IN_{SW4}} = 3.3 \text{ V}$  | —   | 236       | 274 | $\text{m}\Omega$ |
| $R_{ONSW4N}$  | SW4 N-MOSFET $R_{DS(on)}$<br>at $V_{IN} = V_{IN_{SW4}} = 3.3 \text{ V}$  | —   | 293       | 378 | $\text{m}\Omega$ |
| $I_{SW4PQ}$   | SW4 P-MOSFET leakage current<br>$V_{IN} = V_{IN_{SW4}} = 4.5 \text{ V}$  | —   | —         | 6.0 | $\mu\text{A}$    |
| $I_{SW4NQ}$   | SW4 N-MOSFET leakage current<br>$V_{IN} = V_{IN_{SW4}} = 4.5 \text{ V}$  | —   | —         | 2.0 | $\mu\text{A}$    |
| $R_{SW4DIS}$  | Discharge resistance   | —   | 600       | —   | $\Omega$         |

[1] When output is set to  $> 2.6 \text{ V}$ , the output follows the input down when  $V_{IN}$  gets near  $2.8 \text{ V}$ .

[2] The higher output voltage available depends on the voltage drop in the conduction path as given by the following equation:  
 $(V_{IN_{SW3x}} - V_{SW3x}) = I_{SW3x} \cdot (\text{DCR of inductor} + R_{ON_{SW3xP}} + \text{PCB trace resistance})$ .



## 14-channel power management integrated circuit (PMIC) for audio/video applications

Figure 26. SW4 efficiency waveforms:  $V_{IN} = 4.2\text{ V}$ ;  $V_{OUT} = 1.8\text{ V}$ ; consumer versionFigure 27. SW4 efficiency waveforms:  $V_{IN} = 4.2\text{ V}$ ;  $V_{OUT} = 1.8\text{ V}$ ; industrial version

### 10.4.5 Boost regulator

SWBST is a boost regulator with a programmable output from 5.0 V to 5.15 V. SWBST can supply the VUSB regulator for the USB PHY in OTG mode, as well as the VBUS voltage. Note that the parasitic leakage path for a boost regulator causes the SWBSTOUT and SWBSTFB voltage to be a Schottky drop below the input voltage whenever SWBST is disabled. The switching NMOS transistor is integrated on-chip.

Figure 28 shows the block diagram and component connection for the boost regulator.

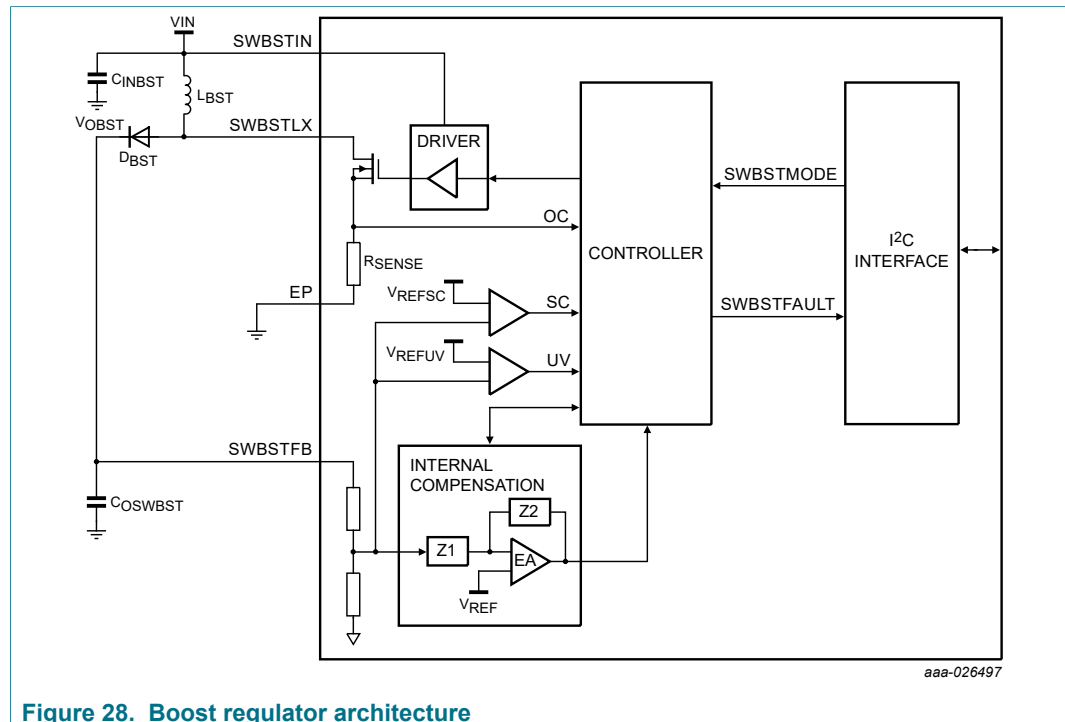


Figure 28. Boost regulator architecture

#### 10.4.5.1 SWBST setup and control

Boost regulator control is done through a single register SWBSTCTL described in Table 86. SWBST is included in the power-up sequence if its OTP power-up timing bits, SWBST\_SEQ[4:0], are not all zeros.

Table 86. Register SWBSTCTL - ADDR 0x66

| Name       | Bit number | R/W | Default | Description   |
|------------|------------|-----|---------|---|
| SWBST1VOLT | 1:0        | R/W | 0x00    | Set the output voltage for SWBST <ul style="list-style-type: none"> <li>00 = 5.000 V</li> <li>01 = 5.050 V</li> <li>10 = 5.100 V</li> <li>11 = 5.150 V</li> </ul>                     |
| SWBST1MODE | 3:2        | R   | 0x02    | Set the switching mode in normal operation <ul style="list-style-type: none"> <li>00 = OFF</li> <li>01 = PFM</li> <li>10 = Auto (default) <sup>[1]</sup></li> <li>11 = APS</li> </ul> |
| UNUSED     | 4          | —   | 0x00    | unused  |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name           | Bit number | R/W | Default | Description   |
|----------------|------------|-----|---------|---|
| SWBST1STBYMODE | 6:5        | R/W | 0x02    | Set the switching mode in standby <ul style="list-style-type: none"> <li>• 00 = OFF</li> <li>• 01 = PFM</li> <li>• 10 = Auto (default)<sup>[1]</sup></li> <li>• 11 = APS</li> </ul> |
| UNUSED         | 7          | —   | 0x00    | unused  |

[1] In auto mode, the controller automatically switches between PFM and APS modes, depending on the load current. The SWBST regulator starts up by default in the auto mode if SWBST is part of the startup sequence.

## 10.4.5.2 SWBST external components

Table 87. SWBST external component requirements

| Components                   | Description                      | Values               |
|------------------------------|----------------------------------|----------------------|
| $C_{INBST}$ <sup>[1]</sup>   | SWBST input capacitor            | 10 $\mu$ F           |
| $C_{INBSTHF}$ <sup>[1]</sup> | SWBST decoupling input capacitor | 0.1 $\mu$ F          |
| $C_{OBST}$ <sup>[1]</sup>    | SWBST output capacitor           | 2 x 22 $\mu$ F       |
| $L_{SBST}$                   | SWBST inductor                   | 2.2 $\mu$ H          |
| $D_{BST}$                    | SWBST boost diode                | 1.0 A, 20 V Schottky |

[1] Use X5R or X7R capacitors.

## 10.4.5.3 SWBST specifications

Table 88. SWBST Electrical Specifications

All parameters are specified at  $T_{MIN}$  to  $T_{MAX}$  (see Table 4),  $V_{IN} = V_{IN_{SWBST}} = 3.6$  V,  $V_{SWBST} = 5.0$  V,  $I_{SWBST} = 100$  mA, typical external component values,  $f_{SWBST} = 2.0$  MHz, otherwise noted. Typical values are characterized at  $V_{IN} = V_{IN_{SWBST}} = 3.6$  V,  $V_{SWBST} = 5.0$  V,  $I_{SWBST} = 100$  mA, and 25 °C, unless otherwise noted.

| Symbol                          | Parameters  | Min  | Typ      | Max        | Units               |
|---------------------------------|---|------|----------|------------|---------------------|
| <b>Switch mode supply SWBST</b> |   |      |          |            |                     |
| $V_{IN_{SWBST}}$                | Input voltage range   | 2.8  | —        | 4.5        | V                   |
| $V_{SWBST}$                     | Nominal output voltage  | —    | Table 86 | —          | V                   |
| $V_{SWBSTACC}$                  | Output voltage accuracy<br>2.8 V $\leq V_{IN} \leq$ 4.5 V<br>0 < $I_{SWBST} < I_{SWBST_{MAX}}$                                      | -4.0 | —        | 3.0        | %                   |
| $\Delta V_{SWBST}$              | Output ripple<br>2.8 V $\leq V_{IN} \leq$ 4.5 V<br>0 < $I_{SWBST} < I_{SWBST_{MAX}}$ , excluding reverse recovery of Schottky diode | —    | —        | 120        | mV <sub>pk-pk</sub> |
| $V_{SWBSTLOR}$                  | DC load regulation<br>0 < $I_{SWBST} < I_{SWBST_{MAX}}$   | —    | 0.5      | —          | mV/mA               |
| $V_{SWBSTLIR}$                  | DC line regulation<br>2.8 V $\leq V_{IN} \leq$ 4.5 V, $I_{SWBST} = I_{SWBST_{MAX}}$   | —    | 50       | —          | mV                  |
| $I_{SWBST}$                     | Continuous load current<br>2.8 V $\leq V_{IN} \leq$ 3.0 V<br>3.0 V $\leq V_{IN} \leq$ 4.5 V   | —    | —        | 500<br>600 | mA                  |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol           | Parameters  | Min  | Typ  | Max  | Units            |
|------------------|---|------|------|------|------------------|
| $I_{SWBSTQ}$     | Quiescent current<br>Auto   | —    | 222  | 289  | $\mu\text{A}$    |
| $R_{DSONBST}$    | MOSFET on resistance  | —    | 206  | 306  | $\text{m}\Omega$ |
| $I_{SWBSTLIM}$   | Peak current limit <sup>[1]</sup>   | 1400 | 2200 | 3200 | $\text{mA}$      |
| $V_{SWBSTOSH}$   | Startup overshoot<br>$I_{SWBST} = 0.0 \text{ mA}$   | —    | —    | 500  | $\text{mV}$      |
| $V_{SWBSTTR}$    | Transient load response<br>$I_{SWBST}$ from 1.0 mA to 100 mA in 1.0 $\mu\text{s}$<br>Maximum transient amplitude      | —    | —    | 300  | $\text{mV}$      |
| $V_{SWBSTTR}$    | Transient load response<br>$I_{SWBST}$ from 100 mA to 1.0 mA in 1.0 $\mu\text{s}$<br>Maximum transient amplitude      | —    | —    | 300  | $\text{mV}$      |
| $t_{SWBSTTR}$    | Transient load response<br>$I_{SWBST}$ from 1.0 mA to 100 mA in 1.0 $\mu\text{s}$<br>Time to settle 80 % of transient | —    | —    | 500  | $\mu\text{s}$    |
| $t_{SWBSTTR}$    | Transient load response<br>$I_{SWBST}$ from 100 mA to 1.0 mA in 1.0 $\mu\text{s}$<br>Time to settle 80 % of transient | —    | —    | 20   | $\text{ms}$      |
| $I_{SWBSTHSQ}$   | NMOS Off leakage<br>$SWBSTIN = 4.5 \text{ V}$ , $SWBSTMODE [1:0] = 00$  | —    | 1.0  | 5.0  | $\mu\text{A}$    |
| $t_{ON_{SWBST}}$ | Turn-on time<br>Enable to 90 % of $V_{SWBST}$ , $I_{SWBST} = 0.0 \text{ mA}$  | —    | —    | 2.0  | $\text{ms}$      |
| $f_{SWBST}$      | Switching frequency   | —    | 2.0  | —    | $\text{MHz}$     |
| $\eta_{SWBST}$   | Efficiency<br>$I_{SWBST} = I_{SWBST_{MAX}}$   | —    | 86   | —    | %                |

[1] Only in auto mode

#### 10.4.6 LDO regulators description

This section describes the LDO regulators provided by the PF4210. All regulators use the main band gap as reference. See [Section 10.3 "Bias and references block description"](#), for more information on the internal reference voltages.

A low-power mode is automatically activated by reducing bias currents when the load current is less than  $I_{Lmax}/5$ . However, the lowest bias currents may be attained by forcing the part into its low-power mode by setting the  $VGENxLPWR$  bit. The use of this bit is only recommended when the load is expected to be less than  $I_{Lmax}/50$ , otherwise performance may be degraded.

When a regulator is disabled, the output is discharged by an internal pull down. The pull down is also activated when  $RESETBMCU$  is low.

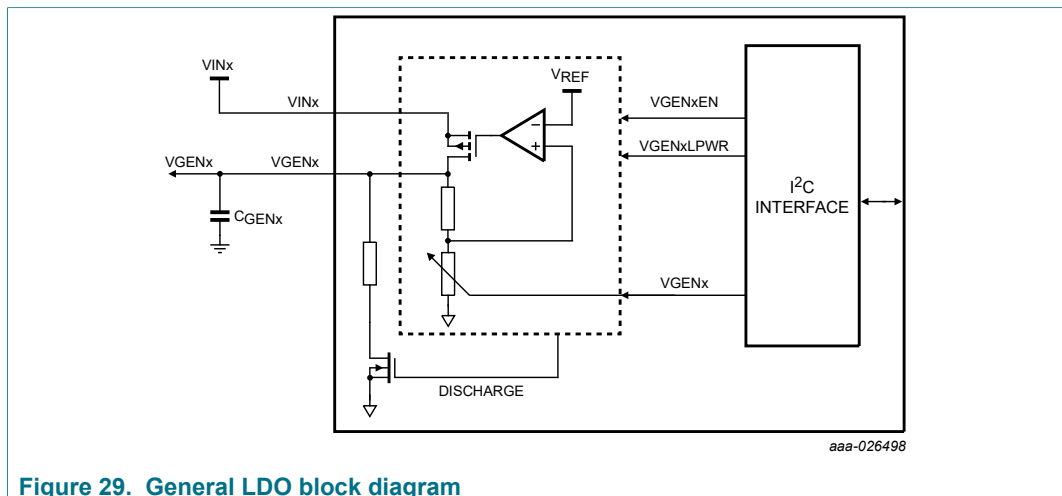


Figure 29. General LDO block diagram

#### 10.4.6.1 Transient response waveforms

Idealized stimulus and response waveforms for transient line and transient load tests are depicted in Figure 30. Note that the transient line and load response refers to the overshoot, or undershoot only, excluding the DC shift.

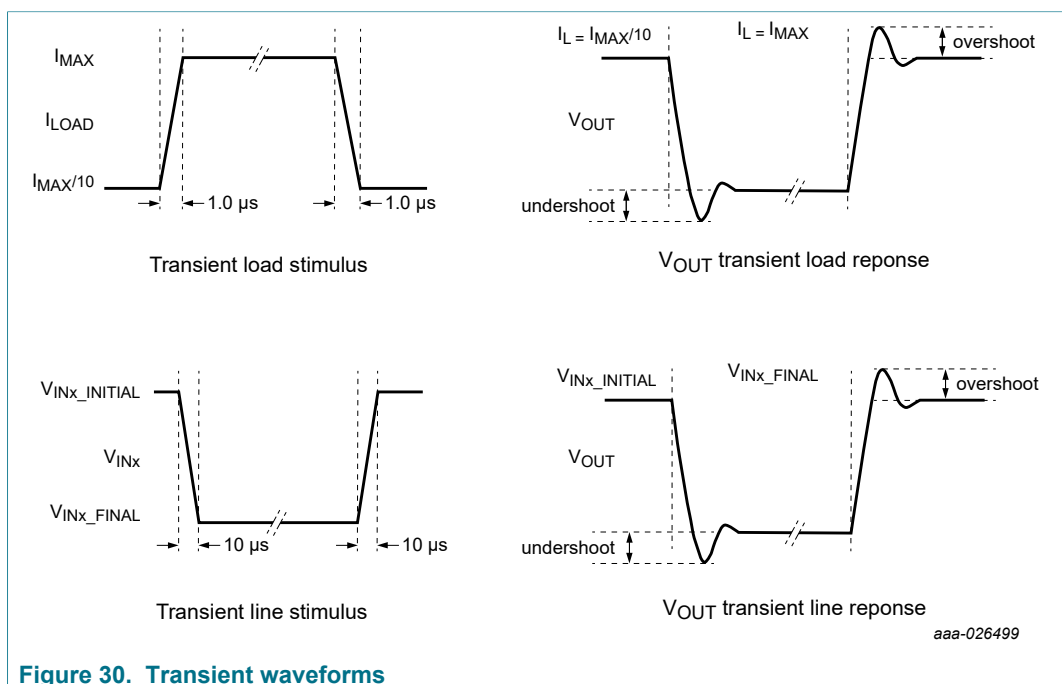


Figure 30. Transient waveforms

#### 10.4.6.2 Short-circuit protection

All general purpose LDOs have short-circuit protection capability. The Short-Circuit Protection (SCP) system includes debounced fault condition detection, regulator shutdown, and processor interrupt generation, to contain failures and minimize the chance of product damage. If a short-circuit condition is detected, the LDO is disabled by resetting its VGENxEN bit, while at the same time, an interrupt VGENxFAULTI is generated to flag the fault to the system processor. The VGENxFAULTI interrupt is maskable through the VGENxFAULTM mask bit.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

The SCP feature is enabled by setting the REGSCPEN bit. If this bit is not set, the regulators do not automatically disable upon a short-circuit detection. However, the current limiter continues to limit the output current of the regulator. By default, the REGSCPEN is not set; therefore, at startup none of the regulators are disabled if an overloaded condition occurs. A fault interrupt, VGENxFAULTI, is generated in an overload condition regardless of the state of the REGSCPEN bit. See [Table 89](#) for SCP behavior configuration.

**Table 89. Short-circuit behavior**

| REGSCPEN[0] | Short-circuit behavior |
|-------------|------------------------|
| 0           | Current limit          |
| 1           | Shutdown               |

**10.4.6.3 LDO regulator control**

Each LDO is fully controlled through its respective VGENxCTL register. This register enables the user to set the LDO output voltage according to [Table 90](#) for VGEN1 and VGEN2; and uses the voltage set point in [Table 91](#) for VGEN3 through VGEN6.

**Table 90. VGEN1, VGEN2 output voltage configuration**

| Set point | VGENx[3:0] | VGENx output (V) |
|-----------|------------|------------------|
| 0         | 0000       | 0.800            |
| 1         | 0001       | 0.850            |
| 2         | 0010       | 0.900            |
| 3         | 0011       | 0.950            |
| 4         | 0100       | 1.000            |
| 5         | 0101       | 1.050            |
| 6         | 0110       | 1.100            |
| 7         | 0111       | 1.150            |
| 8         | 1000       | 1.200            |
| 9         | 1001       | 1.250            |
| 10        | 1010       | 1.300            |
| 11        | 1011       | 1.350            |
| 12        | 1100       | 1.400            |
| 13        | 1101       | 1.450            |
| 14        | 1110       | 1.500            |
| 15        | 1111       | 1.550            |

**Table 91. VGEN3/ 4/ 5/ 6 output voltage configuration**

| Set point | VGENx[3:0] | VGENx output (V) |
|-----------|------------|------------------|
| 0         | 0000       | 1.80             |
| 1         | 0001       | 1.90             |
| 2         | 0010       | 2.00             |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Set point | VGENx[3:0] | VGENx output (V) |
|-----------|------------|------------------|
| 3         | 0011       | 2.10             |
| 4         | 0100       | 2.20             |
| 5         | 0101       | 2.30             |
| 6         | 0110       | 2.40             |
| 7         | 0111       | 2.50             |
| 8         | 1000       | 2.60             |
| 9         | 1001       | 2.70             |
| 10        | 1010       | 2.80             |
| 11        | 1011       | 2.90             |
| 12        | 1100       | 3.00             |
| 13        | 1101       | 3.10             |
| 14        | 1110       | 3.20             |
| 15        | 1111       | 3.30             |

In addition to the output voltage configuration, the LDOs can be enabled or disabled at anytime during normal mode operation, as well as programmed to stay ON or be disabled when the PMIC enters standby mode. Each regulator has associated I<sup>2</sup>C bits for this. [Table 92](#) presents a summary of all valid combinations of the control bits on VGENxCTL register and the expected behavior of the LDO output.

Table 92. LDO control (except VGEN1)

| VGENxEN | VGENxLPWR | VGENxSTBY | STANDBY <sup>[1]</sup> | VGENxOUT  |
|---------|-----------|-----------|------------------------|-----------|
| 0       | X         | X         | X                      | Off       |
| 1       | 0         | 0         | X                      | On        |
| 1       | 1         | 0         | X                      | Low power |
| 1       | X         | 1         | 0                      | On        |
| 1       | 0         | 1         | 1                      | Off       |
| 1       | 1         | 1         | 1                      | Low power |

[1] STANDBY refers to a standby event.

[Table 93](#) through [Table 98](#) provide a description of all registers necessary to operate all six general purpose LDO regulators.

Table 93. Register VGEN1CTL - ADDR 0x6C

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| VGEN1     | 3:0        | R/W | 0x80    | Sets VGEN1 output voltage. See <a href="#">Table 90</a> for all possible configurations.                   |
| VGEN1EN   | 4          | R/W | 0x00    | Enables or disables VGEN1 output <ul style="list-style-type: none"> <li>0 = OFF</li> <li>1 = ON</li> </ul> |
| VGEN1STBY | 5          | R/W | 0x00    | Set VGEN1 output state when in standby. See <a href="#">Table 92</a> .                                     |
| VGEN1LPWR | 6          | R/W | 0x00    | Enable low-power mode for VGEN1. See <a href="#">Table 92</a> .  |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name   | Bit number | R/W | Default | Description |
|--------|------------|-----|---------|-------------|
| UNUSED | 7          | —   | 0x00    | unused      |

Table 94. Register VGEN2CTL - ADDR 0x6D

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| VGEN2     | 3:0        | R/W | 0x80    | Sets VGEN2 output voltage. See <a href="#">Table 90</a> for all possible configurations.                       |
| VGEN2EN   | 4          | R/W | 0x00    | Enables or disables VGEN2 output <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = ON</li> </ul> |
| VGEN2STBY | 5          | R/W | 0x00    | Set VGEN2 output state when in standby. See <a href="#">Table 92</a> .   |
| VGEN2LPWR | 6          | R/W | 0x00    | Enable low-power mode for VGEN2. See <a href="#">Table 92</a> .  |
| UNUSED    | 7          | —   | 0x00    | unused   |

Table 95. Register VGEN3CTL - ADDR 0x6E

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| VGEN3     | 3:0        | R/W | 0x80    | Sets VGEN3 output voltage.<br>See <a href="#">Table 91</a> for all possible configurations.                    |
| VGEN3EN   | 4          | R/W | 0x00    | Enables or disables VGEN3 output <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = ON</li> </ul> |
| VGEN3STBY | 5          | R/W | 0x00    | Set VGEN3 output state when in standby. Refer to <a href="#">Table 92</a> .                                    |
| VGEN3LPWR | 6          | R/W | 0x00    | Enable low-power mode for VGEN3. Refer to <a href="#">Table 92</a> .   |
| UNUSED    | 7          | —   | 0x00    | unused   |

Table 96. Register VGEN4CTL - ADDR 0x6F

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| VGEN4     | 3:0        | R/W | 0x80    | Sets VGEN4 output voltage. See <a href="#">Table 91</a> for all possible configurations.                       |
| VGEN4EN   | 4          | R/W | 0x00    | Enables or disables VGEN4 output <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = ON</li> </ul> |
| VGEN4STBY | 5          | R/W | 0x00    | Set VGEN4 output state when in standby. See <a href="#">Table 92</a> .   |
| VGEN4LPWR | 6          | R/W | 0x00    | Enable low-power mode for VGEN4. See <a href="#">Table 92</a> .  |
| UNUSED    | 7          | —   | 0x00    | unused   |

Table 97. Register VGEN5CTL - ADDR 0x70

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| VGEN5     | 3:0        | R/W | 0x80    | Sets VGEN5 output voltage. See <a href="#">Table 91</a> for all possible configurations.                       |
| VGEN5EN   | 4          | R/W | 0x00    | Enables or disables VGEN5 output <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = ON</li> </ul> |
| VGEN5STBY | 5          | R/W | 0x00    | Set VGEN5 output state when in standby. See <a href="#">Table 92</a> .   |
| VGEN5LPWR | 6          | R/W | 0x00    | Enable low-power mode for VGEN5. See <a href="#">Table 92</a> .  |
| UNUSED    | 7          | —   | 0x00    | unused   |

Table 98. Register VGEN6CTL - ADDR 0x71

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| VGEN6     | 3:0        | R/W | 0x80    | Sets VGEN6 output voltage. See <a href="#">Table 91</a> for all possible configurations.                       |
| VGEN6EN   | 4          | R/W | 0x00    | Enables or disables VGEN6 output <ul style="list-style-type: none"> <li>• 0 = OFF</li> <li>• 1 = ON</li> </ul> |
| VGEN6STBY | 5          | R/W | 0x00    | Set VGEN6 output state when in standby. See <a href="#">Table 92</a> .   |
| VGEN6LPWR | 6          | R/W | 0x00    | Enable low-power mode for VGEN6. See <a href="#">Table 92</a> .  |
| UNUSED    | 7          | —   | 0x00    | unused   |

#### 10.4.6.4 External components

[Table 99](#) lists the typical component values for the general purpose LDO regulators.

Table 99. LDO external components

| Regulator | Output capacitor ( $\mu\text{F}$ ) <sup>[1]</sup> |
|-----------|---|
| VGEN1     | 2.2   |
| VGEN2     | 4.7   |
| VGEN3     | 2.2   |
| VGEN4     | 4.7   |
| VGEN5     | 2.2   |
| VGEN6     | 2.2   |

[1] Use X5R/X7R ceramic capacitors.

## 10.4.6.5 LDO specifications

## 10.4.6.5.1 VGEN1

Table 100. VGEN1 electrical characteristics

All parameters are specified at  $T_{MIN}$  to  $T_{MAX}$  (see Table 4),  $V_{IN} = 3.6$  V,  $V_{IN1} = 3.0$  V,  $V_{GEN1}[3:0] = 1111$ ,  $I_{GEN1} = 10$  mA, typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6$  V,  $V_{IN1} = 3.0$  V,  $V_{GEN1}[3:0] = 1111$ ,  $I_{GEN1} = 10$  mA, and 25 °C, unless otherwise noted.

| Symbol                        | Parameter  | Min         | Typ                  | Max                  | Unit    |
|-------------------------------|--|-------------|----------------------|----------------------|---------|
| <b>VGEN1</b>                  |  |             |                      |                      |         |
| $V_{IN1}$                     | Operating input voltage  | 1.75        | —                    | 3.40                 | V       |
| $V_{GEN1NOM}$                 | Nominal output voltage   | —           | Table 90             | —                    | V       |
| $I_{GEN1}$                    | Operating load current   | 0.0         | —                    | 100                  | mA      |
| <b>VGEN1 DC</b>               |  |             |                      |                      |         |
| $V_{GEN1TOL}$                 | Output voltage tolerance<br>1.75 V < $V_{IN1}$ < 3.4 V<br>0.0 mA < $I_{GEN1}$ < 100 mA<br>$V_{GEN1}[3:0] = 0000$ to 1111             | -3.0        | —                    | 3.0                  | %       |
| $V_{GEN1LOR}$                 | Load regulation<br>( $V_{GEN1}$ at $I_{GEN1} = 100$ mA) - ( $V_{GEN1}$ at $I_{GEN1} = 0.0$ mA)<br>For any 1.75 V < $V_{IN1}$ < 3.4 V | —           | 0.15                 | —                    | mV/mA   |
| $V_{GEN1LIR}$                 | Line regulation<br>( $V_{GEN1}$ at $V_{IN1} = 3.4$ V) - ( $V_{GEN1}$ at $V_{IN1} = 1.75$ V)<br>For any 0.0 mA < $I_{GEN1}$ < 100 mA  | —           | 0.30                 | —                    | mV/mA   |
| $I_{GEN1LIM}$                 | Current limit<br>$I_{GEN1}$ when VGEN1 is forced to $V_{GEN1NOM}/2$  | 122         | 167                  | 200                  | mA      |
| $I_{GEN1OCP}$                 | Overcurrent protection threshold<br>$I_{GEN1}$ required to cause the SCP function to disable LDO when REGSCPEN = 1                   | 115         | —                    | 200                  | mA      |
| $I_{GEN1Q}$                   | Quiescent current<br>No load, change in $I_{VIN}$ and $I_{VIN1}$<br>When VGEN1 enabled   | —           | 14                   | —                    | μA      |
| <b>VGEN1 AC and transient</b> |  |             |                      |                      |         |
| $PSRR_{VGEN1}$                | PSRR <sup>[1]</sup><br>$I_{GEN1} = 75$ mA, 20 Hz to 20 kHz<br>$V_{GEN1}[3:0] = 0000$ to 1101<br>$V_{GEN1}[3:0] = 1110, 1111$         | 50<br>37    | 60<br>45             | —<br>—               | dB      |
| $NOISE_{VGEN1}$               | Output noise density<br>$V_{IN1} = 1.75$ V, $I_{GEN1} = 75$ mA<br>100 Hz to < 1.0 kHz<br>1.0 kHz to < 10 kHz<br>10 kHz to 1.0 MHz    | —<br>—<br>— | -108<br>-118<br>-124 | -100<br>-108<br>-112 | dBV/√Hz |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                | Parameter   | Min    | Typ    | Max          | Unit  |
|-----------------------|---|--------|--------|--------------|-------|
| SLWR <sub>VGEN1</sub> | Turn on slew rate<br>10 % to 90 % of end value<br>1.75 V ≤ V <sub>IN1</sub> ≤ 3.4 V, I <sub>GEN1</sub> = 0.0 mA<br>VGEN1[3:0] = 0000 to 0111<br>VGEN1[3:0] = 1000 to 1111   | —<br>— | —<br>— | 12.5<br>16.5 | mV/μs |
| GEN1 <sub>tON</sub>   | Turn on time<br>Enable to 90 % of end value, V <sub>IN1</sub> = 1.75 V,<br>3.4 V<br>I <sub>GEN1</sub> = 0.0 mA  | 60     | —      | 500          | μs    |
| GEN1 <sub>OSHT</sub>  | Startup overshoot<br>V <sub>IN1</sub> = 1.75 V, 3.4 V, I <sub>GEN1</sub> = 0.0 mA   | —      | 1.0    | 2.0          | %     |
| V <sub>GEN1LOTR</sub> | Transient load response<br>V <sub>IN1</sub> = 1.75 V, 3.4 V<br>I <sub>GEN1</sub> = 10 mA to 100 mA in 1.0 μs. Peak<br>of overshoot or undershoot of VGEN1 with<br>respect to final value<br>Peak of overshoot or undershoot of VGEN1<br>with respect to final value. See <a href="#">Figure 30</a>                                      | —      | —      | 3.0          | %     |
| V <sub>GEN1LITR</sub> | Transient line response<br>I <sub>GEN1</sub> = 75 mA<br>VIN1 <sub>INITIAL</sub> = 1.75 V to VIN1 <sub>FINAL</sub> = 2.25 V<br>for VGEN1[3:0] = 0000 to 1101<br>VIN1 <sub>INITIAL</sub> = V <sub>GEN1</sub> + 0.3 V to VIN1 <sub>FINAL</sub> =<br>V <sub>GEN1</sub> + 0.8 V for VGEN1[3:0] = 1110, 1111<br>See <a href="#">Figure 30</a> | —      | 5.0    | 8.0          | mV    |

[1] The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test.

## 10.4.6.5.2 VGEN2

**Table 101. VGEN2 electrical characteristics**

All parameters are specified at T<sub>MIN</sub> to T<sub>MAX</sub> (see [Table 4](#)), V<sub>IN</sub> = 3.6 V, V<sub>IN1</sub> = 3.0 V, V<sub>GEN2</sub>[3:0] = 1111, I<sub>GEN2</sub> = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V<sub>IN</sub> = 3.6 V, V<sub>IN1</sub> = 3.0 V, V<sub>GEN2</sub>[3:0] = 1111, I<sub>GEN2</sub> = 10 mA and 25 °C, unless otherwise noted.

| Symbol                        | Parameter   | Min  | Typ                      | Max  | Unit |
|-------------------------------|---|------|--------------------------|------|------|
| <b>VGEN2</b>                  |   |      |                          |      |      |
| V <sub>IN1</sub>              | Operating input voltage   | 1.75 | —                        | 3.40 | V    |
| V <sub>GEN2NOM</sub>          | Nominal output voltage  | —    | <a href="#">Table 90</a> | —    | V    |
| I <sub>GEN2</sub>             | Operating load current  | 0.0  | —                        | 250  | mA   |
| <b>VGEN2 active mode - DC</b> |   |      |                          |      |      |
| V <sub>GEN2TOL</sub>          | Output voltage tolerance<br>1.75 V < V <sub>IN1</sub> < 3.4 V<br>0.0 mA < I <sub>GEN2</sub> < 250 mA<br>VGEN2[3:0] = 0000 to 1111 | −3.0 | —                        | 3.0  | %    |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                        | Parameter  | Min         | Typ                  | Max                  | Unit    |
|-------------------------------|--|-------------|----------------------|----------------------|---------|
| V <sub>GEN2LOR</sub>          | Load regulation<br>(V <sub>GEN2</sub> at I <sub>GEN2</sub> = 250 mA) – (V <sub>GEN2</sub> at I <sub>GEN2</sub> = 0.0 mA)<br>For any 1.75 V < V <sub>IN1</sub> < 3.4 V  | —           | 0.05                 | —                    | mV/mA   |
| V <sub>GEN2LIR</sub>          | Line regulation<br>(V <sub>GEN2</sub> at V <sub>IN1</sub> = 3.4 V) – (V <sub>GEN2</sub> at V <sub>IN1</sub> = 1.75 V)<br>For any 0.0 mA < I <sub>GEN2</sub> < 250 mA   | —           | 0.50                 | —                    | mV/mA   |
| I <sub>GEN2LIM</sub>          | Current limit<br>I <sub>GEN2</sub> when V <sub>GEN2</sub> is forced to V <sub>GEN2NOM</sub> /2   | 305         | 417                  | 510                  | mA      |
| I <sub>GEN2OCP</sub>          | Overcurrent protection threshold<br>I <sub>GEN2</sub> required to cause the SCP function to disable LDO when REGSCPEN = 1  | 290         | —                    | 500                  | mA      |
| I <sub>GEN2Q</sub>            | Quiescent current<br>No load, change in I <sub>VIN</sub> and I <sub>VIN1</sub><br>When V <sub>GEN2</sub> enabled   | —           | 16                   | —                    | μA      |
| <b>VGEN2 AC and transient</b> |  |             |                      |                      |         |
| PSRR <sub>VGEN2</sub>         | PSRR <sup>[1]</sup><br>I <sub>GEN2</sub> = 187.5 mA, 20 Hz to 20 kHz<br>V <sub>GEN2</sub> [3:0] = 0000 to 1101<br>V <sub>GEN2</sub> [3:0] = 1110, 1111   | 50<br>37    | 60<br>45             | —<br>—               | dB      |
| NOISE <sub>VGEN2</sub>        | Output noise density<br>V <sub>IN1</sub> = 1.75 V, I <sub>GEN2</sub> = 187.5 mA<br>100 Hz to < 1.0 kHz<br>1.0 kHz to < 10 kHz<br>10 kHz to 1.0 MHz   | —<br>—<br>— | -108<br>-118<br>-124 | -100<br>-108<br>-112 | dBV/√Hz |
| SLWR <sub>VGEN2</sub>         | Turn on slew rate<br>10 % to 90 % of end value<br>1.75 V ≤ V <sub>IN1</sub> ≤ 3.4 V, I <sub>GEN2</sub> = 0.0 mA<br>V <sub>GEN2</sub> [3:0] = 0000 to 0111<br>V <sub>GEN2</sub> [3:0] = 1000 to 1111                          | —<br>—      | —<br>—               | 12.5<br>16.5         | mV/μs   |
| GEN2 <sub>iON</sub>           | Turn on time<br>Enable to 90 % of end value, V <sub>IN1</sub> = 1.75 V, 3.4 V<br>I <sub>GEN2</sub> = 0.0 mA  | 60          | —                    | 500                  | μs      |
| GEN2 <sub>iOFF</sub>          | Turn off time<br>Disable to 10 % of initial value, V <sub>IN1</sub> = 1.75 V<br>I <sub>GEN2</sub> = 0.0 mA   | —           | —                    | 10                   | ms      |
| GEN2 <sub>OSHT</sub>          | Startup overshoot<br>V <sub>IN1</sub> = 1.75 V, 3.4 V, I <sub>GEN2</sub> = 0.0 mA  | —           | 1.0                  | 2.0                  | %       |
| V <sub>GEN2LOTR</sub>         | Transient load response<br>V <sub>IN1</sub> = 1.75 V, 3.4 V<br>I <sub>GEN2</sub> = 25 to 250 mA in 1.0 μs<br>Peak of overshoot or undershoot of V <sub>GEN2</sub> with respect to final value. See <a href="#">Figure 30</a> | —           | —                    | 3.0                  | %       |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                | Parameter  | Min | Typ | Max | Unit |
|-----------------------|--|-----|-----|-----|------|
| V <sub>GEN2LITR</sub> | Transient line response<br>I <sub>GEN2</sub> = 187.5 mA<br>VIN1 <sub>INITIAL</sub> = 1.75 V to VIN1 <sub>FINAL</sub> = 2.25 V<br>for VGEN2[3:0] = 0000 to 1101<br>VIN1 <sub>INITIAL</sub> = V <sub>GEN2</sub> + 0.3 V to VIN1 <sub>FINAL</sub> =<br>V <sub>GEN2</sub> + 0.8 V for VGEN2[3:0] = 1110, 1111<br>See <a href="#">Figure 30</a> | —   | 5.0 | 8.0 | mV   |

[1] The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test.

## 10.4.6.5.3 VGEN3

**Table 102. VGEN3 electrical characteristics**

All parameters are specified at T<sub>MIN</sub> to T<sub>MAX</sub> (see [Table 4](#)), V<sub>IN</sub> = 3.6 V, V<sub>IN2</sub> = 3.6 V, V<sub>GEN3</sub>[3:0] = 1111, I<sub>GEN3</sub> = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V<sub>IN</sub> = 3.6 V, V<sub>IN2</sub> = 3.6 V, V<sub>GEN3</sub>[3:0] = 1111, I<sub>GEN3</sub> = 10 mA, and 25 °C, unless otherwise noted.

| Symbol               | Parameter   | Min                                    | Typ                      | Max        | Unit  |
|----------------------|---|--|--------------------------|------------|-------|
| <b>VGEN3</b>         |   |  |                          |            |       |
| V <sub>IN2</sub>     | Operating input voltage <sup>[1]</sup><br>1.8 V ≤ VGEN3 <sub>NOM</sub> ≤ 2.5 V<br>2.6 V ≤ VGEN3 <sub>NOM</sub> ≤ 3.3 V  | 2.8<br>VGEN3 <sub>NOM</sub><br>+ 0.250 | —                        | 3.6<br>3.6 | V     |
| VGEN3 <sub>NOM</sub> | Nominal output voltage  | —                                      | <a href="#">Table 91</a> | —          | V     |
| I <sub>GEN3</sub>    | Operating load current  | 0.0                                    | —                        | 100        | mA    |
| <b>VGEN3 DC</b>      |   |  |                          |            |       |
| VGEN3TOL             | Output voltage tolerance<br>VIN2 <sub>MIN</sub> < V <sub>IN2</sub> < 3.6 V<br>0.0 mA < I <sub>GEN3</sub> < 100 mA<br>VGEN3[3:0] = 0000 to 1111  | −3.0                                   | —                        | 3.0        | %     |
| VGEN3LOR             | Load regulation<br>(V <sub>GEN3</sub> at I <sub>GEN3</sub> = 100 mA) − (V <sub>GEN3</sub> at I <sub>GEN3</sub><br>= 0.0 mA)<br>For any VIN2 <sub>MIN</sub> < V <sub>IN2</sub> < 3.6 V | —                                      | 0.07                     | —          | mV/mA |
| VGEN3LIR             | Line regulation<br>(V <sub>GEN3</sub> at V <sub>IN2</sub> = 3.6 V) − (V <sub>GEN3</sub> at VIN2 <sub>MIN</sub> )<br>For any 0.0 mA < I <sub>GEN3</sub> < 100 mA                       | —                                      | 0.8                      | —          | mV/mA |
| I <sub>GEN3LIM</sub> | Current limit<br>I <sub>GEN3</sub> when VGEN3 is forced to<br>VGEN3 <sub>NOM</sub> /2   | 127                                    | 167                      | 200        | mA    |
| I <sub>GEN3OCP</sub> | Overcurrent protection threshold<br>I <sub>GEN3</sub> required to cause the SCP function to<br>disable LDO when REGSCPEN = 1  | 120                                    | —                        | 200        | mA    |
| I <sub>GEN3Q</sub>   | Quiescent current<br>No load, change in I <sub>VIN</sub> and I <sub>VIN2</sub><br>When VGEN3 enabled  | —                                      | 13                       | —          | μA    |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                        | Parameter  | Min              | Typ                  | Max                          | Unit    |
|-------------------------------|--|------------------|----------------------|------------------------------|---------|
| <b>VGEN3 AC and transient</b> |  |                  |                      |                              |         |
| PSRR <sub>VGEN3</sub>         | PSRR <sup>[2]</sup><br>I <sub>GEN3</sub> = 75 mA, 20 Hz to 20 kHz<br>VGEN3[3:0] = 0000 to 1110, V <sub>IN2</sub> = VIN2 <sub>MIN</sub> + 100 mV<br>VGEN3[3:0] = 0000 to 1000, V <sub>IN2</sub> = VGEN3 <sub>NOM</sub> + 1.0 V  | 35<br>55         | 40<br>60             | —<br>—                       | dB      |
| NOISE <sub>VGEN3</sub>        | Output noise density<br>V <sub>IN2</sub> = VIN2 <sub>MIN</sub> , I <sub>GEN3</sub> = 75 mA<br>100 Hz to < 1.0 kHz<br>1.0 kHz to < 10 kHz<br>10 kHz to 1.0 MHz  | —<br>—<br>—      | -114<br>-129<br>-135 | -102<br>-123<br>-130         | dBV/√Hz |
| SLWR <sub>VGEN3</sub>         | Turn on slew rate<br>10 % to 90 % of end value<br>VIN2 <sub>MIN</sub> ≤ V <sub>IN2</sub> ≤ 3.6 V, I <sub>GEN3</sub> = 0.0 mA<br>VGEN3[3:0] = 0000 to 0011<br>VGEN3[3:0] = 0100 to 0111<br>VGEN3[3:0] = 1000 to 1011<br>VGEN3[3:0] = 1100 to 1111   | —<br>—<br>—<br>— | —<br>—<br>—<br>—     | 22.0<br>26.5<br>30.5<br>34.5 | mV/μs   |
| GEN3 <sub>ION</sub>           | Turn on time<br>Enable to 90 % of end value, V <sub>IN2</sub> = VIN2 <sub>MIN</sub> , 3.6 V<br>I <sub>GEN3</sub> = 0.0 mA  | 60               | —                    | 500                          | μs      |
| GEN3 <sub>IOFF</sub>          | Turn off time<br>Disable to 10 % of initial value, V <sub>IN2</sub> = VIN2 <sub>MIN</sub><br>I <sub>GEN3</sub> = 0.0 mA  | —                | —                    | 10                           | ms      |
| GEN3 <sub>OSHT</sub>          | Startup overshoot<br>V <sub>IN2</sub> = VIN2 <sub>MIN</sub> , 3.6 V, I <sub>GEN3</sub> = 0.0 mA  | —                | 1.0                  | 2.0                          | %       |
| V <sub>GEN3LOTR</sub>         | Transient load response<br>V <sub>IN2</sub> = VIN2 <sub>MIN</sub> , 3.6 V<br>I <sub>GEN3</sub> = 10 to 100 mA in 1.0 μs<br>Peak of overshoot or undershoot of VGEN3 with respect to final value. See <a href="#">Figure 30</a>   | —                | —                    | 3.0                          | %       |
| V <sub>GEN3LITR</sub>         | Transient line response<br>I <sub>GEN3</sub> = 75 mA<br>VIN2 <sub>INITIAL</sub> = 2.8 V to VIN2 <sub>FINAL</sub> = 3.3 V for VGEN3[3:0] = 0000 to 0111<br>VIN2 <sub>INITIAL</sub> = V <sub>GEN3</sub> + 0.3 V to VIN2 <sub>FINAL</sub> = V <sub>GEN3</sub> + 0.8 V for VGEN3[3:0] = 1000 to 1010<br>VIN2 <sub>INITIAL</sub> = V <sub>GEN3</sub> + 0.25 V to VIN2 <sub>FINAL</sub> = 3.6 V for VGEN3[3:0] = 1011 to 1111<br>See <a href="#">Figure 30</a> | —                | 5.0                  | 8.0                          | mV      |

[1] When the LDO output voltage is set above 2.6 V, the minimum allowed input voltage needs to be at least the output voltage plus 0.25 V, for proper regulation due to the dropout voltage generated through the internal LDO transistor.

[2] The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. VIN2<sub>MIN</sub> refers to the minimum allowed input voltage for a particular output voltage.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

## 10.4.6.5.4 VGEN4

**Table 103. VGEN4 electrical characteristics**

All parameters are specified at  $T_{MIN}$  to  $T_{MAX}$  (see Table 4),  $V_{IN} = 3.6$  V,  $V_{IN2} = 3.6$  V,  $V_{GEN4}[3:0] = 1111$ ,  $I_{GEN4} = 10$  mA, typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6$  V,  $V_{IN2} = 3.6$  V,  $V_{GEN4}[3:0] = 1111$ ,  $I_{GEN4} = 10$  mA, and 25 °C, unless otherwise noted.

| Symbol                        | Parameter   | Min                                    | Typ                  | Max                  | Unit                    |
|-------------------------------|---|--|----------------------|----------------------|-------------------------|
| <b>VGEN4</b>                  |   |  |                      |                      |                         |
| $V_{IN2}$                     | Operating input voltage <sup>[1]</sup><br>1.8 V $\leq$ VGEN4 <sub>NOM</sub> $\leq$ 2.5 V<br>2.6 V $\leq$ VGEN4 <sub>NOM</sub> $\leq$ 3.3 V  | 2.8<br>VGEN4 <sub>NOM</sub><br>+ 0.250 | —                    | 3.6<br>3.6           | V                       |
| VGEN4 <sub>NOM</sub>          | Nominal output voltage  | —                                      | Table 91             | —                    | V                       |
| $I_{GEN4}$                    | Operating load current  | 0.0                                    | —                    | 350                  | mA                      |
| <b>VGEN4 DC</b>               |   |  |                      |                      |                         |
| $V_{GEN4TOL}$                 | Output voltage tolerance<br>$V_{IN2_{MIN}} < V_{IN2} < 3.6$ V<br>$0.0$ mA $< I_{GEN4} < 350$ mA<br>VGEN4[3:0] = 0000 to 1111  | -3.0                                   | —                    | 3.0                  | %                       |
| $V_{GEN4LOR}$                 | Load regulation<br>( $V_{GEN4}$ at $I_{GEN4} = 350$ mA) - ( $V_{GEN4}$ at $I_{GEN4} = 0.0$ mA)<br>For any $V_{IN2_{MIN}} < V_{IN2} < 3.6$ V   | —                                      | 0.07                 | —                    | mV/mA                   |
| $V_{GEN4LIR}$                 | Line regulation<br>( $V_{GEN4}$ at 3.6 V) - ( $V_{GEN4}$ at $V_{IN2_{MIN}}$ )<br>For any $0.0$ mA $< I_{GEN4} < 350$ mA   | —                                      | 0.80                 | —                    | mV/mA                   |
| $I_{GEN4LIM}$                 | Current limit<br>$I_{GEN4}$ when VGEN4 is forced to<br>VGEN4 <sub>NOM</sub> /2  | 435                                    | 584.5                | 700                  | mA                      |
| $I_{GEN4OCP}$                 | Overcurrent protection threshold<br>$I_{GEN4}$ required to cause the SCP function to<br>disable LDO when REGSCPEN = 1   | 420                                    | —                    | 700                  | mA                      |
| $I_{GEN4Q}$                   | Quiescent current<br>No load, change in $I_{VIN}$ and $I_{VIN2}$<br>When VGEN4 enabled  | —                                      | 13                   | —                    | $\mu$ A                 |
| <b>VGEN4 AC and transient</b> |   |  |                      |                      |                         |
| PSRR <sub>VGEN4</sub>         | PSRR <sup>[2]</sup><br>$I_{GEN4} = 262.5$ mA, 20 Hz to 20 kHz<br>VGEN4[3:0] = 0000 to 1110, $V_{IN2} = V_{IN2_{MIN}}$<br>+ 100 mV<br>VGEN4[3:0] = 0000 to 1000, $V_{IN2} =$<br>VGEN4 <sub>NOM</sub> + 1.0 V | 35<br>55                               | 40<br>60             | —<br>—               | dB                      |
| NOISE <sub>VGEN4</sub>        | Output noise density<br>$V_{IN2} = V_{IN2_{MIN}}$ , $I_{GEN4} = 262.5$ mA<br>100 Hz to <1.0 kHz<br>1.0 kHz to <10 kHz<br>10 kHz to 1.0 MHz  | —<br>—<br>—                            | -114<br>-129<br>-135 | -102<br>-123<br>-130 | dBV/ $\sqrt{\text{Hz}}$ |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                | Parameter   | Min | Typ | Max                          | Unit        |
|-----------------------|---|-----|-----|------------------------------|-------------|
| SLWR <sub>VGEN4</sub> | Turn on slew rate<br>10 % to 90 % of end value<br>$V_{IN2_{MIN}} \leq V_{IN2} \leq 3.6 \text{ V}$ , $I_{GEN4} = 0.0 \text{ mA}$<br>VGEN4[3:0] = 0000 to 0011<br>VGEN4[3:0] = 0100 to 0111<br>VGEN4[3:0] = 1000 to 1011<br>VGEN4[3:0] = 1100 to 1111   | —   | —   | 22.0<br>26.5<br>30.5<br>34.5 | mV/ $\mu$ s |
| GEN4 <sub>ION</sub>   | Turn on time<br>Enable to 90 % of end value, $V_{IN2} = V_{IN2_{MIN}}$ , 3.6 V<br>$I_{GEN4} = 0.0 \text{ mA}$   | 60  | —   | 500                          | $\mu$ s     |
| GEN4 <sub>IOFF</sub>  | Turn off time<br>Disable to 10 % of initial value, $V_{IN2} = V_{IN2_{MIN}}$<br>$I_{GEN4} = 0.0 \text{ mA}$   | —   | —   | 10                           | ms          |
| GEN4 <sub>OSHT</sub>  | Startup overshoot<br>$V_{IN2} = V_{IN2_{MIN}}$ , 3.6 V, $I_{GEN4} = 0.0 \text{ mA}$   | —   | 1.0 | 2.0                          | %           |
| V <sub>GEN4LOTR</sub> | Transient load response<br>$V_{IN2} = V_{IN2_{MIN}}$ , 3.6 V<br>$I_{GEN4} = 35$ to 350 mA in 1.0 $\mu$ s<br>Peak of overshoot or undershoot of VGEN4 with respect to final value. See <a href="#">Figure 30</a>   | —   | —   | 3.0                          | %           |
| V <sub>GEN4LITR</sub> | Transient line response<br>$I_{GEN4} = 262.5 \text{ mA}$<br>$V_{IN2_{INITIAL}} = 2.8 \text{ V}$ to $V_{IN2_{FINAL}} = 3.3 \text{ V}$ for VGEN4[3:0] = 0000 to 0111<br>$V_{IN2_{INITIAL}} = V_{GEN4} + 0.3 \text{ V}$ to $V_{IN2_{FINAL}} = V_{GEN4} + 0.8 \text{ V}$ for VGEN4[3:0] = 1000 to 1010<br>$V_{IN2_{INITIAL}} = V_{GEN4} + 0.25 \text{ V}$ to $V_{IN2_{FINAL}} = 3.6 \text{ V}$ for VGEN4[3:0] = 1011 to 1111<br>See <a href="#">Figure 30</a> | —   | 5.0 | 8.0                          | mV          |

- [1] When the LDO output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
- [2] The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test.  $V_{IN2_{MIN}}$  refers to the minimum allowed input voltage for a particular output voltage.

## 10.4.6.5.5 VGEN5

Table 104. VGEN5 electrical characteristics

All parameters are specified at  $T_{MIN}$  to  $T_{MAX}$  (see [Table 4](#)),  $V_{IN} = 3.6 \text{ V}$ ,  $V_{IN3} = 3.6 \text{ V}$ ,  $V_{GEN5[3:0]} = 1111$ ,  $I_{GEN5} = 10 \text{ mA}$ , typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6 \text{ V}$ ,  $V_{IN3} = 3.6 \text{ V}$ ,  $V_{GEN5[3:0]} = 1111$ ,  $I_{GEN5} = 10 \text{ mA}$ , and 25 °C, unless otherwise noted.

| Symbol       | Parameter | Min | Typ | Max | Unit |
|--------------|-----------|-----|-----|-----|------|
| <b>VGEN5</b> |           |     |     |     |      |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                        | Parameter  | Min                             | Typ                  | Max                          | Unit                    |
|-------------------------------|--|---------------------------------|----------------------|------------------------------|-------------------------|
| $V_{IN3}$                     | Operating input voltage <sup>[1]</sup><br>$1.8\text{ V} \leq V_{GEN5_{NOM}} \leq 2.5\text{ V}$<br>$2.6\text{ V} \leq V_{GEN5_{NOM}} \leq 3.3\text{ V}$   | 2.8<br>$V_{GEN5_{NOM}} + 0.250$ | —                    | 4.5<br>4.5                   | V                       |
| $V_{GEN5_{NOM}}$              | Nominal output voltage   | —                               | Table 91             | —                            | V                       |
| $I_{GEN5}$                    | Operating load current   | 0.0                             | —                    | 100                          | mA                      |
| <b>VGEN5 active mode – DC</b> |  |                                 |                      |                              |                         |
| $V_{GEN5_{TOL}}$              | Output voltage tolerance<br>$V_{IN3_{MIN}} < V_{IN3} < 4.5\text{ V}$<br>$0.0\text{ mA} < I_{GEN5} < 100\text{ mA}$<br>$V_{GEN5[3:0]} = 0000\text{ to }1111$  | –3.0                            | —                    | 3.0                          | %                       |
| $V_{GEN5_{LOR}}$              | Load regulation<br>$(V_{GEN5}\text{ at }I_{GEN5} = 100\text{ mA}) - (V_{GEN5}\text{ at }I_{GEN5} = 0.0\text{ mA})$<br>For any $V_{IN3_{MIN}} < V_{IN3} < 4.5\text{ mV}$  | —                               | 0.10                 | —                            | mV/mA                   |
| $V_{GEN5_{LIR}}$              | Line regulation<br>$(V_{GEN5}\text{ at }V_{IN3} = 4.5\text{ V}) - (V_{GEN5}\text{ at }V_{IN3_{MIN}})$<br>For any $0.0\text{ mA} < I_{GEN5} < 100\text{ mA}$  | —                               | 0.50                 | —                            | mV/mA                   |
| $I_{GEN5_{LIM}}$              | Current limit<br>$I_{GEN5}$ when VGEN5 is forced to $V_{GEN5_{NOM}}/2$   | 122                             | 167                  | 200                          | mA                      |
| $I_{GEN5_{OCP}}$              | Overcurrent protection threshold<br>$I_{GEN5}$ required to cause the SCP function to disable LDO when $REGSCPEN = 1$   | 120                             | —                    | 200                          | mA                      |
| $I_{GEN5_{Q}}$                | Quiescent current<br>No load, change in $I_{VIN}$ and $I_{VIN3}$<br>When VGEN5 enabled   | —                               | 13                   | —                            | $\mu\text{A}$           |
| <b>VGEN5 AC and transient</b> |  |                                 |                      |                              |                         |
| $PSRR_{V_{GEN5}}$             | PSRR <sup>[2]</sup><br>$I_{GEN5} = 75\text{ mA}$ , 20 Hz to 20 kHz<br>$V_{GEN5[3:0]} = 0000\text{ to }1111$ , $V_{IN3} = V_{IN3_{MIN}} + 100\text{ mV}$<br>$V_{GEN5[3:0]} = 0000\text{ to }1111$ , $V_{IN3} = V_{GEN5_{NOM}} + 1.0\text{ V}$   | 35<br>52                        | 40<br>60             | —<br>—                       | dB                      |
| $NOISE_{V_{GEN5}}$            | Output noise density<br>$V_{IN3} = V_{IN3_{MIN}}$ , $I_{GEN5} = 75\text{ mA}$<br>100 Hz to <1.0 kHz<br>1.0 kHz to <10 kHz<br>10 kHz to 1.0 MHz   | —<br>—<br>—                     | –114<br>–129<br>–135 | –102<br>–123<br>–130         | dBV/ $\sqrt{\text{Hz}}$ |
| $SLWR_{V_{GEN5}}$             | Turn on slew rate<br>10 % to 90 % of end value<br>$V_{IN3_{MIN}} \leq V_{IN3} \leq 4.5\text{ mV}$ , $I_{GEN5} = 0.0\text{ mA}$<br>$V_{GEN5[3:0]} = 0000\text{ to }0011$<br>$V_{GEN5[3:0]} = 0100\text{ to }0111$<br>$V_{GEN5[3:0]} = 1000\text{ to }1011$<br>$V_{GEN5[3:0]} = 1100\text{ to }1111$ | —<br>—<br>—<br>—                | —<br>—<br>—<br>—     | 22.0<br>26.5<br>30.5<br>34.5 | mV/ $\mu\text{s}$       |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                | Parameter  | Min | Typ | Max | Unit |
|-----------------------|--|-----|-----|-----|------|
| GEN5 <sub>ION</sub>   | Turn on time<br>Enable to 90 % of end value, $V_{IN3} = V_{IN3MIN}$ , 4.5 V<br>$I_{GEN5} = 0.0$ mA   | 60  | —   | 500 | μs   |
| GEN5 <sub>IOFF</sub>  | Turn off time<br>Disable to 10 % of initial value, $V_{IN3} = V_{IN3MIN}$<br>$I_{GEN5} = 0.0$ mA   | —   | —   | 10  | ms   |
| GEN5 <sub>OSHT</sub>  | Startup overshoot<br>$V_{IN3} = V_{IN3MIN}$ , 4.5 V, $I_{GEN5} = 0.0$ mA   | —   | 1.0 | 2.0 | %    |
| V <sub>GEN5LOTR</sub> | Transient load response<br>$V_{IN3} = V_{IN3MIN}$ , 4.5 V<br>$I_{GEN5} = 10$ to 100 mA in 1.0 μs<br>Peak of overshoot or undershoot of V <sub>GEN5</sub> with respect to final value. See <a href="#">Figure 30</a>  | —   | —   | 3.0 | %    |
| V <sub>GEN5LITR</sub> | Transient line response<br>$I_{GEN5} = 75$ mA<br>$V_{IN3INITIAL} = 2.8$ V to $V_{IN3FINAL} = 3.3$ V for VGEN5[3:0] = 0000 to 0111<br>$V_{IN3INITIAL} = V_{GEN5} + 0.3$ V to $V_{IN3FINAL} = V_{GEN5} + 0.8$ V for VGEN5[3:0] = 1000 to 1111<br>See <a href="#">Figure 30</a> | —   | 5.0 | 8.0 | mV   |

- [1] When the LDO output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
- [2] The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test.  $V_{IN3MIN}$  refers to the minimum allowed input voltage for a particular output voltage.

## 10.4.6.5.6 VGEN6

Table 105. VGEN6 electrical characteristics

All parameters are specified at  $T_{MIN}$  to  $T_{MAX}$  (see [Table 4](#)),  $V_{IN} = 3.6$  V,  $V_{IN3} = 3.6$  V,  $V_{GEN6[3:0]} = 1111$ ,  $I_{GEN6} = 10$  mA, typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6$  V,  $V_{IN3} = 3.6$  V,  $V_{GEN6[3:0]} = 1111$ ,  $I_{GEN6} = 10$  mA, and 25 °C, unless otherwise noted.

| Symbol               | Parameter  | Min                                    | Typ                      | Max | Unit |
|----------------------|--|--|--------------------------|-----|------|
| <b>VGEN6</b>         |  |  |                          |     |      |
| V <sub>IN3</sub>     | Operating input voltage <sup>[1]</sup><br>$1.8 \text{ V} \leq V_{GEN6NOM} \leq 2.5 \text{ V}$<br>$2.6 \text{ V} \leq V_{GEN6NOM} \leq 3.3 \text{ V}$ | 2.8<br>VGEN6 <sub>NOM</sub><br>+ 0.250 | —                        | 4.5 | V    |
| VGEN6 <sub>NOM</sub> | Nominal output voltage   | —                                      | <a href="#">Table 91</a> | —   | V    |
| I <sub>GEN6</sub>    | Operating load current   | 0.0                                    | —                        | 200 | mA   |
| <b>VGEN6 DC</b>      |  |  |                          |     |      |
| V <sub>GEN6TOL</sub> | Output voltage tolerance<br>$V_{IN3MIN} < V_{IN3} < 4.5 \text{ V}$<br>$0.0 \text{ mA} < I_{GEN6} < 200 \text{ mA}$<br>VGEN6[3:0] = 0000 to 1111      | -3.0                                   | —                        | 3.0 | %    |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                        | Parameter   | Min              | Typ                  | Max                          | Unit             |
|-------------------------------|---|------------------|----------------------|------------------------------|------------------|
| $V_{GEN6LOR}$                 | Load regulation<br>( $V_{GEN6}$ at $I_{GEN6} = 200$ mA) – ( $V_{GEN6}$ at $I_{GEN6} = 0.0$ mA)<br>For any $V_{IN3MIN} < V_{IN3} < 4.5$ V  | —                | 0.10                 | —                            | mV/mA            |
| $V_{GEN6LIR}$                 | Line regulation<br>( $V_{GEN6}$ at $V_{IN3} = 4.5$ V) – ( $V_{GEN6}$ at $V_{IN3MIN}$ )<br>For any $0.0$ mA $< I_{GEN6} < 200$ mA  | —                | 0.50                 | —                            | mV/mA            |
| $I_{GEN6LIM}$                 | Current limit<br>$I_{GEN6}$ when $V_{GEN6}$ is forced to $V_{GEN6NOM}/2$  | 232              | 333                  | 475                          | mA               |
| $I_{GEN6OCP}$                 | Overcurrent protection threshold<br>$I_{GEN6}$ required to cause the SCP function to disable LDO when $REGSCPEN = 1$  | 220              | —                    | 475                          | mA               |
| $I_{GEN6Q}$                   | Quiescent current<br>No load, change in $I_{VIN}$ and $I_{VIN3}$<br>When $V_{GEN6}$ enabled   | —                | 13                   | —                            | $\mu$ A          |
| <b>VGEN6 AC and transient</b> |   |                  |                      |                              |                  |
| $PSRR_{VGEN6}$                | PSRR <sup>[2]</sup><br>$I_{GEN6} = 150$ mA, 20 Hz to 20 kHz<br>$V_{GEN6}[3:0] = 0000$ to $1111$ , $V_{IN3} = V_{IN3MIN} + 100$ mV<br>$V_{GEN6}[3:0] = 0000$ to $1111$ , $V_{IN3} = V_{GEN6NOM} + 1.0$ V   | 35<br>52         | 40<br>60             | —<br>—                       | dB               |
| $NOISE_{VGEN6}$               | Output noise density<br>$V_{IN3} = V_{IN3MIN}$ , $I_{GEN6} = 150$ mA<br>100 Hz to $<1.0$ kHz<br>1.0 kHz to $<10$ kHz<br>10 kHz to 1.0 MHz   | —<br>—<br>—      | -114<br>-129<br>-135 | -102<br>-123<br>-130         | dBV/ $\sqrt{Hz}$ |
| $SLWR_{VGEN6}$                | Turn on slew rate<br>10 % to 90 % of end value<br>$V_{IN3MIN} \leq V_{IN3} \leq 4.5$ V, $I_{GEN6} = 0.0$ mA<br>$V_{GEN6}[3:0] = 0000$ to $0011$<br>$V_{GEN6}[3:0] = 0100$ to $0111$<br>$V_{GEN6}[3:0] = 1000$ to $1011$<br>$V_{GEN6}[3:0] = 1100$ to $1111$ | —<br>—<br>—<br>— | —<br>—<br>—<br>—     | 22.0<br>26.5<br>30.5<br>34.5 | mV/ $\mu$ s      |
| $GEN6_{tON}$                  | Turn on time<br>Enable to 90 % of end value, $V_{IN3} = V_{IN3MIN}$ , 4.5 V<br>$I_{GEN6} = 0.0$ mA  | 60               | —                    | 500                          | $\mu$ s          |
| $GEN6_{tOFF}$                 | Turn-off time<br>Disable to 10 % of initial value, $V_{IN3} = V_{IN3MIN}$<br>$I_{GEN6} = 0.0$ mA  | —                | —                    | 10                           | ms               |
| $GEN6_{OSHT}$                 | Startup overshoot<br>$V_{IN3} = V_{IN3MIN}$ , 4.5 V, $I_{GEN6} = 0$ mA  | —                | 1.0                  | 2.0                          | %                |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                | Parameter   | Min | Typ | Max | Unit |
|-----------------------|---|-----|-----|-----|------|
| V <sub>GEN6LOTR</sub> | Transient load response<br>V <sub>IN3</sub> = VIN3 <sub>MIN</sub> , 4.5 V<br>I <sub>GEN6</sub> = 20 to 200 mA in 1.0 μs<br>Peak of overshoot or undershoot of V <sub>GEN6</sub> with respect to final value. See <a href="#">Figure 30</a> .  | —   | —   | 3.0 | %    |
| V <sub>GEN6LITR</sub> | Transient line response<br>I <sub>GEN6</sub> = 150 m<br>VIN3 <sub>INITIAL</sub> = 2.8 V to VIN3 <sub>FINAL</sub> = 3.3 V for VGEN6[3:0] = 0000 to 0111<br>VIN3 <sub>INITIAL</sub> = V <sub>GEN6</sub> + 0.3 V to VIN3 <sub>FINAL</sub> = V <sub>GEN6</sub> + 0.8 V for VGEN6[3:0] = 1000 to 1111<br>See <a href="#">Figure 30</a> | —   | 5.0 | 8.0 | mV   |

- [1] When the LDO output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
- [2] The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. VIN3<sub>MIN</sub> refers to the minimum allowed input voltage for a particular output voltage.

#### 10.4.6.6 VSNVS LDO/switch

VSNVS powers the low-power SNVS/RTC domain on the processor. It derives its power from either VIN, or coin cell, and cannot be disabled. When powered by both, VIN takes precedence when above the appropriate comparator threshold. When powered by VIN, VSNVS is an LDO capable of supplying seven voltages: 3.0, 1.8, 1.5, 1.3, 1.2, 1.1, and 1.0. The bits VSNVSVOLT[2:0] in register VSNVS\_CONTROL determine the output voltage. When powered by coin cell, VSNVS is an LDO capable of supplying 1.8, 1.5, 1.3, 1.2, 1.1, 1.0 as shown in [Table 106](#).

If the 3.0 V option is chosen with the coin cell, VSNVS tracks the coin cell voltage by means of a switch, whose maximum resistance is 100 Ω. In this case, the VSNVS voltage is simply the coin cell voltage minus the voltage drop across the switch, which is 40 mV at a rated maximum load current of 1.5 mA (consumer version) or 1.0 mA (industrial version).

The default setting of the VSNVSVOLT[2:0] is 110, or 3.0 V, unless programmed otherwise in OTP. However, when the coin cell is applied for the very first time, VSNVS outputs 1.0 V. Only when V<sub>IN</sub> is applied, VSNVS transitions to its default, or programmed value if different. Upon subsequent removal of V<sub>IN</sub>, with the coin cell attached, VSNVS changes configuration from an LDO to a switch for the 110 setting, and remains as an LDO for the other settings, continuing to output the same voltage as when V<sub>IN</sub> is applied, provided certain conditions are met as described in [Table 106](#).

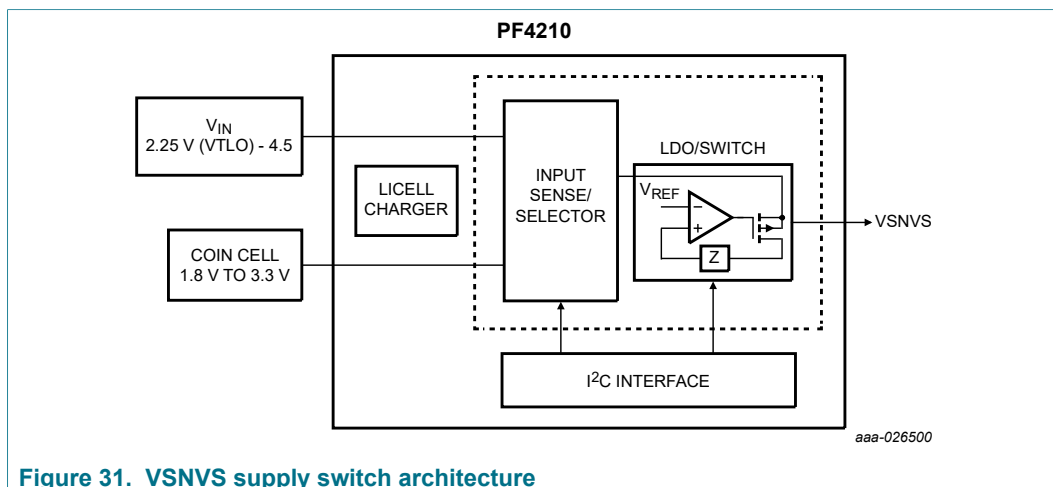


Figure 31. VSNVS supply switch architecture

Table 106 provides a summary of the VSNVS operation at different input voltage  $V_{IN}$  and with or without coin cell connected to the system.

Table 106. VSNVS modes of operation

| VSNVSVOLT[2:0] | VIN    | Mode             |
|----------------|--------|------------------|
| 110            | > VTH1 | VIN LDO 3.0 V    |
| 110            | < VTL1 | Coin cell switch |
| 000 to 101     | > VTH0 | VIN LDO          |
| 000 to 101     | < VTL0 | Coin cell LDO    |

#### 10.4.6.6.1 VSNVS control

The VSNVS output level is configured through the VSNVSVOLT[2:0] bits in VSNVSCTL register as shown in Table 107.

Table 107. Register VSNVSCTL - ADDR 0x6B

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| VSNVSVOLT | 2:0        | R/W | 0x80    | Configures VSNVS output voltage <sup>[1]</sup> <ul style="list-style-type: none"> <li>• 000 = 1.0 V</li> <li>• 001 = 1.1 V</li> <li>• 010 = 1.2 V</li> <li>• 011 = 1.3 V</li> <li>• 100 = 1.5 V</li> <li>• 101 = 1.8 V</li> <li>• 110 = 3.0 V</li> <li>• 111 = RSVD</li> </ul> |
| UNUSED    | 7:3        | —   | 0x00    | unused   |

[1] Only valid when a valid input voltage is present.

#### 10.4.6.6.2 VSNVS external components

Table 108. VSNVS external components

| Capacitor | Value ( $\mu\text{F}$ ) |
|-----------|-------------------------|
| VSNVS     | 0.47                    |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

## 10.4.6.6.3 VSNVS specifications

Table 109. VSNVS electrical characteristics

All parameters are specified at  $T_{MIN}$  to  $T_{MAX}$  (see Table 4),  $V_{IN} = 3.6\text{ V}$ ,  $V_{SNVS} = 3.0\text{ V}$ ,  $I_{SNVS} = 5.0\text{ }\mu\text{A}$ , typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6\text{ V}$ ,  $V_{SNVS} = 3.0\text{ V}$ ,  $I_{SNVS} = 5.0\text{ }\mu\text{A}$ , and  $25\text{ }^\circ\text{C}$ , unless otherwise noted.

| Symbol   | Parameter  | Min               | Typ        | Max        | Unit          |
|--|--|-------------------|------------|------------|---------------|
| <b>VSNVS</b>   |  |                   |            |            |               |
| $V_{INSNVS}$   | Operating input voltage  |                   |            |            | V             |
|  | Valid coin cell range  | 1.8               | —          | 3.3        |               |
|  | Valid $V_{IN}$   | 2.25              | —          | 4.5        |               |
| $I_{SNVS}$   | Operating load current   |                   |            |            | $\mu\text{A}$ |
|  | $V_{INMIN} < V_{IN} < V_{INMAX}$ $T_A = 0\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$         | 1500              | 1800       | —          |               |
|  | $V_{INMIN} < V_{IN} < V_{INMAX}$ $T_A = -40\text{ }^\circ\text{C}$ to $105\text{ }^\circ\text{C}$      |                   | 1000       | —          |               |
| <b>VSNVS DC, LDO</b>   |  |                   |            |            |               |
| $V_{SNVS}$   | Output voltage <sup>[1]</sup>  |                   |            |            | V             |
|  | $5.0\text{ }\mu\text{A} < I_{SNVS} < I_{SNVS\text{ MAX}}$ (OFF)  |                   |            |            |               |
|  | $3.20\text{ V} < V_{IN} < 4.5\text{ V}$ , VSNVSVOLT[2:0] = 110   | -5.0 %            | 3.0        | 7.0 %      |               |
|  | $V_{TLO}/V_{TH} < V_{IN} < 4.5\text{ V}$ , VSNVSVOLT[2:0] = [000] - [101]                              | -8.0 %            | 1.0 to 1.8 | 7.0 %      |               |
|  | $5.0\text{ }\mu\text{A} < I_{SNVS} < I_{SNVS\text{ MAX}}$ (ON)   |                   |            |            |               |
|  | $3.20\text{ V} < V_{IN} < 4.5\text{ V}$ , VSNVSVOLT[2:0] = 110   | -5.0 %            | 3.0        | 5.0 %      |               |
|  | UVDET $< V_{IN} < 4.5\text{ V}$ , VSNVSVOLT[2:0] = [000] - [101]                                       | -4.0 %            | 1.0 to 1.8 | 4.0 %      |               |
| $5.0\text{ }\mu\text{A} < I_{SNVS} < I_{SNVS\text{ MAX}}$ (Coin cell mode) |  |                   |            |            |               |
|  | $2.84\text{ V} < V_{COIN} < 3.3\text{ V}$ , VSNVSVOLT[2:0] = 110                                       | $V_{COIN} - 0.04$ | —          | $V_{COIN}$ |               |
|  | $1.8\text{ V} < V_{COIN} < 3.3\text{ V}$ , VSNVSVOLT[2:0] = [000] - [101]                              | -8.0 %            | 1.0 to 1.8 | 7.0 %      |               |
| $V_{SNVSDROP}$   | Dropout voltage  |                   |            |            | mV            |
|  | $V_{IN} = V_{COIN} = 2.85\text{ V}$ , VSNVSVOLT[2:0] = 110, $I_{SNVS\text{ MAX}}$                      | —                 | —          | 50         |               |
| $I_{SNVSLIM}$  | Current limit  |                   |            |            | $\mu\text{A}$ |
|  | $V_{IN} > V_{TH1}$ , VSNVSVOLT[2:0] = 110  | —                 | —          | 6750       |               |
|  | $V_{IN} > V_{TH0}$ , VSNVSVOLT[2:0] = 000 to 101   | —                 | —          | 6750       |               |
|  | $V_{IN} < V_{TLO}$ , VSNVSVOLT[2:0] = 000 to 101   | —                 | —          | 4500       |               |
| $V_{TH0}$  | $V_{IN}$ threshold (coin cell powered to $V_{IN}$ powered)<br>$V_{IN}$ going high with valid coin cell |                   |            |            | V             |
|  | VSNVSVOLT[2:0] = 000, 001, 010, 011, 100, 101  | 2.25              | 2.40       | 2.55       |               |
| $V_{TLO}$  | $V_{IN}$ threshold ( $V_{IN}$ powered to coin cell powered)<br>$V_{IN}$ going low with valid coin cell |                   |            |            | V             |
|  | VSNVSVOLT[2:0] = 000, 001, 010, 011, 100, 101  | 2.20              | 2.35       | 2.50       |               |
| $V_{HYST1}$  | $V_{IN}$ threshold hysteresis for $V_{TH1} - V_{TL1}$  | 5.0               | —          | —          | mV            |
| $V_{HYST0}$  | $V_{IN}$ threshold hysteresis for $V_{TH0} - V_{TL0}$  | 5.0               | —          | —          | mV            |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Symbol                        | Parameter  | Min      | Typ          | Max      | Unit   |
|-------------------------------|--|----------|--------------|----------|--------|
| VSNVSCROSS                    | Output voltage during crossover <sup>[2]</sup><br>VSNVSVOLT[2:0] = 110<br>V <sub>COIN</sub> > 2.9 V<br>Switch to LDO: V <sub>IN</sub> > 2.825 V, I <sub>SNVS</sub> = 100 μA<br>LDO to Switch: V <sub>IN</sub> < 3.05 V, I <sub>SNVS</sub> = 100 μA   | 2.7      | —            | —        | V      |
| <b>VSNVS AC and transient</b> |  |          |              |          |        |
| tON <sub>SNVS</sub>           | Turn on time (load capacitor, 0.47 μF) <sup>[3] [4]</sup><br>V <sub>IN</sub> > UVDET to 90 % of V <sub>SNVS</sub><br>V <sub>COIN</sub> = 0.0 V, I <sub>SNVS</sub> = 5.0 μA<br>VSNVSVOLT[2:0] = 000 to 110  | —        | —            | 24       | ms     |
| V <sub>SNVSOSH</sub>          | Startup overshoot<br>VSNVSVOLT[2:0] = 000 to 110<br>I <sub>SNVS</sub> = 5.0 μA<br>dV <sub>IN</sub> /dt = 50 mV/μs  | —        | 40           | 70       | mV     |
| V <sub>SNVSLITR</sub>         | Transient line response I <sub>SNVS</sub> = 75 % of I <sub>SNVS</sub><br>MAX<br>3.2 V < V <sub>IN</sub> < 4.5 V, VSNVSVOLT[2:0] = 110<br>2.45 V < V <sub>IN</sub> < 4.5 V, VSNVSVOLT[2:0] = [000] - [101]  | —<br>—   | 32<br>22     | —<br>—   | mV     |
| V <sub>SNVSLOTR</sub>         | Transient load response<br>VSNVSVOLT[2:0] = 110<br>3.1 V (UVDETL) < V <sub>IN</sub> ≤ 4.5 V<br>I <sub>SNVS</sub> = 75 to 750 μA<br>VSNVSVOLT[2:0] = 000 to 101<br>2.45 V < V <sub>IN</sub> ≤ 4.5 V<br>V <sub>TL0</sub> > V <sub>IN</sub> , 1.8 V ≤ V <sub>COIN</sub> ≤ 3.3 V<br>I <sub>SNVS</sub> = 40 μA to I <sub>SNVS</sub> MAX<br>Refer to <a href="#">Figure 30</a> | 2.8<br>— | —<br>1.0     | —<br>2.0 | V<br>% |
| <b>VSNVS DC, switch</b>       |  |          |              |          |        |
| V <sub>INSNVS</sub>           | Operating input voltage<br>Valid coin cell range   | 1.8      | —            | 3.3      | V      |
| I <sub>SNVS</sub>             | Operating load current<br>T <sub>A</sub> = 0 °C to 85 °C<br>T <sub>A</sub> = -40 °C to 105 °C  | 1500     | 1800<br>1000 | —<br>—   | μA     |
| R <sub>DS(ON)SNVS</sub>       | Internal switch R <sub>DS(on)</sub><br>V <sub>COIN</sub> = 2.6 V   | —        | —            | 100      | Ω      |
| V <sub>TL1</sub>              | V <sub>IN</sub> threshold (V <sub>IN</sub> powered to coin cell powered) <sup>[2]</sup><br>VSNVSVOLT[2:0] = 110  | 2.725    | 2.90         | 3.00     | V      |
| V <sub>TH1</sub>              | V <sub>IN</sub> threshold (coin cell powered to V <sub>IN</sub> powered)<br>VSNVSVOLT[2:0] = 110   | 2.775    | 2.95         | 3.1      | V      |

[1] For 1.8 V I<sub>SNVS</sub> limited to 100 μA for V<sub>COIN</sub> < 2.1 V

[2] During crossover from V<sub>IN</sub> to LICELL, the VSNVS output voltage may drop to 2.7 V before going to the LICELL voltage. This momentary drop does not cause any malfunction. The i.MX RTC continues to operate through the transition, and as a worst case it may switch to the internal RC oscillator for a few clock cycles before switching back to the external crystal oscillator.

[3] The start-up of VSNVS is not monotonic. It first rises to 1.0 V and then settles to its programmed value within the specified tr<sub>1</sub> time.

[4] From coin cell insertion to VSNVS = 1.0 V, the delay time is typically 400 ms.

#### 10.4.6.7 Coin cell battery backup

The LICELL pin provides for a connection of a coin cell backup battery or a super capacitor. If the voltage at VIN goes below the VIN threshold (V<sub>TL1</sub> and V<sub>TL0</sub>), contact-bounced, or removed, the coin cell maintained logic is powered by the voltage applied to LICELL.

The supply for internal logic and the VSNVS rail switches over to the LICELL pin when VIN goes below VTL1 or VTL0, even in the absence of a voltage at the LICELL pin, resulting in clearing of memory and turning off of VSNVS. When system operation below VTL1 is required, for systems not utilizing a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.0 V. A small capacitor should be placed from LICELL to ground under all circumstances.

##### 10.4.6.7.1 Coin cell charger control

The coin cell charger circuit functions as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHEN bit while the coin cell voltage is programmable through the VCOIN[2:0] bits on register COINCTL in [Table 111](#). The coin cell charger voltage is programmable. In the on state, the charger current is fixed at ICOINHI. In sleep and standby modes, the charger current is reduced to a typical 10  $\mu$ A. In the off state, coin cell charging is not available as the main battery could be depleted unnecessarily. The coin cell charging stops when VIN is below UVDET.

**Table 110. Coin cell charger voltage**

| VCOIN[2:0] | V <sub>COIN</sub> (V) <sup>[1]</sup> |
|------------|--------------------------------------|
| 000        | 2.50                                 |
| 001        | 2.70                                 |
| 010        | 2.80                                 |
| 011        | 2.90                                 |
| 100        | 3.00                                 |
| 101        | 3.10                                 |
| 110        | 3.20                                 |
| 111        | 3.30                                 |

[1] Coin cell voltage selected is based on the type of LICELL used in the system.

**Table 111. Register COINCTL - ADDR 0x1A**

| Name     | Bit number | R/W | Default | Description  |
|----------|------------|-----|---------|--|
| VCOIN    | 2:0        | R/W | 0x00    | Coin cell charger output voltage selection. See <a href="#">Table 110</a> for all options selectable through these bits. |
| COINCHEN | 3          | R/W | 0x00    | Enable or disable the coin cell charger  |
| UNUSED   | 7:4        | —   | 0x00    | unused   |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

## 10.4.6.7.2 External components

Table 112. Coin cell charger external components

| Component               | Value | Units |
|-------------------------|-------|-------|
| LICELL bypass capacitor | 100   | nF    |

## 10.4.6.7.3 Coin cell specifications

Table 113. Coin cell charger specifications

| Parameter                                   | Typ | Unit |
|---|-----|------|
| Voltage accuracy                            | 100 | mV   |
| Coin cell charge current in on mode ICOINH1 | 60  | μA   |
| Current accuracy                            | 30  | %    |

10.5 Control interface I<sup>2</sup>C block description

The PF4210 contains an I<sup>2</sup>C interface port which allows access by a processor, or any I<sup>2</sup>C master, to the register set. Via these registers the resources of the IC can be controlled. The registers also provide status information about how the IC is operating.

The SCL and SDA lines should be routed away from noisy signals and planes to minimize noise pick up. To prevent reflections in the SCL and SDA traces from creating false pulses, the rise and fall times of the SCL and SDA signals must be greater than 20 ns. This can be accomplished by reducing the drive strength of the I<sup>2</sup>C master via software. Alternatively, this can be accomplished by using small capacitors from SCL and SDA to ground. For example, use 5.1 pF capacitors from SCL and SDA to ground for bus pull-up resistors of 4.8 kΩ.

10.5.1 I<sup>2</sup>C device ID

I<sup>2</sup>C interface protocol requires a device ID for addressing the target IC on a multi-device bus. To allow flexibility in addressing for bus conflict avoidance, fuse programmability is provided to allow configuration for the lower 3 address LSB(s). See [Section 10.1.2 "One time programmability \(OTP\)"](#) for more details. This product supports 7-bit addressing only; support is not provided for 10-bit or general call addressing.

**Note:** When the TBB bits for the I<sup>2</sup>C slave address are written, the next access to the chip, must then use the new slave address; these bits take affect right away.

10.5.2 I<sup>2</sup>C operation

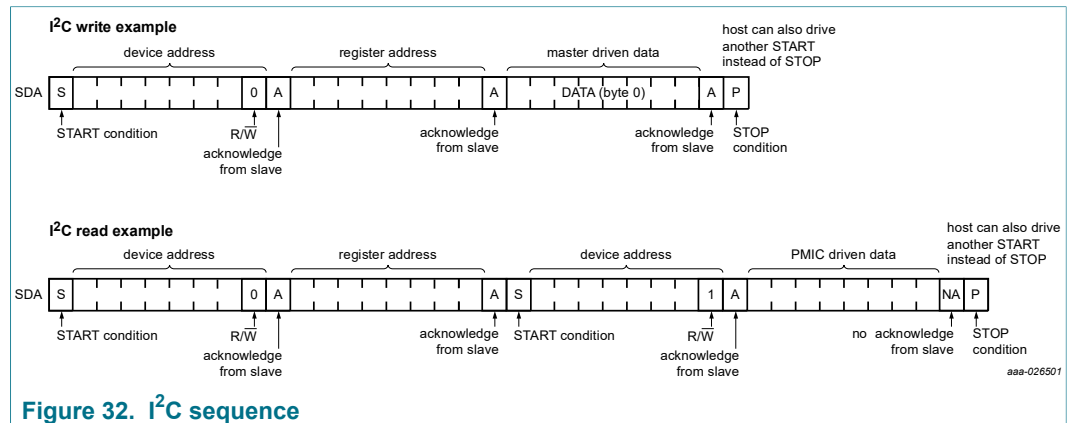
The I<sup>2</sup>C mode of the interface is implemented generally following the fast mode definition which supports up to 400 kbits/s operation (exceptions to the standard are noted to be 7-bit only addressing and no support for general call addressing). Timing diagrams, electrical specifications, and further details can be found in the I<sup>2</sup>C specification, which is available for download at:

[http://www.nxp.com/acrobat\\_download/literature/9398/39340011.pdf](http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf)

I<sup>2</sup>C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and each byte is sent out unless a STOP command or NACK is received prior to completion.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

The following examples show how to write and read data to and from the IC. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device responds to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NACK is received, the host should terminate the current transaction and retry the transaction.

Figure 32. I<sup>2</sup>C sequence

### 10.5.3 Interrupt handling

The system is informed about important events based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INTB pin low.

Each interrupt is latched so even if the interrupt source becomes inactive, the interrupt remains set until cleared. Each interrupt can be cleared by writing a 1 to the appropriate bit in the Interrupt Status register; this also causes the INTB pin to go high. If there are multiple interrupt bits set, the INTB pin remains low until all are either masked or cleared. If a new interrupt occurs while the processor clears an existing interrupt bit, the INTB pin remains low.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin does not go low. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the INTB pin goes low after unmasking.

The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable.

Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the INT summary [Table 114](#). Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

### 10.5.4 Interrupt bit summary

[Table 114](#) summarizes all interrupt, mask, and sense bits associated with INTB control.

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 114. Interrupt, mask and sense bits

| Interrupt   | Mask        | Sense       | Purpose   | Trigger | Debounce time (ms)   |
|-------------|-------------|-------------|---|---------|----------------------|
| LOWVINI     | LOWVINM     | LOWVINS     | Low input voltage detect<br>Sense is 1 if below 2.80 V threshold    | H to L  | 3.9 <sup>[1]</sup>   |
| PWRONI      | PWRONM      | PWRONS      | Power on button event<br>Sense is 1 if PWRON is high.               | H to L  | 31.25 <sup>[1]</sup> |
|             |             |             |   | L to H  | 31.25                |
| THERM110    | THERM110M   | THERM110S   | Thermal 110 °C threshold<br>Sense is 1 if above threshold           | Dual    | 3.9                  |
| THERM120    | THERM120M   | THERM120S   | Thermal 120 °C threshold<br>Sense is 1 if above threshold           | Dual    | 3.9                  |
| THERM125    | THERM125M   | THERM125S   | Thermal 125 °C threshold<br>Sense is 1 if above threshold           | Dual    | 3.9                  |
| THERM130    | THERM130M   | THERM130S   | Thermal 130 °C threshold<br>Sense is 1 if above threshold           | Dual    | 3.9                  |
| SW1AFAULTI  | SW1AFAULTM  | SW1AFAULTS  | Regulator 1A overcurrent limit<br>Sense is 1 if above current limit | L to H  | 8.0                  |
| SW1BFAULTI  | SW1BFAULTM  | SW1BFAULTS  | Regulator 1B overcurrent limit<br>Sense is 1 if above current limit | L to H  | 8.0                  |
| SW1CFAULTI  | SW1CFAULTM  | SW1CFAULTS  | Regulator 1C overcurrent limit<br>Sense is 1 if above current limit | L to H  | 8.0                  |
| SW2FAULTI   | SW2FAULTM   | SW2FAULTS   | Regulator 2 overcurrent limit<br>Sense is 1 if above current limit  | L to H  | 8.0                  |
| SW3AFAULTI  | SW3AFAULTM  | SW3AFAULTS  | Regulator 3A overcurrent limit<br>Sense is 1 if above current limit | L to H  | 8.0                  |
| SW3BFAULTI  | SW3BFAULTM  | SW3BFAULTS  | Regulator 3B overcurrent limit<br>Sense is 1 if above current limit | L to H  | 8.0                  |
| SW4FAULTI   | SW4FAULTM   | SW4FAULTS   | Regulator 4 overcurrent limit<br>Sense is 1 if above current limit  | L to H  | 8.0                  |
| SWBSTFAULTI | SWBSTFAULTM | SWBSTFAULTS | SWBST overcurrent limit<br>Sense is 1 if above current limit        | L to H  | 8.0                  |
| VGEN1FAULTI | VGEN1FAULTM | VGEN1FAULTS | VGEN1 overcurrent limit<br>Sense is 1 if above current limit        | L to H  | 8.0                  |
| VGEN2FAULTI | VGEN2FAULTM | VGEN2FAULTS | VGEN2 overcurrent limit<br>Sense is 1 if above current limit        | L to H  | 8.0                  |
| VGEN3FAULTI | VGEN3FAULTM | VGEN3FAULTS | VGEN3 overcurrent limit<br>Sense is 1 if above current limit        | L to H  | 8.0                  |
| VGEN4FAULTI | VGEN4FAULTM | VGEN4FAULTS | VGEN4 overcurrent limit<br>Sense is 1 if above current limit        | L to H  | 8.0                  |
| VGEN5FAULTI | VGEN5FAULTM | VGEN1FAULTS | VGEN5 overcurrent limit<br>Sense is 1 if above current limit        | L to H  | 8.0                  |
| VGEN6FAULTI | VGEN6FAULTM | VGEN6FAULTS | VGEN6 overcurrent limit<br>Sense is 1 if above current limit        | L to H  | 8.0                  |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Interrupt | Mask     | Sense    | Purpose  | Trigger | Debounce time (ms) |
|-----------|----------|----------|--|---------|--------------------|
| OTP_ECCI  | OTP_ECCM | OTP_ECCS | 1 or 2 bit error detected in OTP registers<br>Sense is 1 if error detected | L to H  | 8.0                |

[1] Debounce timing for the falling edge can be extended with PWRONDBNC[1:0].

A full description of all interrupt, mask, and sense registers is provided in [Table 115](#) to [Table 126](#).

**Table 115. Register INTSTAT0 - ADDR 0x05**

| Name      | Bit number | R/W   | Default | Description                  |
|-----------|------------|-------|---------|------------------------------|
| PWRONI    | 0          | R/W1C | 0       | Power on interrupt bit       |
| LOWVINI   | 1          | R/W1C | 0       | Low-voltage interrupt bit    |
| THERM110I | 2          | R/W1C | 0       | 110 °C Thermal interrupt bit |
| THERM120I | 3          | R/W1C | 0       | 120 °C Thermal interrupt bit |
| THERM125I | 4          | R/W1C | 0       | 125 °C Thermal interrupt bit |
| THERM130I | 5          | R/W1C | 0       | 130 °C Thermal interrupt bit |
| UNUSED    | 7:6        | —     | 00      | unused                       |

**Table 116. Register INTMASK0 - ADDR 0x06**

| Name      | Bit number | R/W   | Default | Description                       |
|-----------|------------|-------|---------|-----------------------------------|
| PWRONM    | 0          | R/W1C | 1       | Power on interrupt mask bit       |
| LOWVINM   | 1          | R/W1C | 1       | Low-voltage interrupt mask bit    |
| THERM110M | 2          | R/W1C | 1       | 110 °C thermal interrupt mask bit |
| THERM120M | 3          | R/W1C | 1       | 120 °C thermal interrupt mask bit |
| THERM125M | 4          | R/W1C | 1       | 125 °C thermal interrupt mask bit |
| THERM130M | 5          | R/W1C | 1       | 130 °C thermal interrupt mask bit |
| UNUSED    | 7:6        | —     | 00      | unused                            |

**Table 117. Register INTSENSE0 - ADDR 0x07**

| Name      | Bit number | R/W | Default | Description  |
|-----------|------------|-----|---------|--|
| PWRONS    | 0          | R   | 0       | Power on sense bit<br>• 0 = PWRON low<br>• 1 = PWRON high                  |
| LOWVINS   | 1          | R   | 0       | Low-voltage sense bit<br>• 0 = VIN > 2.8 V<br>• 1 = VIN ≤ 2.8 V            |
| THERM110S | 2          | R   | 0       | 110 °C thermal sense bit<br>• 0 = Below threshold<br>• 1 = Above threshold |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name      | Bit number | R/W | Default | Description   |
|-----------|------------|-----|---------|---|
| THERM120S | 3          | R   | 0       | 120 °C thermal sense bit<br>• 0 = Below threshold<br>• 1 = Above threshold                          |
| THERM125S | 4          | R   | 0       | 125 °C thermal sense bit<br>• 0 = Below threshold<br>• 1 = Above threshold                          |
| THERM130S | 5          | R   | 0       | 130 °C thermal sense bit<br>• 0 = Below threshold<br>• 1 = Above threshold                          |
| UNUSED    | 6          | —   | 0       | unused  |
| VDDOTPS   | 7          | R   | 00      | Additional VDDOTP voltage sense pin<br>• 0 = VDDOTP grounded<br>• 1 = VDDOTP to VCOREDIG or greater |

Table 118. Register INTSTAT1 - ADDR 0x08

| Name       | Bit number | R/W   | Default | Description                    |
|------------|------------|-------|---------|--------------------------------|
| SW1AFAULTI | 0          | R/W1C | 0       | SW1A overcurrent interrupt bit |
| SW1BFAULTI | 1          | R/W1C | 0       | SW1B overcurrent interrupt bit |
| SW1CFAULTI | 2          | R/W1C | 0       | SW1C overcurrent interrupt bit |
| SW2FAULTI  | 3          | R/W1C | 0       | SW2 overcurrent interrupt bit  |
| SW3AFAULTI | 4          | R/W1C | 0       | SW3A overcurrent interrupt bit |
| SW3BFAULTI | 5          | R/W1C | 0       | SW3B overcurrent interrupt bit |
| SW4FAULTI  | 6          | R/W1C | 0       | SW4 overcurrent interrupt bit  |
| UNUSED     | 7          | —     | 0       | unused                         |

Table 119. Register INTMASK1 - ADDR 0x09

| Name       | Bit number | R/W | Default | Description                         |
|------------|------------|-----|---------|-------------------------------------|
| SW1AFAULTM | 0          | R/W | 1       | SW1A overcurrent interrupt mask bit |
| SW1BFAULTM | 1          | R/W | 1       | SW1B overcurrent interrupt mask bit |
| SW1CFAULTM | 2          | R/W | 1       | SW1C overcurrent interrupt mask bit |
| SW2FAULTM  | 3          | R/W | 1       | SW2 overcurrent interrupt mask bit  |
| SW3AFAULTM | 4          | R/W | 1       | SW3A overcurrent interrupt mask bit |
| SW3BFAULTM | 5          | R/W | 1       | SW3B overcurrent interrupt mask bit |
| SW4FAULTM  | 6          | R/W | 1       | SW4 overcurrent interrupt mask bit  |
| UNUSED     | 7          | —   | 0       | unused                              |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 120. Register INTSENSE1 - ADDR 0x0A

| Name       | Bit number | R/W | Default | Description   |
|------------|------------|-----|---------|---|
| SW1AFAULTS | 0          | R   | 0       | SW1A overcurrent sense bit<br>• 0 = Normal operation<br>• 1 = Above current limit |
| SW1BFAULTS | 1          | R   | 0       | SW1B overcurrent sense bit<br>• 0 = Normal operation<br>• 1 = Above current limit |
| SW1CFAULTS | 2          | R   | 0       | SW1C overcurrent sense bit<br>• 0 = Normal operation<br>• 1 = Above current limit |
| SW2FAULTS  | 3          | R   | 0       | SW2 overcurrent sense bit<br>• 0 = Normal operation<br>• 1 = Above current limit  |
| SW3AFAULTS | 4          | R   | 0       | SW3A overcurrent sense bit<br>• 0 = Normal operation<br>• 1 = Above current limit |
| SW3BFAULTS | 5          | R   | 0       | SW3B overcurrent sense bit<br>• 0 = Normal operation<br>• 1 = Above current limit |
| SW4FAULTS  | 6          | R   | 0       | SW4 overcurrent sense bit<br>• 0 = Normal operation<br>• 1 = Above current limit  |
| UNUSED     | 7          | —   | 0       | unused  |

Table 121. Register INTSTAT3 - ADDR 0x0E

| Name        | Bit number | R/W   | Default | Description                           |
|-------------|------------|-------|---------|---------------------------------------|
| SWBSTFAULTI | 0          | R/W1C | 0       | SWBST overcurrent limit interrupt bit |
| UNUSED      | 6:1        | —     | 0x00    | unused                                |
| OTP_ECCI    | 7          | R/W1C | 0       | OTP error interrupt bit               |

Table 122. Register INTMASK3 - ADDR 0x0F

| Name        | Bit number | R/W | Default | Description                                |
|-------------|------------|-----|---------|--|
| SWBSTFAULTM | 0          | R/W | 1       | SWBST overcurrent limit interrupt mask bit |
| UNUSED      | 6:1        | —   | 0x00    | unused                                     |
| OTP_ECCM    | 7          | R/W | 1       | OTP error interrupt mask bit               |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

Table 123. Register INTSENSE3 - ADDR 0x10

| Name        | Bit number | R/W | Default | Description   |
|-------------|------------|-----|---------|---|
| SWBSTFAULTS | 0          | R   | 0       | SWBST overcurrent limit sense bit <ul style="list-style-type: none"> <li>0 = Normal operation</li> <li>1 = Above current limit</li> </ul> |
| UNUSED      | 6:1        | —   | 0x00    | unused  |
| OTP_ECCS    | 7          | R   | 0       | OTP error sense bit <ul style="list-style-type: none"> <li>0 = No error detected</li> <li>1 = OTP error detected</li> </ul>               |

Table 124. Register INTSTAT4 - ADDR 0x11

| Name        | Bit number | R/W   | Default | Description                     |
|-------------|------------|-------|---------|---------------------------------|
| VGEN1FAULTI | 0          | R/W1C | 0       | VGEN1 overcurrent interrupt bit |
| VGEN2FAULTI | 1          | R/W1C | 0       | VGEN2 overcurrent interrupt bit |
| VGEN3FAULTI | 2          | R/W1C | 0       | VGEN3 overcurrent interrupt bit |
| VGEN4FAULTI | 3          | R/W1C | 0       | VGEN4 overcurrent interrupt bit |
| VGEN5FAULTI | 4          | R/W1C | 0       | VGEN5 overcurrent interrupt bit |
| VGEN6FAULTI | 5          | R/W1C | 0       | VGEN6 overcurrent interrupt bit |
| UNUSED      | 7:6        | —     | 00      | unused                          |

Table 125. Register INTMASK4 - ADDR 0x12

| Name        | Bit number | R/W | Default | Description                          |
|-------------|------------|-----|---------|--------------------------------------|
| VGEN1FAULTM | 0          | R/W | 1       | VGEN1 overcurrent interrupt mask bit |
| VGEN2FAULTM | 1          | R/W | 1       | VGEN2 overcurrent interrupt mask bit |
| VGEN3FAULTM | 2          | R/W | 1       | VGEN3 overcurrent interrupt mask bit |
| VGEN4FAULTM | 3          | R/W | 1       | VGEN4 overcurrent interrupt mask bit |
| VGEN5FAULTM | 4          | R/W | 1       | VGEN5 overcurrent interrupt mask bit |
| VGEN6FAULTM | 5          | R/W | 1       | VGEN6 overcurrent interrupt mask bit |
| UNUSED      | 7:6        | —   | 00      | unused                               |

Table 126. Register INTSENSE4 - ADDR 0x13

| Name        | Bit number | R/W | Default | Description   |
|-------------|------------|-----|---------|---|
| VGEN1FAULTS | 0          | R   | 0       | VGEN1 overcurrent sense bit <ul style="list-style-type: none"> <li>0 = Normal operation</li> <li>1 = Above current limit</li> </ul> |
| VGEN2FAULTS | 1          | R   | 0       | VGEN2 overcurrent sense bit <ul style="list-style-type: none"> <li>0 = Normal operation</li> <li>1 = Above current limit</li> </ul> |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name        | Bit number | R/W | Default | Description  |
|-------------|------------|-----|---------|--|
| VGEN3FAULTS | 2          | R   | 0       | VGEN3 overcurrent sense bit<br><ul style="list-style-type: none"> <li>• 0 = Normal operation</li> <li>• 1 = Above current limit</li> </ul> |
| VGEN4FAULTS | 3          | R   | 0       | VGEN4 overcurrent sense bit<br><ul style="list-style-type: none"> <li>• 0 = Normal operation</li> <li>• 1 = Above current limit</li> </ul> |
| VGEN5FAULTS | 4          | R   | 0       | VGEN5 overcurrent sense bit<br><ul style="list-style-type: none"> <li>• 0 = Normal operation</li> <li>• 1 = Above current limit</li> </ul> |
| VGEN6FAULTS | 5          | R   | 0       | VGEN6 overcurrent sense bit<br><ul style="list-style-type: none"> <li>• 0 = Normal operation</li> <li>• 1 = Above current limit</li> </ul> |
| UNUSED      | 7:6        | —   | 00      | unused   |

## 10.6 Specific registers

### 10.6.1 IC and version identification

The IC and other version details can be read via identification bits. These are hard-wired on chip and described in [Table 127](#) to [Table 129](#).

**Table 127. Register DEVICEID - ADDR 0x00**

| Name     | Bit number | R/W | Default | Description  |
|----------|------------|-----|---------|--|
| DEVICEID | 3:0        | R   | 0x00    | Die version<br><ul style="list-style-type: none"> <li>• 0000 = PF4210</li> </ul> |
| UNUSED   | 7:4        | —   | 0x01    | unused   |

**Table 128. Register SILICON REV- ADDR 0x03**

| Name            | Bit number | R/W | Default | Description  |
|-----------------|------------|-----|---------|--|
| METAL_LAYER_REV | 3:0        | R   | 0x00    | Represents the metal mask revision<br><ul style="list-style-type: none"> <li>• Pass 0.0 = 0000</li> <li>• ...</li> <li>• Pass 0.15 = 1111</li> </ul> |
| FULL_LAYER_REV  | 7:4        | R   | 0x01    | Represents the full mask revision<br><ul style="list-style-type: none"> <li>• Pass 1.0 = 0001</li> <li>• ...</li> <li>• Pass 15.0 = 1111</li> </ul>  |

**Table 129. Register FABID - ADDR 0x04**

| Name | Bit number | R/W | Default | Description  |
|------|------------|-----|---------|--|
| FIN  | 1:0        | R   | 0x00    | Allows for characterizing different options within the same reticule |
| FAB  | 3:2        | R   | 0x00    | Represents the wafer manufacturing facility                          |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Name   | Bit number | R/W | Default | Description |
|--------|------------|-----|---------|-------------|
| Unused | 7:0        | R   | 0x00    | unused      |

### 10.6.2 Embedded memory

There are four register banks of general purpose embedded memory to store critical data. The data written to MEMA[7:0], MEMB[7:0], MEMC[7:0], and MEMD[7:0] is maintained by the coin cell when the main battery is deeply discharged, removed, or contact-bounced. The contents of the embedded memory are reset by COINPORB. The banks can be used for any system need for bit retention with coin cell backup.

Table 130. Register MEMA ADDR 0x1C

| Name | Bit number | R/W | Default | Description   |
|------|------------|-----|---------|---------------|
| MEMA | 7:0        | R/W | 0       | Memory bank A |

Table 131. Register MEMB ADDR 0x1D

| Name | Bit number | R/W | Default | Description   |
|------|------------|-----|---------|---------------|
| MEMB | 7:0        | R/W | 0       | Memory bank B |

Table 132. Register MEMC ADDR 0x1E

| Name | Bit number | R/W | Default | Description   |
|------|------------|-----|---------|---------------|
| MEMC | 7:0        | R/W | 0       | Memory bank C |

Table 133. Register MEMD ADDR 0x1F

| Name | Bit number | R/W | Default | Description   |
|------|------------|-----|---------|---------------|
| MEMD | 7:0        | R/W | 0       | Memory bank D |

## 10.7 Register bitmap

The register map is comprised of thirty-two pages, and its address and data fields are each eight bits wide. Only the first two pages can be accessed. On each page, registers 0 to 0x7F are referred to as *functional*, and registers 0x80 to 0xFF as *extended*. On each page, the functional registers are the same, but the extended registers are different. To access registers in [Table 135](#), write 0x01 to the page register at address 0x7F, and to access registers in [Table 136](#), write 0x02 to the page register at address 0x7F. To access [Table 134](#), from one of the extended pages, no write to the page register is necessary.

Registers missing in the sequence are reserved; reading from them returns a value 0x00, and writing to them has no effect.

The contents of all registers are given in the tables defined in this chapter. Each table is structured as follows:

**Name:** Name of the bit.

**Bit number:** The bit location in the register (7-0)

## 14-channel power management integrated circuit (PMIC) for audio/video applications

**R/W:** Read / Write access and control

- R is read-only access
- R/W is read and write access
- RW1C is read and write access with write 1 to clear

**Reset:** Reset signals are color coded based on the following legend.

|  |
|--|
| Bits reset by SC and VCOREDIG_PORB                         |
| Bits reset by PWRON or loaded default or OTP configuration |
| Bits reset by DIGRESETB                                    |
| Bits reset by PORB or RESETBMCU                            |
| Bits reset by VCOREDIG_PORB                                |
| Bits reset by POR or OFFB                                  |

**Default:** The value after reset, as noted in the default column of the memory map.

- Fixed defaults are explicitly declared as 0 or 1
- X corresponds to read/write bits that are initialized at startup, based on the OTP fuse settings or default if VDDOTP = 1.5 V. Bits are subsequently I<sup>2</sup>C modifiable, when their reset has been released. X may also refer to bits which may have other dependencies. For example, some bits may depend on the version of the IC, or a value from an analog block, for instance the sense bits for the interrupts.

## 10.7.1 Register map

Table 134. Functional page

| Add | Register name | R/W  | Default      | BITS[7:0]           |           |            |            |                      |            |            |             |
|-----|---------------|------|--------------|---------------------|-----------|------------|------------|----------------------|------------|------------|-------------|
|     |               |      |              | 7                   | 6         | 5          | 4          | 3                    | 2          | 1          | 0           |
| 00  | DeviceID      | R    | 8'b0001_0000 | —                   | —         | —          | —          | DEVICE ID [3:0]      |            |            |             |
|     |               |      |              | 0                   | 0         | 0          | 1          | 0                    | 0          | 0          | 0           |
| 03  | SILICONREVID  | R    | 8'b0001_0000 | FULL_LAYER_REV[3:0] |           |            |            | METAL_LAYER_REV[3:0] |            |            |             |
|     |               |      |              | x                   | x         | x          | x          | x                    | x          | x          | x           |
| 04  | FABID         | R    | 8'b0000_0000 | —                   | —         | —          | —          | FAB[1:0]             |            | FIN[1:0]   |             |
|     |               |      |              | 0                   | 0         | 0          | 0          | 0                    | 0          | 0          | 0           |
| 05  | INTSTAT0      | RW1C | 8'b0000_0000 | —                   | —         | THERM130I  | THERM125I  | THERM120I            | THERM110I  | LOWVINI    | PWRONI      |
|     |               |      |              | 0                   | 0         | 0          | 0          | 0                    | 0          | 0          | 0           |
| 06  | INTMASK0      | R/W  | 8'b0011_1111 | —                   | —         | THERM130M  | THERM125M  | THERM120M            | THERM110M  | LOWVINM    | PWRONM      |
|     |               |      |              | 0                   | 0         | 1          | 1          | 1                    | 1          | 1          | 1           |
| 07  | INTSENSE0     | R    | 8'b00xx_xxxx | VDDOTPS             | RSVD      | THERM130S  | THERM125S  | THERM120S            | THERM110S  | LOWVINS    | PWRONS      |
|     |               |      |              | 0                   | 0         | x          | x          | x                    | x          | x          | x           |
| 08  | INTSTAT1      | RW1C | 8'b0000_0000 | —                   | SW4FAULTI | SW3BFAULTI | SW3AFAULTI | SW2FAULTI            | SW1CFAULTI | SW1BFAULTI | SW1AFAULTI  |
|     |               |      |              | 0                   | 0         | 0          | 0          | 0                    | 0          | 0          |             |
| 09  | INTMASK1      | R/W  | 8'b0111_1111 | —                   | SW4FAULTM | SW3BFAULTM | SW3AFAULTM | SW2FAULTM            | SW1CFAULTM | SW1BFAULTM | SW1AFAULTM  |
|     |               |      |              | 0                   | 1         | 1          | 1          | 1                    | 1          | 1          |             |
| 0A  | INTSENSE1     | R    | 8'b0xxx_xxxx | —                   | SW4FAULTS | SW3BFAULTS | SW3AFAULTS | SW2FAULTS            | SW1CFAULTS | SW1BFAULTS | SW1AFAULTS  |
|     |               |      |              | 0                   | x         | x          | x          | x                    | x          | x          |             |
| 0E  | INTSTAT3      | RW1C | 8'b0000_0000 | OTP_ECCI            | —         | —          | —          | —                    | —          | —          | SWBSTFAULTI |
|     |               |      |              | 0                   | 0         | 0          | 0          | 0                    | 0          | 0          |             |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Add | Register name | R/W   | Default      | BITS[7:0]          |            |                 |             |                |             |             |             |             |
|-----|---------------|-------|--------------|--------------------|------------|-----------------|-------------|----------------|-------------|-------------|-------------|-------------|
|     |               |       |              | 7                  | 6          | 5               | 4           | 3              | 2           | 1           | 0           |             |
| 0F  | INTMASK3      | R/W   | 8'b1000_0001 | OTP_ECCM           | —          | —               | —           | —              | —           | —           | —           | SWBSTFAULTM |
|     |               |       |              | 1                  | 0          | 0               | 0           | 0              | 0           | 0           | 0           | 1           |
| 10  | INTSENSE3     | R     | 8'b0000_000x | OTP_ECCS           | —          | —               | —           | —              | —           | —           | —           | SWBSTFAULTS |
|     |               |       |              | 0                  | 0          | 0               | 0           | 0              | 0           | 0           | 0           | x           |
| 11  | INTSTAT4      | RW1C  | 8'b0000_0000 | —                  | —          | VGEN6FAULTI     | VGEN5FAULTI | VGEN4FAULTI    | VGEN3FAULTI | VGEN2FAULTI | VGEN1FAULTI |             |
|     |               |       |              | 0                  | 0          | 0               | 0           | 0              | 0           | 0           | 0           | 0           |
| 12  | INTMASK4      | R/W   | 8'b0011_1111 | —                  | —          | VGEN6FAULTM     | VGEN5FAULTM | VGEN4FAULTM    | VGEN3FAULTM | VGEN2FAULTM | VGEN1FAULTM |             |
|     |               |       |              | 0                  | 0          | 1               | 1           | 1              | 1           | 1           | 1           |             |
| 13  | INTSENSE4     | R     | 8'b00xx_xxxx | —                  | —          | VGEN6FAULTS     | VGEN5FAULTS | VGEN4FAULTS    | VGEN3FAULTS | VGEN2FAULTS | VGEN1FAULTS |             |
|     |               |       |              | 0                  | 0          | x               | x           | x              | x           | x           | x           |             |
| 1A  | COINCTL       | R/W   | 8'b0000_0000 | —                  | —          | —               | —           | COINCHEN       |             | VCOIN[2:0]  |             |             |
|     |               |       |              | 0                  | 0          | 0               | 0           | 0              | 0           | 0           | 0           |             |
| 1B  | PWRCTL        | R/W   | 8'b0001_0000 | REGSCPEN           | STANDBY1NV | STBYDLY[1:0]    |             | PWRONDBNC[1:0] |             | PWRONRSTEN  | RESTARTEN   |             |
|     |               |       |              | 0                  | 0          | 0               | 1           | 0              | 0           | 0           | 0           |             |
| 1C  | MEMA          | R/W   | 8'b0000_0000 | MEMA[7:0]          |            |                 |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | 0               | 0           | 0              | 0           | 0           | 0           |             |
| 1D  | MEMB          | R/W   | 8'b0000_0000 | MEMB[7:0]          |            |                 |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | 0               | 0           | 0              | 0           | 0           | 0           |             |
| 1E  | MEMC          | R/W   | 8'b0000_0000 | MEMC[7:0]          |            |                 |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | 0               | 0           | 0              | 0           | 0           | 0           |             |
| 1F  | MEMD          | R/W   | 8'b0000_0000 | MEMD[7:0]          |            |                 |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | 0               | 0           | 0              | 0           | 0           | 0           |             |
| 20  | SW1ABVOLT     | R/W/M | 8'b00xx_xxxx | —                  | —          | SW1AB[5:0]      |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | x               | x           | x              | x           | x           | x           |             |
| 21  | SW1ABSTBY     | R/W   | 8'b00xx_xxxx | —                  | —          | SW1ABSTBY[5:0]  |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | x               | x           | x              | x           | x           | x           |             |
| 22  | SW1ABOFF      | R/W   | 8'b00xx_xxxx | —                  | —          | SW1ABOFF[5:0]   |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | x               | x           | x              | x           | x           | x           |             |
| 23  | SW1ABMODE     | R/W   | 8'b0000_1000 | —                  | —          | SW1ABOMODE      | —           | SW1ABMODE[3:0] |             |             |             |             |
|     |               |       |              | 0                  | 0          | 0               | 0           | 1              | 0           | 0           | 0           |             |
| 24  | SW1ABCONF     | R/W   | 8'bx00_xx00  | SW1ABDVSSPEED[1:0] |            | SW1BAPHASE[1:0] |             | SW1ABFREQ[1:0] |             | —           | SW1ABILIM   |             |
|     |               |       |              | x                  | x          | 0               | 0           | x              | x           | 0           | 0           |             |
| 2E  | SW1CVOLT      | R/W   | 8'b00xx_xxxx | —                  | —          | SW1C[5:0]       |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | x               | x           | x              | x           | x           | x           |             |
| 2F  | SW1CSTBY      | R/W   | 8'b00xx_xxxx | —                  | —          | SW1CSTBY[5:0]   |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | x               | x           | x              | x           | x           | x           |             |
| 30  | SW1COFF       | R/W   | 8'b00xx_xxxx | —                  | —          | SW1COFF[5:0]    |             |                |             |             |             |             |
|     |               |       |              | 0                  | 0          | x               | x           | x              | x           | x           | x           |             |
| 31  | SW1CMODE      | R/W   | 8'b0000_1000 | —                  | —          | SW1COMODE       | —           | SW1CMODE[3:0]  |             |             |             |             |
|     |               |       |              | 0                  | 0          | 0               | 0           | 1              | 0           | 0           | 0           |             |
| 32  | SW1CCONF      | R/W   | 8'bx00_xx00  | SW1CDVSSPEED[1:0]  |            | SW1CPHASE[1:0]  |             | SW1CFREQ[1:0]  |             | —           | SW1CILIM    |             |
|     |               |       |              | x                  | x          | 0               | 0           | x              | x           | 0           | 0           |             |
| 35  | SW2VOLT       | R/W   | 8'b0xxx_xxxx | —                  | SW2[6:0]   |                 |             |                |             |             |             |             |
|     |               |       |              | 0                  | x          | x               | x           | x              | x           | x           | x           |             |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Add | Register name | R/W | Default      | BITS[7:0]         |                     |                |           |                 |   |                 |          |
|-----|---------------|-----|--------------|-------------------|---------------------|----------------|-----------|-----------------|---|-----------------|----------|
|     |               |     |              | 7                 | 6                   | 5              | 4         | 3               | 2 | 1               | 0        |
| 36  | SW2STBY       | R/W | 8'b0xxx_xxxx | —                 | SW2STBY[6:0]        |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 37  | SW2OFF        | R/W | 8'b0xxx_xxxx | —                 | SW2OFF[6:0]         |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 38  | SW2MODE       | R/W | 8'b0000_1000 | —                 | —                   | SW2OMODE       | —         | SW2MODE[3:0]    |   |                 |          |
|     |               |     |              | 0                 | 0                   | 0              | 0         | 1               | 0 | 0               | 0        |
| 39  | SW2CONF       | R/W | 8'bxx01_xx00 | SW2DVSSPEED[1:0]  |                     | SW2PHASE[1:0]  |           | SW2FREQ[1:0]    |   | —               | SW2ILIM  |
|     |               |     |              | x                 | x                   | 0              | 1         | x               | x | 0               | 0        |
| 3C  | SW3AVOLT      | R/W | 8'b0xxx_xxxx | —                 | SW3A[6:0]           |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 3D  | SW3ASTBY      | R/W | 8'b0xxx_xxxx | —                 | SW3ASTBY[6:0]       |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 3E  | SW3AOFF       | R/W | 8'b0xxx_xxxx | —                 | SW3AOFF[6:0]        |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 3F  | SW3AMODE      | R/W | 8'b0000_1000 | —                 | —                   | SW3AOMODE      | —         | SW3AMODE[3:0]   |   |                 |          |
|     |               |     |              | 0                 | 0                   | 0              | 0         | 1               | 0 | 0               | 0        |
| 40  | SW3ACONF      | R/W | 8'bxx10_xx00 | SW3ADVSSPEED[1:0] |                     | SW3APHASE[1:0] |           | SW3AFREQ[1:0]   |   | —               | SW3AILIM |
|     |               |     |              | x                 | x                   | 1              | 0         | x               | x | 0               | 0        |
| 43  | SW3BVOLT      | R/W | 8'b0xxx_xxxx | —                 | SW3B[6:0]           |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 44  | SW3BSTBY      | R/W | 8'b0xxx_xxxx | —                 | SW3BSTBY[6:0]       |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 45  | SW3BOFF       | R/W | 8'b0xxx_xxxx | —                 | SW3BOFF[6:0]        |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 46  | SW3BMODE      | R/W | 8'b0000_1000 | —                 | —                   | SW3BOMODE      | —         | SW3BMODE[3:0]   |   |                 |          |
|     |               |     |              | 0                 | 0                   | 0              | 0         | 1               | 0 | 0               | 0        |
| 47  | SW3BCONF      | R/W | 8'bxx10_xx00 | SW3BDVSSPEED[1:0] |                     | SW3BPHASE[1:0] |           | SW3BFREQ[1:0]   |   | —               | SW3BILIM |
|     |               |     |              | x                 | x                   | 1              | 0         | x               | x | 0               | 0        |
| 4A  | SW4VOLT       | R/W | 8'b0xxx_xxxx | —                 | SW4[6:0]            |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 4B  | SW4STBY       | R/W | 8'b0xxx_xxxx | —                 | SW4STBY[6:0]        |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 4C  | SW4OFF        | R/W | 8'b0xxx_xxxx | —                 | SW4OFF[6:0]         |                |           |                 |   |                 |          |
|     |               |     |              | 0                 | x                   | x              | x         | x               | x | x               | x        |
| 4D  | SW4MODE       | R/W | 8'b0000_1000 | —                 | —                   | SW4OMODE       | —         | SW4MODE[3:0]    |   |                 |          |
|     |               |     |              | 0                 | 0                   | 0              | 0         | 1               | 0 | 0               | 0        |
| 4E  | SW4CONF       | R/W | 8'bxx11_xx00 | SW4DVSSPEED[1:0]  |                     | SW4PHASE[1:0]  |           | SW4FREQ[1:0]    |   | —               | SW4ILIM  |
|     |               |     |              | x                 | x                   | 1              | 1         | x               | x | 0               | 0        |
| 66  | SWBSTCTL      | R/W | 8'b0xx0_10xx | —                 | SWBST1STBYMODE[1:0] |                | —         | SWBST1MODE[1:0] |   | SWBST1VOLT[1:0] |          |
|     |               |     |              | 0                 | x                   | x              | 0         | 1               | 0 | x               | x        |
| 6A  | VREFDDRCTL    | R/W | 8'b000x_0000 | —                 | —                   | —              | VREFDDREN | —               | — | —               | —        |
|     |               |     |              | 0                 | 0                   | 0              | x         | 0               | 0 | 0               | 0        |
| 6B  | VSNVCTL       | R/W | 8'b0000_0xxx | —                 | —                   | —              | —         | VSNVSVOLT[2:0]  |   |                 |          |
|     |               |     |              | 0                 | 0                   | 0              | 0         | 0               | 0 | x               | x        |
| 6C  | VGEN1CTL      | R/W | 8'b000x_xxxx | —                 | —                   | —              | —         | VGEN1[3:0]      |   |                 |          |
|     |               |     |              | 0                 | 0                   | 0              | 0         | x               | x | x               | x        |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Add | Register name | R/W | Default      | BITS[7:0] |               |           |           |            |   |   |   |
|-----|---------------|-----|--------------|-----------|---------------|-----------|-----------|------------|---|---|---|
|     |               |     |              | 7         | 6             | 5         | 4         | 3          | 2 | 1 | 0 |
| 6D  | VGEN2CTL      | R/W | 8'b000x_XXXX | —         | VGEN2LPW<br>R | VGEN2STBY | VGEN2EN   | VGEN2[3:0] |   |   |   |
|     |               |     |              | 0         | 0             | 0         | x         | x          | x | x | x |
| 6E  | VGEN3CTL      | R/W | 8'b000x_XXXX | —         | VGEN3LPW<br>R | VGEN3STBY | VGEN3EN   | VGEN3[3:0] |   |   |   |
|     |               |     |              | 0         | 0             | 0         | x         | x          | x | x | x |
| 6F  | VGEN4CTL      | R/W | 8'b000x_XXXX | —         | VGEN4LPW<br>R | VGEN4STBY | VGEN4EN   | VGEN4[3:0] |   |   |   |
|     |               |     |              | 0         | 0             | 0         | x         | x          | x | x | x |
| 70  | VGEN5CTL      | R/W | 8'b000x_XXXX | —         | VGEN5LPW<br>R | VGEN5STBY | VGEN5EN   | VGEN5[3:0] |   |   |   |
|     |               |     |              | 0         | 0             | 0         | x         | x          | x | x | x |
| 71  | VGEN6CTL      | R/W | 8'b000x_XXXX | —         | VGEN6LPW<br>R | VGEN6STBY | VGEN6EN   | VGEN6[3:0] |   |   |   |
|     |               |     |              | 0         | 0             | 0         | x         | x          | x | x | x |
| 7F  | Page Register | R/W | 8'b0000_0000 | —         | —             | —         | PAGE[4:0] |            |   |   |   |
|     |               |     |              | 0         | 0             | 0         | 0         | 0          | 0 | 0 | 0 |

Table 135. Extended page 1

| Address | Register name    | TYPE | Default      | BITS[7:0] |                |                 |                 |         |                 |             |              |                  |
|---------|------------------|------|--------------|-----------|----------------|-----------------|-----------------|---------|-----------------|-------------|--------------|------------------|
|         |                  |      |              | 7         | 6              | 5               | 4               | 3       | 2               | 1           | 0            |                  |
| 80      | OTP FUSE READ EN | R/W  | 8'b000x_XXX0 | —         | —              | —               | —               | —       | —               | —           | —            | OTP FUSE READ EN |
|         |                  |      |              | 0         | 0              | 0               | x               | x       | x               | x           | 0            |                  |
| 84      | OTP LOAD MASK    | R/W  | 8'b0000_0000 | START     | RL PWBRTN      | FORCE PWRCTL    | RL PWRCTL       | RL OTP  | RL OTP ECC      | RL OTP FUSE | RL TRIM FUSE |                  |
|         |                  |      |              | 0         | 0              | 0               | 0               | 0       | 0               | 0           | 0            |                  |
| 8A      | OTP ECC SE1      | R    | 8'bxxx0_0000 | —         | —              | —               | ECC5_SE         | ECC4_SE | ECC3_SE         | ECC2_SE     | ECC1_SE      |                  |
|         |                  |      |              | x         | x              | x               | 0               | 0       | 0               | 0           | 0            |                  |
| 8B      | OTP ECC SE2      | R    | 8'bxxx0_0000 | —         | —              | —               | ECC10_SE        | ECC9_SE | ECC8_SE         | ECC7_SE     | ECC6_SE      |                  |
|         |                  |      |              | x         | x              | x               | 0               | 0       | 0               | 0           | 0            |                  |
| 8C      | OTP ECC DE1      | R    | 8'bxxx0_0000 | —         | —              | —               | ECC5_DE         | ECC4_DE | ECC3_DE         | ECC2_DE     | ECC1_DE      |                  |
|         |                  |      |              | x         | x              | x               | 0               | 0       | 0               | 0           | 0            |                  |
| 8D      | OTP ECC DE2      | R    | 8'bxxx0_0000 | —         | —              | —               | ECC10_DE        | ECC9_DE | ECC8_DE         | ECC7_DE     | ECC6_DE      |                  |
|         |                  |      |              | x         | x              | x               | 0               | 0       | 0               | 0           | 0            |                  |
| A0      | OTP SW1AB VOLT   | R/W  | 8'b00xx_XXXX | —         | —              | SW1AB_VOLT[5:0] |                 |         |                 |             |              |                  |
|         |                  |      |              | 0         | 0              | x               | x               | x       | x               | x           | x            |                  |
| A1      | OTP SW1AB SEQ    | R/W  | 8'b000x_XXxX | —         | SW1AB_SEQ[4:0] |                 |                 |         |                 |             |              |                  |
|         |                  |      |              | 0         | 0              | 0               | x               | x       | x               | x           | x            |                  |
| A2      | OTP SW1AB CONFIG | R/W  | 8'b0000_XXXX | —         | —              | —               | SW1_CONFIG[1:0] |         | SW1AB_FREQ[1:0] |             |              |                  |
|         |                  |      |              | 0         | 0              | 0               | 0               | x       | x               | x           | x            |                  |
| A8      | OTP SW1C VOLT    | R/W  | 8'b00xx_XXXX | —         | —              | SW1C_VOLT[5:0]  |                 |         |                 |             |              |                  |
|         |                  |      |              | 0         | 0              | x               | x               | x       | x               | x           | x            |                  |
| A9      | OTP SW1C SEQ     | R/W  | 8'b000x_XXXX | —         | SW1C_SEQ[4:0]  |                 |                 |         |                 |             |              |                  |
|         |                  |      |              | 0         | 0              | 0               | x               | x       | x               | x           | x            |                  |
| AA      | OTP SW1C CONFIG  | R/W  | 8'b0000_00xx | —         | —              | —               | SW1C_FREQ[1:0]  |         |                 |             |              |                  |
|         |                  |      |              | 0         | 0              | 0               | 0               | 0       | 0               | x           | x            |                  |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Address | Register name   | TYPE | Default      | BITS[7:0] |                |   |   |                  |               |                |   |  |
|---------|-----------------|------|--------------|-----------|----------------|---|---|------------------|---------------|----------------|---|--|
|         |                 |      |              | 7         | 6              | 5 | 4 | 3                | 2             | 1              | 0 |  |
| AC      | OTP SW2 VOLT    | R/W  | 8'b0xxx_xxxx | —         | SW2_VOLT[5:0]  |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | x              | x | x | x                | x             | x              | x |  |
| AD      | OTP SW2 SEQ     | R/W  | 8'b000x_xxxx | —         | SW2_SEQ[4:0]   |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | x | x                | x             | x              | x |  |
| AE      | OTP SW2 CONFIG  | R/W  | 8'b0000_00xx | —         | —              |   |   | SW2_FREQ[1:0]    |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | 0 | 0                | 0             | x              | x |  |
| B0      | OTP SW3A VOLT   | R/W  | 8'b0xxx_xxxx | —         | SW3A_VOLT[6:0] |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | x              | x | x | x                | x             | x              | x |  |
| B1      | OTP SW3A SEQ    | R/W  | 8'b000x_xxxx | —         | SW3A_SEQ[4:0]  |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | x | x                | x             | x              | x |  |
| B2      | OTP SW3A CONFIG | R/W  | 8'b0000_xxxx | —         | —              |   |   | SW3_CONFIG[1:0]  |               | SW3A_FREQ[1:0] |   |  |
|         |                 |      |              | 0         | 0              | 0 | 0 | x                | x             | x              | x |  |
| B4      | OTP SW3B VOLT   | R/W  | 8'b0xxx_xxxx | —         | SW3B_VOLT[6:0] |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | x              | x | x | x                | x             | x              | x |  |
| B5      | OTP SW3B SEQ    | R/W  | 8'b000x_xxxx | —         | SW3B_SEQ[4:0]  |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | x | x                | x             | x              | x |  |
| B6      | OTP SW3B CONFIG | R/W  | 8'b0000_00xx | —         | —              |   |   | SW3B_CONFIG[1:0] |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | 0 | 0                | 0             | x              | x |  |
| B8      | OTP SW4 VOLT    | R/W  | 8'b00xx_xxxx | —         | SW4_VOLT[6:0]  |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | 0              | x | x | x                | x             | x              | x |  |
| B9      | OTP SW4 SEQ     | R/W  | 8'b000x_xxxx | —         | SW4_SEQ[4:0]   |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | x | x                | x             | x              | x |  |
| BA      | OTP SW4 CONFIG  | R/W  | 8'b000x_xxxx | —         | —              |   |   | VTT              | SW4_FREQ[1:0] |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | x | x                | x             | x              | x |  |
| BC      | OTP SWBST VOLT  | R/W  | 8'b0000_00xx | —         | —              |   |   | SWBST_VOLT[1:0]  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | 0 | 0                | 0             | x              | x |  |
| BD      | OTP SWBST SEQ   | R/W  | 8'b0000_xxxx | —         | SWBST_SEQ[4:0] |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | 0 | x                | x             | x              | x |  |
| C0      | OTP VSNVS VOLT  | R/W  | 8'b0000_0xxx | —         | —              |   |   | VSNVS_VOLT[2:0]  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | 0 | 0                | 0             | x              | x |  |
| C4      | OTP VREFDDR SEQ | R/W  | 8'b000x_x0xx | —         | —              |   |   | VREFDDR_SEQ[4:0] |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | x | x                | 0             | x              | x |  |
| C8      | OTP VGEN1 VOLT  | R/W  | 8'b0000_xxxx | —         | —              |   |   | VGEN1_VOLT[3:0]  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | 0 | x                | x             | x              | x |  |
| C9      | OTP VGEN1 SEQ   | R/W  | 8'b000x_xxxx | —         | —              |   |   | —                |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | 0 | 0                | 0             | 0              | 1 |  |
| CC      | OTP VGEN2 VOLT  | R/W  | 8'b0000_xxxx | —         | —              |   |   | VGEN2_VOLT[3:0]  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | 0 | x                | x             | x              | x |  |
| CD      | OTP VGEN2 SEQ   | R/W  | 8'b000x_xxxx | —         | VGEN2_SEQ[4:0] |   |   |                  |               |                |   |  |
|         |                 |      |              | 0         | 0              | 0 | x | x                | x             | x              | x |  |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Address           | Register name     | TYPE  | Default      | BITS[7:0] |              |   |                |                 |              |                     |              |
|-------------------|-------------------|-------|--------------|-----------|--------------|---|----------------|-----------------|--------------|---------------------|--------------|
|                   |                   |       |              | 7         | 6            | 5 | 4              | 3               | 2            | 1                   | 0            |
| D0                | OTP VGEN3 VOLT    | R/W   | 8'b0000_XXXX | —         | —            | — | —              | VGEN3_VOLT[3:0] |              |                     |              |
|                   |                   |       |              | 0         | 0            | 0 | 0              | x               | x            | x                   | x            |
| D1                | OTP VGEN3 SEQ     | R/W   | 8'b000x_XXXX | —         | —            | — | VGEN3_SEQ[4:0] |                 |              |                     |              |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| D4                | OTP VGEN4 VOLT    | R/W   | 8'b0000_XXXX | —         | —            | — | —              | VGEN4_VOLT[3:0] |              |                     |              |
|                   |                   |       |              | 0         | 0            | 0 | 0              | x               | x            | x                   | x            |
| D5                | OTP VGEN4 SEQ     | R/W   | 8'b000x_XXXX | —         | —            | — | VGEN4_SEQ[4:0] |                 |              |                     |              |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| D8                | OTP VGEN5 VOLT    | R/W   | 8'b0000_XXXX | —         | —            | — | —              | VGEN5_VOLT[3:0] |              |                     |              |
|                   |                   |       |              | 0         | 0            | 0 | 0              | x               | x            | x                   | x            |
| D9                | OTP VGEN5 SEQ     | R/W   | 8'b000x_XXXX | —         | —            | — | VGEN5_SEQ[4:0] |                 |              |                     |              |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| DC                | OTP VGEN6 VOLT    | R/W   | 8'b0000_XXXX | —         | —            | — | —              | VGEN6_VOLT[3:0] |              |                     |              |
|                   |                   |       |              | 0         | 0            | 0 | 0              | x               | x            | x                   | x            |
| DD                | OTP VGEN6 SEQ     | R/W   | 8'b000x_XXXX | —         | —            | — | VGEN6_SEQ[4:0] |                 |              |                     |              |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| E0                | OTP PU CONFIG1    | R/W   | 8'b000x_XXXX | —         | —            | — | PWRON_CFG1     | SWDVS_CLK1[1:0] |              | SEQ_CLK_SPEED1[1:0] |              |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| E1                | OTP PU CONFIG2    | R/W   | 8'b000x_XXXX | —         | —            | — | PWRON_CFG2     | SWDVS_CLK2[1:0] |              | SEQ_CLK_SPEED2[1:0] |              |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| E2                | OTP PU CONFIG3    | R/W   | 8'b000x_XXXX | —         | —            | — | PWRON_CFG3     | SWDVS_CLK3[1:0] |              | SEQ_CLK_SPEED3[1:0] |              |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| E3                | OTP PU CONFIG XOR | R     | 8'b000x_XXXX | —         | —            | — | PWRON_CFG_XOR  | SWDVS_CLK3_XOR  |              | SEQ_CLK_SPEED_XOR   |              |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| E4 <sup>[1]</sup> | OTP FUSE POR1     | R/W   | 8'b0000_00x0 | TBB_POR   | SOFT_FUSEPOR | — | —              | —               | —            | FUSE_POR1           | —            |
|                   |                   |       |              | 0         | 0            | 0 | 0              | 0               | 0            | 0                   | x            |
| E5                | OTP FUSE POR1     | R/W   | 8'b0000_00x0 | RSVD      | RSVD         | — | —              | —               | —            | FUSE_POR2           | —            |
|                   |                   |       |              | 0         | 0            | 0 | 0              | 0               | 0            | 0                   | x            |
| E6                | OTP FUSE POR1     | R/W   | 8'b0000_00x0 | RSVD      | RSVD         | — | —              | —               | —            | FUSE_POR3           | —            |
|                   |                   |       |              | 0         | 0            | 0 | 0              | 0               | 0            | 0                   | x            |
| E7                | OTP FUSE POR XOR  | R     | 8'b0000_00x0 | RSVD      | RSVD         | — | —              | —               | —            | FUSE_POR_XOR        | —            |
|                   |                   |       |              | 0         | 0            | 0 | 0              | 0               | 0            | 0                   | x            |
| E8                | OTP PWRGD EN      | R/W/M | 8'b0000_000x | —         | —            | — | —              | —               | —            | —                   | OTP_PG_EN    |
|                   |                   |       |              | 0         | 0            | 0 | 0              | 0               | 0            | 0                   | x            |
| F0                | OTP EN ECCO       | R/W   | 8'b000x_XXXX | —         | —            | — | EN_ECC_BANK5   | EN_ECC_BANK4    | EN_ECC_BANK3 | EN_ECC_BANK2        | EN_ECC_BANK1 |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| F1                | OTP EN ECC1       | R/W   | 8'b000x_XXXX | —         | —            | — | EN_ECC_BANK10  | EN_ECC_BANK9    | EN_ECC_BANK8 | EN_ECC_BANK7        | EN_ECC_BANK6 |
|                   |                   |       |              | 0         | 0            | 0 | x              | x               | x            | x                   | x            |
| F4                | OTP SPARE2_4      | R/W   | 8'b0000_XXXX | —         | —            | — | RSVD           |                 |              |                     |              |
|                   |                   |       |              | 0         | 0            | 0 | 0              | x               | x            | x                   | x            |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Address | Register name | TYPE | Default      | BITS[7:0] |   |   |   |                 |                   |          |   |
|---------|---------------|------|--------------|-----------|---|---|---|-----------------|-------------------|----------|---|
|         |               |      |              | 7         | 6 | 5 | 4 | 3               | 2                 | 1        | 0 |
| F5      | OTP SPARE4_3  | R/W  | 8'b0000_0xxx | —         | — | — | — | —               | RSVD              |          |   |
|         |               |      |              | 0         | 0 | 0 | 0 | 0               | x                 | x        | x |
| F6      | OTP SPARE6_2  | R/W  | 8'b0000_00xx | —         | — | — | — | —               | RSVD              |          |   |
|         |               |      |              | 0         | 0 | 0 | 0 | 0               | 0                 | x        | x |
| F7      | OTP SPARE7_1  | R/W  | 8'b0000_0xxx | —         | — | — | — | —               | RSVD              |          |   |
|         |               |      |              | 0         | 0 | 0 | 0 | 0               | x                 | x        | x |
| FE      | OTP DONE      | R/W  | 8'b0000_000x | —         | — | — | — | —               | —                 | OTP_DONE |   |
|         |               |      |              | 0         | 0 | 0 | 0 | 0               | 0                 | 0        | x |
| FF      | OTP I2C ADDR  | R/W  | 8'b0000_0xxx | —         | — | — | — | I2C_SLV_ADDR[3] | I2C_SLV_ADDR[2:0] |          |   |
|         |               |      |              | 0         | 0 | 0 | 0 | 1               | x                 | x        | x |

- [1] In the PF4210 FUSE\_POR1, FUSE\_POR2, and FUSE\_POR3 are XOR'ed into the FUSE\_POR\_XOR bit. The FUSE\_POR\_XOR has to be 1 for fuses to be loaded. This can be achieved by setting any one or all of the FUSE\_PORx bits. In PF4210, the XOR function is removed. It is required to set all of the FUSE\_PORx bits to be able to load the fuses.

Table 136. Extended Page 2

| Address | Register name          | TYPE | Default      | BITS[7:0]                      |                     |                |                    |                |                   |                   |                |
|---------|------------------------|------|--------------|--------------------------------|---------------------|----------------|--------------------|----------------|-------------------|-------------------|----------------|
|         |                        |      |              | 7                              | 6                   | 5              | 4                  | 3              | 2                 | 1                 | 0              |
| 81      | SW1AB PWRSTG           | R/W  | 8'b1111_1111 | RSVD                           | RSVD                | RSVD           | RSVD               | RSVD           | SW1AB_PWRSTG[2:0] |                   |                |
|         |                        |      |              | 1                              | 1                   | 1              | 1                  | 1              | 1                 | 1                 | 1              |
| 82      | PWRSTG RSVD            | R    | 8'b0000_0000 | PWRSTGRSVD                     |                     |                |                    |                |                   |                   |                |
|         |                        |      |              | 0                              | 0                   | 0              | 0                  | 0              | 0                 | 0                 | 0              |
| 83      | SW1C PWRSTG            | R    | 8'b1111_1111 | RSVD                           | RSVD                | RSVD           | RSVD               | RSVD           | SW1C_PWRSTG[2:0]  |                   |                |
|         |                        |      |              | 1                              | 1                   | 1              | 1                  | 1              | 1                 | 1                 | 1              |
| 84      | SW2 PWRSTG             | R    | 8'b1111_1111 | RSVD                           | RSVD                | RSVD           | RSVD               | RSVD           | SW2_PWRSTG[2:0]   |                   |                |
|         |                        |      |              | 1                              | 1                   | 1              | 1                  | 1              | 1                 | 1                 | 1              |
| 85      | SW3A PWRSTG            | R    | 8'b1111_1111 | RSVD                           | RSVD                | RSVD           | RSVD               | RSVD           | SW3A_PWRSTG[2:0]  |                   |                |
|         |                        |      |              | 1                              | 1                   | 1              | 1                  | 1              | 1                 | 1                 | 1              |
| 86      | SW3B PWRSTG            | R    | 8'b1111_1111 | RSVD                           | RSVD                | RSVD           | RSVD               | RSVD           | SW3B_PWRSTG[2:0]  |                   |                |
|         |                        |      |              | 1                              | 1                   | 1              | 1                  | 1              | 1                 | 1                 | 1              |
| 87      | SW4 PWRSTG             | R    | 8'b0111_1111 | FSLEXT_THERM_DISABLE           | PWRGD_SHDWN_DISABLE | RSVD           | RSVD               | RSVD           | SW4_PWRSTG[2:0]   |                   |                |
|         |                        |      |              | 0                              | 0                   | 1              | 1                  | 1              | 1                 | 1                 | 1              |
| 88      | PWRCTRL OTP CTRL       | R/W  | 8'b0000_0001 | —                              | —                   | —              | —                  | —              | PWRGD_EN          | OTP_SHDWN_EN      |                |
|         |                        |      |              | 0                              | 0                   | 0              | 0                  | 0              | 0                 | 0                 | 1              |
| 8D      | I2C WRITE ADDRESS TRAP | R/W  | 8'b0000_0000 | I2C_WRITE_ADDRESS_TRAP[7:0]    |                     |                |                    |                |                   |                   |                |
|         |                        |      |              | 0                              | 0                   | 0              | 0                  | 0              | 0                 | 0                 | 0              |
| 8E      | I2C TRAP PAGE          | R/W  | 8'b0000_0000 | LET_IT_ROLL                    | RSVD                | RSVD           | I2C_TRAP_PAGE[4:0] |                |                   |                   |                |
|         |                        |      |              | 0                              | 0                   | 0              | 0                  | 0              | 0                 | 0                 | 0              |
| 8F      | I2C TRAP CNTR          | R/W  | 8'b0000_0000 | I2C_WRITE_ADDRESS_COUNTER[7:0] |                     |                |                    |                |                   |                   |                |
|         |                        |      |              | 0                              | 0                   | 0              | 0                  | 0              | 0                 | 0                 | 0              |
| 90      | IO DRV                 | R/W  | 8'b00xx_xxxx | SDA_DRV[1:0]                   |                     | SDWNB_DRV[1:0] |                    | INTB_DRV[1:0]  |                   | RESETMCU_DRV[1:0] |                |
|         |                        |      |              | 0                              | 0                   | x              | x                  | x              | x                 | x                 | x              |
| DO      | OTP AUTO ECC0          | R/W  | 8'b0000_0000 | —                              | —                   | —              | AUTO_ECC_BANK5     | AUTO_ECC_BANK4 | AUTO_ECC_BANK3    | AUTO_ECC_BANK2    | AUTO_ECC_BANK1 |
|         |                        |      |              | 0                              | 0                   | 0              | 0                  | 0              | 0                 | 0                 | 0              |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Address           | Register name  | TYPE | Default      | BITS[7:0]    |                |                    |                 |                |                |                |                |   |
|-------------------|----------------|------|--------------|--------------|----------------|--------------------|-----------------|----------------|----------------|----------------|----------------|---|
|                   |                |      |              | 7            | 6              | 5                  | 4               | 3              | 2              | 1              | 0              |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| D1                | OTP AUTO ECC1  | R/W  | 8'b0000_0000 | —            | —              | —                  | AUTO_ECC_BANK10 | AUTO_ECC_BANK9 | AUTO_ECC_BANK8 | AUTO_ECC_BANK7 | AUTO_ECC_BANK6 |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| D8 <sup>[1]</sup> | Reserved       | —    | 8'b0000_0000 | RSVD         |                |                    |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| D9 <sup>[1]</sup> | Reserved       | —    | 8'b0000_0000 | RSVD         |                |                    |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| E1                | OTP ECC CTRL1  | R/W  | 8'b0000_0000 | ECC1_EN_TBB  | ECC1_CALC_CIN  | ECC1_CIN_TBB[5:0]  |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| E2                | OTP ECC CTRL2  | R/W  | 8'b0000_0000 | ECC2_EN_TBB  | ECC2_CALC_CIN  | ECC2_CIN_TBB[5:0]  |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| E3                | OTP ECC CTRL3  | R/W  | 8'b0000_0000 | ECC3_EN_TBB  | ECC3_CALC_CIN  | ECC3_CIN_TBB[5:0]  |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| E4                | OTP ECC CTRL4  | R/W  | 8'b0000_0000 | ECC4_EN_TBB  | ECC4_CALC_CIN  | ECC4_CIN_TBB[5:0]  |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| E5                | OTP ECC CTRL5  | R/W  | 8'b0000_0000 | ECC5_EN_TBB  | ECC5_CALC_CIN  | ECC5_CIN_TBB[5:0]  |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| E6                | OTP ECC CTRL6  | R/W  | 8'b0000_0000 | ECC6_EN_TBB  | ECC6_CALC_CIN  | ECC6_CIN_TBB[5:0]  |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| E7                | OTP ECC CTRL7  | R/W  | 8'b0000_0000 | ECC7_EN_TBB  | ECC7_CALC_CIN  | ECC7_CIN_TBB[5:0]  |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| E8                | OTP ECC CTRL8  | R/W  | 8'b0000_0000 | ECC8_EN_TBB  | ECC8_CALC_CIN  | ECC8_CIN_TBB[5:0]  |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| E9                | OTP ECC CTRL9  | R/W  | 8'b0000_0000 | ECC9_EN_TBB  | ECC9_CALC_CIN  | ECC9_CIN_TBB[5:0]  |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| EA                | OTP ECC CTRL10 | R/W  | 8'b0000_0000 | ECC10_EN_TBB | ECC10_CALC_CIN | ECC10_CIN_TBB[5:0] |                 |                |                |                |                |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| F1                | OTP FUSE CTRL1 | R/W  | 8'b0000_0000 | —            | —              | —                  | —               | ANTIFUSE1_EN   | ANTIFUSE1_LOAD | ANTIFUSE1_RW   | BYPASS1        |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| F2                | OTP FUSE CTRL2 | R/W  | 8'b0000_0000 | —            | —              | —                  | —               | ANTIFUSE2_EN   | ANTIFUSE2_LOAD | ANTIFUSE2_RW   | BYPASS2        |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| F3                | OTP FUSE CTRL3 | R/W  | 8'b0000_0000 | —            | —              | —                  | —               | ANTIFUSE3_EN   | ANTIFUSE3_LOAD | ANTIFUSE3_RW   | BYPASS3        |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| F4                | OTP FUSE CTRL4 | R/W  | 8'b0000_0000 | —            | —              | —                  | —               | ANTIFUSE4_EN   | ANTIFUSE4_LOAD | ANTIFUSE4_RW   | BYPASS4        |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |
| F5                | OTP FUSE CTRL5 | R/W  | 8'b0000_0000 | —            | —              | —                  | —               | ANTIFUSE5_EN   | ANTIFUSE5_LOAD | ANTIFUSE5_RW   | BYPASS5        |   |
|                   |                |      |              | 0            | 0              | 0                  | 0               | 0              | 0              | 0              | 0              | 0 |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Address | Register name   | TYPE | Default      | BITS[7:0] |   |   |   |               |                 |               |          |
|---------|-----------------|------|--------------|-----------|---|---|---|---------------|-----------------|---------------|----------|
|         |                 |      |              | 7         | 6 | 5 | 4 | 3             | 2               | 1             | 0        |
| F6      | OTP FUSE CTRL6  | R/W  | 8'b0000_0000 | —         | — | — | — | ANTIFUSE6_EN  | ANTIFUSE6_LOAD  | ANTIFUSE6_RW  | BYPASS6  |
|         |                 |      |              | 0         | 0 | 0 | 0 | 0             | 0               | 0             | 0        |
| F7      | OTP FUSE CTRL7  | R/W  | 8'b0000_0000 | —         | — | — | — | ANTIFUSE7_EN  | ANTIFUSE7_LOAD  | ANTIFUSE7_RW  | BYPASS7  |
|         |                 |      |              | 0         | 0 | 0 | 0 | 0             | 0               | 0             | 0        |
| F8      | OTP FUSE CTRL8  | R/W  | 8'b0000_0000 | —         | — | — | — | ANTIFUSE8_EN  | ANTIFUSE8_LOAD  | ANTIFUSE8_RW  | BYPASS8  |
|         |                 |      |              | 0         | 0 | 0 | 0 | 0             | 0               | 0             | 0        |
| F9      | OTP FUSE CTRL9  | R/W  | 8'b0000_0000 | —         | — | — | — | ANTIFUSE9_EN  | ANTIFUSE9_LOAD  | ANTIFUSE9_RW  | BYPASS9  |
|         |                 |      |              | 0         | 0 | 0 | 0 | 0             | 0               | 0             | 0        |
| FA      | OTP FUSE CTRL10 | R/W  | 8'b0000_0000 | —         | — | — | — | ANTIFUSE10_EN | ANTIFUSE10_LOAD | ANTIFUSE10_RW | BYPASS10 |
|         |                 |      |              | 0         | 0 | 0 | 0 | 0             | 0               | 0             | 0        |

[1] Do not write in reserved registers.

## 11 Typical applications

### 11.1 Introduction

[Figure 33](#) provides a typical application diagram of the PF4210 PMIC together with its functional components. For details on component references and additional components such as filters, see individual sections.

11.1.1 Application diagram

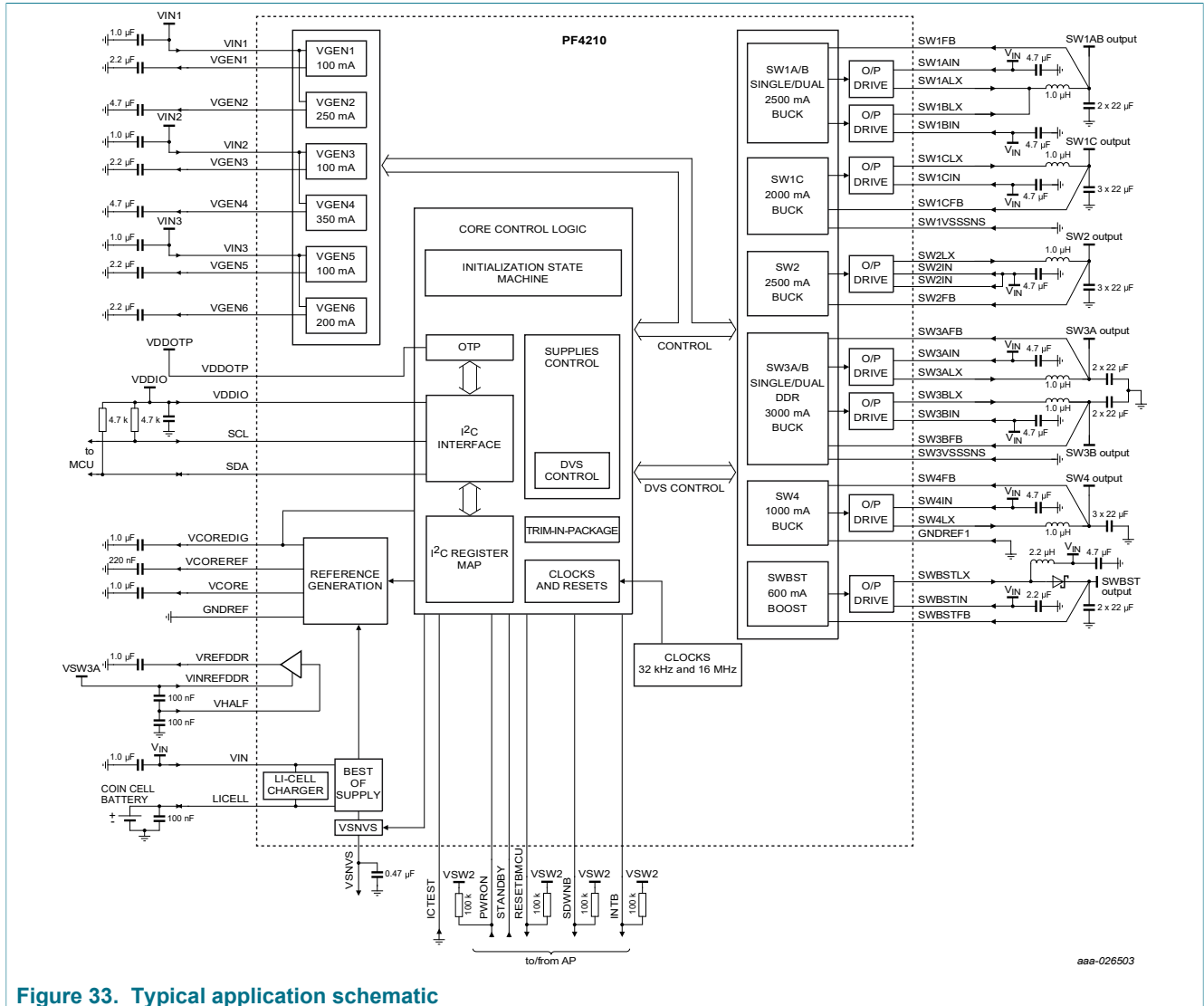


Figure 33. Typical application schematic

11.1.2 Bill of materials

The following table provides a complete list of the recommended components on a full-featured system using the PF4210 device for 0 °C to 85 °C applications. Components are provided with an example part number. Equivalent components may be used.

Table 137. Bill of materials 0 °C to 85 °C applications

| Value  | Qty | Description  | Part number       | Manufacturer [1] | Component/pin   |
|--|-----|--|-------------------|------------------|-----------------|
| <b>PMIC</b>                                  |     |  |                   |                  |                 |
|  | 1   | Power management IC  | PF4210            | NXP              |                 |
| <b>Buck, SW1AB (0.300 to 1.875 V), 2.5 A</b> |     |  |                   |                  |                 |
| 1.0 µH                                       | 1   | 2.5 x 2 x 1.2<br>I <sub>SAT</sub> = 3.4 A for 10 % drop,<br>DCR <sub>MAX</sub> = 49 mΩ | DFE252012R-H-1R0M | TOKO INC.        | Output inductor |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Value  | Qty | Description  | Part number        | Manufacturer <sup>[1]</sup> | Component/pin      |
|--|-----|--|--------------------|-----------------------------|--------------------|
| 22 µH  | 4   | 10 V X5R 0603  | GRM188R61A226ME15  | Murata                      | Output capacitance |
| 4.7 µF                                       | 2   | 10 V X5R 0402  | GRM155R61A475MEAA  | Murata                      | Input capacitance  |
| 0.1 µF                                       | 1   | 10 V X5R 0201  | GRM033R61A104ME84  | Murata                      | Input capacitance  |
| <b>Buck, SW1C (0.300 to 1.875 V), 2.0 A</b>  |     |  |                    |                             |                    |
| 1.0 µH                                       | 1   | 2.5 x 2 x 1.2<br>$I_{SAT} = 3.0$ A for 10 % drop,<br>$DCR_{MAX} = 59$ mΩ | DFE252012C-1R0M    | TOKO INC.                   | Output inductor    |
| 22 µF  | 3   | 10 V X5R 0603  | GRM188R61A226ME15  | Murata                      | Output capacitance |
| 4.7 µF                                       | 1   | 10 V X5R 0402  | GRM155R61A475MEAA  | Murata                      | Input capacitance  |
| 0.1 µF                                       | 1   | 10 V X5R 0201  | GRM033R61A104ME84  | Murata                      | Input capacitance  |
| <b>Buck, SW2 (0.400 to 3.300 V), 2.5 A</b>   |     |  |                    |                             |                    |
| 1.0 µH                                       | 1   | 2.5 x 2 x 1.2<br>$I_{SAT} = 3.0$ A for 10 % drop,<br>$DCR_{MAX} = 59$ mΩ | DFE252012C-1R0M    | TOKO INC.                   | Output inductor    |
| 22 µF  | 3   | 10 V X5R 0603  | GRM188R61A226ME15  | Murata                      | Output capacitance |
| 4.7 µF                                       | 1   | 10 V X5R 0402  | GRM155R61A475MEAA  | Murata                      | Input capacitance  |
| 0.1 µF                                       | 1   | 10 V X5R 0201  | GRM033R61A104ME84  | Murata                      | Input capacitance  |
| <b>Buck, SW3AB (0.400 to 3.300 V), 3.0 A</b> |     |  |                    |                             |                    |
| 1.0 µH                                       | 1   | 2.5 x 2 x 1.2<br>$I_{SAT} = 3.4$ A for 10 % drop,<br>$DCR_{MAX} = 49$ mΩ | DFE252012R-1R0M    | TOKO INC.                   | Output inductor    |
| 22 µF  | 3   | 10 V X5R 0603  | GRM188R61A226ME15  | Murata                      | Output capacitance |
| 4.7 µF                                       | 2   | 10 V X5R 0402  | GRM155R61A475MEAA  | Murata                      | Input capacitance  |
| 0.1 µF                                       | 1   | 10 V X5R 0201  | GRM033R61A104ME84  | Murata                      | Input capacitance  |
| <b>Buck, SW4 (0.400 to 3.300 V), 1.0 A</b>   |     |  |                    |                             |                    |
| 1.0 µH                                       | 1   | 2 x 1.6 x 0.9<br>$I_{SAT} = 2.0$ A for 30 % drop,<br>$DCR_{MAX} = 80$ mΩ | LQM2MPN1R0MGH      | Murata                      | Output inductor    |
| 22 µF  | 3   | 10 V X5R 0603  | GRM188R61A226ME15  | Murata                      | Output capacitance |
| 4.7 µF                                       | 2   | 10 V X5R 0402  | GRM155R61A475MEAA  | Murata                      | Input capacitance  |
| 0.1 µF                                       | 1   | 10 V X5R 0201  | GRM033R61A104ME84  | Murata                      | Input capacitance  |
| <b>BOOST, SWBST 5.0 V, 600 mA</b>            |     |  |                    |                             |                    |
| 2.2 µH                                       | 1   | 2 x 1.6 x 1<br>$I_{SAT} = 2.4$ A for 10 % drop                           | DFE201610E-2R2M    | TOKO INC.                   | Output inductor    |
| 22 µF  | 2   | 10 V X5R 0603  | GRM188R61A226ME15D | Murata                      | Output capacitance |
| 10 µF  | 3   | 10 V X5R 0402  | GRM155R61A106ME11  | Murata                      | Input capacitance  |
| 2.2 µF                                       | 1   | 10 V X5R 0201  | GRM033R61A225ME47  | Murata                      | Input capacitance  |
| 0.1 µF                                       | 1   | 10 V X5R 0201  | GRM033R61A104KE84  | Murata                      | Input capacitance  |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Value                            | Qty | Description                          | Part number       | Manufacturer <sup>[1]</sup> | Component/pin                                       |
|----------------------------------|-----|--------------------------------------|-------------------|-----------------------------|---|
| 1.0 A                            | 1   | DIODE SCH PWR RECT<br>1.0 A 20 V SMT | MBR120LSFT3G      | ON Semiconductor            | Schottky diode                                      |
| <b>LDO, VGEN1, 2, 3, 4, 5, 6</b> |     |                                      |                   |                             |   |
| 4.7 $\mu$ F                      | 1   | 10 V X5R 0402                        | GRM155R61A475MEAA | Murata                      | VGEN2, 4 output capacitors                          |
| 2.2 $\mu$ F                      | 1   | 10 V X5R 0201                        | GRM033R61A225ME47 | Murata                      | VGEN1, 3, 5, 6 output capacitors                    |
| 1.0 $\mu$ F                      | 1   | 10 V X5R 0402                        | GRM033R61A105ME44 | Murata                      | VGEN1, 2, 3, 4, 5, 6 input capacitors               |
| <b>Miscellaneous</b>             |     |                                      |                   |                             |   |
| 1.0 $\mu$ F                      | 1   | 10 V X5R 0402                        | GRM033R61A105ME44 | Murata                      | VCORE, VCOREDIG, VREFDDR, VINREFDDR, VIN capacitors |
| 0.22 $\mu$ F                     | 1   | 10 V X5R 0201                        | GRM033R61A224ME90 | Murata                      | VCOREREFF output capacitor                          |
| 0.47 $\mu$ F                     | 1   | 10 V X5R 0201                        | GRM033R61A474ME90 | Murata                      | VSNVS output capacitor                              |
| 0.1 $\mu$ F                      | 1   | 10 V X5R 0201                        | GRM033R61A104KE84 | Murata                      | VHALF, VINREFDDR, VDDIO, LICELL capacitors          |
| 100 k $\Omega$                   | 2   | RES MF 100 k 1/16 W 1 %<br>0402      | RC0402FR-07100KL  | Yageo America               | Pull-up resistors                                   |
| 4.7 k $\Omega$                   | 2   | RES MF 4.70 K 1/20 W 1 %<br>0201     | RC0201FR-074K7L   | Yageo America               | I <sup>2</sup> C pull-up resistors                  |

[1] NXP does not assume liability, endorse, or warrant components from external manufacturers referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

The following table provides a complete list of the recommended components on a full-featured system using the PF4210 device for  $-40\text{ }^{\circ}\text{C}$  to  $105\text{ }^{\circ}\text{C}$  applications. Components are provided with an example part number. Equivalent components may be used.

**Table 138. Bill of materials  $-40\text{ }^{\circ}\text{C}$  to  $105\text{ }^{\circ}\text{C}$  applications**

| Value  | Qty | Description  | Part number       | Manufacturer <sup>[1]</sup> | Component/pin      |
|--|-----|--|-------------------|-----------------------------|--------------------|
| <b>PMIC</b>                                  |     |  |                   |                             |                    |
|  | 1   | Power management IC  | PF4210            | NXP                         |                    |
| <b>Buck, SW1AB (0.300 to 1.875 V), 2.5 A</b> |     |  |                   |                             |                    |
| 1.0 $\mu$ H                                  | 1   | 2.5 x 2 x 1.2<br>$I_{SAT} = 3.4\text{ A}$ for 10 % drop<br>$DCR_{MAX} = 49\text{ m}\Omega$ | DFE252012R-H-1R0M | TOKO INC.                   | Output inductor    |
| 22 $\mu$ H                                   | 4   | 10 V X7T 0805  | GRM21BD71A226ME44 | Murata                      | Output capacitance |
| 4.7 $\mu$ F                                  | 2   | 10 V X7S 0603  | GRM188C71A475KE11 | Murata                      | Input capacitance  |
| 0.1 $\mu$ F                                  | 1   | 10 V X7S 0201  | GRM033C71A104KE14 | Murata                      | Input capacitance  |
| <b>Buck, SW1C (0.300 to 1.875 V), 2.0 A</b>  |     |  |                   |                             |                    |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Value   | Qty | Description  | Part number       | Manufacturer <sup>[1]</sup> | Component/pin      |
|---|-----|--|-------------------|-----------------------------|--------------------|
| 1.0 $\mu$ H                                   | 1   | 2 x 1.6 x 1<br>$I_{SAT} = 2.9$ A for 10 % drop                                   | DFE201610E-1R0M   | TOKO INC.                   | Output inductor    |
| 22 $\mu$ F                                    | 3   | 10 V X7T 0805  | GRM21BD71A226ME44 | Murata                      | Output capacitance |
| 4.7 $\mu$ F                                   | 1   | 10 V X7S 0603  | GRM188C71A475KE11 | Murata                      | Input capacitance  |
| 0.1 $\mu$ F                                   | 1   | 10 V X7S 0201  | GRM033C71A104KE14 | Murata                      | Input capacitance  |
| <b>Buck, SW1ABC (0.300 to 1.875 V), 4.5 A</b> |     |  |                   |                             |                    |
| 1.0 $\mu$ H                                   | 1   | 4.2 x 4.2 x 2<br>$I_{SAT} = 5.1$ A for 10 % drop,<br>$DCR_{MAX} = 29$ m $\Omega$ | FSDS0420-H-1R0M   | TOKO INC.                   | Output inductor    |
| 22 $\mu$ F                                    | 6   | 10 V X7T 0805  | GRM21BD71A226ME44 | Murata                      | Output capacitance |
| 4.7 $\mu$ F                                   | 2   | 10 V X7S 0603  | GRM188C71A475KE11 | Murata                      | Input capacitance  |
| 0.1 $\mu$ F                                   | 1   | 10 V X7S 0201  | GRM033C71A104KE14 | Murata                      | Input capacitance  |
| <b>Buck, SW2 (0.400 to 3.300 V), 2.5 A</b>    |     |  |                   |                             |                    |
| 1.0 $\mu$ H                                   | 1   | 2 x 1.6 x 1<br>$I_{SAT} = 2.9$ A for 10 % drop                                   | DFE201610E-1R0M   | TOKO INC.                   | Output inductor    |
| 22 $\mu$ F                                    | 3   | 10 V X7T 0805  | GRM21BD71A226ME44 | Murata                      | Output capacitance |
| 4.7 $\mu$ F                                   | 1   | 10 V X7S 0603  | GRM188C71A475KE11 | Murata                      | Input capacitance  |
| 0.1 $\mu$ F                                   | 1   | 10 V X7S 0201  | GRM033C71A104KE14 | Murata                      | Input capacitance  |
| <b>Buck, SW3AB (0.400 to 3.300 V), 3.0 A</b>  |     |  |                   |                             |                    |
| 1.0 $\mu$ H                                   | 1   | 2 x 1.6 x 1<br>$I_{SAT} = 2.9$ A for 10 % drop                                   | DFE201610E-1R0M   | TOKO INC.                   | Output inductor    |
| 22 $\mu$ F                                    | 3   | 10 V X7T 0805  | GRM21BD71A226ME44 | Murata                      | Output capacitance |
| 4.7 $\mu$ F                                   | 1   | 10 V X7S 0603  | GRM188C71A475KE11 | Murata                      | Input capacitance  |
| 0.1 $\mu$ F                                   | 1   | 10 V X7S 0201  | GRM033C71A104KE14 | Murata                      | Input capacitance  |
| <b>Buck, SW4 (0.400 to 3.300 V), 1.0 A</b>    |     |  |                   |                             |                    |
| 1.0 $\mu$ H                                   | 1   | 2 x 1.6 x 1<br>$I_{SAT} = 2.9$ A for 30 % drop                                   | DFE201610E-1R0M   | Murata                      | Output inductor    |
| 22 $\mu$ F                                    | 3   | 10 V X7T 0805  | GRM21BD71A226ME44 | Murata                      | Output capacitance |
| 4.7 $\mu$ F                                   | 1   | 10 V X7S 0603  | GRM188C71A475KE11 | Murata                      | Input capacitance  |
| 0.1 $\mu$ F                                   | 1   | 10 V X7S 0201  | GRM033C71A104KE14 | Murata                      | Input capacitance  |
| <b>BOOST, SWBST 5.0 V, 600 mA</b>             |     |  |                   |                             |                    |
| 2.2 $\mu$ H                                   | 1   | 2 x 1.6 x 1<br>$I_{SAT} = 2.4$ A for 10 % drop                                   | DFE201610E-2R2M   | TOKO INC.                   | Output inductor    |
| 22 $\mu$ F                                    | 2   | 10 V X7T 0805  | GRM21BD71A226ME44 | Murata                      | Output capacitance |
| 10 $\mu$ F                                    | 3   | 10 V X7T 0603  | GRM188D71A106MA73 | Murata                      | Input capacitance  |
| 2.2 $\mu$ F                                   | 1   | 10 V X7S 0402  | GRM155C71A225KE11 | Murata                      | Input capacitance  |
| 0.1 $\mu$ F                                   | 1   | 10 V X7S 0201  | GRM033C71A104KE14 | Murata                      | Input capacitance  |
| 1.0 A   | 1   | DIODE SCH PWR RECT<br>1.0 A 20 V SMT   | MBR120LSFT3G      | ON Semiconductor            | Schottky diode     |

## 14-channel power management integrated circuit (PMIC) for audio/video applications

| Value                            | Qty | Description                   | Part number       | Manufacturer <sup>[1]</sup> | Component/pin                                       |
|----------------------------------|-----|-------------------------------|-------------------|-----------------------------|---|
| <b>LDO, VGEN1, 2, 3, 4, 5, 6</b> |     |                               |                   |                             |   |
| 4.7 $\mu$ F                      | 1   | 10 V X7S 0603                 | GRM188C71A475KE11 | Murata                      | VGEN2, 4 output capacitors                          |
| 2.2 $\mu$ F                      | 1   | 10 V X7S 0402                 | GRM155C71A225KE11 | Murata                      | VGEN1, 3, 5, 6 output capacitors                    |
| 1.0 $\mu$ F                      | 1   | 10 V X7S 0402                 | GRM155C71A105KE11 | Murata                      | VGEN1, 2, 3, 4, 5, 6 input capacitors               |
| <b>Miscellaneous</b>             |     |                               |                   |                             |   |
| 1.0 $\mu$ F                      | 1   | 10 V X7S 0402                 | GRM155C71A105KE11 | Murata                      | VCORE, VCOREDIG, VREFDDR, VINREFDDR, VIN capacitors |
| 0.22 $\mu$ F                     | 1   | 10 V X7R 0402                 | GRM155R71A224KE01 | Murata                      | VCOREREF output capacitor                           |
| 0.47 $\mu$ F                     | 1   | 10 V X7R 0402                 | GRM155R71A474KE01 | Murata                      | VSNVS output capacitor                              |
| 0.1 $\mu$ F                      | 1   | 10 V X7S 0201                 | GRM033C71A104KE14 | Murata                      | VHALF, VINREFDDR, VDDIO, LICELL capacitors          |
| 100 k $\Omega$                   | 2   | RES MF 100 k 1/16 W 1 % 0402  | RC0402FR-07100KL  | Yageo America               | Pull-up resistors                                   |
| 4.7 k $\Omega$                   | 2   | RES MF 4.70 K 1/20 W 1 % 0201 | RC0201FR-074K7L   | Yageo America               | I <sup>2</sup> C pull-up resistors                  |

[1] NXP does not assume liability, endorse, or warrant components from external manufacturers referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

## 12 PF4210 layout guidelines

### 12.1 General board recommendations

- It is recommended to use an eight-layer board stack-up arranged as follows:
  - High current signal
  - GND
  - Signal
  - Power
  - Power
  - Signal
  - GND
  - High current signal
- Allocate top and bottom PCB layers for power routing (high current signals), copper-pour the unused area.
- Use internal layers sandwiched between two GND planes for the signal routing.

## 12.2 Component placement

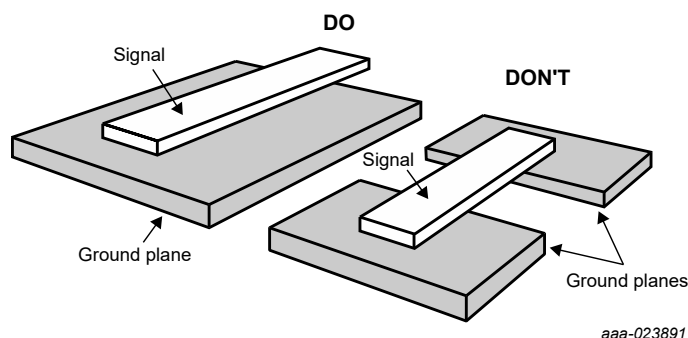
It is desirable to keep all components related to the power stage as close to the PMIC as possible, especially decoupling input and output capacitors.

## 12.3 General routing requirements

- Some recommended things to keep in mind for manufacturability:
  - Via in pads require a 4.5 mil minimum annular ring. Each pad must be 9.0 mils larger than its hole
  - Maximum copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
  - Minimum allowed spacing between line and hole pad is 3.5 mils
  - Minimum allowed spacing between line and line is 3.0 mils
- Care must be taken with SWx<sub>FB</sub> pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high-power signals, like the ones on the SW<sub>xIN</sub>, SW<sub>x</sub>, SW<sub>xLX</sub>, SW<sub>BSTIN</sub>, SW<sub>BST</sub>, and SW<sub>BSTLX</sub> pins. They could also be shielded.
- Shield feedback traces of the regulators and keep them as short as possible (trace them on the bottom so the ground and power planes shield these traces).
- Avoid coupling traces between important signal/low-noise supplies (like REFCORE, V<sub>CORE</sub>, V<sub>COREDIG</sub>) from any switching node (for example, SW<sub>1ALX</sub>, SW<sub>1BLX</sub>, SW<sub>1CLX</sub>, SW<sub>2LX</sub>, SW<sub>3ALX</sub>, SW<sub>3BLX</sub>, SW<sub>4LX</sub>, and SW<sub>BSTLX</sub>).
- Make sure that all components related to a specific block are referenced to the corresponding ground.

## 12.4 Parallel routing requirements

- I<sup>2</sup>C signal routing
  - CLK is the fastest signal of the system, therefore it must be given special care.
  - To avoid contamination of these delicate signals by nearby high-power or high-frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the entire signal trace length.



- These signals can be placed on an outer layer of the board to reduce their capacitance with respect to the ground plane.
- Care must be taken with these signals not to contaminate analog signals, as they are high-frequency signals. Another good practice is to trace them perpendicularly on different layers, so there is a minimum area of proximity between signals.

## 12.5 Switching regulator layout recommendations

- Per design, the switching regulators in PF4210 are designed to operate with only one input bulk capacitor. However, it is recommended to add a high-frequency filter input capacitor ( $C_{IN\_HF}$ ), to filter out any noise at the regulator input. This capacitor should be in the range of 100 nF and should be placed right next to or under the IC, close to the IC pins.
- Make high-current ripple traces low-inductance (short, high W/L ratio).
- Make high-current traces wide or copper islands.
- Make high-current traces symmetrical for dualphase regulators (SW1, SW3).

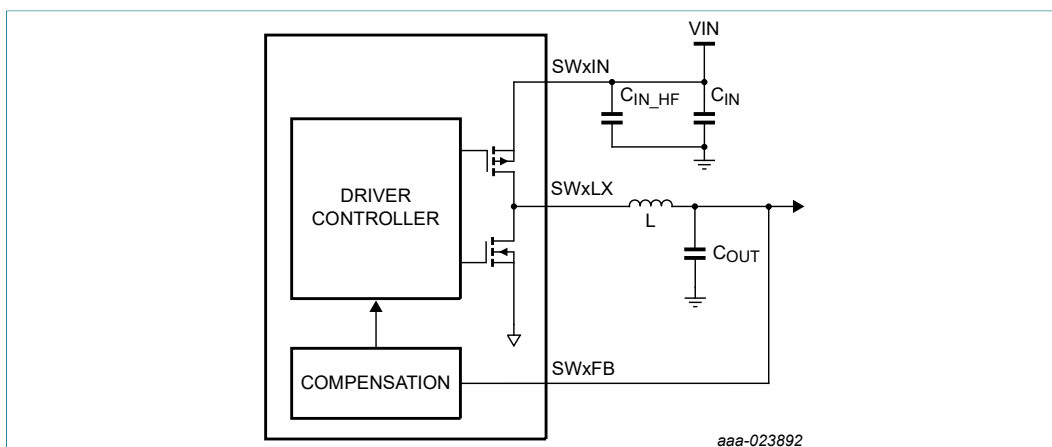


Figure 34. Generic buck regulator architecture

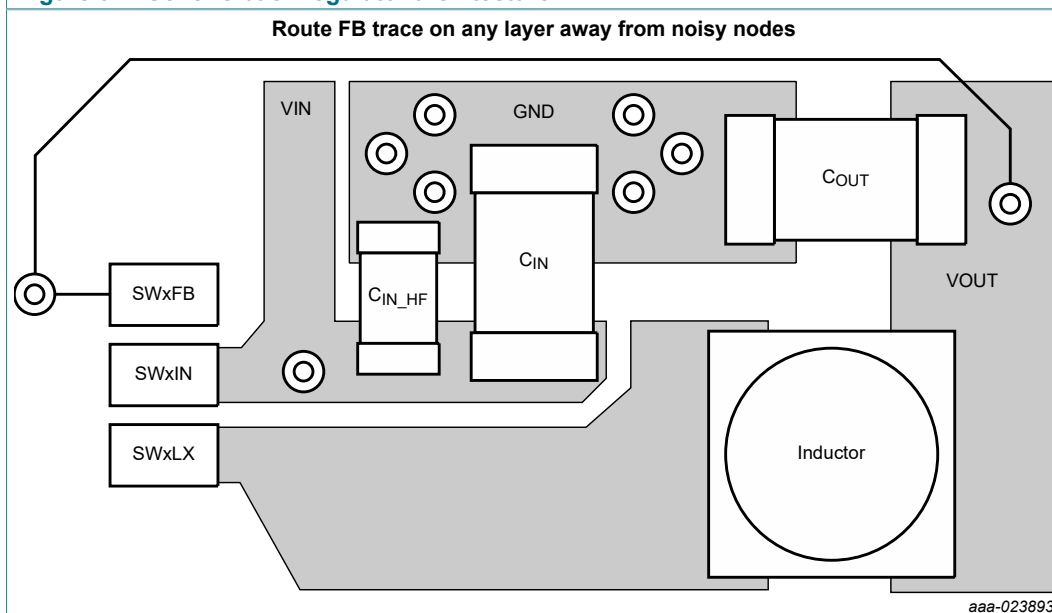


Figure 35. Layout example for buck regulators

## 12.6 Thermal information

### 12.6.1 Rating data

The thermal rating data of the packages has been simulated with the results listed in [Table 4](#).

Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol  $R_{\theta JA}$  or  $\theta_{JA}$  (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment.  $R_{\theta JMA}$  or  $\theta_{JMA}$  (Theta-JMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, continues to be commonly used.

The JEDEC standards can be consulted at <http://www.jedec.org/>.

### 12.6.2 Estimation of junction temperature

An estimation of the chip junction temperature  $T_J$  can be obtained from the equation:  
 $T_J = T_A + (R_{\theta JA} \times P_D)$  with

$T_A$  = Ambient temperature for the package in °C

$R_{\theta JA}$  = Junction to ambient thermal resistance in °C/W

$P_D$  = Power dissipation in the package in W

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage:

- The value determined on a single layer board  $R_{\theta JA}$
- The value obtained on a four layer board  $R_{\theta JMA}$

Actual application PCBs show a performance close to the simulated four layer board value. This performance may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature  $T_J$  is estimated using the following equation  $T_J = T_B + (R_{\theta JB} \times P_D)$  with

$T_B$  = Board temperature at the package perimeter in °C

$R_{\theta JB}$  = Junction to board thermal resistance in °C/W

$P_D$  = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. See [Section 10 "Functional block requirements and behaviors"](#) for more details on thermal management.

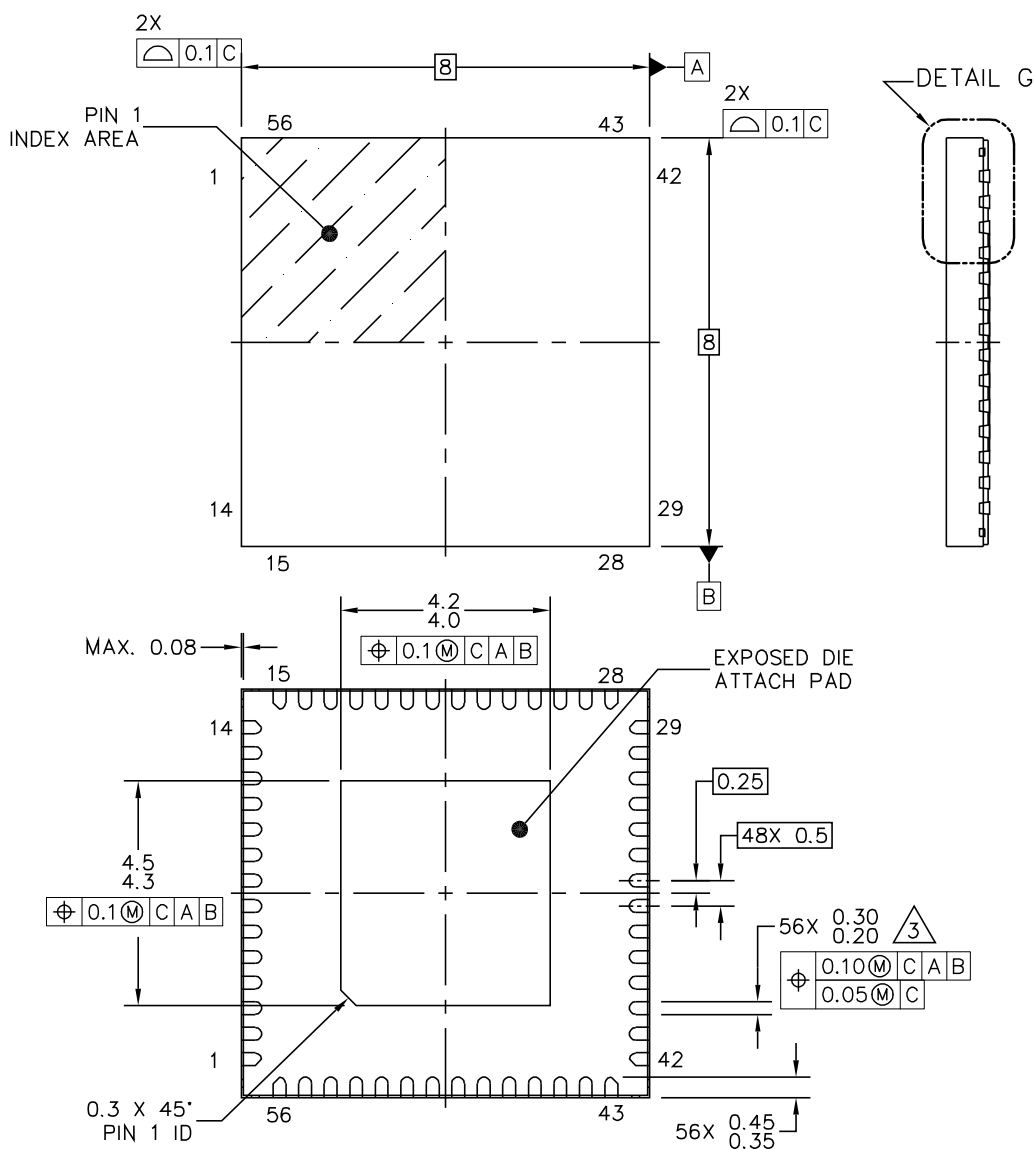
## 13 Packaging

**Table 139. Package drawing information**

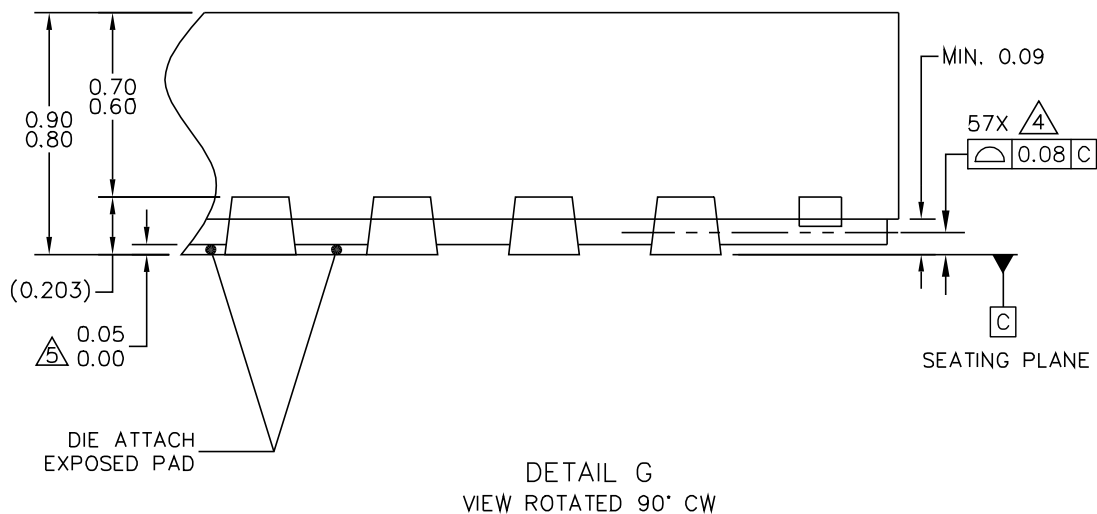
| Package  | Suffix | Package outline drawing number |
|--|--------|--------------------------------|
| 56 QFN 8x8 mm - 0.5 mm pitch.<br>WF-type (wetable flank) | ES     | 98ASA00589D                    |

13.1 Packaging dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to [www.nxp.com](http://www.nxp.com) and perform a keyword search for the drawing's document number. See [Section 8.2 "Thermal characteristics"](#) for specific thermal characteristics for each package.



|   |                          |                            |
|---|--------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V.<br>ALL RIGHTS RESERVED                          | MECHANICAL OUTLINE       | PRINT VERSION NOT TO SCALE |
| TITLE:<br>QFN, THERMALLY ENHANCED<br>8 X 8 X 0.85, 0.5 PITCH, 56 TERMINAL | DOCUMENT NO: 98ASA00589D | REV: C                     |
|   | STANDARD: NON-JEDEC      |                            |
|   | SOT684-18                | 19 APR 2016                |



|   |                          |                            |
|---|--------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V.<br>ALL RIGHTS RESERVED                          | MECHANICAL OUTLINE       | PRINT VERSION NOT TO SCALE |
| TITLE:<br>QFN, THERMALLY ENHANCED<br>8 X 8 X 0.85, 0.5 PITCH, 56 TERMINAL | DOCUMENT NO: 98ASA00589D | REV: C                     |
|   | STANDARD: NON-JEDEC      |                            |
|   | SOT684-18                | 19 APR 2016                |

## 14-channel power management integrated circuit (PMIC) for audio/video applications



## NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
3. THIS DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DIMENSION APPLIES ONLY FOR TERMINALS.

|   |                          |                            |
|---|--------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V.<br>ALL RIGHTS RESERVED                          | MECHANICAL OUTLINE       | PRINT VERSION NOT TO SCALE |
| TITLE:<br>QFN, THERMALLY ENHANCED<br>8 X 8 X 0.85, 0.5 PITCH, 56 TERMINAL | DOCUMENT NO: 98ASA00589D | REV: C                     |
|   | STANDARD: NON-JEDEC      |                            |
|   | SOT684-18                | 19 APR 2016                |

Figure 36. Package dimensions

## 14 Revision history

Table 140. Revision history

| Document ID   | Release date  | Data sheet status | Change notice | Supersedes  |
|---------------|---|-------------------|---------------|-------------|
| PF4210 v2.0   | 20181114  | Technical data    | —             | PF4210 v1.0 |
| Modifications | <ul style="list-style-type: none"> <li>• Added MC32PF4210A4ES and MC34PF4210A4ES part numbers to <a href="#">Table 1</a></li> <li>• Added sequencing information for A4 to <a href="#">Table 8</a></li> <li>• Corrected typo in <a href="#">Table 8</a> for PU CONFIG, SWDVS_CLK (changed ms to <math>\mu</math>s)</li> </ul> |                   |               |             |
| PF4210 v1.0   | 20180214  | Technical data    | —             | —           |

## 15 Legal information

### 15.1 Data sheet status

| Document status <sup>[1][2]</sup>       | Product status <sup>[3]</sup> | Definition   |
|---|-------------------------------|--|
| [short] Data sheet: product preview     | Development                   | This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice.  |
| [short] Data sheet: advance information | Qualification                 | This document contains information on a new product. Specifications and information herein are subject to change without notice.   |
| [short] Data sheet: technical data      | Production                    | This document contains the product specification. NXP Semiconductors reserves the right to change the detail specifications as may be required to permit improvements in the design of its products. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a technical data data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the technical data data sheet.

### 15.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual

## 14-channel power management integrated circuit (PMIC) for audio/video applications

agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall

use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**NXP** — is a trademark of NXP B.V.

## Contents

|           |  |           |           |  |            |
|-----------|--|-----------|-----------|--|------------|
| <b>1</b>  | <b>General description</b>                         | <b>1</b>  | 10.4.4    | Buck regulators                            | 32         |
| <b>2</b>  | <b>Features and benefits</b>                       | <b>1</b>  | 10.4.4.1  | Current limit                              | 33         |
| <b>3</b>  | <b>Simplified application diagram</b>              | <b>2</b>  | 10.4.4.2  | General control                            | 33         |
| <b>4</b>  | <b>Applications</b>                                | <b>3</b>  | 10.4.4.3  | SW1A/B/C                                   | 38         |
| <b>5</b>  | <b>Orderable parts</b>                             | <b>3</b>  | 10.4.4.4  | SW2  | 53         |
| <b>6</b>  | <b>Internal block diagram</b>                      | <b>4</b>  | 10.4.4.5  | SW3A/B                                     | 61         |
| <b>7</b>  | <b>Pinning information</b>                         | <b>5</b>  | 10.4.4.6  | SW4  | 74         |
| 7.1       | Pinning  | 5         | 10.4.5    | Boost regulator                            | 82         |
| 7.2       | Pin definitions                                    | 5         | 10.4.5.1  | SWBST setup and control                    | 82         |
| <b>8</b>  | <b>General product characteristics</b>             | <b>8</b>  | 10.4.5.2  | SWBST external components                  | 83         |
| 8.1       | Absolute maximum ratings                           | 8         | 10.4.5.3  | SWBST specifications                       | 83         |
| 8.2       | Thermal characteristics                            | 8         | 10.4.6    | LDO regulators description                 | 84         |
| 8.3       | Power dissipation                                  | 9         | 10.4.6.1  | Transient response waveforms               | 85         |
| 8.4       | Electrical characteristics                         | 10        | 10.4.6.2  | Short-circuit protection                   | 85         |
| 8.4.1     | General specifications                             | 10        | 10.4.6.3  | LDO regulator control                      | 86         |
| 8.4.2     | Current consumption                                | 11        | 10.4.6.4  | External components                        | 89         |
| <b>9</b>  | <b>Detailed description</b>                        | <b>11</b> | 10.4.6.5  | LDO specifications                         | 90         |
| 9.1       | Features   | 11        | 10.4.6.6  | VSNVS LDO/switch                           | 100        |
| 9.2       | Functional block diagram                           | 13        | 10.4.6.7  | Coin cell battery backup                   | 104        |
| 9.3       | Functional description                             | 13        | 10.5      | Control interface I2C block description    | 105        |
| 9.3.1     | Power generation                                   | 13        | 10.5.1    | I2C device ID                              | 105        |
| 9.3.2     | Control logic                                      | 14        | 10.5.2    | I2C operation                              | 105        |
| 9.3.2.1   | Interface signals                                  | 14        | 10.5.3    | Interrupt handling                         | 106        |
| <b>10</b> | <b>Functional block requirements and behaviors</b> | <b>15</b> | 10.5.4    | Interrupt bit summary                      | 106        |
| 10.1      | Startup  | 15        | 10.6      | Specific registers                         | 112        |
| 10.1.1    | Device startup configuration                       | 15        | 10.6.1    | IC and version identification              | 112        |
| 10.1.2    | One time programmability (OTP)                     | 18        | 10.6.2    | Embedded memory                            | 113        |
| 10.1.2.1  | Startup sequence and timing                        | 18        | 10.7      | Register bitmap                            | 113        |
| 10.1.2.2  | PWRON pin configuration                            | 19        | 10.7.1    | Register map                               | 114        |
| 10.1.2.3  | I2C address configuration                          | 19        | <b>11</b> | <b>Typical applications</b>                | <b>122</b> |
| 10.1.2.4  | Soft start ramp rate                               | 20        | 11.1      | Introduction                               | 122        |
| 10.1.3    | OTP prototyping                                    | 20        | 11.1.1    | Application diagram                        | 123        |
| 10.1.4    | Reading OTP fuses                                  | 21        | 11.1.2    | Bill of materials                          | 123        |
| 10.1.5    | Programming OTP fuses                              | 21        | <b>12</b> | <b>PF4210 layout guidelines</b>            | <b>127</b> |
| 10.2      | 16 MHz and 32 kHz clocks                           | 21        | 12.1      | General board recommendations              | 127        |
| 10.2.1    | Clock adjustment                                   | 22        | 12.2      | Component placement                        | 128        |
| 10.3      | Bias and references block description              | 22        | 12.3      | General routing requirements               | 128        |
| 10.3.1    | Internal core voltage references                   | 22        | 12.4      | Parallel routing requirements              | 128        |
| 10.3.1.1  | External components                                | 23        | 12.5      | Switching regulator layout recommendations | 129        |
| 10.3.2    | VREFDDR voltage reference                          | 23        | 12.6      | Thermal information                        | 130        |
| 10.3.2.1  | VREFDDR control register                           | 23        | 12.6.1    | Rating data                                | 130        |
| 10.4      | Power generation                                   | 25        | 12.6.2    | Estimation of junction temperature         | 130        |
| 10.4.1    | Modes of operation                                 | 25        | <b>13</b> | <b>Packaging</b>                           | <b>130</b> |
| 10.4.1.1  | On mode  | 26        | 13.1      | Packaging dimensions                       | 131        |
| 10.4.1.2  | Off mode   | 26        | <b>14</b> | <b>Revision history</b>                    | <b>134</b> |
| 10.4.1.3  | Standby mode                                       | 26        | <b>15</b> | <b>Legal information</b>                   | <b>135</b> |
| 10.4.1.4  | Sleep mode   | 27        |           |  |            |
| 10.4.1.5  | Coin cell mode                                     | 28        |           |  |            |
| 10.4.2    | State machine flow summary                         | 28        |           |  |            |
| 10.4.2.1  | Turn on events                                     | 29        |           |  |            |
| 10.4.2.2  | Turn off events                                    | 30        |           |  |            |
| 10.4.3    | Power tree   | 30        |           |  |            |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

## OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we stricly control the quality of products and services. Welcome your RFQ to

Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.