

MCF51MM256VLL Datasheet

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DiGi Electronics Part Number	MCF51MM256VLL-DG
Manufacturer	NXP USA Inc.
Manufacturer Product Number	MCF51MM256VLL
Description	IC MCU 32BIT 256KB FLASH 100LQFP
Detailed Description	Coldfire V1 MCF51MM Microcontroller IC 32-Bit Single-Core 50MHz 256KB (256K x 8) FLASH 100-LQFP (14x14)

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Manufacturer Product Number:

MCF51MM256VLL

Series:

MCF51MM

DiGi-Electronics Programmable:

Not Verified

Core Size:

32-Bit Single-Core

Connectivity:

CANbus, EBI/EMI, I2C, SCI, SPI, USB OTG

Number of I/O:

65

Program Memory Type:

FLASH

RAM Size:

32K x 8

Data Converters:

A/D 8x16b; D/A 1x12b

Operating Temperature:

-40°C ~ 105°C (TA)

Supplier Device Package:

100-LQFP (14x14)

Base Product Number:

MCF51

Manufacturer:

NXP USA Inc.

Product Status:

Active

Core Processor:

Coldfire V1

Speed:

50MHz

Peripherals:

LVD, PWM, WDT

Program Memory Size:

256KB (256K x 8)

EEPROM Size:

-

Voltage - Supply (Vcc/Vdd):

1.8V ~ 3.6V

Oscillator Type:

External

Mounting Type:

Surface Mount

Package / Case:

100-LQFP

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.31.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A991A2

Freescale Semiconductor

Data Sheet: Technical Data

Document Number: MCF51MM256
Rev. 5, 07/2012



An Energy-Efficient Solution from Freescale

MCF51MM256/128

The MCF51MM256 series devices are members of the low-cost, low-power, high-performance ColdFire V1 family of 32-bit microcontrollers (MCUs) designed for handheld metering devices.

Not all features are available in all devices or packages; see [Table 1](#) for a comparison of features by device.



80-LQFP
12mm x 12mm



81-BGA
10mm x 10mm



100-LQFP
14mm x 14mm



104-BGA
10mm x 10mm

32-Bit ColdFire V1 Central Processor Unit (CPU)

- Up to 50.33 MHz ColdFire CPU above 2.4 V and 40 MHz CPU above 2.1V and 20 MHz CPU above 1.8 V across temperature range of -40°C to 105°C.
- ColdFire Instruction Set Revision C (ISA_C).
- 32-bit multiply and accumulate (MAC) supports signed or unsigned integer or signed fractional inputs.

On-Chip Memory

- 256 K Flash comprised of two independent 128 K flash arrays; read/program/erase over full operating voltage and temperature; allows interrupt processing while programming.
- 32 KB System Random-access memory (RAM).
- Security circuitry to prevent unauthorized access to RAM and Flash contents.

Power-Saving Modes

- Two ultra-low power stop modes. Peripheral clock enable register can disable clocks to unused modules to reduce currents.
- Time of Day (TOD) — Ultra low-power 1/4 sec counter with up to 64 sec timeout.
- Ultra-low power external oscillator that can be used in stop modes to provide accurate clock source to the TOD. 6 μ s typical wake up time from stop3 mode.

Clock Source Options

- Oscillator (XOSC1) — Loop-control Pierce oscillator; 32.768 kHz crystal or ceramic resonator dedicated for TOD operation.
- Oscillator (XOSC2) for high frequency crystal input for MCG reference to be used for system clock and USB operations.
- Multipurpose Clock Generator (MCG) — PLL and FLL; precision trimming of internal reference allows 0.2% resolution and typical +0.5% to -1% deviation over temperature and voltage; supports CPU frequencies from 4 kHz to 50 MHz.

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock.
- Low-voltage detection with reset or interrupt; selectable trip points; separate low voltage warning with optional interrupt; selectable trip points.
- Illegal opcode and illegal address detection with reset.
- Flash block protection for each array to prevent accidental write / erasure.
- Hardware CRC to support fast cyclic redundancy checks.

Development Support

- Integrated ColdFire DEBUG_Rev_B+ interface with single wire BDM connection supports same electrical interface used by the S08 family debug modules.
- Real-time debug with 6 hardware breakpoints (4 PC, 1 address and 1 data).
- On-chip trace buffer provides programmable start/stop recording conditions.

Peripherals

- USB** — Dual-role USB On-The-Go (OTG) device, supports USB in either device, host or OTG configuration. On-chip transceiver and 3.3V regulator help save system cost, fully compliant with USB Specification

- 2.0. Allows control, bulk, interrupt and isochronous transfers.
- SC1x** — Two serial communications interfaces with optional 13-bit break; option to connect Rx input to PRACMP output on SCI1 and SCI2; High current drive on Tx on SCI1 and SCI2; wake-up from stop3 on Rx edge.
- SPI1** — Serial peripheral interface with 32-bit FIFO buffer; 16-bit or 8-bit data transfers; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting.
- SPI2** — Serial peripheral interface with full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting.
- IIC** — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 11-bit addressing.
- CMT** — Carrier Modulator timer for remote control communications. Carrier generator, modulator and driver for dedicated infrared out (IRO). Can be used as an output compare timer.
- TPMx** — Two 4-channel Timer/PWM Module; Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; external clock input/pulse accumulator.
- Mini-FlexBus** — Multi-function external bus interface with user programmable chip selects and the option to multiplex address and data lines.
- PRACMP** — Analog comparator with selectable interrupt; compare option to programmable internal reference voltage; operation in stop3.

Measurement Engine

- ADC16** — 16-bit successive approximation ADC with up to 4 dedicated differential channels and 8 single-ended channels; range compare function; 1.7 mV/xC temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V. Configurable hardware trigger for 8 Channel select and result registers.
- PDB** — Programmable delay block with 16-bit counter and modulus and prescale to set reference clock to bus divided by 1 to bus divided by 2048; 8 trigger outputs for ADC module provides periodic coordination of ADC sampling sequence with sequence completion interrupt; Back-to-Back mode and Timed mode.
- DAC** — 12-bit resolution DAC; configurable settling time.
- OPAMPx** — 2 flexible operational amplifiers configurable for general operations; Low offset and temperature drift.
- TRIAMPx** — 2 trans-impedance amplifiers dedicated for converting current inputs into voltages.

Input/Output

- Up to 68 GPIOs and 1 output-only pin.
- Voltage Reference output (VREFO).
- Dedicated infrared output pin (IRO) with high current sink capability.
- Up to 16 KBI pins with selectable polarity.
- Up to 16 pins of rapid general purpose I/O (RGPIO).



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The following table provides a cross-comparison of the features of the MCF51MM256/128 according to package.

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FEATURE	-E				-E	
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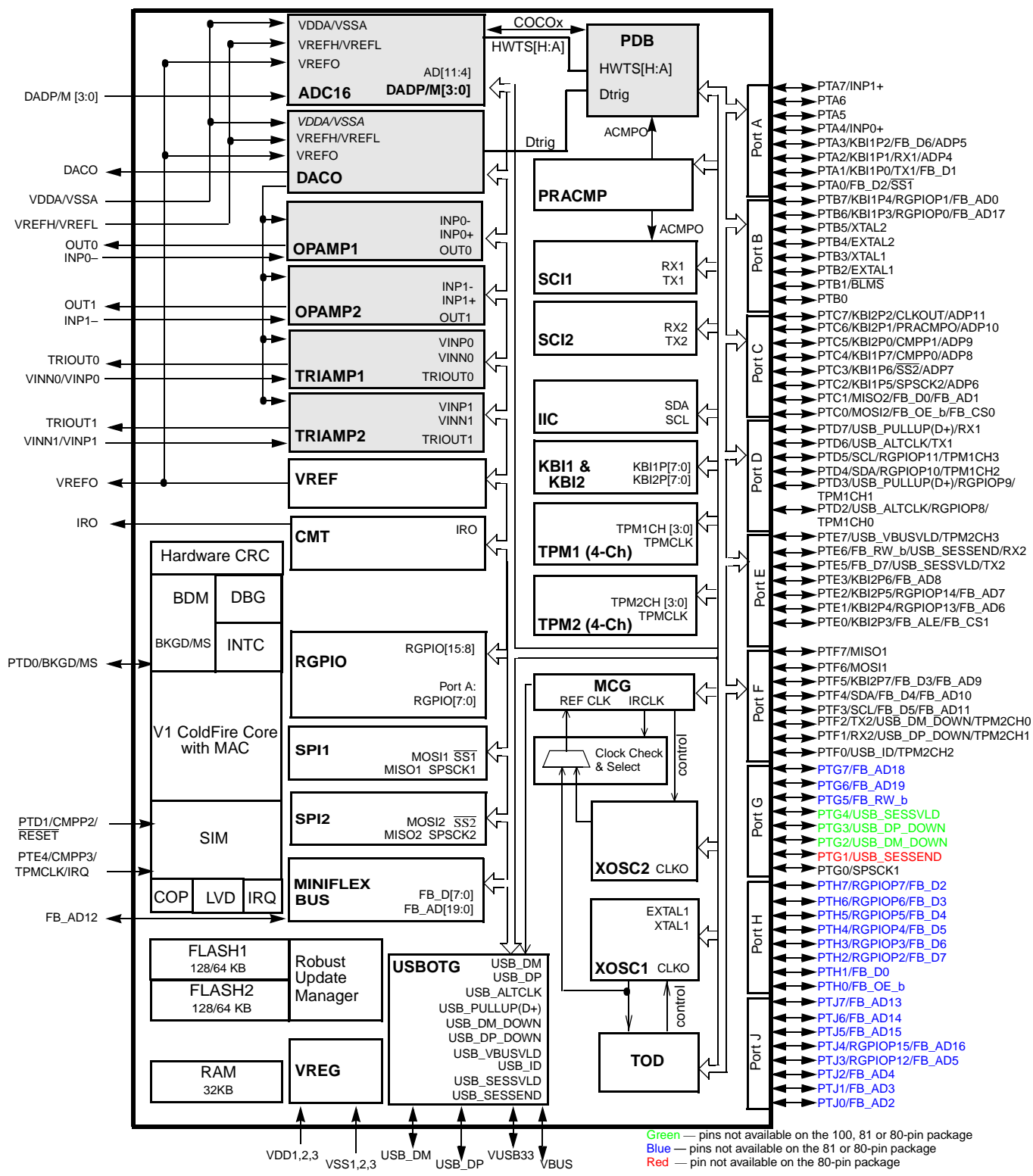


Figure 1. MCF51MM256 Series Block Diagram

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The following figure shows the 104-pin MAPBGA pinout configuration.

!	TÚOH	TÚOI	ÚÚÑaET	ÚÚÑaER	ÚÚÚÑ€	TÚOF	TÚO€	ÔÑaNCEÈĐ	TÚOI	TÚOG	TÚOF	N
Ñ	TÚOÈ	TÚNÈ	TÚO€	ÚÑÚÚ	TÚOG	TÚOH	TÚOÈ	TÚOG	TÚOÈ	TÚOÈ	TÚOĐ	Ñ
O	ŮŠ	TÚOF	TÚNH	TÚOĐ	TÚOH	TÚOG	TÚOI	TÚOÈ	TÚOF	TÚOH	TÚOI	O
œ	TÚNG	TÚNF	TÚNÈ	ÚœœÈ		ÚœœĐ		Úœœ€	TÚNÈ	TÚO€	TÚOĐ	œ
Ó	ÚÚÚN	TÚNI	TÚNÈ						TÚNĐ	TÚO€	TÚOÈ	Ó
ô	ÚÚÓÓQ	ŮSTÈÈ	ŮSTĐÈ	TÚOÈ				TÚOI	TÚOĐ	TÚOÈ	TÚOÈ	ô
ö	ÚÚŠÚÚÈ	ŠÚÚÈ	ŠÚÚĐ						TÚœG	TÚœI	TÚOÈ	ö
ò	ÚŮSTÈ	ÚŮSSÈ	TÚN€	ÚÚÚÈ		ÚÚÚĐ		ÚÚÚ€	TÚœF	TÚœ€	TÚœĐ	ò
õ	œNœTÈ	œNœRÈ	TÚOI	TÚOH	TÚOF	TÚO€	TÚOĐ	TÚœH	TÚOĐ	TÚOÈ	TÚOÈ	õ
P	ÚŮSTĐ	ÚŮSSĐ	œNœTÈ	TÚOG	TÚNH	TÚNI	TÚO€	TÚœÈ	TÚOF	TÚOG	TÚOH	P
Q	ÚÚŠÚÚĐ	œNOŠ	œNœRÈ	ÚÚÓÓŠ	ÚÚÓÓÒ	ÚœœN	TÚN€	TÚNĐ	TÚœÈ	TÚNG	TÚNF	Q
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The following figure shows the 100-pin LQFP pinout configuration.

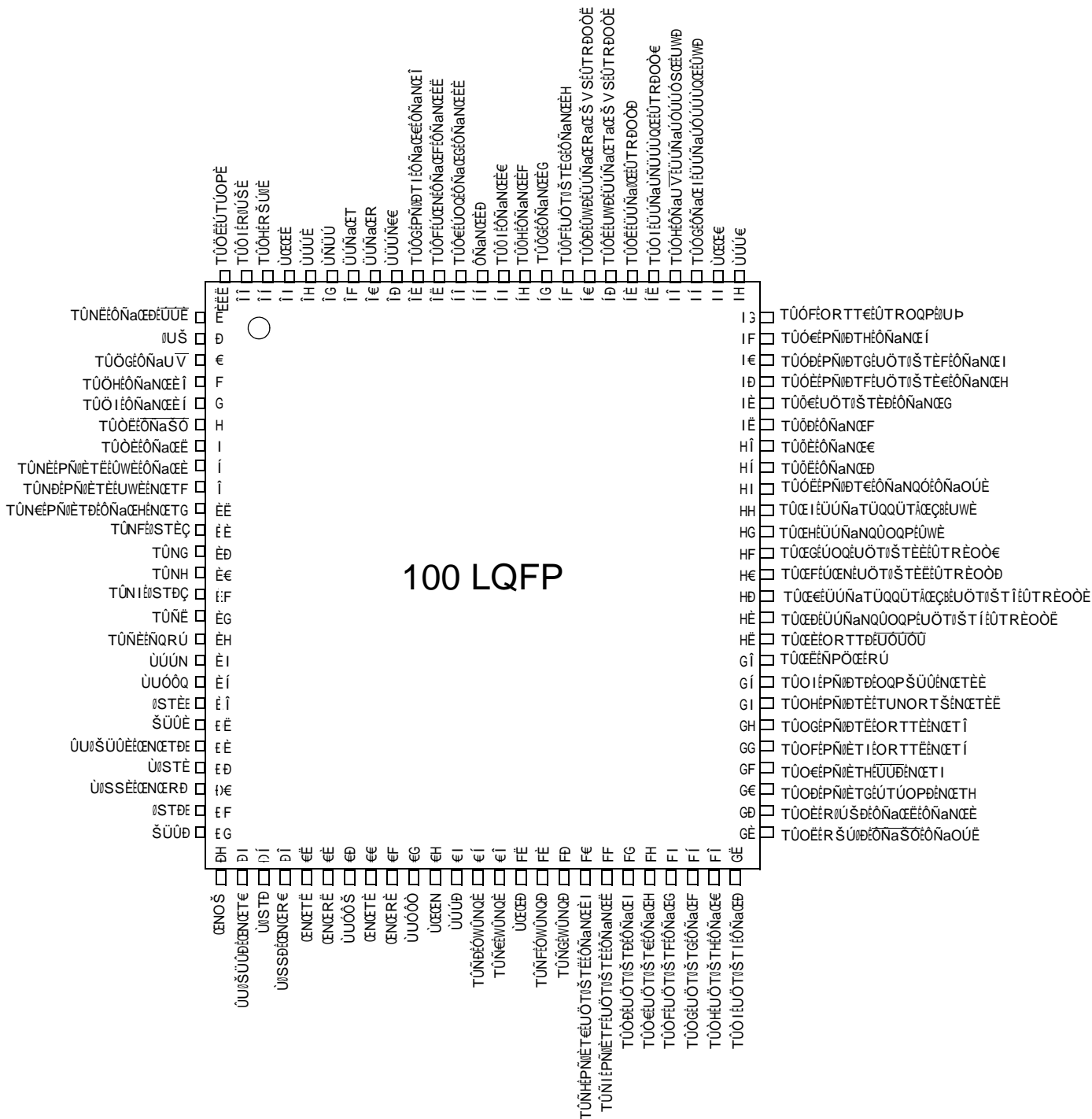


FIGURE 01N,10

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The following figure shows the 81-pin MAPBGA pinout configuration.

!	ĐUŠ	TÚÖÈ	TÚÖH	ÚÚŃaĈET	ÚŃŮÚ	ÚÚŮŃ€€	TÚÔF	TÚÔ€	TÚÓF	N
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Ó	ŠŮÛÈ	ÚŮSSÈ	ŠŮÛĐ	ÚĈĈĐ	ÚĈĈ€	ÚĈĈÈ	TÚĈĐ	TÚĈ€	TÚĈH	Ó
Ô	ÚĐSTÈ	ÚŮŠŮÛÈ	ĐSTĐÈ	ÚÚÚĐ	ÚÚÚ€	ÚÚÚÈ	TÚŃI	TÚÓI	TÚĈF	Ô
Ö	ĈĈĈÈÈ	ĈĈŮŠ	ÚŮŠŮÛĐ	ÚŮSSĐ	ÚŮÓÓŠ	TÚŃH	TÚÔÈ	TÚÔÈ	TÚÔĐ	Ö
Ò	ĈĈĈÈÈ	ĈĈĈÈÈ	ĈĈĈÈÈ	ÚĐSTĐ	TÚÔ€	TÚÔF	TÚĈÈÈ	TÚÓG	TÚOH	Ò
Ō	ÚÚÚŃ	ÚŮÓÓQ	ÚŮÓÓÒ	ÚĈĈĈŃ	TÚŃĐ	TÚŃ€	TÚĈÈÈ	TÚŃF	TÚŃG	Ō
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OH	€	-	-	TŪŌG	ŌÑaUŪ	-	-	TŪŌGĚŌÑaUŪ
OG	F	-	-	TŪŌH	ŌÑaŒĚĪ	-	-	TŪŌHĚŌÑaŒĚĪ
OI	G	-	-	TŪŌI	ŌÑaŒĚĪ	-	-	TŪŌIĚŌÑaŒĚĪ
ÑI	H	-	-	TŪŌĚ	ŌÑaŠŌ	-	-	TŪŌĚĚŌÑaŠŌ
OÍ	I	-	-	TŪŌĚ	ŌÑaŒĚĚ	-	-	TŪŌĚĚĚŌÑaŒĚĚ
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ÓĪ	Ī	ŒG	F	TŪNĐ	PÑŃĚTĚ	UWĚ	NŒTF	TŪNĐĚPÑŃĚTĚĚUWĚĚNŒTF
Ò€	ĚĚ	ŒH	G	TŪN€	PÑŃĚTĐ	ŌÑaŒH	NŒTG	TŪN€ĚPÑŃĚTĐĚŌÑaŒHĚNŒTG
ŒĐ	ÈÈ	OÈ	H	TŪNF	ŮSTĚÇ	-	-	TŪNFĚŮSTĚÇ
ŒÈ	ÈĐ	OĐ	I	TŪNG	-	-	-	TŪNG
O€	È€	O€	Ī	TŪNH	-	-	-	TŪNH
ÓĐ	ÈF	ŒĐ	Ī	TŪNI	ŮSTĐÇ	-	-	TŪNIĚŮSTĐÇ
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ŌĐ	ÈĪ	ŒÈ	ÈF	ŮSTĚĚ	-	-	-	ŮSTĚĚ
ŌĐ	ĐĚ	ŌÈ	ÈG	ŠŪŪÈ	-	-	-	ŠŪŪÈ
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Ō€	ĐF	Ō€	ÈĪ	ŮSTĐĚ	-	-	-	ŮSTĐĚ
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ŒĐ	€È	ŒÈ	ĐH	ŒENÇERÈ	-	-	-	ŒENÇERÈ
QF	€Đ	ŒG	ĐI	ŒUÓŒŠ	-	-	-	ŒUÓŒŠ
P€	€€	Œ€	ĐÍ	ŒENÇETÈ	-	-	-	ŒENÇETÈ
Q€	€F	ŒĐ	ĐÍ	ŒENÇERÈ	-	-	-	ŒENÇERÈ
QG	€G	Œ€	€È	ŒUÓŒŒ	-	-	-	ŒUÓŒŒ
QH	€H	ŒF	€È	ŒÇEN	-	-	-	ŒÇEN
ŒH	€I	ŒF	€Đ	ŒÚÚĐ	-	-	-	ŒÚÚĐ
QÍ	€Í	ŒG	€€	TŒŒĐ	ŒWŒNQÈ	-	-	TŒŒĐŒWŒNQÈ
QI	€Í	ŒH	€F	TŒŒ€	WŒNQÈ	-	-	TŒŒ€WŒNQÈ
ŒH	FÈ	ŒF	€G	ŒÇEN	-	-	-	ŒÇEN
QÈÈ	FÈ	ŒÍ	€H	TŒŒF	ŒWŒNQĐ	-	-	TŒŒFŒWŒNQĐ
QÈÈ	FĐ	ŒÍ	€I	TŒŒG	WŒNQĐ	-	-	TŒŒGŒWŒNQĐ
PG	F€	ŒH	€Í	TŒŒH	PŒŒÈT€	ŒŒTŒŠTÈ	ŒŒNaŒÈI	TŒŒHŒPŒŒÈT€ŒŒŒTŒŠTÈŒŒNaŒÈI
PH	FF	ŒI	€Í	TŒŒI	PŒŒÈTF	ŒŒTŒŠTÈ	ŒŒNaŒÈÈ	TŒŒIŒPŒŒÈTFŒŒŒTŒŠTÈŒŒNaŒÈÈ
ŒI	FG	-	-	TŒŒĐ	ŒŒTŒŠTĐ	ŒŒNaŒI	-	TŒŒĐŒŒTŒŠTĐŒŒNaŒI
ŒH	FH	-	-	TŒŒ€	ŒŒTŒŠT€	ŒŒNaŒH	-	TŒŒ€ŒŒTŒŠT€ŒŒNaŒH
ŒG	FI	-	-	TŒŒF	ŒŒTŒŠTF	ŒŒNaŒG	-	TŒŒFŒŒTŒŠTFŒŒNaŒG
PF	FÍ	-	-	TŒŒG	ŒŒTŒŠTG	ŒŒNaŒF	-	TŒŒGŒŒTŒŠTGŒŒNaŒF
ŒF	FÍ	-	-	TŒŒH	ŒŒTŒŠTH	ŒŒNaŒ€	-	TŒŒHŒŒTŒŠTHŒŒNaŒ€
Œ€	GÈ	-	-	TŒŒI	ŒŒTŒŠTI	ŒŒNaŒĐ	-	TŒŒIŒŒTŒŠTIŒŒNaŒĐ
ŒÈÈ	GÈ	ŒI	FÈ	TŒŒÈ	RŒŒĐ	ŒŒNaŒŒ	ŒŒNaŒŒÈ	TŒŒÈŒRŒŒĐŒŒNaŒŒÈŒŒNaŒÈÈ
ŒÈÈ	GĐ	ŒÍ	FÈ	TŒŒÈ	RŒŒĐ	ŒŒNaŒÈÈ	ŒŒNaŒÈÈ	TŒŒÈŒRŒŒĐŒŒNaŒÈÈÈŒŒNaŒÈÈÈ
ŒÍ	G€	ŒÍ	FĐ	TŒŒĐ	PŒŒÈTG	ŒŒTŒŠTĐ	NŒETH	TŒŒĐŒPŒŒÈTGŒŒTŒŠTĐNŒETH
PI	GF	ŒG	F€	TŒŒ€	PŒŒÈTH	ŒŒTŒŠTĐ	NŒETI	TŒŒ€ŒPŒŒÈTHŒŒTŒŠTĐNŒETI
PÍ	GG	ŒH	FF	TŒŒF	PŒŒÈTI	ORTTÈ	NŒETÍ	TŒŒFŒPŒŒÈTIŒORTTÈNŒETÍ
PÈÈ	GH	ŒÍ	FG	TŒŒG	PŒŒÈTÈ	ORTTÈ	NŒETÍ	TŒŒGŒPŒŒÈTÈŒORTTÈNŒETÍ
PÈÈ	GI	ŒÍ	FH	TŒŒH	PŒŒÈTÈ	TUNORTŠ	NŒETÈÈ	TŒŒHŒPŒŒÈTÈŒTUNORTŠŒNŒETÈÈ
ŒÍ	GÍ	ŒÍ	FI	TŒŒI	PŒŒÈTĐ	OQPSŒŒ	NŒETÈÈ	TŒŒIŒPŒŒÈTĐŒOQPSŒŒŒNŒETÈÈ
QÍ	GÍ	ŒI	FÍ	TŒŒÈ	ŒPŒÈ	RŒ	-	TŒŒÈÈŒPŒÈŒRŒ
PÍ	HÈ	ŒI	FÍ	TŒŒÈ	ORTTĐ	ŒŒTŒŠTĐ	-	TŒŒÈÈORTTĐŒŒTŒŠTĐ

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ÉÉF RNTÑÖN	ÉÉÉ QPÖT	ÍÉ RNTÑÖN	ÍÉ QPÖT					
ÖÈÈ	HÈ	ÓI	GÈ	TÛŒÐ	ÛÚÑaNQÛOQP	UÖTŸŠTÍ	ÛTRÈOÖÈ	TÛŒÐÈÛÚÑaNQÛOQPÈUÖTŸŠTÍÈÛTRÈOÖÈ
ÒÈÈ	HÐ	ÓÍ	GÈ	TÛŒ€	ÛÚÑaTÛQQÛT ÄŒÇB	UÖTŸŠTÍ	ÛTRÈOÖÈ	TÛŒ€ÈÛÚÑaTÛQQÛTÄŒÇBÈUÖTŸŠTÍÈÛTRÈOÖÈ
ÒÎ	H€	ÔÎ	GÐ	TÛŒF	ÛŒEN	UÖTŸŠTÈÈ	ÛTRÈOÖÐ	TÛŒFÈÛŒENÈUÖTŸŠTÈÈÈÛTRÈOÖÐ
ÖÎ	HF	ŒI	G€	TÛŒG	ÛOQ	UÖTŸŠTÈÈ	ÛTRÈOÖ€	TÛŒGÈÛOQÈUÖTŸŠTÈÈÈÛTRÈOÖ€
ÔÍ	HG	ÓÍ	GF	TÛŒH	ÛÚÑaNQÛOQP	ÛWÈ	-	TÛŒHÈÛÚÑaNQÛOQPÈÛWÈ
ÖÈÈ	HH	ŒÍ	GG	TÛŒI	ÛÚÑaTÛQQÛT ÄŒÇB	UWÈ	-	TÛŒÈÈÛÚÑaTÛQQÛTÄŒÇBÈUWÈ
ÖÈÈ	HI	ŒÍ	GH	TÛŒÈ	PÑŸÐT€	ÔÑaNQÓ	ÔÑaOÚÈ	TÛŒÈÈPÑŸÐT€ÈÔÑaNQÓÈÔÑaOÚÈ
ÔÈÈ	HÍ	-	-	TÛŒÈ	ÔÑaNŒÐ	-	-	TÛŒÈÈÔÑaNŒÐ
ÔÈÈ	HÍ	-	-	TÛŒÈ	ÔÑaNŒ€	-	-	TÛŒÈÈÔÑaNŒ€
ÔÎ	IÈ	-	-	TÛŒÐ	ÔÑaNŒF	-	-	TÛŒÐÈÔÑaNŒF
ÓÈÈ	IÈ	-	-	TÛŒ€	UÖTŸŠTÈÐ	ÔÑaNŒG	-	TÛŒ€ÈUÖTŸŠTÈÐÈÔÑaNŒG
ÓÈÈ	IÐ	OÍ	GI	TÛŒÈ	PÑŸÐTF	UÖTŸŠTÈ€	ÔÑaNŒH	TÛŒÈÈPÑŸÐTFÈUÖTŸŠTÈÈÈÔÑaNŒH
ŒÈÈ	I€	OÍ	GÍ	TÛŒÐ	PÑŸÐTG	UÖTŸŠTÈF	ÔÑaNŒI	TÛŒÐÈPÑŸÐTGÈUÖTŸŠTÈFÈÔÑaNŒI
ŒÈÈ	IF	ÑÍ	GÍ	TÛŒ€	PÑŸÐTH	ÔÑaNŒÍ	-	TÛŒ€ÈPÑŸÐTHÈÔÑaNŒÍ
OÎ	IG	NÍ	HÈ	TÛŒF	ORTT€	ÛTROQP	ÛUP	TÛŒFÈORTT€ÈÛTROQPÈÛUP
ÒÍ	IH	ÔG	HÈ	ÛÚÚ€	-	-	-	ÛÚÚ€
ŒÍ	II	ÔG	HÐ	ÛŒŒ€	-	-	-	ÛŒŒ€
ÑÍ	IÍ	OI	H€	TÛŒG	ÔÑaŒI	ÛÚÑa ÛÓÚÚÚŒ€	ÛWÐ	TÛŒGÈÔÑaŒIÈÛÚÑaÛÓÚÚÚŒ€ÈÛWÐ
OÈÈ	IÍ	OH	HF	TÛŒH	ÔÑaUŸ	ÛÚÑa ÛÓÚÚÚŒŒ	UWÐ	TÛŒHÈÔÑaUŸÈÛÚÑaÛÓÚÚÚŒŒÈUWÐ
OÈÈ	ÍÈ	ÑH	HG	TÛŒI	ÛÚÑa ÛÑÚÚÚŒ€	ÛTRÐOÖ€	-	TÛŒÈÈÛÚÑaÛÑÚÚÚŒ€ÈÛTRÐOÖ€
ÑÍ	ÍÈ	ÑÍ	HH	TÛŒÈ	ÛÚÑaŒŒ	ÛTRÐOÖÐ	-	TÛŒÈÈÛÚÑaŒŒÈÛTRÐOÖÐ
ÑÈÈ	ÍÐ	ÑI	HI	TÛŒÈ	UWÐ	ÛÚÑaŒTaŒ ŠVS	ÛTRÐOÖÈ	TÛŒÈÈUWÐÈÛÚÑaŒTaŒŠVSÈÛTRÐOÖÈ
ÑÈÈ	Í€	OG	HÍ	TÛŒÐ	ÛWÐ	ÛÚÑaŒRaŒ ŒŠVS	ÛTRÐOÖÈ	TÛŒÐÈÛWÐÈÛÚÑaŒRaŒŒŠVSÈÛTRÐOÖÈ
NÈÈ	ÍF	-	-	TÛŒF	UÖTŸŠTÈG	ÔÑaNŒÈH	-	TÛŒFÈUÖTŸŠTÈGÈÔÑaNŒÈH
NÈÈ	ÍG	-	-	TÛŒG	ÔÑaNŒÈG	-	-	TÛŒGÈÔÑaNŒÈG
ÑH	ÍH	-	-	TÛŒH	ÔÑaNŒÈF	-	-	TÛŒHÈÔÑaNŒÈF
NÍ	ÍI	-	-	TÛŒI	ÔÑaNŒÈ€	-	-	TÛŒIÈÔÑaNŒÈ€

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This section contains electrical specification tables and reference timing diagrams for the MCF51MM256/128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

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The parameters specified in this data sheet supersede any values found in the module specifications.

0PARAMETER#ASSIFICATION

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

4ABLE 0ARA METER#ASSIFICATION

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The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 4. Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Input clamp voltage	V_{IC}	$V_{DD} + 1$	V
Output clamp voltage	V_{OC}	$V_{DD} + 1$	V
Power supply voltage	V_{DD}	-0.5 to 1.8	V
Power supply current	I_{DD}	-10 to 10	mA
Storage temperature	T_{STG}	-55 to 150	°C

- Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.
- All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .
- Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{IN} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
T _{amb}	Ambient temperature	ROGERRDGH	°C
		ROGERRRÉÍ	
		Value	
T _{max}	Maximum operating temperature	Value	°C
		Value	
		Value	
		Value	
		Value	
T _{min}	Minimum operating temperature	Value	°C
		Value	
		Value	
		Value	
		Value	

T_{amb} : Ambient temperature
 T_{max} : Maximum operating temperature
 T_{min} : Minimum operating temperature
 P_{int} : Chip internal power
 $P_{I/O}$: Power dissipation on input and output pins

The average chip-junction temperature (T_J) in qC can be obtained from:

$$T_J = T_{amb} + (P_{int} + P_{I/O}) \times R_{JA} \quad \text{Eqn. 1}$$

where:

- T_A = Ambient temperature, qC
- T_{JA} = Package thermal resistance, junction-to-ambient, qC/W
- $P_D = P_{int} + P_{I/O}$
- $P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
- $P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O}$, P_{int} and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K(T_J - T_A) + P_{int} \tag{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = \frac{P_D - P_{int}}{T_J - T_A} \tag{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

PROTECTION CHARACTERISTICS

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (<http://www.aecouncil.com/>) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

TABLE 3. STANDARD TEST CONDITIONS

MODEL	DESCRIPTION	SYMBOL	VALUE	UNIT
01BAV100	U _{ESD}	U _E	±5000	V
	U _{ESD} (peak)	O	±5000	V
	S _{ESD} (rise time)	-	10	ns
RAA100	U _{ESD}	U _E	±5000	V
	U _{ESD} (peak)	O	±5000	V
	S _{ESD} (rise time)	-	10	ns
QAA100	R _{ESD} (resistance)	-	1000	Ω
	R _{ESD} (resistance)	-	1000	Ω

U_{ESD} is the peak voltage of the ESD pulse. U_E is the peak voltage of the ESD pulse. O is the peak voltage of the ESD pulse. S_{ESD} is the rise time of the ESD pulse. R_{ESD} is the resistance of the ESD pulse.

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
U _{ESD}	±5000	R _{ESD}	1000	U _{ESD}	±5000	O	T
U _{ESD} (peak)	±5000	R _{ESD}	1000	U _{ESD}	±5000	O	T
S _{ESD} (rise time)	10	R _{ESD}	1000	U _{ESD}	±5000	O	T

TABLE 38. NAND FLASH PROTECTION CHARACTERISTICS CONTINUED

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ÈÐ	U _{TÇE}	Ø\~â \ââ { äEæ c \ [â]- } [[^F	-	ÈÉÉG	-	GÐÉG	@Y	T		
È€	Ú _{0O}	ÖO -\~âä~ \ ä![[â~GD HD Ú~\ääâ { -\ ä~b~	Ú ₀₀ L Ú _{0IS} L Ú _{CECE}	èÉÉÐ	-	ÉÉÐ	bN	Ö		
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			Ú ₀₀ L Ú _{0IS} L Ú _{CECE}	èG	-	G	bN	Ö		
ÉF	O _{0\}	Ø\{ ~ Oâ{ää~â\ääð äää { -\ }	-	-	-	Í	{Ö	O		
ÈG	Ú _{UNR}	UNR [â~â\~ \ • ð~ääâ	-	-	ÉÉH	ÉÉÉ	Û	O		
ÈH	Ú _{TŠU}	TŠU [âÉâ[b • ð~ääâ ^I	-	ÉÉÍ	ÉÉF	ÉÉÍ	Û	O		
ÈI	Ú _{TŠU}	TŠU [âÉâ[b ~bâ	-	ÈÈ	-	-	{ }	Ö		
ÉÍ	Ú _{QÜCEO} Í	Q cE • ð~ääâ æâ~âä~ \ ~^ [â] ^ äæ - ^~â^ [â\ää	Ú _{CECE} äää~\â	-	ÐÉÉÈ	ÐÉÉH	ÐÉÉÐ	Û	T	
			Ú _{CECE} [-]~\â	-	ÐÉÉH	ÐÉÉÈ	ÐÉÉI	Û	T	
ÉÎ	Ú _{QÜCEQ}	Q cE • ð~ääâ æâ~âä~ \ ~^ [â] ^ äæ - â c [â\ää ^I	Ú _{CECE} äää~\â	-	ÉÉÍÈ	ÉÉÍÐ	ÉÉÍÈ	Û	T	
			Ú _{CECE} [-]~\â	-	ÉÉÍH	ÉÉÍÈ	ÉÉÍÍ	Û	T	

TABLE 4. CHARACTERISTICS

SYM	SYMBOL	CHARACTERISTIC	CONDITION	V _{IN}	V _{DD}	V _{AX}	V _{NIT}	#	
D1	U _{QV0}	Q cE i ¹ a ² a ³ a ⁴ câ[\-]â ~^[\]^\]â - ^-\^ [\^]ââ ¹	U _{CECE} âââ-\ â	-	D1EH	D1FH	D1GH	U	T
		U _{CECE} [-]â	-	D1EH	D1FH	D1GH	U	T	
D2	U _{QVQ}	Q cE i ¹ a ² a ³ a ⁴ câ[\-]â ~^[\]^\]â - â c [\^]ââ ¹	U _{CECE} âââ-\ â	-	D2EH	D2EH	D2ED	U	T
		U _{CECE} [-]â	-	D2EH	D2ED	D2ED	U	T	
D3	U _{^c}	Q cE i ¹ a ² a ³ a ⁴ - \ ^ - ~ [\]â\â[\]ââ •â[\^c]~â[\]â]â ¹	-	-	G1	-	bU	O	
D4	U _{N0}	Nâ\âââ { U i ¹ a ² a ³ a ⁴ Uââ[\]ââ ¹	-	E1E1E1	E1E1	E1E1E1	U	T	

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 E[\] \ | ~ - ââ | ââ â ââ | â b | ââ | â { - \] E C ââ - ââ â \ ââ | â { - \] ^ | i¹ ââ \ | ~ â { i¹ ââ ~ | U_{CECE} | [U_{QV} â \ â] ^ | i¹ ââ ~ | â - \ â c ^ \ \ | ~ |] ââ ~ | [ââ | ââ â | [[â \ i¹ âââââ

4 Rââ | [ââ c - ^ U₀ K U_{CECE}

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 Maximum is highest voltage that POR is guaranteed.

9 Run at 1 MHz bus frequency

10 Low voltage detection and warning limits measured at 1 MHz bus frequency.

11 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

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G	W _I DD	Wait mode supply current ÔÔÔ b æàð áää b æ!ià] ŠÔÔ€	ÐĠÈÈĠG RÔ,	€	ÈĤĠG	-	mA	-40 to 105	O
			ÐĒ RÔ,	€	ÈÈÈ€	-	mA	-40 to 105	Û
			Í RÔ,	€	HÈH	-	mA	-40 to 105	Û
			È RÔ,	€	ÈÈI	-	mA	-40 to 105	Û
H	LPW _I DD	Low-Power Wait mode supply current	ÈĤ PÔ,	€	ÐÍ	HÐ	µA	-40 to 105	Û
I	S2 _I DD	Stop2 mode supply current ⁴	SÈN	€	ÈÈÈÈÈÈ	ÈÈÈÈÈÈ	µA	-40 to 25	T
			SÈN	€	€ÈI	ÈÈ	µA	70	O
			SÈN	€	ÈÈ	ÐÈ	µA	85	O
			SÈN	€	ÐÈ	€ÈÈĠG	µA	105	T
			SÈN	Ð	ÈÈÈÈÈÈ	ÈÈÈÈÈÈ	µA	-40 to 25	O
			SÈN	Ð	€ÈÈÈÈÈÈ	ÈÈÈÈÈÈ	µA	70	O
			SÈN	Ð	ÈÈÈÈÈÈ	ÈÈÈÈÈÈ	µA	85	O
			SÈN	Ð	ÐÈÈÈÈÈÈÈ	ÈÈÈÈÈÈÈÈ	µA	105	O

TABLE 3. SUPPLY CURRENT CHARACTERISTICS (CONTINUED)

#	Symbol	Parameter	Bus Freq	V _{DD} (V)	Typ ¹	Max	Unit	Temp (°C)	C
I	S3I _{DD}	Stop3 mode supply current ⁴ No clocks active	n/a	3	0.750	1.3	PA	-40 to 25	P
					8.5	18		70	C
					20	28		85	C
					53	63		105	P
				2	0.400	0.900		-40 to 25	C
					8.2	16		70	C
					18	26		85	C
					47	59		105	C

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

² ON = System Clock Gating Control registers turn on system clock to the corresponding modules.

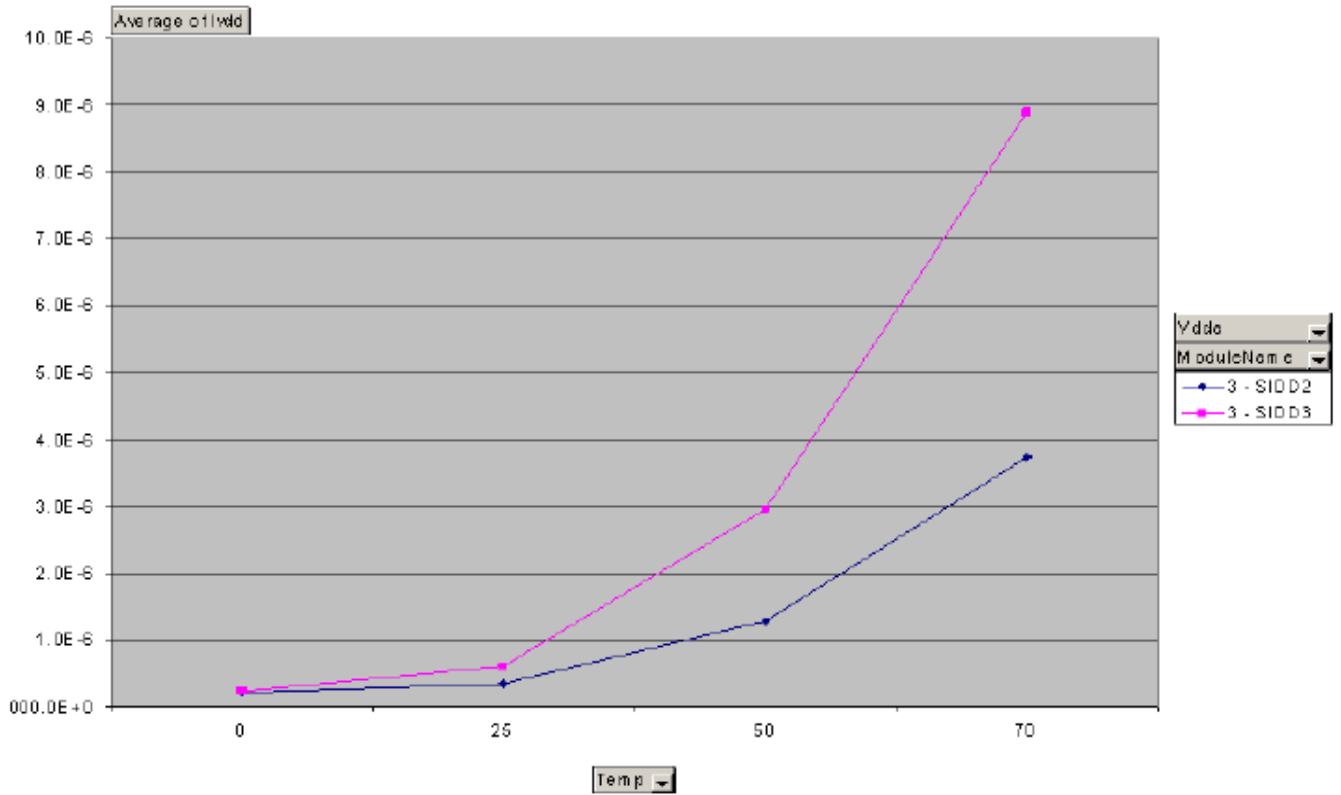
³ OFF = System Clock Gating Control registers turn off system Clock to the corresponding modules.

⁴ All digital pins must be configured to a known state to prevent floating pins from adding current. Smaller packages may have some pins that are not bonded out; however, software must still be configured to the largest pin package available so that all pins are in a known state. Otherwise, floating pins that are not bonded in the smaller packages may result in a higher current draw. NOTE: I/O pins are configured to output low; input-only pins are configured to pullup-enabled. IRO pin connects to ground. FB_AD12 pin is pullup-enabled. TRIAMPx, OPAMPx, DACO, and VREFO pins are at reset state and unconnected.

TABLE 4. TYPICAL STOP-MODE CURRENTS

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
E	LPO	-	50	75	100	150	250	nA	D
D	EREFSTEN	RANGE = HGO = 0	600	650	750	850	1000	nA	D
€	IREFSTEN ¹	-	—	73	80	93	125	PA	T
F	TOD	Does not include clock source current	50	75	100	150	250	nA	D
G	LVD ¹	LVDSE = 1	116	117	126	132	172	PA	T
H	PRACMP ¹	Not using the bandgap (BGBE = 0)	17	18	24	35	74	PA	T
I	ADC ¹	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	190	195	210	220	260	PA	T
I	DAC ¹	High-Power mode; no load on DACO	339	345	346	346	360	PA	T
		Low-Power mode	41	43	43	44	50	PA	T
I	OPAMP ¹	High-Power mode	276	350	370	376	390	PA	T
		Low-Power mode	42	49	57	58	68	PA	T
E	TRIAMP ¹	High-Power mode	420	432	433	438	478	PA	T
		Low-Power mode	52	52	52	55	60	PA	T

¹ Not available in stop2 mode.



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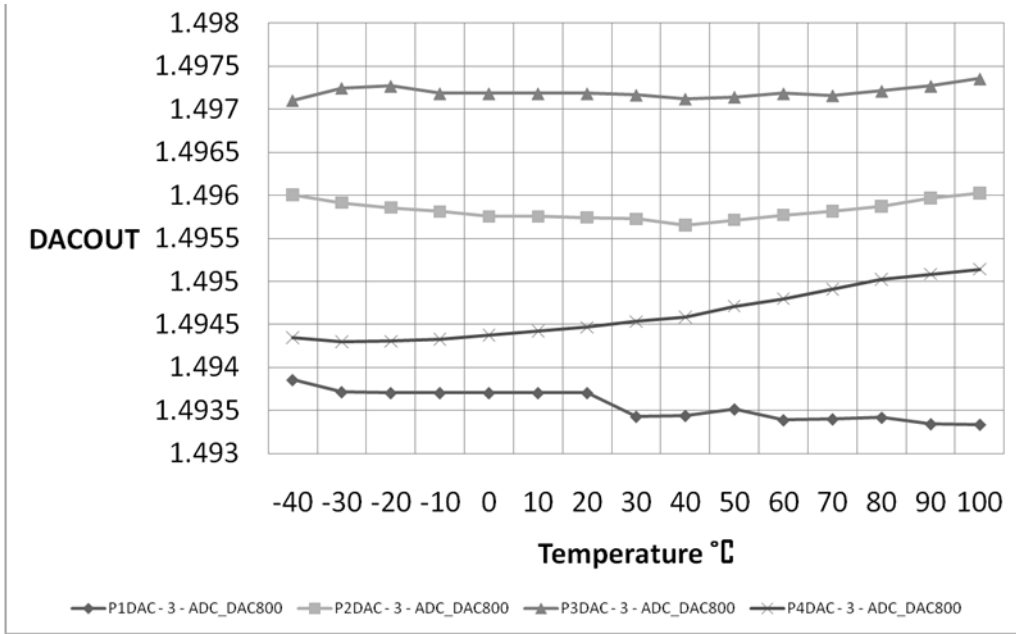
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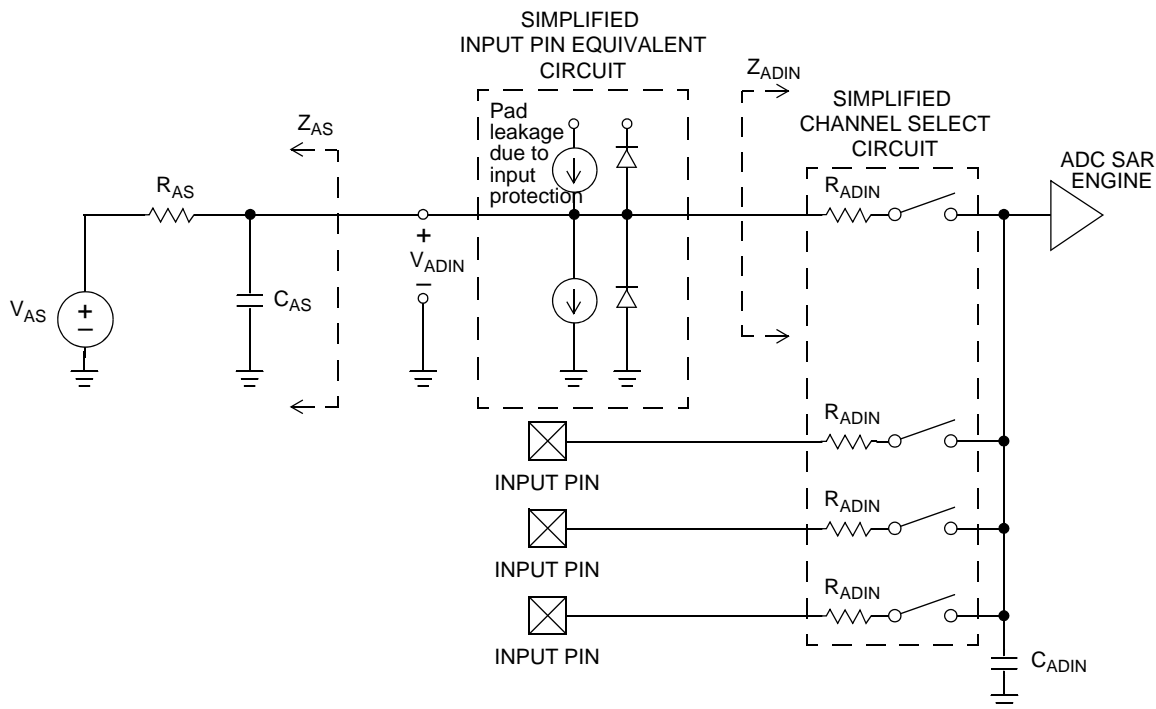
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TABLE OPERATING CONDITIONS CONTINUED

	3MB #	CHARACTERISTIC	CONDITIONS	-IN	4P	-AX	5NIT	#	COMMENT
G	U _{U00Q}	U _a U _i a _{aa} Q c		U _{UUN}	U _{UUN}	U _{UUN}	U	œ	
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¹ Typical values assume V_D = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
² DC potential difference.



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4ABLE -#EMPERATURE2ANGEnTO

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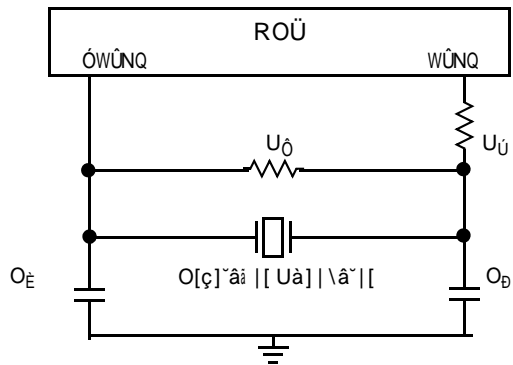
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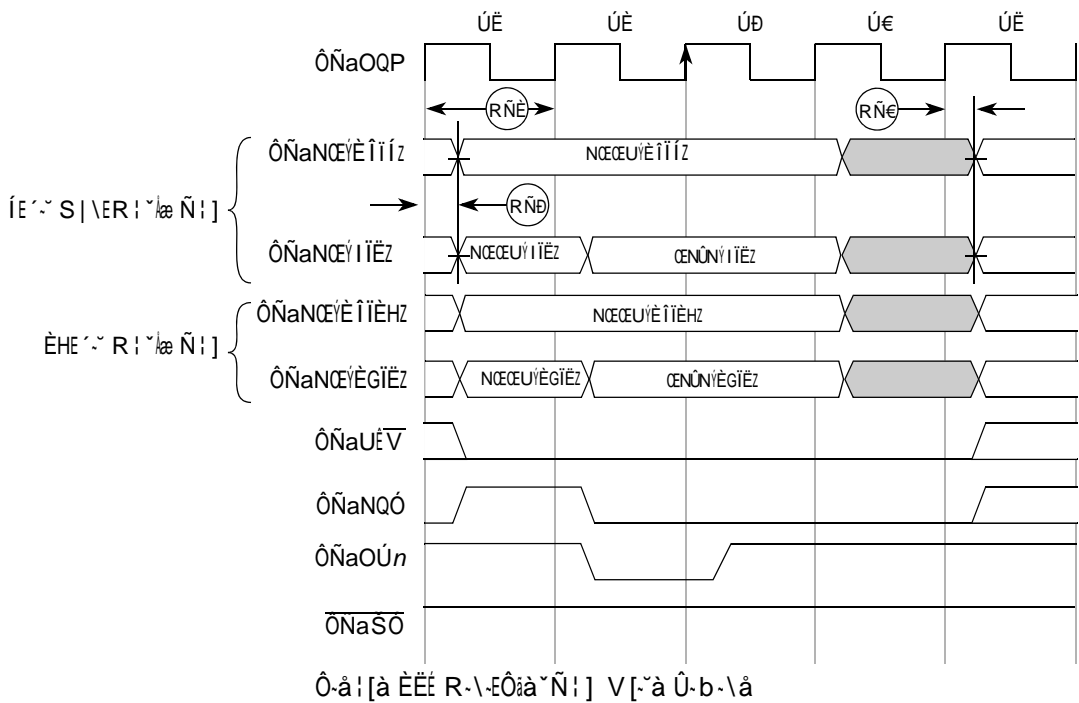


-INIKS4IMING3PECIFICATIONS

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of ÐGÈÈHHH RÒ. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

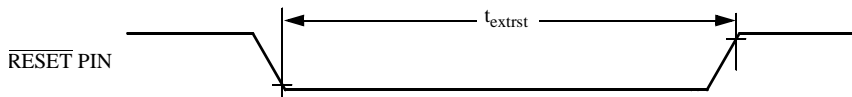
The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.



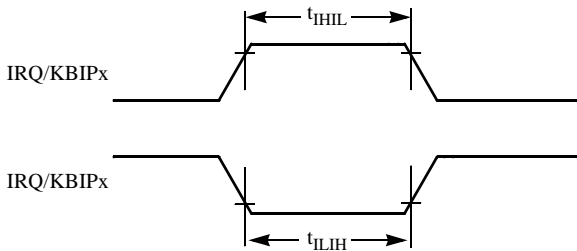
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4.1.2.1 Synchronizer

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

TABLE 40-1. INPUT TIMING

Symbol	#	FUNCTION	SYMBOL	MIN	MAX	UNIT
t_{TPMext}	-	External clock period	t_{TPMext}	100	1000	ns
t_{clkh}	-	External clock high pulse width	t_{clkh}	10	100	ns
t_{ckl}	1	External clock low pulse width	t_{ckl}	10	100	ns
t_{F}	1	External clock rise/fall time	t_{F}	10	100	ns
t_{G}	1	External clock setup/hold time	t_{G}	10	100	ns

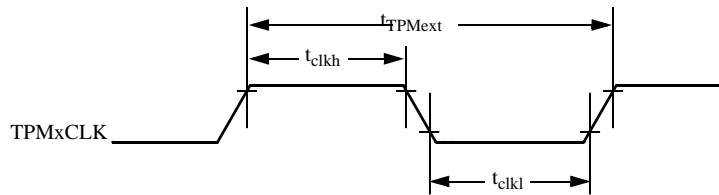


FIGURE 41-1. EXTERNAL CLOCK

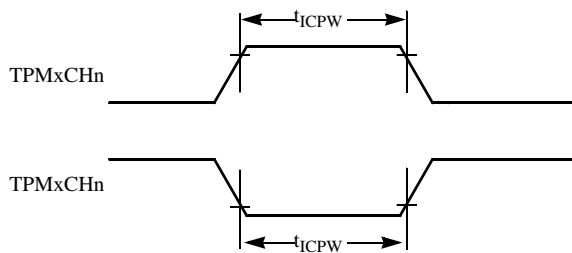
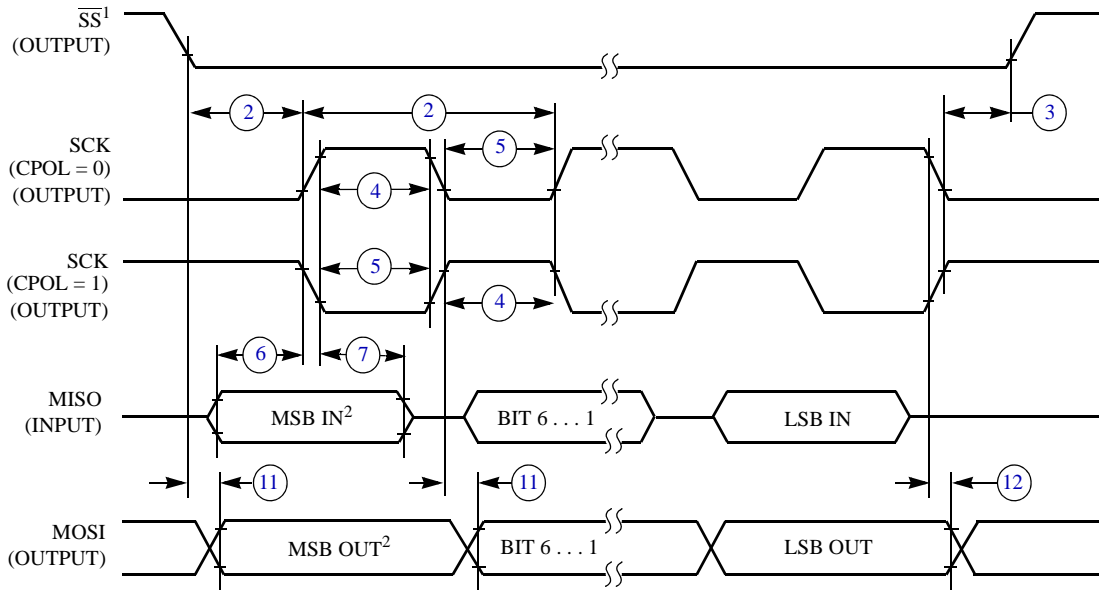


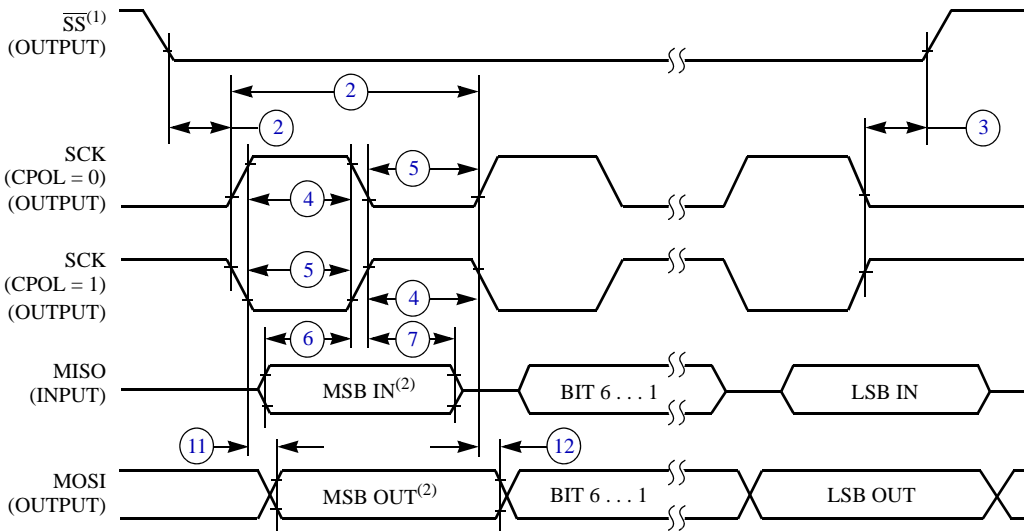
FIGURE 41-2. INPUT CAPTURE PULSE



NOTES:

1. \overline{SS}^1 output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

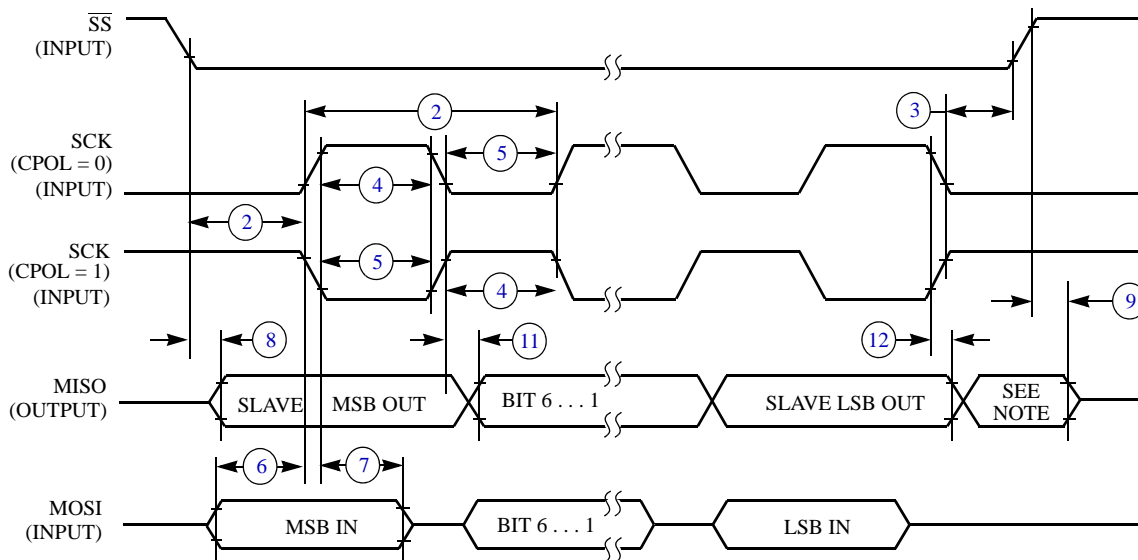
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NOTES:

1. $\overline{SS}^{(1)}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

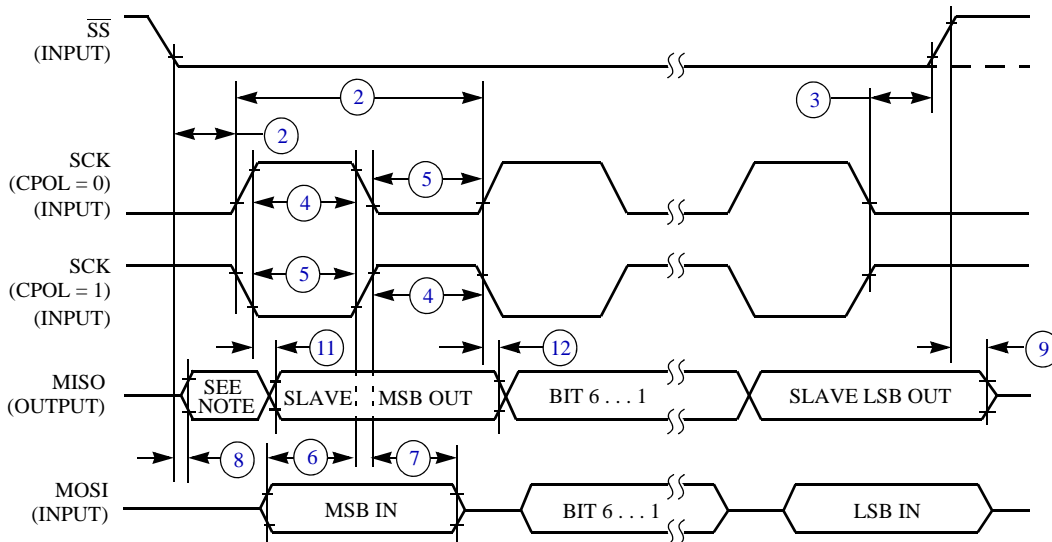
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NOTE:

1. Not defined, but normally MSB of character just received

Ô-â| [à È É ÚTØ Úâ•à Û·b·\â ĀOTÒN K ÈB



NOTE:

1. Not defined, but normally LSB of character just received

Ô-â| [à È É ÚTØ Úâ•à Û·b·\â ĀOTÒN K ÈB

Flash Memory Characteristics

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51MM256RM).

TABLE 4. FLASH MEMORY CHARACTERISTICS

Characteristic	Symbol	Unit	Min	Typical	Max	Notes	#
Program time per byte	t _{PGM}	μs	1.5	—	3	—	1
Erase time per byte	t _{ERASE}	ms	1.5	—	3	—	1
Program time per word	t _{PGM}	μs	4.5	—	9	—	1
Erase time per word	t _{ERASE}	ms	4.5	—	9	—	1
Program time per sector	t _{PGM}	ms	15	—	30	—	1
Erase time per sector	t _{ERASE}	ms	15	—	30	—	1
Program time per page	t _{PGM}	ms	15	—	30	—	1
Erase time per page	t _{ERASE}	ms	15	—	30	—	1
Program time per block	t _{PGM}	ms	15	—	30	—	1
Erase time per block	t _{ERASE}	ms	15	—	30	—	1
Program time per array	t _{PGM}	ms	15	—	30	—	1
Erase time per array	t _{ERASE}	ms	15	—	30	—	1
Program time per sector	t _{PGM}	ms	15	—	30	—	1
Erase time per sector	t _{ERASE}	ms	15	—	30	—	1
Program time per page	t _{PGM}	ms	15	—	30	—	1
Erase time per page	t _{ERASE}	ms	15	—	30	—	1
Program time per block	t _{PGM}	ms	15	—	30	—	1
Erase time per block	t _{ERASE}	ms	15	—	30	—	1
Program time per array	t _{PGM}	ms	15	—	30	—	1
Erase time per array	t _{ERASE}	ms	15	—	30	—	1

1 The frequency of this clock is controlled by a software setting.
 2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.
 3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.
 4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

TABLE 1. INTERNAL 530mV TO 660mV REGULATOR CHARACTERISTICS

Symbol	Characteristic	Symbol	Min	Typ	Max	Unit	Notes
V _{REG}	Regulator Voltage	V _{REG}	0.53	0.53	0.66	V	0
I _{REG}	Regulator Current	I _{REG}	1.0	1.0	1.0	mA	1
V _{REG} (I _{REG})	Regulator Voltage (I _{REG})	V _{REG} (I _{REG})	0.53	0.53	0.66	V	0
V _{REG} (I _{REG})	Regulator Voltage (I _{REG})	V _{REG} (I _{REG})	0.53	0.53	0.66	V	0

3.16 VREF Electrical Specifications

Table 26. VREF Electrical Specifications

#	Characteristic	Symbol	Min	Max	Unit	C
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ÈĐ	Q âæ Uàâ îâ~ \ R ŠÇÈÓaQŨ K ÈÈ	-	-	ÈÈÈ	{ ÛÈbN	O
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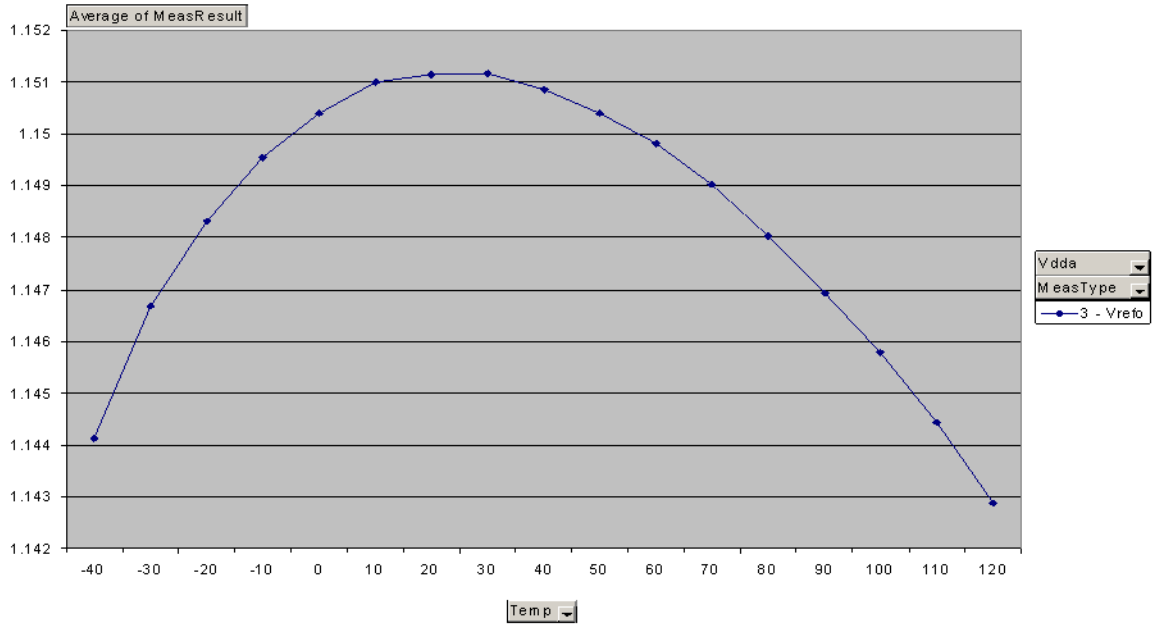
¹ See typical chart that follows (Figure 20).

² Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging PV/year. VREF0 data recorded per month.

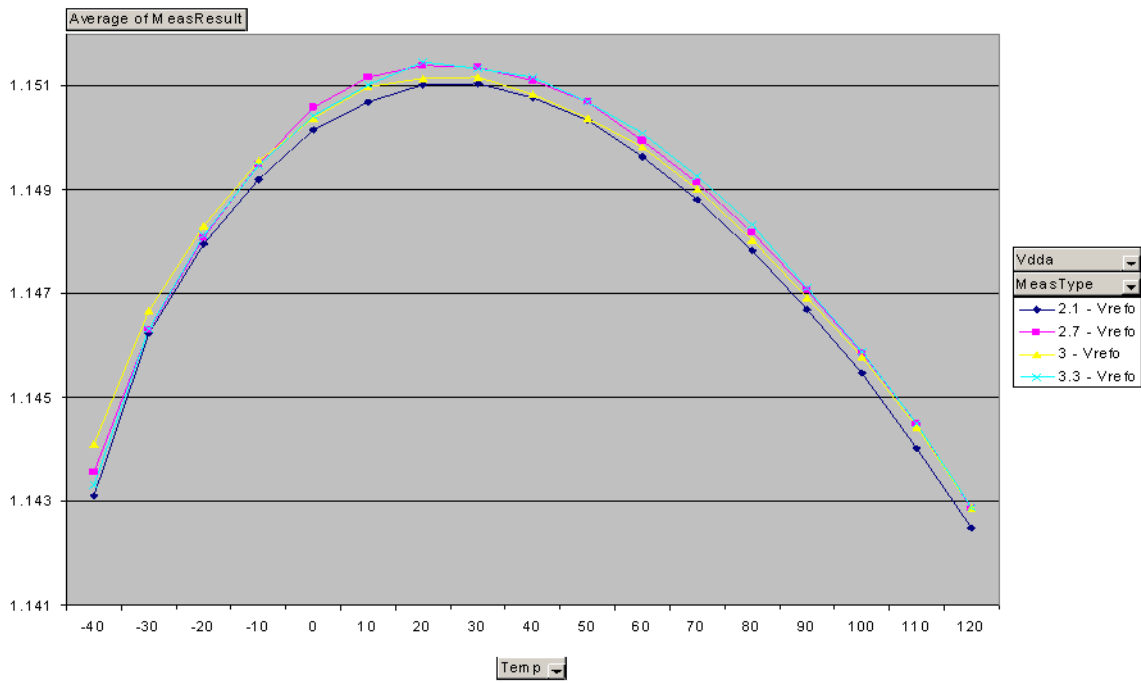
Table 27. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C
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¹ See typical chart that follows (Figure 20).



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È€	NO Ø\{i` Ø b {àæà\àà ÄÖS KÈÈÈ@Ò, B	^WòS^	-	È	-	RY	œ
ÈF	Ø\{i` O b b \ R æà Uà`ää`- \ Uà`-	ORUU	HÈ	IÈ	-	æÑ	Ù
ÈG	T cà[Ú {iç Uà`ää`- \ Uà`- \	TÚUU	HÈ	IÈ	-	æÑ	Ù
ÈH	Úiàc Uà`-à ÄÖS KÈÈÈ b ÙB Q cE{ cà[b æà	ÚU	-	ÈÈÈ	-	ÙÈ{ }	Ù
ÈI	Úiàc Uà`-à ÄÖS KÈÈÈ b ÙB Ò-â^E] {ààæ b æà	ÚU	-	È	-	ÙÈ{ }	Ù
ÈÍ	Û\`ç Öâ-\ Ñà\æc-æ^ ÁQ cE{ cà[b æàB GÈ{Ò	ÖÑV	ÈÈÈG	ÈÈDG	-	RÒ,	Ù
ÈÎ	Û\`ç Öâ-\ Ñà\æc-æ^ ÁÒ-â^E] {ààæ b æàB GÈ{Ò	ÖÑV	-	ÈÈH	-	RÒ,	Ù
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ÈÍ	Ø\{ ~ O b b \ R æà Uà~ää~ \ Uà~	ORUU	GG	HG	-	æÑ	Ù
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ÐÈ	Úiàc Uà~ã Á _S Û _Ü KËÈÈ b Û Ò-á^EÚ { àæã b æàB	ÛU	È	-	-	ÙÉ{ }	Ù
ÐÐ	Û\~ç Öâ- \ Ñã \ æc-æ^ ÁQ cET cà b æàB	ÖÑV	ÈÈÐ	-	-	RÒ,	Ù
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^Ð Cèâ^â-\ Úç{-ääi à|i; b \ cá] á^á[ää^à[-],æ â~ €ÈÈ UÐ ÐGóO [|~] ç{-ääi [ää| b b à\æàæ •âi|âÈ

4 Ordering Information

This section contains ordering information for the device numbering system. See [Table 1](#) for feature summary by package information.

4.1 Part Numbers

Table 30. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
RO0GERRDGHURQ	RO0GERRDGH O 0- [à R-à [à \] à [8GHPÉDP	ÉÉF RNTÑÖN	èFÈ ~ ÈÈG öO
RO0GERRDGHUQQ	RO0GERRDGH O 0- [à R-à [à \] à [8GHPÉDP	ÈÈÈ QPÖT	èFÈ ~ ÈÈG öO
RO0GERRDGHURN	RO0GERRDGH O 0- [à R-à [à \] à [8GHPÉDP	ÍÉ RNTÑÖN	èFÈ ~ ÈÈG öO
RO0GERRDGHUQP	RO0GERRDGH O 0- [à R-à [à \] à [8GHPÉDP	ÍÉ QPÖT	èFÈ ~ ÈÈG öO
RO0GERRREDÍURN	RO0GERRREDÍ O 0- [à R-à [à \] à [ÈDÍPÉDP	ÍÉ RNTÑÖN	èFÈ ~ ÈÈG öO
RO0GERRREDÍUQP	RO0GERRREDÍ O 0- [à R-à [à \] à [ÈDÍPÉDP	ÍÉ QPÖT	èFÈ ~ ÈÈG öO

4.2 Package Information

Table 31. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
ÈÈÈ	Q c P àæ Ôiâ` Tää@âââ	QPÖT	QQ	ÍÍÉÉÉ	ÍÍNUÚDÉÉÍV
ÍÉ	Q c P àæ Ôiâ` Tää@âââ	QPÖT	QP	ÉFÉÍ	ÍÍNUÚDÉÉIFV
ÉÉF	RNT ÑÖN Tää@âââ	RNTÑÖN	RQ	ÈDÍGEÉD	ÍÍNUÒÍÍDHIN
ÍÉ	RNT ÑÖN Tää@âââ	RNTÑÖN	RÑ	ÈHHDEÉÉ	ÍÍNUNÈÈHIÉÇE

4.3 Mechanical Drawings

[Table 31](#) provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51MM256/128 Product Summary pages at <http://www.freescale.com>.

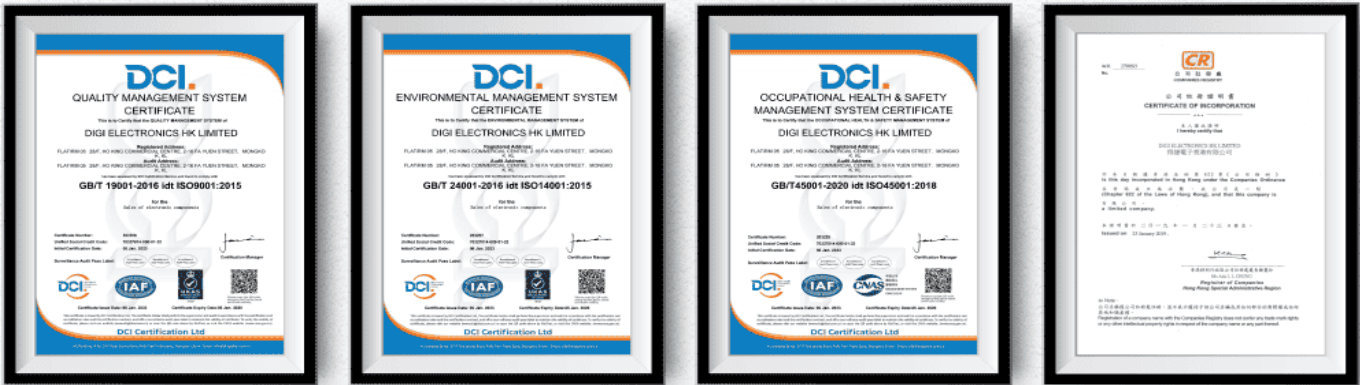
To view the latest drawing, either:

- Click on the appropriate link in [Table 31](#), or
- Open a browser to the Freescale website (<http://www.freescale.com>), and enter the appropriate document number (from [Table 31](#)) in the “Enter Keyword” search box at the top of the page.

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