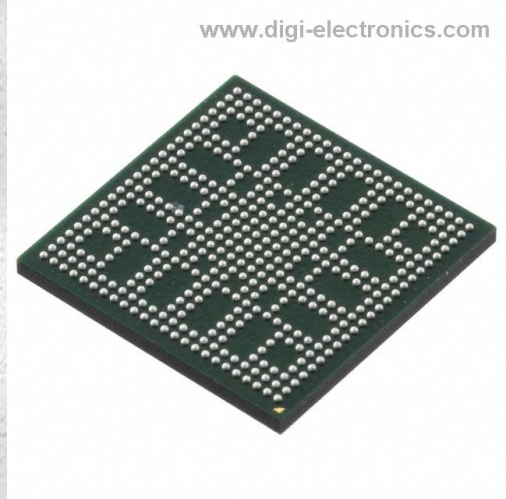
MCIMX6L8DVN10AB Datasheet



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DiGi Electronics Part Number	MCIMX6L8DVN10AB-DG
Manufacturer	NXP USA Inc.
Manufacturer Product Number	MCIMX6L8DVN10AB
Description	IC MPU I.MX6SL 1.0GHZ 432MAPBGA
Detailed Description	ARM® Cortex®-A9 Microprocessor IC i.MX6SL 1 Core, 32-Bit 1.0GHz 432-MAPBGA (13x13)

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Manufacturer Product Number:	Manufacturer:
MCIMX6L8DVN10AB	NXP USA Inc.
Series:	Product Status:
i.MX6SL	Active
Core Processor:	Number of Cores/Bus Width:
ARM® Cortex®-A9	1 Core, 32-Bit
Speed:	Co-Processors/DSP:
1.0GHz	Multimedia; NEON™ SIMD
RAM Controllers:	Graphics Acceleration:
LPDDR2, LVDDR3, DDR3	Yes
Display & Interface Controllers:	Ethernet:
Keypad, LCD	10/100Mbps (1)
SATA:	USB:
-	USB 2.0 + PHY (3)
Voltage - I/O:	Operating Temperature:
1.2V, 1.8V, 3.0V	0°C ~ 95°C (TJ)
Mounting Type:	Package / Case:
Surface Mount	432-TFBGA
Supplier Device Package:	Additional Interfaces:
432-MAPBGA (13x13)	AC97, I2C, I2S, MMC/SD/SDIO, SPI, SSI, UART
Base Product Number:	
MCIMX6	

Environmental & Export classification

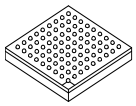
RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	3 (168 Hours)
REACH Status:	ECCN:
REACH Unaffected	5A992C
HTSUS:	
8542.31.0001	

NXP Semiconductors
Data Sheet: Technical Data

Document Number: IMX6SLCEC
Rev. 6, 11/2018

MCIMX6LxDVN10xx
MCIMX6LxEVN10xx

i.MX 6SoloLite Applications Processors for Consumer Products



Package Information
Plastic Package
13 x 13 mm, 0.5 mm pitch

Ordering Information
See Table 1 on page 3

1 Introduction

The i.MX 6SoloLite processor represents the latest achievement in integrated multimedia applications processors, which are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption.

The processor features NXP's advanced implementation of the a single ARM® Cortex®-A9 MPCore™ multicore processor, which operates at speeds up to 1 GHz. It includes 2D graphics processor and integrated power management. The processor provides a 32-bit DDR3-800 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

The i.MX 6SoloLite processor is specifically useful for applications, such as:

- Color and monochrome eReaders
- Entry level tablets
- Barcode scanners

1 Introduction 1
1.1 Ordering Information 2
1.2 Features 4
1.3 Updated Signal Naming Convention 7
2 Architectural Overview 8
2.1 Block Diagram 8
3 Modules List 9
3.1 Special Signal Considerations 15
3.2 Recommended Connections for Unused Analog Interfaces 17
4 Electrical Characteristics 17
4.1 Chip-Level Conditions 17
4.2 Power Supplies Requirements and Restrictions . . 26
4.3 Integrated LDO Voltage Regulator Parameters . . 27
4.4 PLL's Electrical Characteristics 29
4.5 On-Chip Oscillators 30
4.6 I/O DC Parameters 31
4.7 I/O AC Parameters 35
4.8 Output Buffer Impedance Parameters 38
4.9 System Modules Timing 40
4.10 External Peripheral Interface Parameters 52
5 Boot Mode Configuration 80
5.1 Boot Mode Configuration Pins 80
5.2 Boot Devices Interfaces Allocation 81
6 Package Information and Contact Assignments 82
6.1 Updated Signal Naming Convention 82
6.2 13 x 13mm Package Information 83
7 Revision History 101

NXP Reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

The i.MX 6SoloLite processor features:

- Applications processor—The processor enhances the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS requirements of operating systems and games. The Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processor has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processor improves the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: 2D BLit engine, a 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—The processor supports connections to a variety of interfaces: LCD controller, CMOS sensor interface (parallel), high-speed USB on-the-go with PHY, high-speed USB host PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100 Mbps Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio).
- Electronic Paper Display Controller—The processor integrates EPD controller that supports E Ink color and monochrome with up to 2048 x 1536 resolution at 106 Hz refresh, 4096 x 4096 resolution at 20 Hz refresh and 5-bit grayscale (32-levels per color channel).
- Advanced security—The processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6SoloLite security reference manual (IMX6SLSRM). Contact your local NXP representative for more information.
- Integrated power management—The processor integrates linear regulators and generate internally all the voltage levels for different domains. This significantly simplifies system power management structure.
- GPIO with interrupt capabilities—The new GPIO pad design supports configurable dual voltage rails at 1.8 V and 3.3 V supplies. The pad is configurable to interface at either voltage level.

1.1 Ordering Information

Table 1 provides examples of orderable part numbers covered by this data sheet. Table 1 does not include all possible orderable part numbers. The latest part numbers are available on nxp.com/imx6series. If your

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desired part number is not listed in Table 1, or you have questions about available parts, see nxp.com/imx6series or contact your NXP representative.

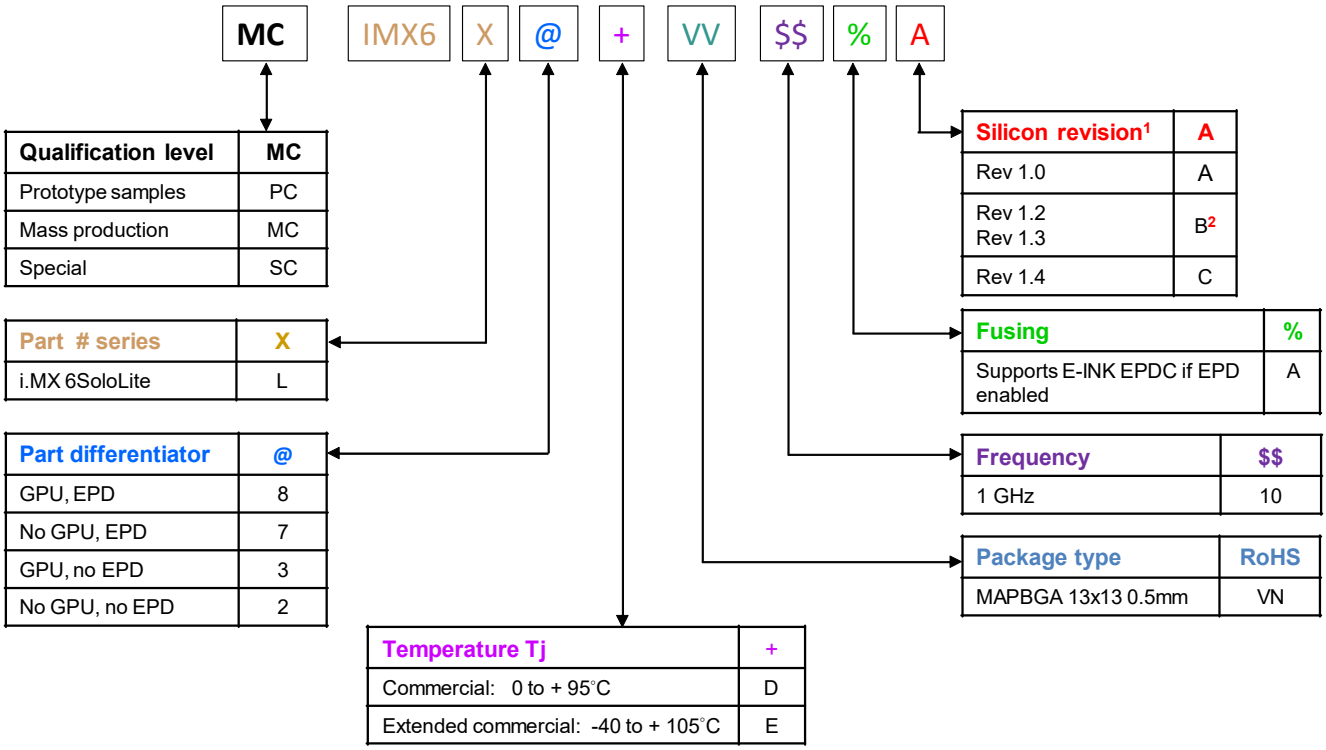
Table 1. Example Orderable Part Numbers

Part Number	Options	Speed Grade[1]	Temperature (Tj)	Package[2]
MCIMX6L8DVN10AB	GPU, EPDC	1GHz	0°C to +95°C	13x13mm, 0.5mm pitch BGA
MCIMX6L8DVN10AC	GPU, EPDC	1GHz	0°C to +95°C	13x13mm, 0.5mm pitch BGA
MCIMX6L7DVN10AB	EPDC, no GPU	1GHz	0°C to +95°C	13x13mm, 0.5mm pitch BGA
MCIMX6L7DVN10AC	EPDC, no GPU	1GHz	0°C to +95°C	13x13mm, 0.5mm pitch BGA
MCIMX6L3DVN10AB	GPU, no EPDC	1GHz	0°C to +95°C	13x13mm, 0.5mm pitch BGA
MCIMX6L3DVN10AC	GPU, no EPDC	1GHz	0°C to +95°C	13x13mm, 0.5mm pitch BGA
MCIMX6L3EVN10AB	GPU, no EPDC	1GHz	-40°C to +105°C	13x13mm, 0.5mm pitch BGA
MCIMX6L3EVN10AC	GPU, no EPDC	1GHz	-40°C to +105°C	13x13mm, 0.5mm pitch BGA
MCIMX6L2DVN10AB	no GPU, no EPDC	1GHz	0°C to +95°C	13x13mm, 0.5mm pitch BGA
MCIMX6L2DVN10AC	no GPU, no EPDC	1GHz	0°C to +95°C	13x13mm, 0.5mm pitch BGA
MCIMX6L2EVN10AB	no GPU, no EPDC	1GHz	-40°C to +105°C	13x13mm, 0.5mm pitch BGA
MCIMX6L2EVN10AC	no GPU, no EPDC	1GHz	-40°C to +105°C	13x13mm, 0.5mm pitch BGA

1 If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

2 Case 2240 is RoHS compliant, lead-free moisture sensitivity level 3 (MSL).

Figure 1 describes the part number nomenclature so that users can identify the characteristics of the specific part number they have (for example, Cores, Frequency, Temperature Grade, Fuse options, Silicon revision).



1. See the nxp.com\imx6series Web page for latest information on the available silicon revision.
2. Rev 1.2 (USB_ANALOG_DIGPROG register = 0x0062_0002)
   Rev 1.3 (USB_ANALOG_DIGPROG register = 0x0062_0003)

Figure 1. Part Number Nomenclature—i.MX 6SoloLite

1.2 Features

The i.MX 6SoloLite processor is based on ARM Cortex-A9 MPCore multicore processor, which has the following features:

- ARM Cortex-A9 MPCore CPU processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 256 KB unified I/D L2 cache
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including NEON and L1 cache) as per Table 9, "Operating Ranges," on page 21

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
- External memory interfaces:
  - 16-bit, and 32-bit DDR3-800, and LPDDR2-800 channels
  - 16/32-bit NOR Flash.
  - 16/32-bit PSRAM, Cellular RAM (32 bits or less)

Each i.MX 6SoloLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total of three interfaces are available.
  - LCD, 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz)
  - EPDC, color, and monochrome E Ink, up to 1650 x 2332 resolution and 5-bit grayscale
- Camera sensors:
  - Parallel Camera port (up to 16-bit and up to 66 MHz peak)
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
    - 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
- USB:
  - Two High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
  - One USB 2.0 (480 Mbps) hosts:
    - One HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Miscellaneous IPs and interfaces:
  - SSI block—capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I^2S mode
  - Five UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode

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  - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
- Four eCSPI (Enhanced CSPI)
- Three I^2C, supporting 400 kbps
- Ethernet Controller, 10/100 Mbps
- Four Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- Sony Philips Digital Interface (SPDIF), Rx and Tx
- Two Watchdog timers (WDOG)
- Audio MUX (AUDMUX)

The i.MX 6SoloLite processor integrates advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6SoloLite processor uses dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6SoloLite processor incorporates the following hardware accelerators:

- GPU2Dv2—2D Graphics Processing Unit (BitBlt).
- GPUVG—OpenVG 1.1 Graphics Processing Unit.
- PXP—PiXel Processing Pipeline. Off loading key pixel processing operations are required to support the EPD display applications.

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock.
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

NOTE

The actual feature set depends on the part numbers as described in Table 1, "Example Orderable Part Numbers," on page 3. Functions, such as 2D hardware graphics acceleration or E Ink may not be enabled for specific part numbers.

1.3 Updated Signal Naming Convention

The signal names of the i.MX6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6SoloLite processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6SoloLite processor system.

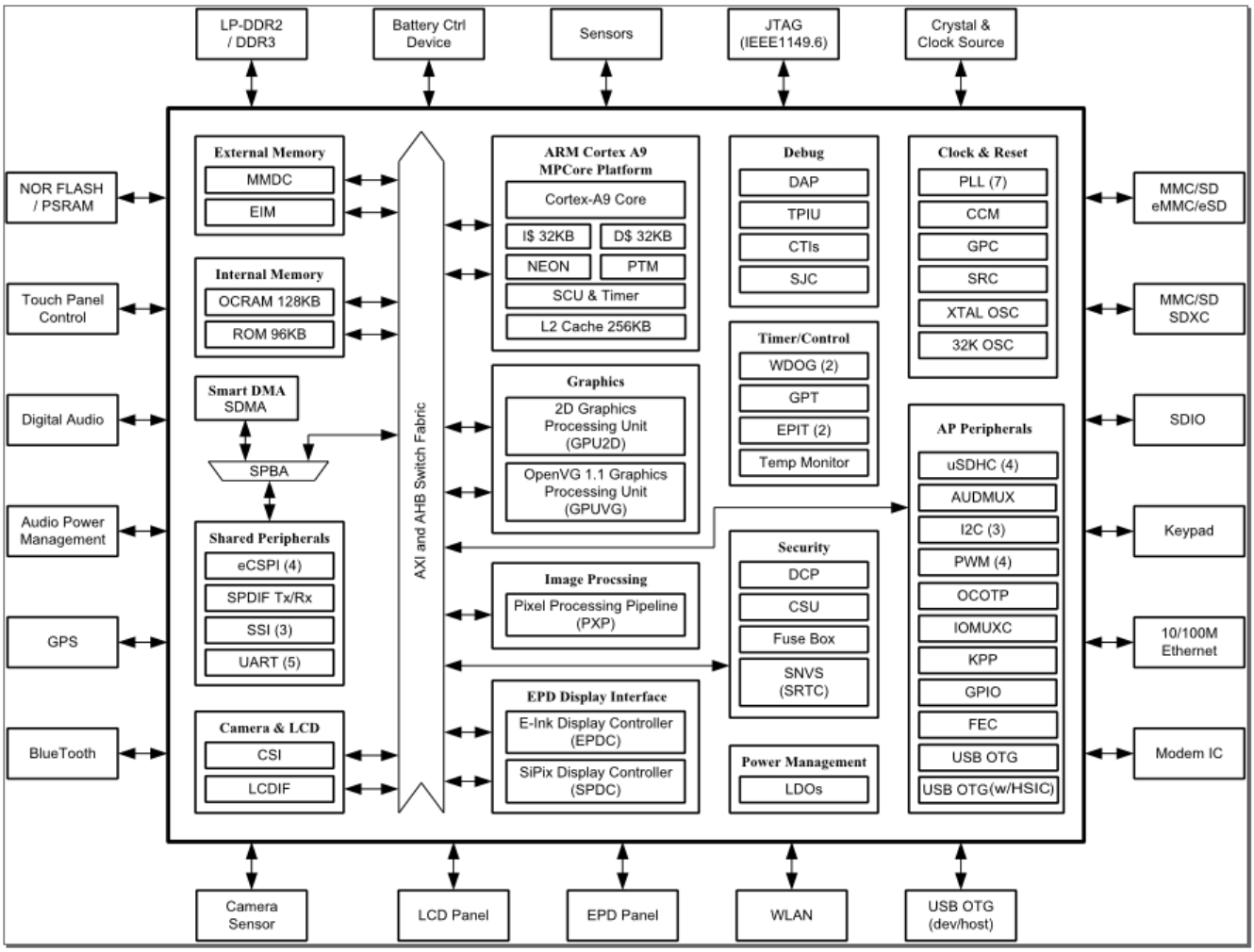

Figure 2. i.MX 6SoloLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

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3 Modules List

The i.MX 6SoloLite processor contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6SoloLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
128x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6SoloLite processor consists of 2-128x8-bit fuse box accessible through OCOTP_CTRL interface.
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of a Cortex-A9 core version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SoloLite platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-1 CTI-2 CTI-3 CTI-4 CTI-5	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI-1 eCSPI-2 eCSPI-3 eCSPI-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E Ink EPD panels, supporting a wide variety of TFT backplanes.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPUVGv2	Vector Graphics Processing Unit, ver2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LCDIF	LCD Interface	Multimedia Peripherals	The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes.
MMDC	DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 16/32-bit DDR3-800 or LPDDR2-800 • Supports up to 2 GByte DDR memory space
OCOTP_ CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6SoloLite processor, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OCRAM_L2	On-Chip Memory Controller for L2 Cache	Data Path	The On-Chip Memory controller for L2 cache (OCRAM_L2) module is designed as an interface between system's AXI bus and internal (on-chip) L2 cache memory module during boot mode.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from external crystal.
PMU	Power Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with either of the integrated EPD controllers.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RNGB	Random Number Generator	Security	Random number generating module.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Software switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloLite processor uses JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP, for detecting high temperature conditions. The Temperature sensor IP for detecting die temperature. The temperature read out does not reflect case or ambient temperature, but the proximity of the temperature sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5.0 Mbps. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH2A	2x USB 2.0 High Speed OTG and 1x HS Hosts	Connectivity Peripherals	USBO2H contains: • Two high-speed OTG module with integrated HS USB PHY • One identical high-speed Host modules connected to HSIC USB ports

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SoloLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Conforms to the SD Host Controller Standard Specification version 3.0. • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4/4.41/4.5 including high-capacity (size > 2 GB) cards HC MMC. Hardware reset as specified for eMMC cards is supported at ports 3 and 4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances 1 and 2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports 1 and 2 in four bit configuration (SD interface). Port 3 is placed in an independent power domain and port 4 shares its power domain with other interfaces.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system’s security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6SoloLite processor. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are provided in the *i.MX 6SoloLite reference manual* (IMX6SLRM).

Table 3. Special Signal Considerations

Signal Name	Remarks
XTALOSC_CLK1_P/ XTALOSC_CLK1_N	One general purpose differential high speed clock Input/output is provided. It could be used to: • To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for Audio interfaces, etc. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the i.MX 6SoloLite reference manual for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard, the maximum clock out frequency range supported is 528 MHz. Alternatively one may use single ended signal to drive XTALOSC_CLK1_P input. In this case, the corresponding XTALOSC_CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See LVDS pad electrical specification for further details. After initialization, the XTALOSC_CLK1 input/output could be disabled (if not used). If unused, the XTALOSC_CLK1_N/P pair can remain unconnected.
DRAM_VREF	When using DRAM_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DRAM_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DRAM_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6SoloLite are drawing current on the resistor divider. It is recommended to use regulated power supply for "big" memory configurations (more that eight devices).
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MODE must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MODE set to high configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MODE set to low configures the JTAG interface for common Software debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and must remain unconnected by the user.
SRC_ONOFF	In normal mode may be connected to ONOFF button (de-bouncing provided at this input). Internally this pad is pulled up. A short duration (<5s) connection to GND in OFF mode causes the internal power management state machine to change the state to ON. In ON mode, a short duration connection to GND generates interrupt (intended to initiate a software controllable power down). A long duration (above ~5s) connection to GND causes "forced" OFF.
SRC_POR_B	This cold reset negative logic input resets all modules and logic in the IC.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
RTC_XTALI/ RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In the case when a high accuracy real time clock is not required, the system may use an internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and leave RTC_XTALO unconnected.
TEST_MODE	TEST_MODE is for NXP factory use. This signal is internally connected to an on-chip pull-down device. The user must either leave this signal unconnected or tie it to GND.
XTALI/XTALO	• A 24.0 MHz crystal must be connected between XTALI and XTALO. The level and frequency must be <32 MHz under typical conditions. • The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typically 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. • The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO remains unconnected. The XTALI signal level must swing from ~0.8 x NVCC_PLL_OUT to ~0.2 V. • This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. • See the XTALOSC chapter and relevant interface specifications chapters of the i.MX 6SoloLite reference manual (IMX6SLRM), for details.
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRST_B	Input	47 kΩ pull-up
JTAG_MODE	Input	100 kΩ pull-up

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused?
XTALOSC	XTALOSC_CLK1_N, XTALOSC_CLK1_P	Leave unconnected
USB	USB_OTGx_DN, USB_OTGx_DP, USB_OTGx_VBUS, USB_OTG_CHD_B	Leave unconnected

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SoloLite.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6SoloLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 18
BGA Case 2240 Package Thermal Resistance	on page 19
Operating Ranges	on page 21
External Clock Sources	on page 23
Maximum Supply Currents	on page 24
Low Power Mode Supply Currents	on page 25
USB PHY Current Consumption	on page 26

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Table 9, "Operating Ranges" or subsequent parameters tables is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7 provides the absolute maximum operating ratings.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply input voltage (LDO enabled)	VDD_ARM_IN VDD_SOC_IN VDD_PU_IN	-0.3	1.6	V
Core supply input voltage (LDO bypass)	VDD_ARM_IN VDD_SOC_IN VDD_PU_IN	-0.3	1.4	V
Core supply output voltage (LDO enabled)	VDD_ARM_CAP VDD_SOC_CAP VDD_PU_CAP	-0.3	1.4	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.7	V
VDD_HIGH_CAP supply output voltage	VDD_HIGH_CAP	-0.3	2.6	V
DDR I/O supply voltage	NVCC_DRAM	-0.4	1.975 (See note 1)	V
DDR pre-drivers supply voltage	NVCC_DRAM_2P5	-0.3	2.85	V
GPIO dual supply 1P8V I/O supply voltage	NVCC18_IO	-0.5	2.1	V
GPIO dual supply 3P3V I/O supply voltage	NVCC33_IO	-0.5	3.7	V
SNVS IN supply voltage (Secure Non-Volatile Storage and Real Time Clock)	VDD_SNVS_IN	-0.3	3.7	V
USB I/O supply voltage	USB_H1_DN USB_H1_DP USB_OTG_DN USB_OTG_DP USB_OTG_CHD_B	-0.3	3.63	V
USB VBUS supply voltage	USB_OTG_VBUS	—	5.25	V
Vin/Vout I/O voltage range (non-DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.3 (See note 2)	V
Vin/Vout I/O voltage range (DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.4 (See notes1& 2)	V
ESD immunity (HBM)	Vesd_HBM	—	2000	V
ESD immunity (CDM)	Vesd_CDM	—	500	V
Storage temperature range	$T_{STORAGE}$	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

NOTE

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432

4.1.2.1 BGA Case 2240 Package Thermal Resistance

Table 8 provides the MAPBGA package thermal resistance data.

Table 8. Package Thermal Resistance Data

Rating	Board	Symbol	No Lid	Unit
Junction to Ambient[1] (natural convection)	Single layer board (1s)	$R_{\theta JA}$	51	°C/W
	Four layer board (2s2p)	$R_{\theta JA}$	28	°C/W
Junction to Ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board[2]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[3] (Top)	—	$R_{\theta JCtop}$	9	°C/W
Junction to Package Top[4]	Natural Convection	Ψ_{JT}	2	°C/W

1 Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating Ranges

Figure 3 shows major power systems blocks and internal/external connections for the i.MX 6SoloLite processor.

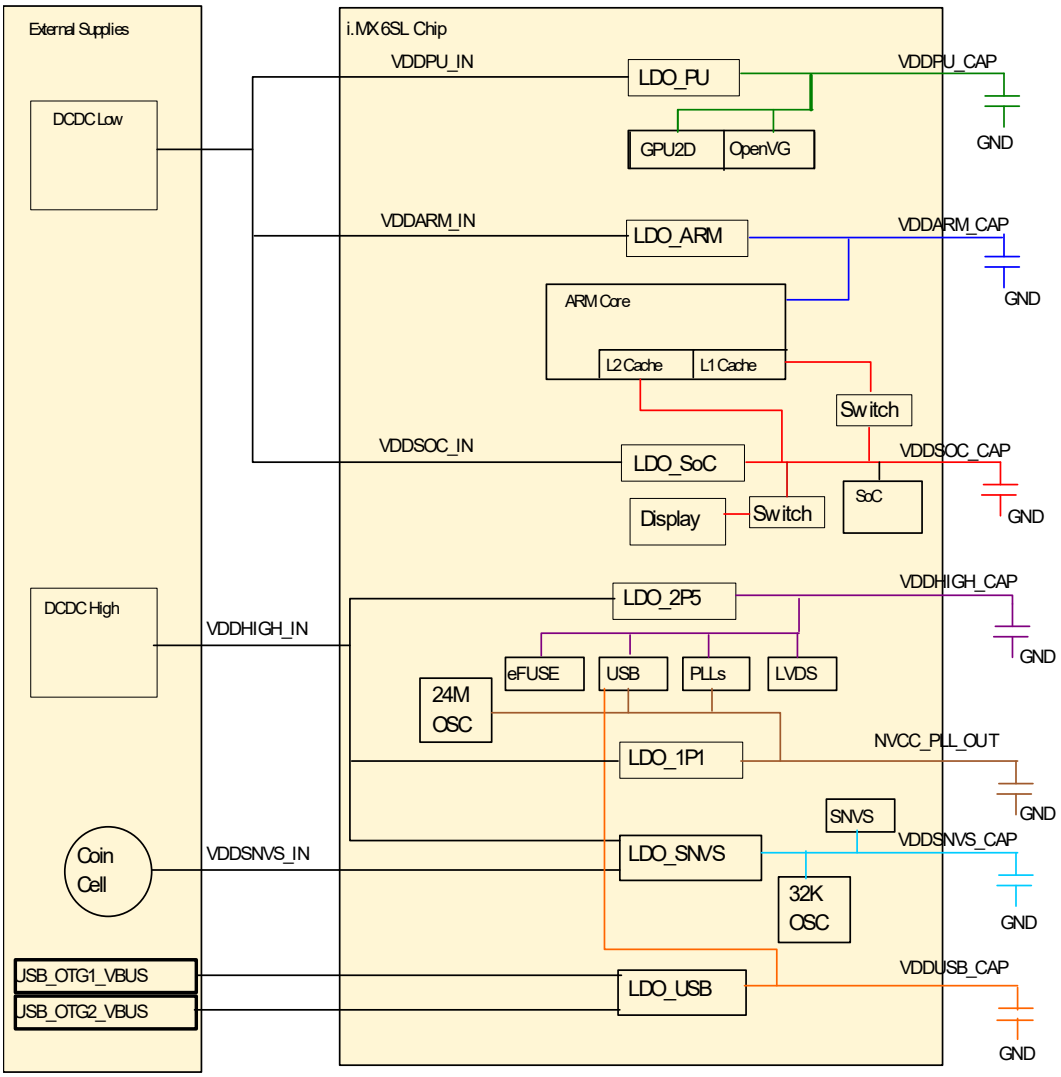

Figure 3. i.MX 6SoloLite SoC Power Block Diagram

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 9 provides the operating ranges of the i.MX 6SoloLite processor. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6SoloLite Reference Manual* (IMX6SLRM).

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDD_ARM_IN	1.375[2]	—	1.5	V	LDO output set at 1.250V minimum for operation up to 996 MHz
		1.275[2]	—	1.5	V	LDO output set at 1.150V minimum for operation up to 792 MHz
		1.075[2]	—	1.5	V	LDO output set at 0.95V minimum for operation up to 396 MHz
		1.075[2]	—	1.5	V	LDO output set at 0.950V minimum for operation up to 192 MHz
		1.050[2]	—	1.5	V	LDO output set at 0.9250V minimum for operation up to 24 MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.275[2,4]	—	1.5	V	VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum
Run mode: LDO bypassed	VDD_ARM_IN	1.250	—	1.3	V	LDO bypassed for operation up to 996 MHz
		1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		0.950	—	1.3	V	LDO bypassed for operation up to 396 MHz
		0.950	—	1.3	V	LDO bypassed for operation up to 192 MHz
		0.925	—	1.3	V	LDO bypassed for operation up to 24 MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.15[4]	—	1.3	V	—
Standby/DSM Mode	VDD_ARM_IN	0.9	—	1.3	V	See Table 12, "Stop Mode Current and Power Consumption," on page 25.
	VDD_SOC_IN VDD_PU_IN	0.9	—	1.3	V	
VDDHIGH internal Regulator	VDD_HIGH_IN[5]	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.7	—	3.6	V	Should be supplied from the same supply as VDD_HIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS USB_OTG2_VBUS	4.4	—	5.25	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
	NVCC_DRAM_2P5	2.5	2.5	2.75	V	—

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
GPIO supplies[6]	NVCC33_IO	2.8	3.0	3.3	V	Worst case, assuming all SOC I/O operating at 1.8V. NVCC33_IO must always be greater than NVCC18_IO.
	NVCC18_IO	1.62	1.8	1.98	V	—
	NVCC_1P2V	1.14	1.2	1.3	V	—
Junction temperature	T_J	0	—	95	°C	Commercial See *i.MX 6SoloLite Product Lifetime Usage Estimates Application Note*, AN4726, for information on product lifetime (power-on years) for this processor.
Junction temperature	T_J	-40	—	105	—	Extended commercial See *i.MX 6SoloLite Product Lifetime Usage Estimates Application Note*, AN4726, for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

3 VDD_SOC_CAP and VDD_PU_CAP must be equal.

4 VDD_SOC and VDD_PU output voltage must be set to this rule: VDD_ARM - VDD_SOC / VDD_PU < 50mV.

5 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

6 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

4.1.4 External Clock Sources

Each i.MX 6SoloLite processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the RTC_XTALI, in case accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

Table 10 shows the interface frequency requirements.

Table 10. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1, 2]	f_{ckil}	—	32.768[(see 3)]/32.0	—	kHz
XTALI Oscillator[4, 2]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision to choose a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum Supply Currents

The Power Virus numbers shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 11, however a robust thermal design is required for the increased system power dissipation.

See the *i.MX 6SoloLite Power Consumption Measurement Application Note* (AN4580) for more details on typical power consumption under various use case definitions.

Table 11. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	1 GHz ARM clock based on Power Virus operation	1100	mA
VDD_SOC_IN	1 GHz ARM clock	650	mA
VDD_PU_IN	1 GHz ARM clock	150	mA
VDD_HIGH_IN	—	30[1]	mA
VDD_SNVS_IN	—	250[2]	µA
USB_OTG1_VBUS USB_OTG2_VBUS	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	(see[4])	
NVCC33_IO	N=156	Use maximum IO Equation[5]	
NVCC18_IO	N=156	Use maximum IO Equation[5]	
NVCC_1P2V	N=2	Use maximum IO Equation[5]	mA
MISC			
DRAM_VREF	—	1	mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination.
See the i.MX 6SoloLite Power Consumption Measurement Application Note or examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

4.1.6 Low Power Mode Supply Currents

Table 12 shows the current core consumption (not including I/O) of i.MX 6SoloLite processor in selected low power modes.

Table 12. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.375 V)	4	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN(3.0 V)	9	
		Total	44.9	mW
STOP_ON	• ARM LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.375 V)	2.5	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN (3.0 V)	4.5	
		Total	29.3	mW
STOP_OFF	• ARM LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.375 V)	2.5	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	0.1	
		VDD_HIGH_IN (3.0 V)	4.0	
		Total	25.9	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • XTAL is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SoC_IN (0.9 V)	1.0	
		VDD_PU_IN (0.9 V)	0.1	
		VDD_HIGH_IN (3.0 V)	3	
		Total	10.1	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • XTAL and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SoC_IN (0.9 V)	0.75	
		VDD_PU_IN (0.9 V)	0.1	
		VDD_HIGH_IN (3.0 V)	0.15	
		Total	1.3	mW
SNVS Only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	µW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the USB_OTGx_VBUS valid detectors, typical condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY Current Consumption in Power Down Mode

	VDD_USB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- SRC_POR_B signal is used to control the processor POR. SRC_POR_B must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and can be powered at any time.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

NOTE

For customers beginning new designs with the i.MX 6SoloLite and the PF0100 PMIC, it is recommended to use the F3 OTP option instead of the F1 OTP option and the F4 OTP option instead of the F2 OTP option.

4.2.2 Power-Down Sequence

There are no special requirements on the power-down sequence other than the VDD_SNVS_IN supply should be the last to turn off.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 66, "13 x 13 mm Functional Contact Assignments," on page 86.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6SoloLite reference manual for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6SoloLite reference manual.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for min and max input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. LDO_1P1 supplies the USB Phy and the PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloLite Applications Processors (IMX6SLHDG). For additional information, see the i.MX 6SoloLite reference manual.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the USB Phy, LVDS Phy and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloLite Applications Processors (IMX6SLHDG).

For additional information, see the i.MX 6SoloLite reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG1_VBUS and USB_OTG2_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets. If no VBUS voltage is present, then the VBUSVALID threshold setting will prevent the regulator from being enabled.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloLite Applications Processors (IMX6SLHDG).

For additional information, see the i.MX 6SoloLite reference manual.

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 14. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles (15 μs)

4.4.3 Ethernet PLL

Table 16. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

4.4.4 480 MHz PLL

Table 17. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles (15 μs)

4.4.5 ARM PLL

Table 18. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz~1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles (50 μs)

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. It also implements a power mux such that the oscillator can be powered from NVCC_1P2V or VDD_SOC. NVCC_1P2V should be the cleaner supply and is the preferable choice, however, if the oscillator is required to run in *stop mode* then it is necessary to run from VDD_SOC, which is 0.9 V in stop mode.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux.

Table 19. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 μA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μA should be added to this value.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	—	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes

NOTE

The term OVDD in this section refers to the associated supply rail of an input or output.

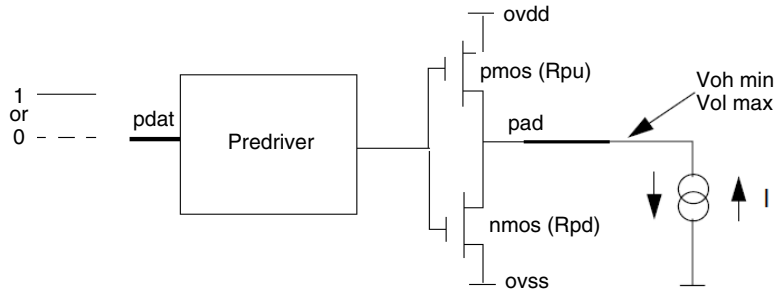

Figure 4. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 20 shows the DC parameters for the clock inputs.

Table 20. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2V	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1[1]	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2V	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
XTALI input leakage at startup	$I_{XTALI_STARTUP}$	Power-on startup for 0.15 msec with a driven 24 MHz clock at 1.1 V. [2]	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

[1] This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

[2] This current draw is present even if an external clock source directly drives XTALI.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 Dual Voltage General Purpose IO Cell Set (DVGPIO) DC Parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 21. DVGPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage [1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage [1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+, [3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–, [3, 4]	VT–	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1.25	1.25	µA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	µA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	µA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin= OVDD	—	48 1	µA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	µA
Keeper circuit resistance	Rkeep	Vin = 0.3 x OVDD Vin = 0.7 x OVDD	105	205	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 DSE is the Drive Strength Field setting in the associated IOMUX control register.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3 operational modes.

4.6.3.1 LPDDR2 Mode I/O DC Parameters

The parameters in Table 22 are guaranteed per the operating ranges in Table 9, unless otherwise noted. For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC)”.

Table 22. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA	0.9 × OVDD	—	V
Low-level output voltage	Vol	Iol = 0.1 mA	—	0.1 × OVDD	V
Input reference voltage	Vref	—	0.49 × OVDD	0.51 × OVDD	V
DC input High Voltage	Vih(dc)	—	Vref+0.13V	OVDD	V
DC input Low Voltage	Vil(dc)	—	OVSS	Vref-0.13V	V
Differential Input Logic High	Vih(diff)	—	0.26	See Note [2]	V
Differential Input Logic Low	Vil(diff)	—	See Note [2]	-0.26	V
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.5	2.5	µA
Pull-up/pull-down impedance Mismatch	MMpupd	—	-15	+15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance	Rkeep	—	110	175	kΩ

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 26).

4.6.3.2 DDR3 Mode I/O DC Parameters

The parameters in Table 23 are guaranteed per the operating ranges in Table 9, unless otherwise noted. For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC)”.

Table 23. DDR3 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA Voh (DSE = 001)	0.8 × OVDD[2]	—	V
		Ioh = -1 mA Voh (for all except DSE = 001)			
Low-level output voltage	Vol	Iol = 0.1 mA Vol (DSE = 001)	—	0.2 × OVDD	V
		Iol = 1 mA Vol (for all except DSE = 001)			
Input reference voltage	Vref[3]	—	0.49 × OVDD	0.51 × OVDD	
DC input Logic High	Vih(dc)	—	Vref+0.1	OVDD	V
DC input Logic Low	Vil(dc)	—	OVSS	Vref-0.1	V
Differential input Logic High	Vih(diff)	—	0.2	See Note[4]	V
Differential input Logic Low	Vil(diff)	—	See Note[4]	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49 × OVDD	0.51 × OVDD	V

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 23. DDR3 I/O DC Electrical Parameters[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.9	2.9	µA
Pull-up/pull-down impedance mismatch	MMpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance[5]	Rkeep	—	105	175	kΩ

1 Note that the JEDEC DDR3 specification (JESD79_3D) supersedes any specification in this document.

2 OVDD – I/O power supply (1.425 V – 1.575 V for DDR3

3 Vref – DDR3 external reference voltage

4 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 27).

5 Use an off-chip pull resistor of 10 kΩ or less to override this keeper.

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Dual Voltage General Purpose I/O (DVGPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

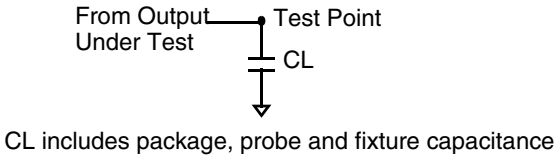

Figure 5. Load Circuit for Output

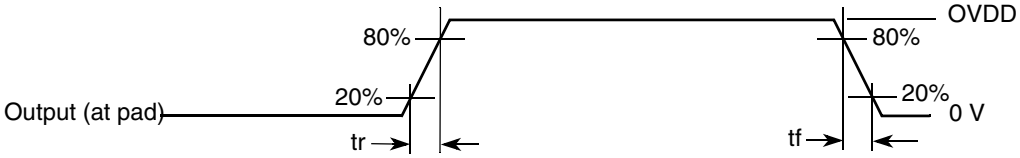

Figure 6. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 24 and Table 25, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 24. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 25. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

4.7.2 DDR I/O AC Parameters

Table 26 shows the AC parameters for DDR I/O operating in LPDDR2 mode. For details on supported DDR memory configurations, see Section 4.9.4, "Multi-Mode DDR Controller (MMDC)".

Table 26. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 4 0 Ω ±30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω ±30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the "true" input signal and Vcp is the "complementary" input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 27 shows the AC parameters for DDR I/O operating in DDR3 mode.

Table 27. DDR I/O DDR3 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref – 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns

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Table 27. DDR I/O DDR3 Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6SoloLite processor for the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3 modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).

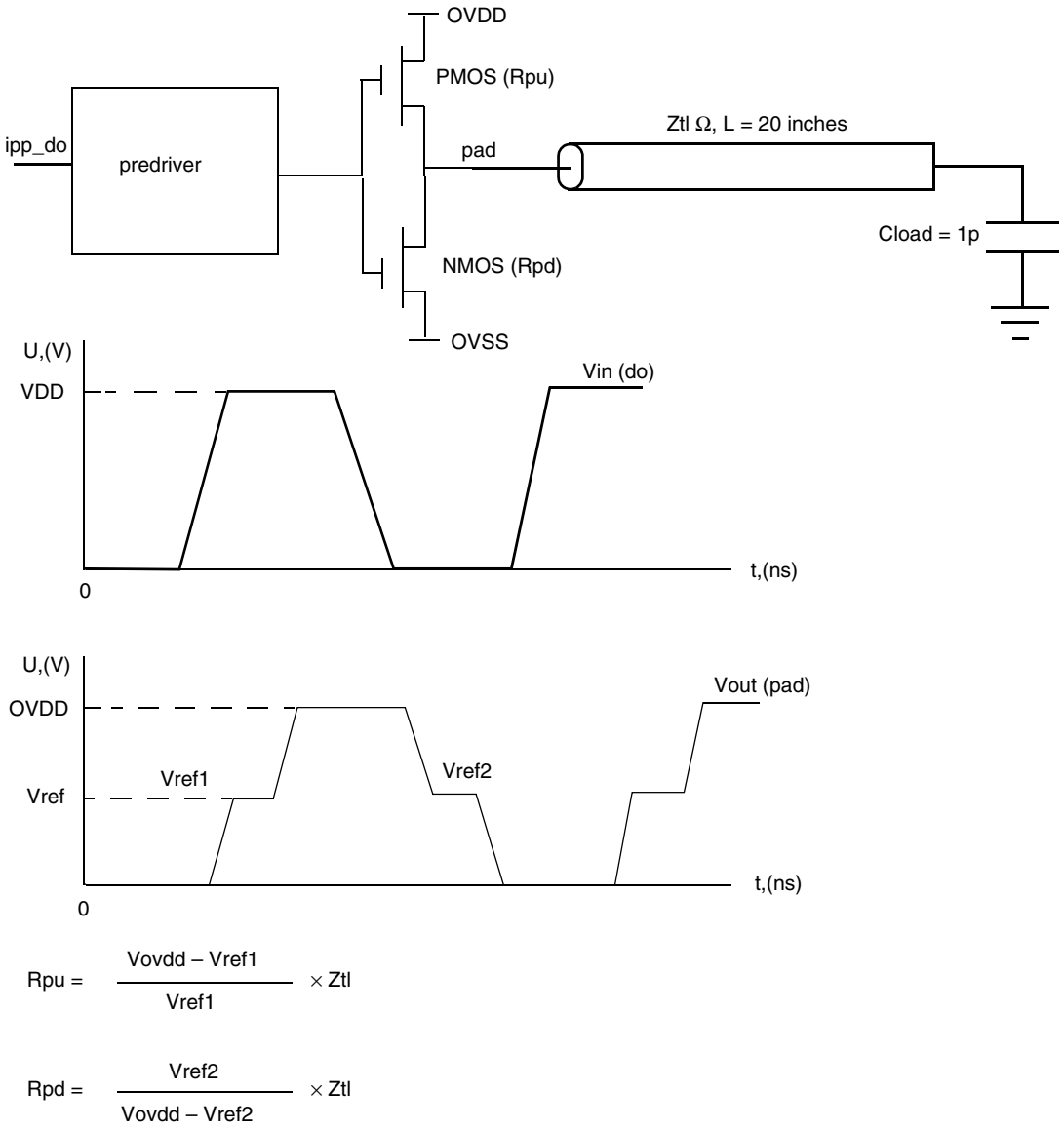

Figure 7. Impedance Matching Load for Measurement

4.8.1 Dual Voltage GPIO Output Buffer Impedance

Table 28 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 28. DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	262 134 88 62 51 43 37	Ω

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Table 29 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 29. DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	247 126 84 57 47 40 34	Ω

4.8.2 DDR I/O Output Buffer Impedance

For details on supported DDR memory configurations, see Section 4.9.4, "Multi-Mode DDR Controller (MMDC)."

Table 30 shows DDR I/O output buffer impedance of i.MX 6SoloLite processor.

Table 30. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) = 000 001 010 011 100 101 110 111	 Hi-Z 240 120 80 60 48 40 34	 Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SoloLite processor.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 31 lists the timing parameters.

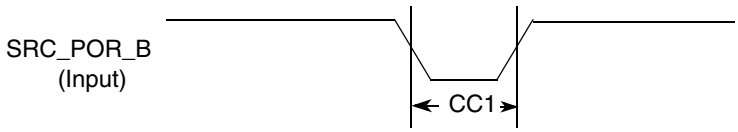

Figure 8. Reset Timing Diagram

Table 31. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	XTALOSC_RTC_XTALI

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 32 lists the timing parameters.

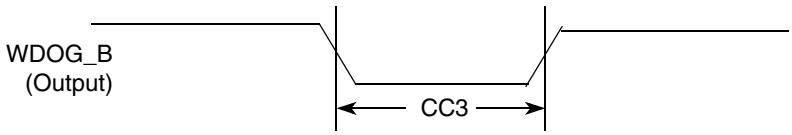

Figure 9. WDOG_B Timing Diagram

Table 32. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated bins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. The maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit, and 8-bit devices operating in address/data separate or multiplexed modes. Table 33 provides EIM interface pads allocation in different modes.

Table 33. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode			Multiplexed Address/Data mode	
	8 Bit		16 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 001	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_DATA [09:00]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	EIM_DATA [15:08]	EIM_AD [15:08]	EIM_AD [15:08]
EIM_DATA [23:16], EIM_EB2_B	—	—	—	—	EIM_DATA [07:00]
EIM_DATA [31:24], EIM_EB3_B	—	—	—	—	EIM_DATA [15:08]

[1] For more information on configuration ports mentioned in this table, see the i.MX 6SololLite reference manual.

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 34 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

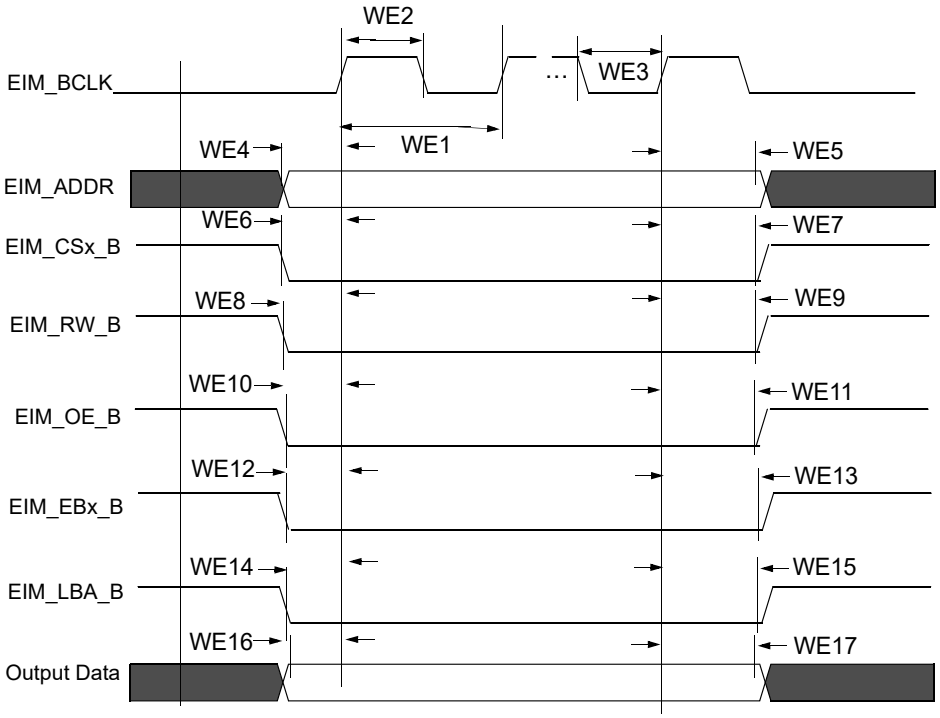

Figure 10. EIM Output Timing Diagram

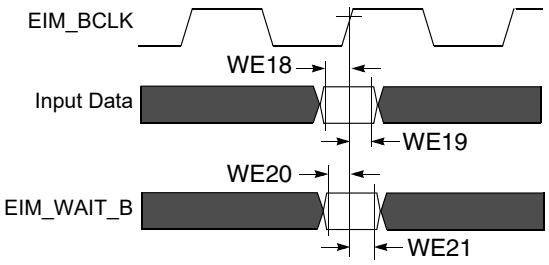

Figure 11. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 34. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK cycle time[2]	t × (k+1)	—	ns
WE2	EIM_BCLK high level width	0.4 × t × (k+1)	—	ns
WE3	EIM_BCLK low level width	0.4 × t × (k+1)	—	ns
WE4	Clock rise to address valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns

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Table 34. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE5	Clock rise to address invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE7	Clock rise to EIM_CSx_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE8	Clock rise to EIM_RW_B valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE9	Clock rise to EIM_RW_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE10	Clock rise to EIM_OE_B valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE11	Clock rise to EIM_OE_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE12	Clock rise to EIM_EBx_B valid	0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE13	Clock rise to EIM_EBx_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE14	Clock rise to EIM_LBA_B valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE15	Clock rise to EIM_LBA_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE16	Clock rise to output data valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE17	Clock rise to output data invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

1 k represents register setting BCD value

2 t is clock period (1/Freq). For 104 MHz, t = 9.165 ns

Figure 12 to Figure 15 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

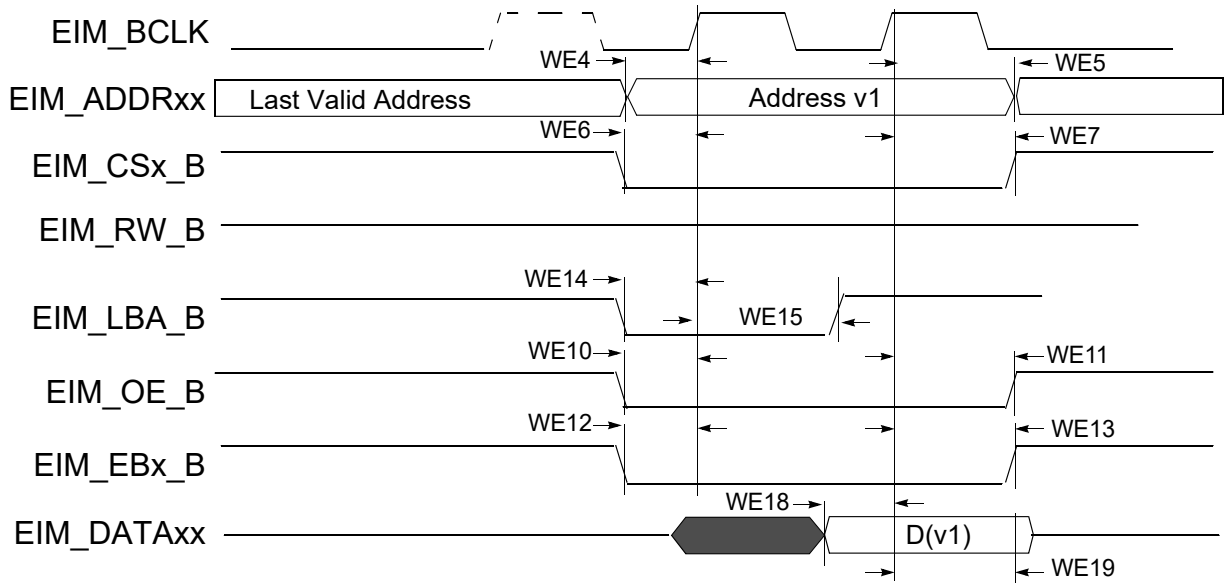

Figure 12. Synchronous Memory Read Access, WSC=1

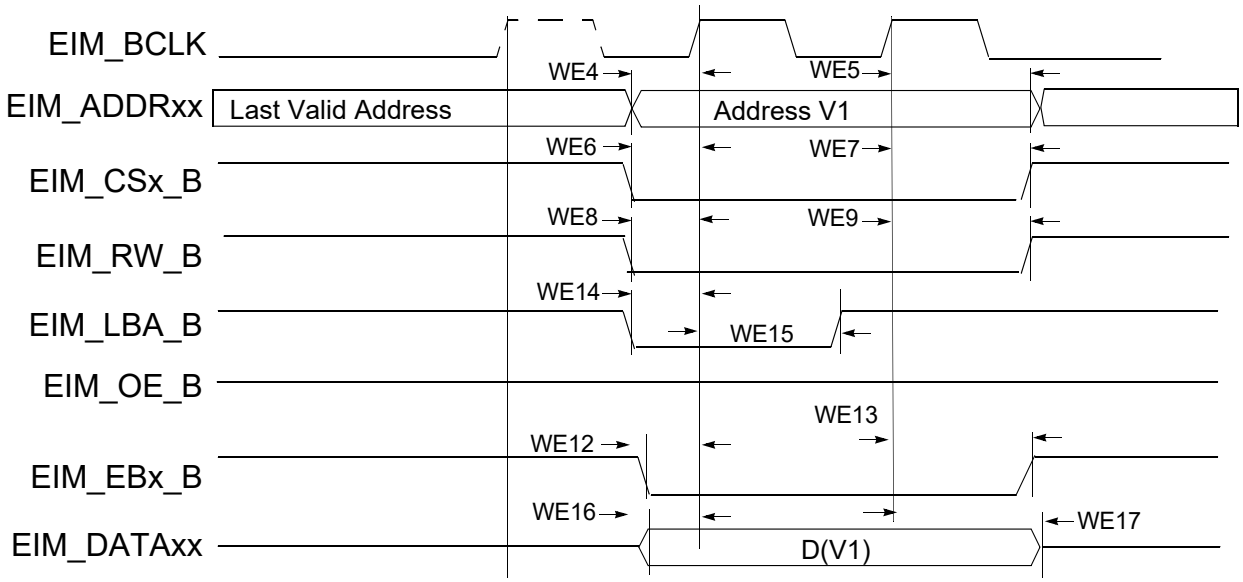

Figure 13. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

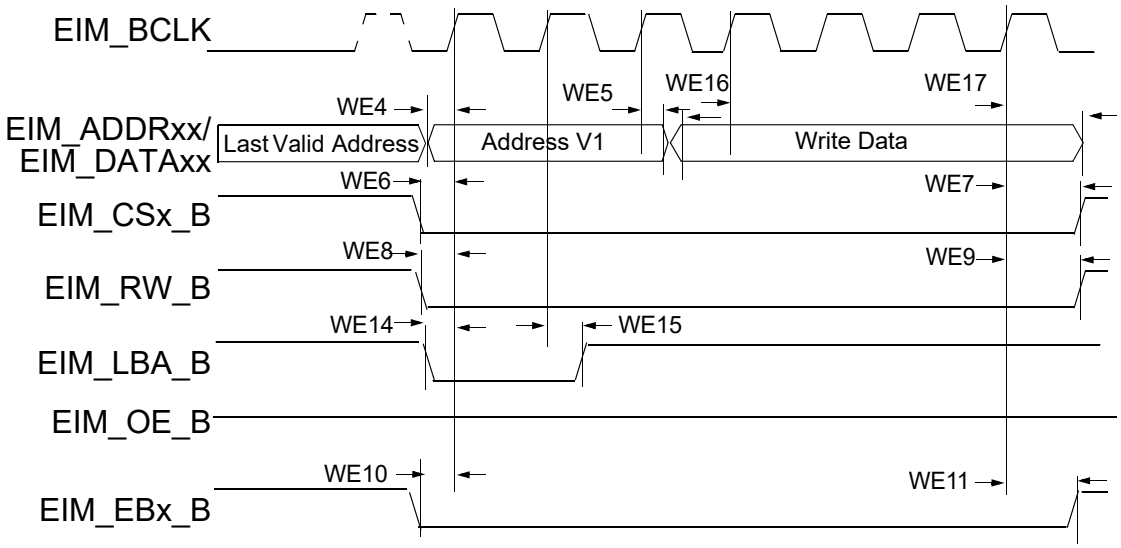

Figure 14. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

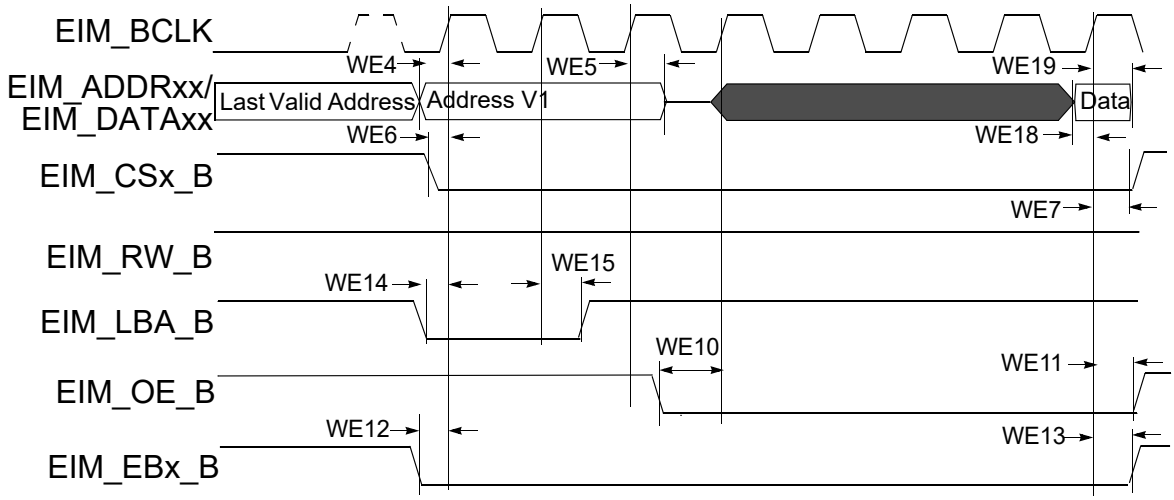

Figure 15. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 16 through Figure 20, and Table 35 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read and write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN and CSN is configured differently. See the i.MX 6SoloLite reference manual for the EIM programming model.

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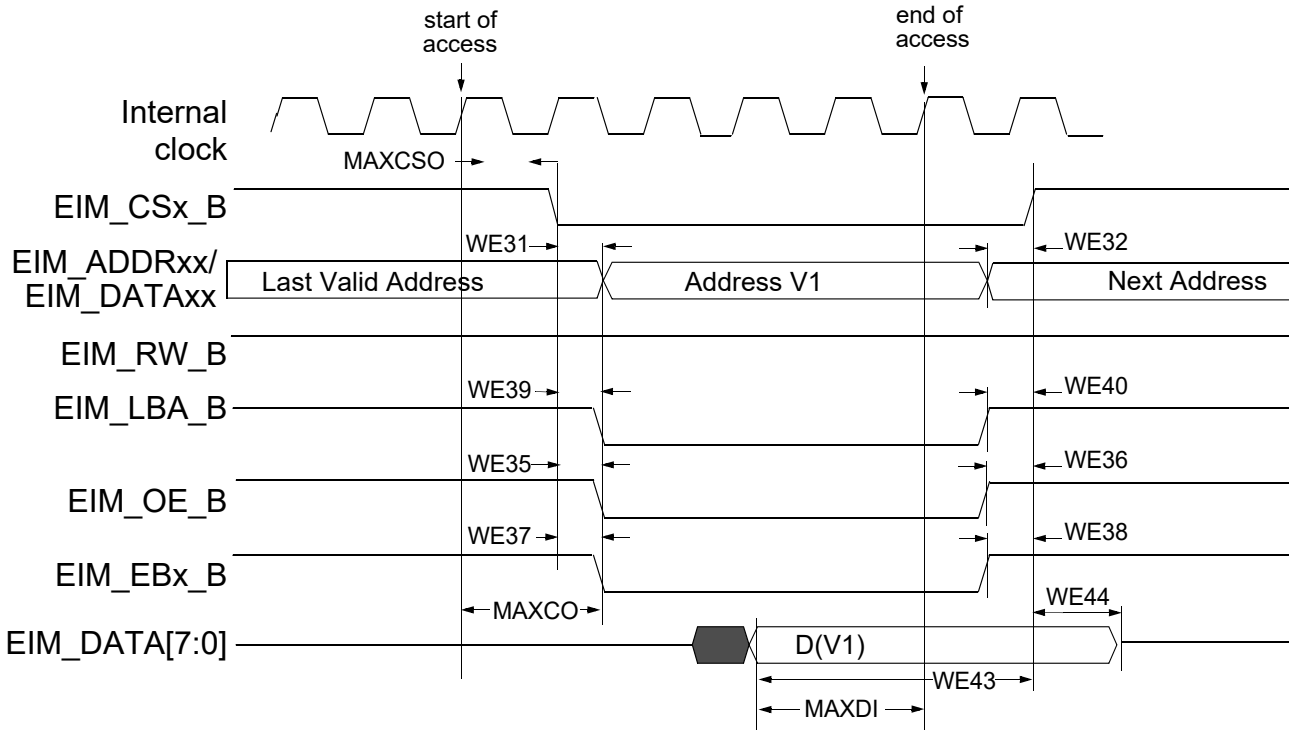

Figure 16. Asynchronous Memory Read Access (RWSC = 5)

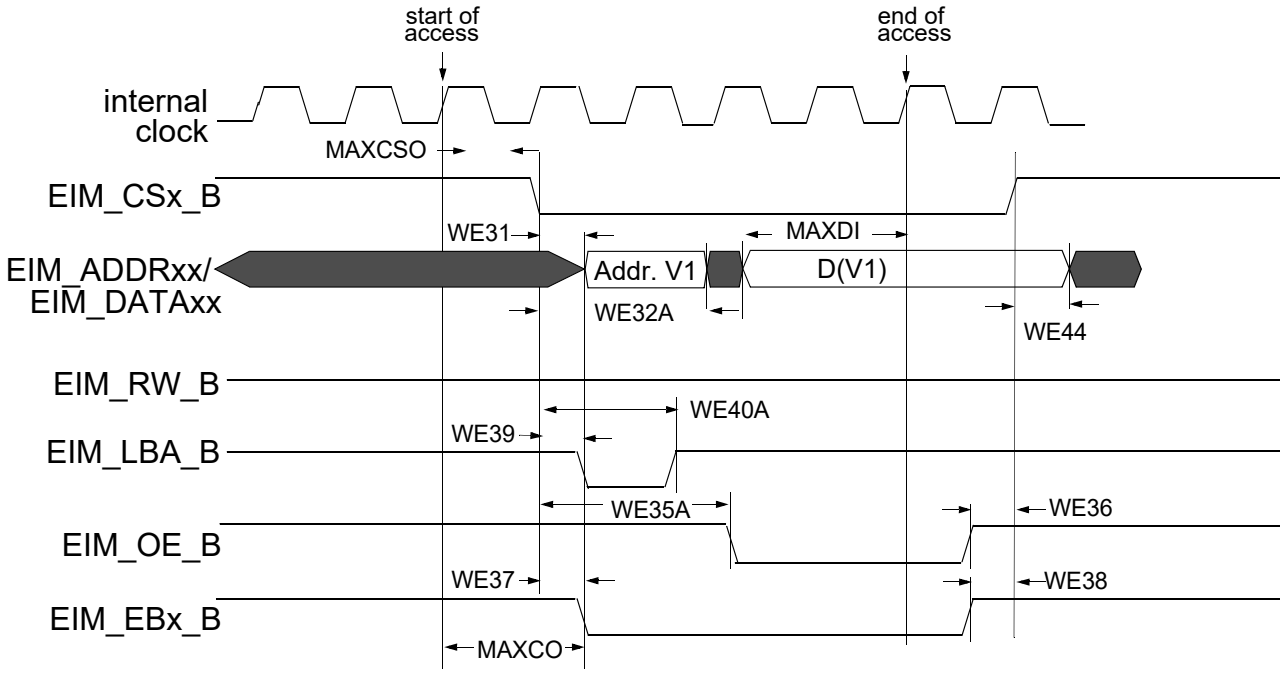

Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

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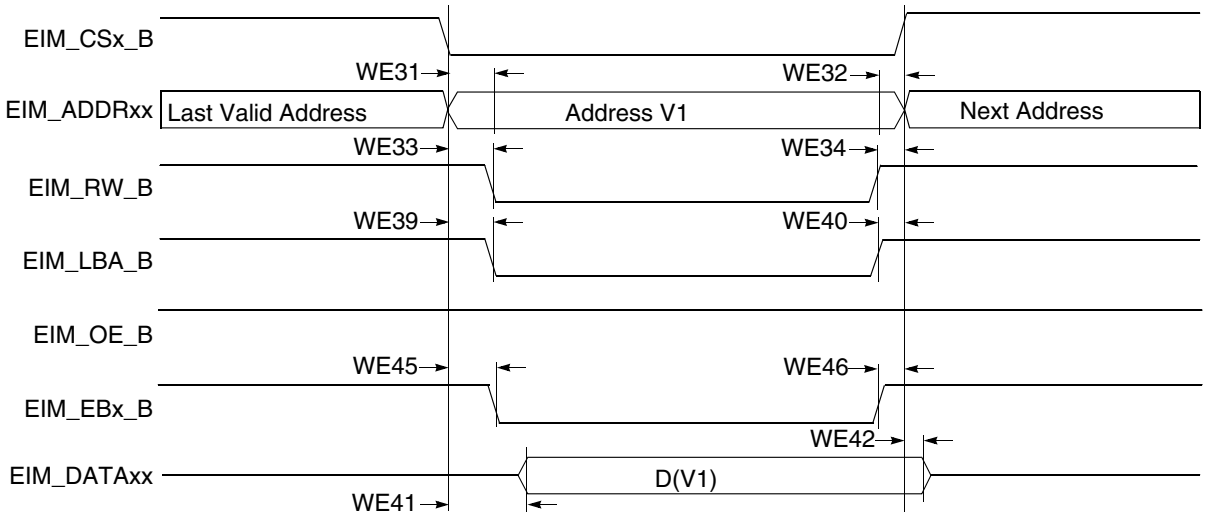

Figure 18. Asynchronous Memory Write Access

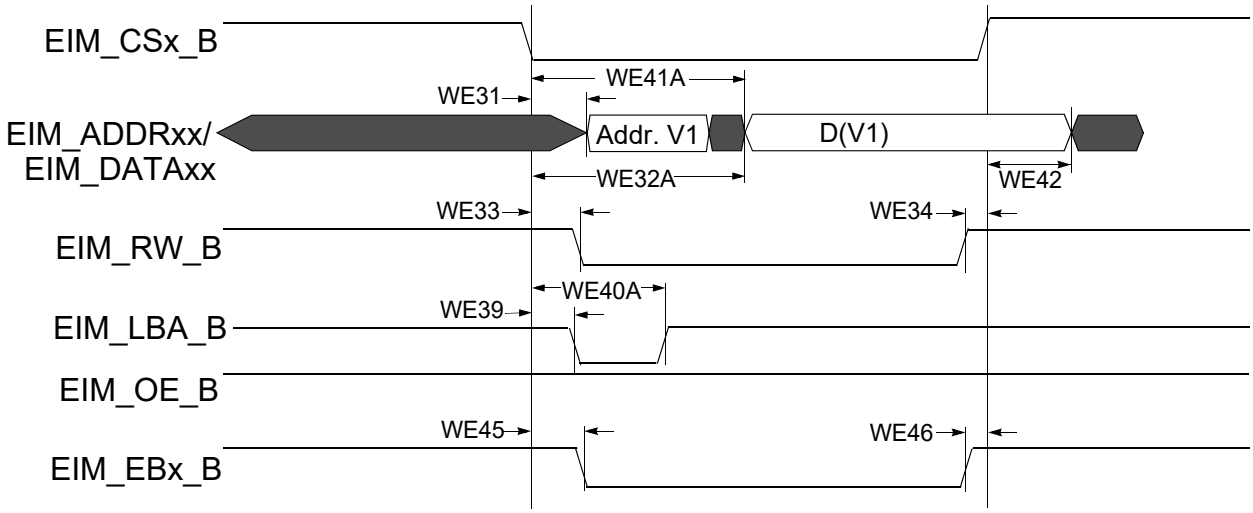

Figure 19. Asynchronous A/D Muxed Write Access

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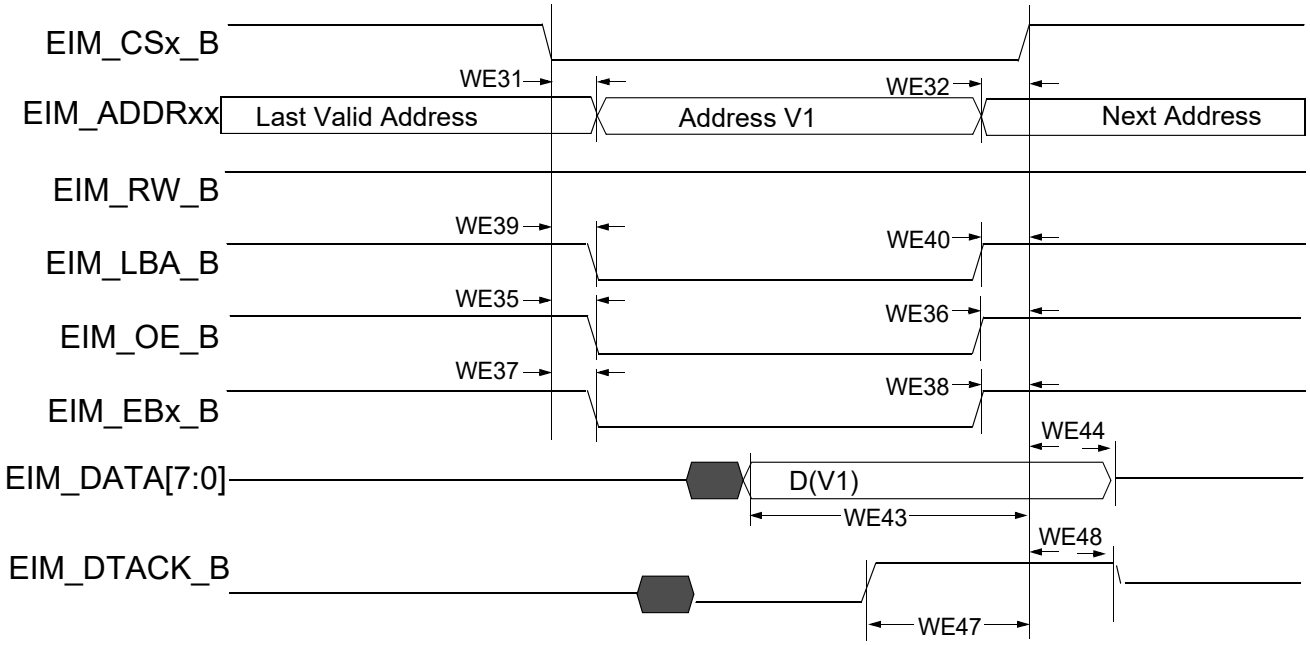

Figure 20. DTACK Read Access (DAP=0)

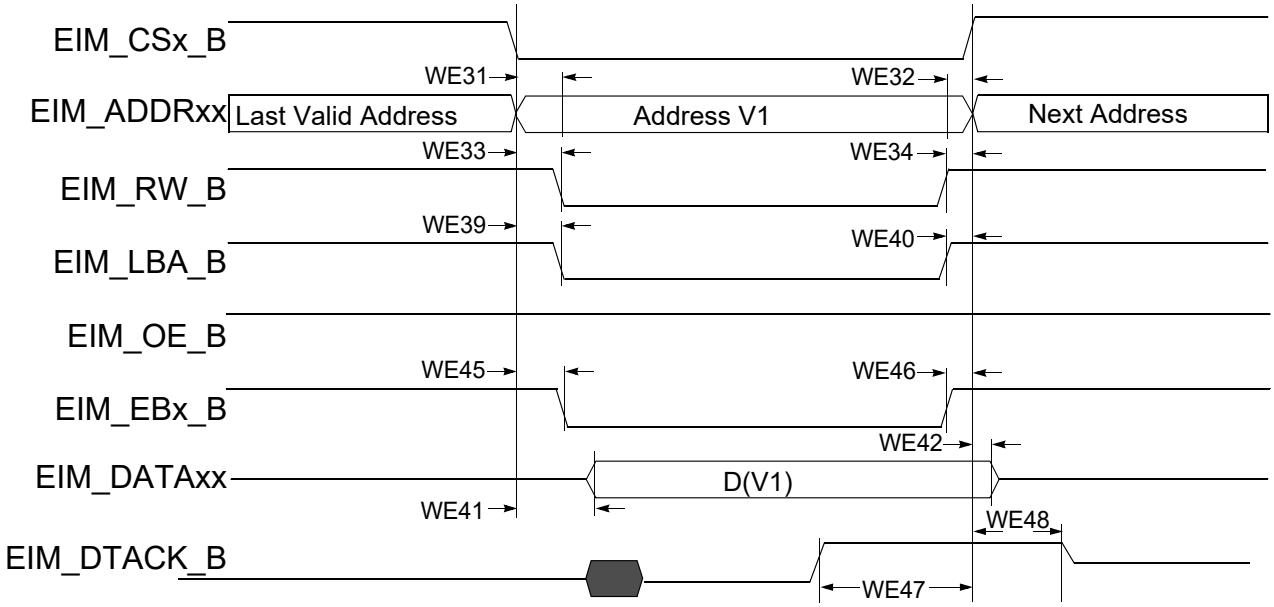

Figure 21. DTACK Write Access (DAP=0)

Table 35. EIM Asynchronous Timing Parameters Table Relative Chip Select

Reference Number	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4-WE6-CSA×t[2]	-3.5-CSA×t	3.5-CSA×t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7-WE5-CSN×t[3]	-3.5-CSN×t	3.5-CSN×t	ns
WE32A (muxed A/D)	EIM_CSx_B valid to Address Invalid	t[4]+WE4-WE7+(ADVN+ADVA+1-CSA[2,5,6])×t	t - 3.5 + (ADVN + ADVA + 1 - CSA)×t	t+3.5+(ADVN+ADVA + 1 - CSA)×t	ns
WE33	EIM_CSx_B Valid to EIM_RW_WE_B Valid	WE8-WE6+(WEA-WCSA)×t	-3.5+(WEA-WCSA)×t	3.5+(WEA-CSA)×t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7-WE9+(WEN-WCSN)×t	-3.5+(WEN-WCSN)×t	3.5-(WEN-WCSN)×t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10-WE6+(OEA-RCSA)×t	-3.5+(OEA-RCSA)×t	3.5+(OEA-RCSA)×t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10-WE6+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	-3.5 + (OEA + RADVN+RADVA+ADH+1-RCSA)×t	3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7-WE11+(OEN-RCSN)×t	-3.5+(OEN-RCSN)×t	3.5+(OEN-RCSN)×t	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12-WE6+(RBEA-RCSA)×t	-3.5+(RBEA- RCSA)×t	3.5+(RBEA[7]-RCSA)×t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7-WE13+(RBEN-RCSN)×t	-3.5+(RBEN-RCSN)×t	3.5+(RBEN-RCSN)×t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14-WE6+(ADVA-CSA)×t	-3.5+(ADVA-CSA)×t	3.5+(ADVA-CSA)×t	ns
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7-WE15-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14-WE6+(ADVN+ADVA+1-CSA)×t	-3.5+(ADVN+ADVA+1-CSA)×t	3.5+(ADVN+ADVA+1-CSA)×t	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16-WE6-WCSA×t	-3.5-WCSA×t	3.5-WCSA×t	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16-WE6+(WADVN+WADVA+ADH+1-WCSA)×t	-3.5+(WADVN+WADVA+ADH+1-WCSA)×t	3.5+(WADVN+WADVA+ADH+1-WCSA)×t	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17-WE7-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns

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Table 35. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Reference Number	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs.	10	—	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out.	10	—	10	ns
MAXDI	EIM_DATAxx MAXIMUM delay from chip input data to its internal flip-flop	5	—	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDI	MAXCO-MAXCSO+MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12-WE6+(WBEA-WCSA)×t	-3.5+(WBEA-WCSA)×t	3.5+(WBEA-WCSA)×t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7-WE13+(WBEN-WCSN)×t	-3.5+(WBEN-WCSN)×t	3.5+(WBEN-WCSN)×t	ns
MAXDTI	Maximum delay from EIM_DTACK_B input to its internal flip-flop + 2 cycles for synchronization	10	—	10	ns
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDTI	MAXCO-MAXCSO+MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6SoloLite reference manual.

2 CSA means register setting for WCSA when in write operations or RCSA when in read operations.

3 CSN means register setting for WCSN when in write operations or RCSN when in read operations.

4 t means clock period from axi_clk frequency.

5 ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

6 ADVN means register setting for WADVN when in write operations or RADVN when in read operations.

7 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

4.9.4 Multi-Mode DDR Controller (MMDC)

The Multi-mode DDR Controller is a dedicated interface to DDR3/LPDDR2 SDRAM.

4.9.4.1 MMDC Compatibility with JEDEC-Compliant SDRAMs

The i.MX 6SoloLite MMDC is compatible with the following JEDEC-compliant memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3 SDRAM compliant to JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for i.MX 6SoloLite Applications Processors* (IMXSLHDG).

4.9.4.2 MMDC Supported DDR3/LPDDR2 Configurations

Table 36 shows the supported DDR3/LPDDR2 configurations.

Table 36. i.MX 6SoloLite Supported DDR3/LPDDR2 Configurations

Parameter	LPDDR2	DDR3
Clock frequency	400 MHz	400 MHz
Bus width	16-/32-bit	16-/32-bit
Channel	Single	Single
Chip selects	2	2

4.10 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.10.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.10.2 CMOS Sensor Interface (CSI) Timing Parameters

4.10.2.0.1 Gated Clock Mode Timing

Figure 22 and Figure 23 shows the gated clock mode timings for CSI, and Table 37 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

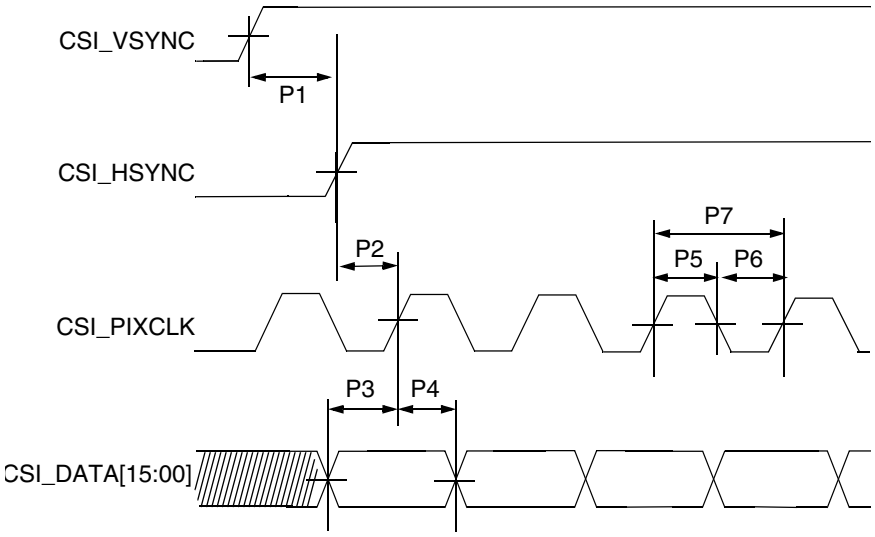

Figure 22. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

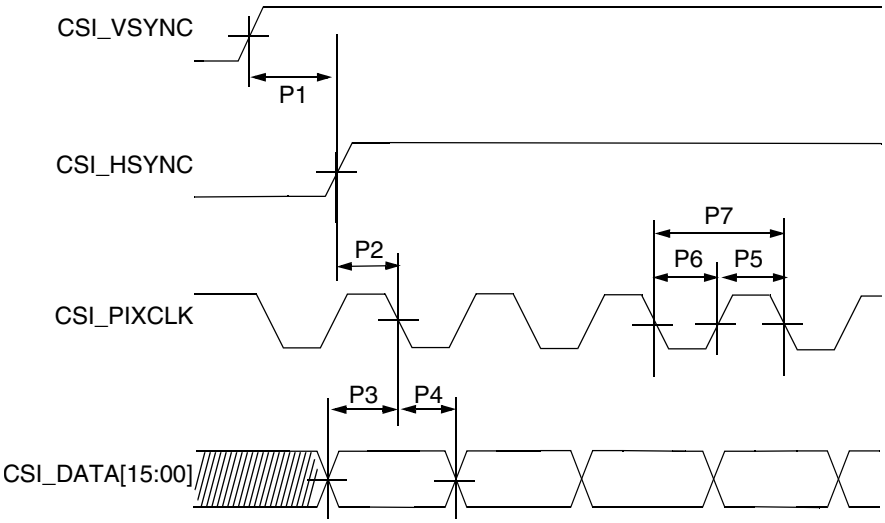

Figure 23. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 37. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	67.5	—	ns
P2	CSI_HSYNC setup time	tHsu	2	—	ns
P3	CSI DATA setup time	tDsu	2.5	—	ns

Table 37. CSI Gated Clock Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Units
P4	CSI DATA hold time	tDh	1.2	—	ns
P5	CSI pixel clock high time	tCLKh	7.5	—	ns
P6	CSI pixel clock low time	tCLKl	7.5	—	ns
P7	CSI pixel clock frequency	fCLK	—	66	MHz

4.10.2.0.2 Ungated Clock Mode Timing

Figure 24 shows the ungated clock mode timings of CSI, and Table 38 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

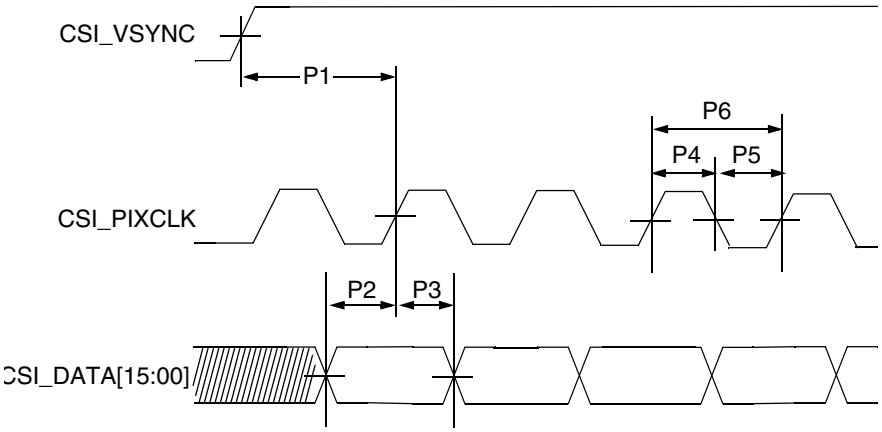

Figure 24. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 38. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	67.5	—	ns
P2	CSI DATA setup time	tDsu	2.5	—	ns
P3	CSI DATA hold time	tDh	1.2	—	ns
P4	CSI pixel clock high time	tCLKh	7.5	—	ns
P5	CSI pixel clock low time	tCLKl	7.5	—	ns
P6	CSI pixel clock frequency	fCLK	—	66	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

4.10.3 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI block. The ECSPI has separate timing parameters for master and slave modes.

4.10.3.1 ECSPI Master Mode Timing

Figure 25 depicts the timing of ECSPI in master mode and Table 39 lists the ECSPI master mode timing characteristics.

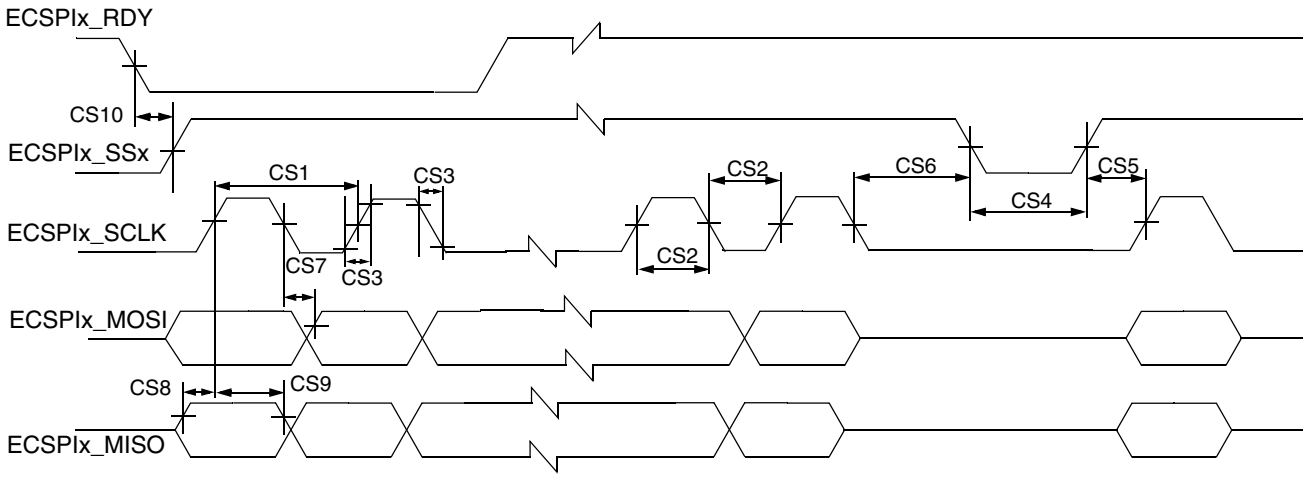

Figure 25. ECSPI Master Mode Timing Diagram

NOTE

ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Table 39. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 46 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 22 20 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[3]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns

Table 39. ECSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	Half ECSPI_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-0.5	2	ns
CS8	ECSPIx_MISO Setup Time • Slow group[1] • Fast group[2]	t_{Smiso}	— 14 12	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	ECSPIx_RDY to ECSPIx_SSx Time[4]	t_{SDRY}	5	—	ns

1 ECSPI slow group includes:
ECSPI2/EPDC_SDLE, ECSPI3/EPDC_D9, ECSPI4/EPDC_D1

2 ECSPI fast group includes:
ECSPI1/LCD_DATA01, ECSPI1/ECSPI1_MISO, ECSPI2/LCD_DATA10, ECSPI2/ECSPI2_MISO, ECSPI3/AUDx_TXC, ECSPI3/SD2_DAT1, ECSPI4/KEY_ROW1, ECSPI4/FEC_RX_DV

3 See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

4 ECSPIx_RDY is sampled internally by ipg_clk and is asynchronous to all other eCSPI signals.

4.10.3.2 ECSPI Slave Mode Timing

Figure 26 depicts the timing of ECSPI in slave mode and Table 40 lists the ECSPI slave mode timing characteristics.

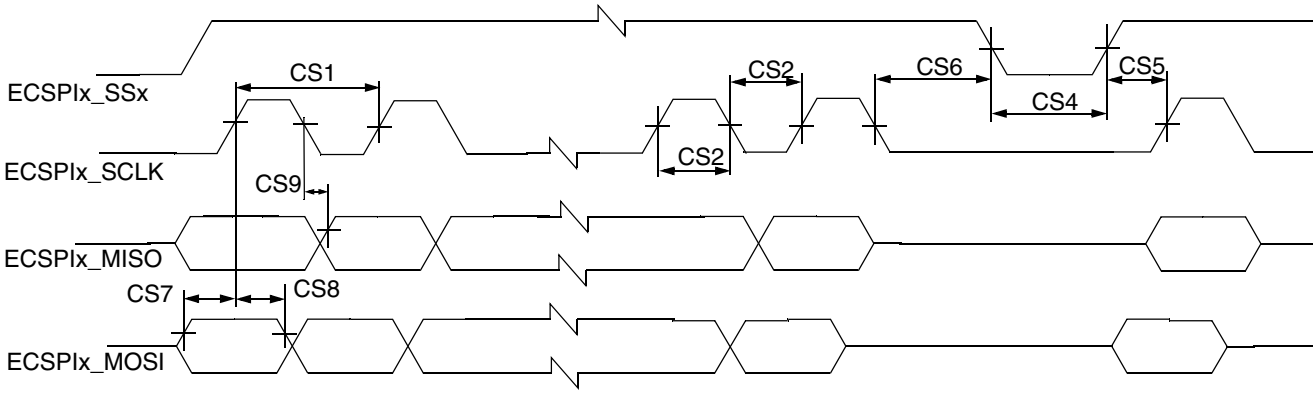

Figure 26. ECSPI Slave Mode Timing Diagram

NOTE

ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Table 40. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	20 7	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	17	ns

4.10.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.41 (Dual Date Rate) timing.

4.10.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing Parameters

Figure 27 depicts the timing of SD/eMMC4.3, and Table 41 lists the SD/eMMC4.3 timing characteristics.

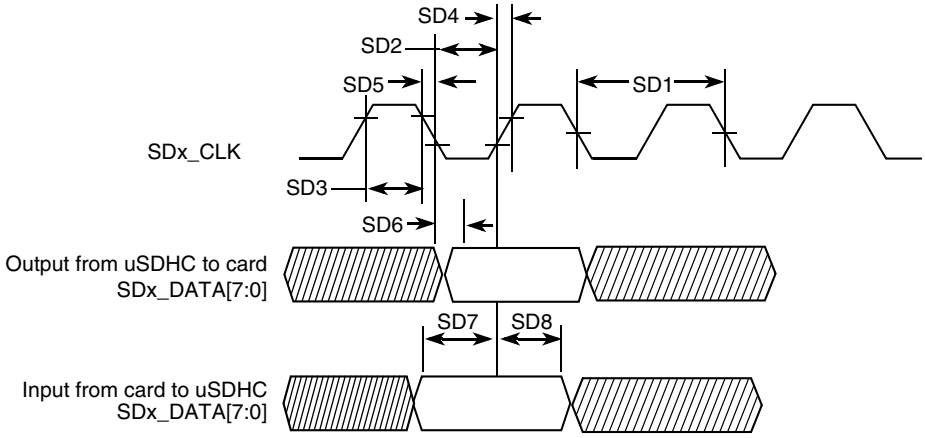

Figure 27. SD/eMMC4.3 Timing Diagram

Table 41. SD/eMMC4.3 Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (Low Speed)	f_{PP}[2]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[3]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[4]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
eSDHC Output/Card Inputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns
eSDHC Input/Card Outputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[5]	t_{IH}	1.5	—	ns

1 Clock duty cycle will be in the range of 47% to 53%.

2 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

3 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

4 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

5 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.10.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing Parameters

Figure 28 depicts the timing of eMMC4.4/4.41. Table 42 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SDx_CMD).

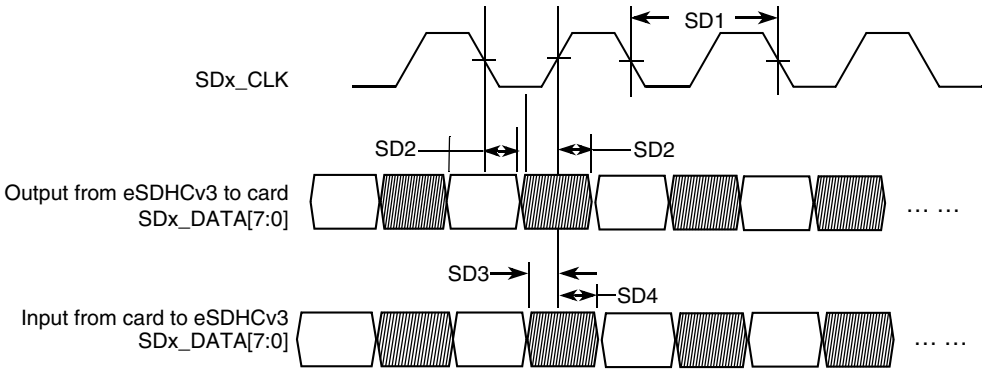

Figure 28. eMMC4.4/4.41 Timing Diagram

Table 42. eMMC4.4/4.41 Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.10.4.3 SDR50/SDR104 AC Timing Parameters

Figure 29 depicts the timing of SDR50/SDR104, and Table 43 lists the SDR50/SDR104 timing characteristics.

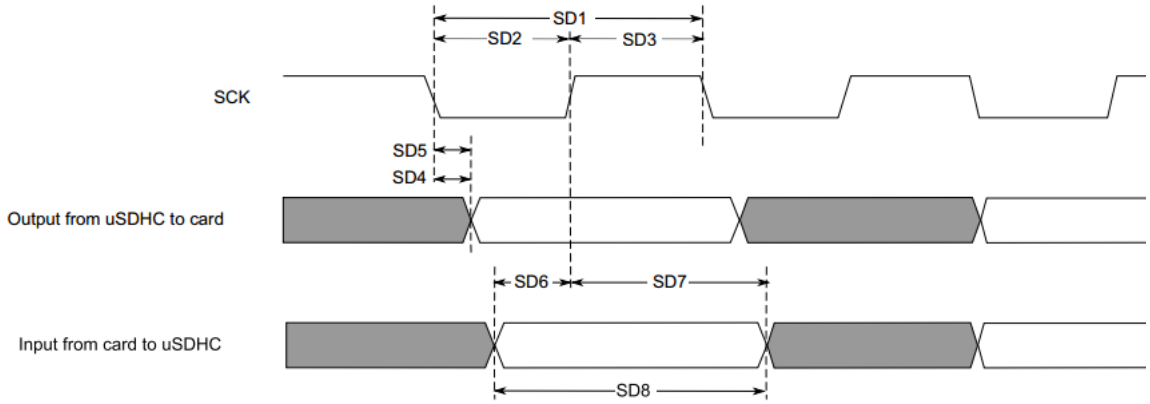

Figure 29. SDR50/SDR104 Timing Diagram

Table 43. SDR50/SDR104 Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SD_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SD_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay[1]	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SD_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SD_DATAx in SDR104 (Reference to CLK)[2]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

1 If using KEY_COL1, KEY_ROW1, KEY_COL2 and KEY_ROW2 for SD3_DATA4–SD3_DATA7, note the difference in timing: t_{od} minimum is -1.1 and t_{od} maximum is 1.5.

2 Data window in SDR100 mode is variable.

4.10.5 HS200 Mode Timing Parameters

Figure 30 depicts the timing of HS200 mode, and Table 44 lists the HS200 timing characteristics.

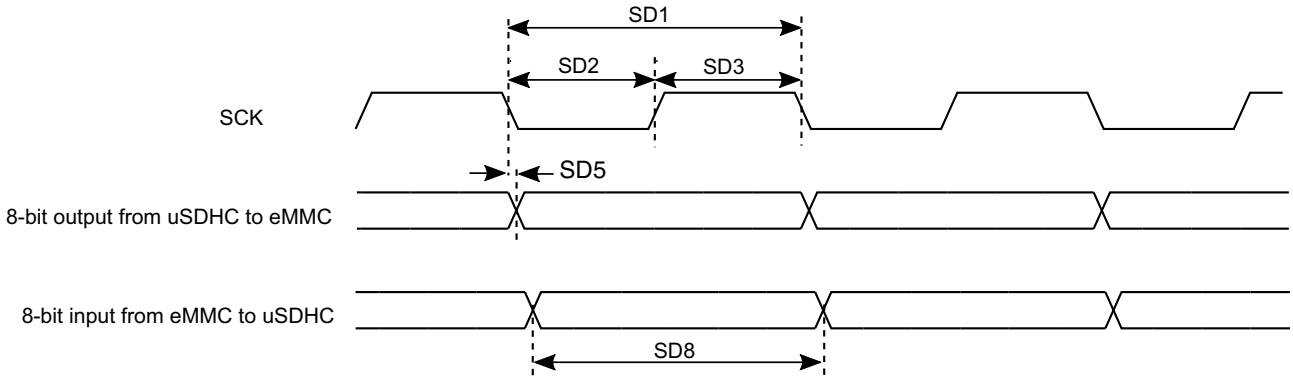

Figure 30. HS200 Mode Timing Diagram

Table 44. HS200 Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay Setup Time	t_{OD}	-1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

1 HS200 is for 8 bits while SDR104 is for 4 bits.

4.10.6 FEC AC Timing Parameters

This section describes the electrical information of the Fast Ethernet Controller (FEC) module. The FEC is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps RMII (10 pins in total) and the 10 Mbps (only 7-wire interface, which uses 7 of the RMII pins), for connection to an external Ethernet transceiver. For the pin list of RMII and 7-wire, see the i.MX 6SoloLite Reference Manual.

This section describes the AC timing specifications of the FEC. The RMII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.10.6.1 RMII Mode Timing Parameters

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz ±50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TX_DATA[1:0], FEC_RX_DATA[1:0] and optional FEC_RX_ER.

The RMII mode timing parameters are shown in Figure 31 and Table 45.

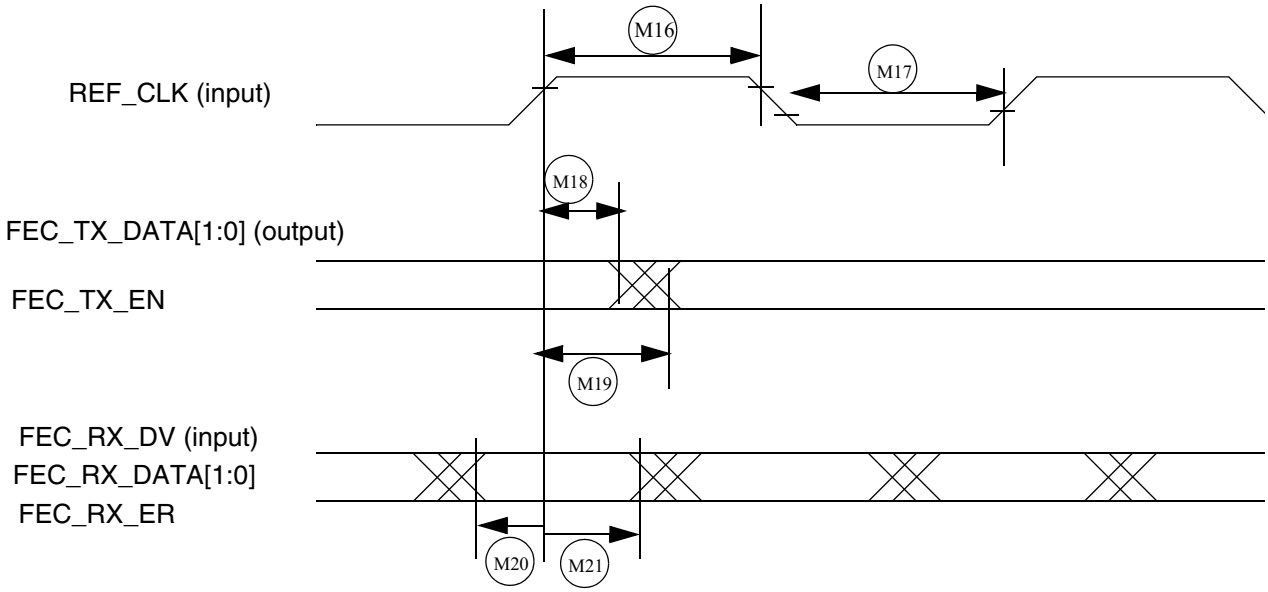

Figure 31. RMII Mode Signal Timing Diagram

Table 45. RMII Signal Timing Parameters

No.	Characteristics[1]	Min	Max	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TX_DATA[1:0], FEC_TX_EN invalid	2	—	ns
M19	REF_CLK to FEC_TX_DATA[1:0], FEC_TX_EN valid	—	16	ns
M20	FEC_RX_DATA[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	4	—	ns
M21	REF_CLK to FEC_RX_DATA[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

[1] Test conditions: 25pF on each output signal.

4.10.7 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 32 depicts the timing of I²C module, and Table 46 lists the I²C module timing characteristics.

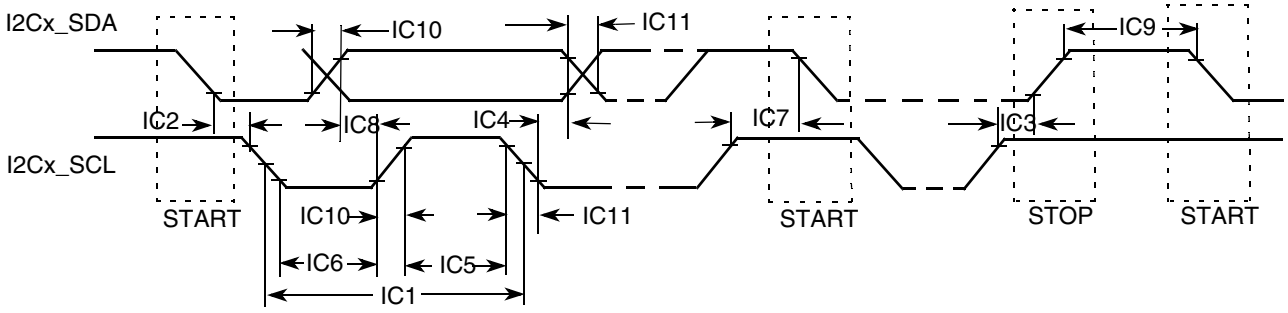

Figure 32. I²C Bus Timing Diagram

Table 46. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal in order to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.10.8 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMx_OUT) external pin (see external signals table in the i.MX 6SoloLite reference manual for PWM pin assignments).

Figure 33 depicts the timing of the PWM, and Table 47 lists the PWM timing parameters.

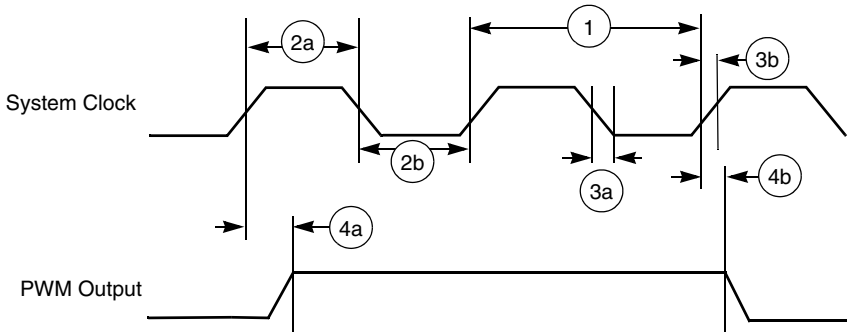

Figure 33. PWM Timing Diagram

Table 47. PWM Output Timing Parameters

Reference Number	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns

[1] CL of PWMx_OUT = 30 pF

4.10.9 SCAN JTAG Controller (SJC) Timing Parameters

Figure 34 depicts the SJC test clock input timing. Figure 35 depicts the SJC boundary scan timing. Figure 36 depicts the SJC test access port. Signal parameters are listed in Table 48.

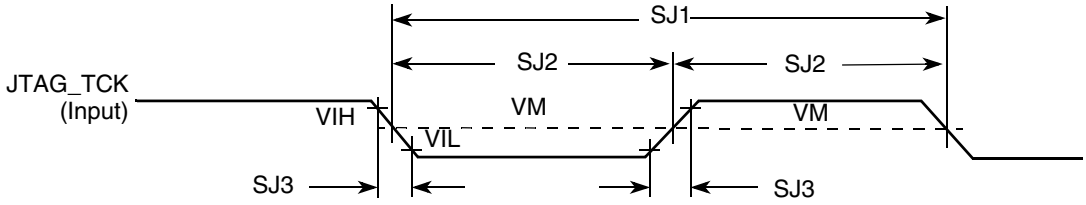

Figure 34. Test Clock Input Timing Diagram

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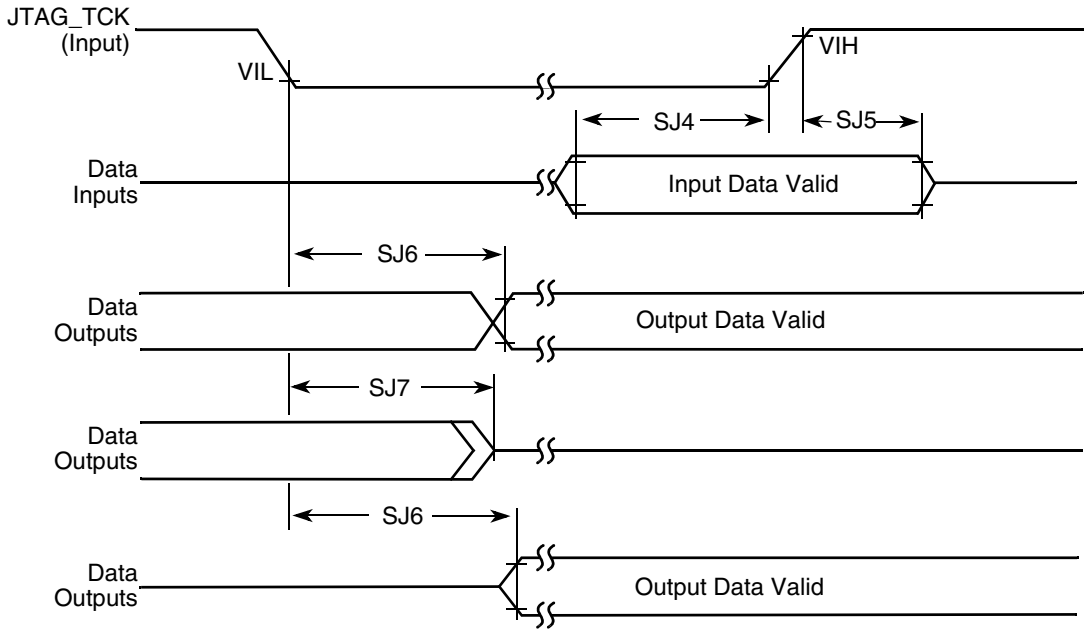

Figure 35. Boundary Scan (JTAG) Timing Diagram

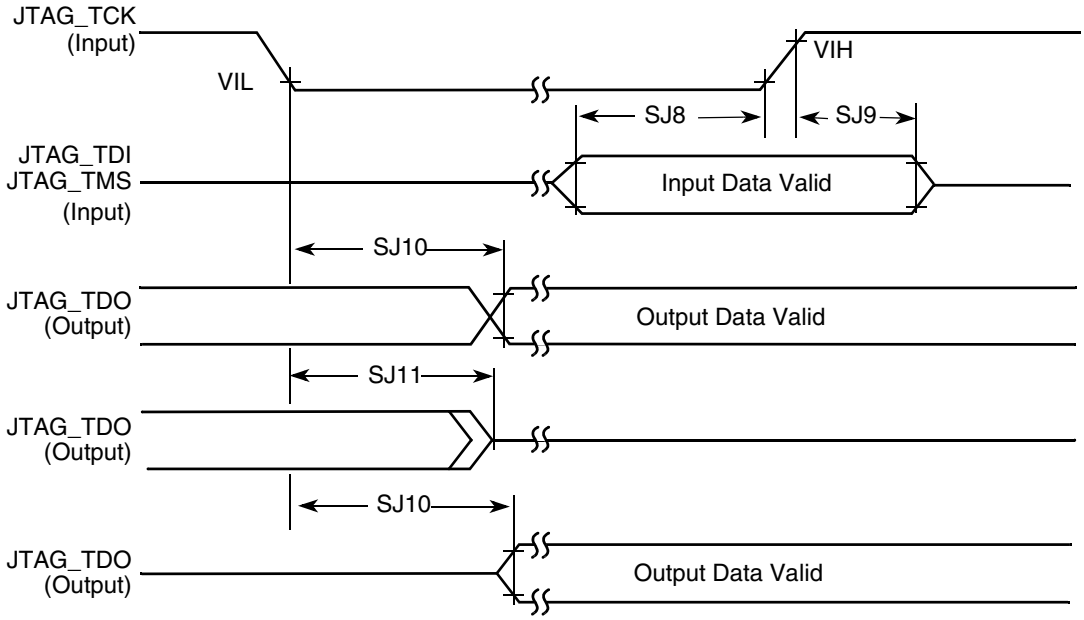

Figure 36. Test Access Port Timing Diagram

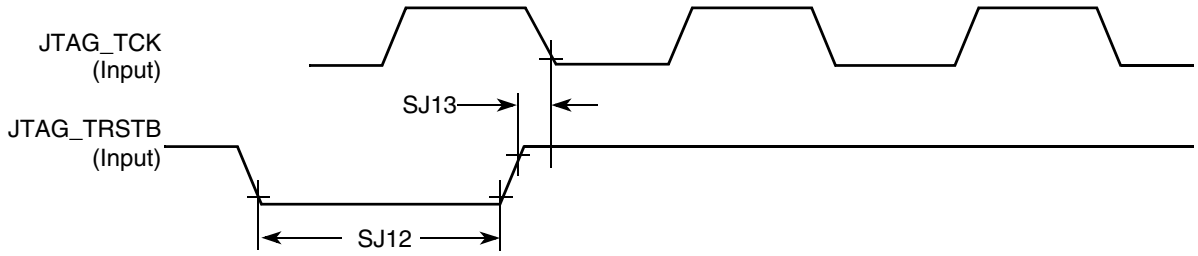

Figure 37. $\overline{\text{TRST}}$ Timing Diagram

Table 48. JTAG Timing Parameters

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRSTB assert time	100	—	ns
SJ13	JTAG_TRSTB set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.10.10 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 49, Figure 38, and Figure 39 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

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Table 49. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

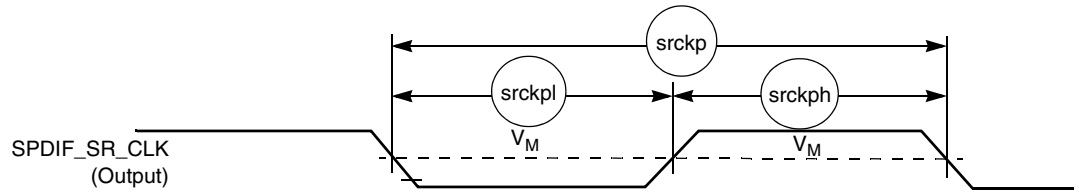

Figure 38. SRCK Timing Diagram

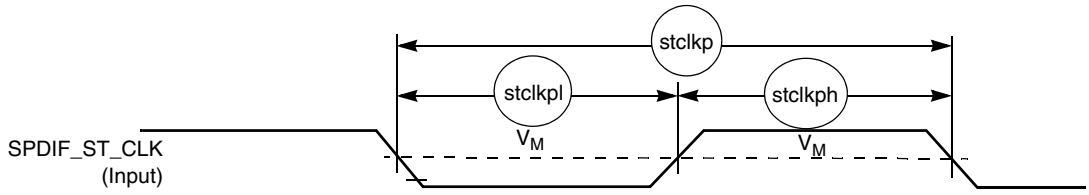

Figure 39. STCLK Timing Diagram

4.10.11 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 50.

Table 50. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – I2C2 and LCD, or ECSPI1, or SD2 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EPDC or SD3 I/O through IOMUXC
AUDMUX port 6	AUD6	External – FEC or KEY_ROW and KEY_COL through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

4.10.11.1 SSI Transmitter Timing with Internal Clock

Figure 40 depicts the SSI transmitter internal clock timing and Table 51 lists the timing parameters for the SSI transmitter internal clock.

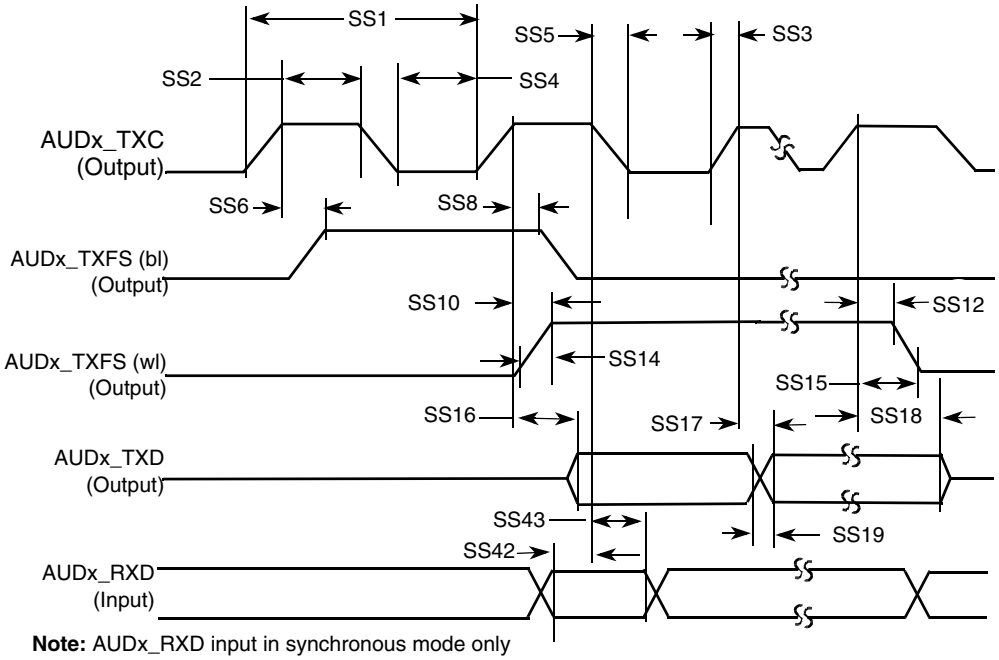

Figure 40. SSI Transmitter Internal Clock Timing Diagram

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Table 51. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.11.2 SSI Receiver Timing with Internal Clock

Figure 41 depicts the SSI receiver internal clock timing and Table 52 lists the timing parameters for the receiver timing with the internal clock.

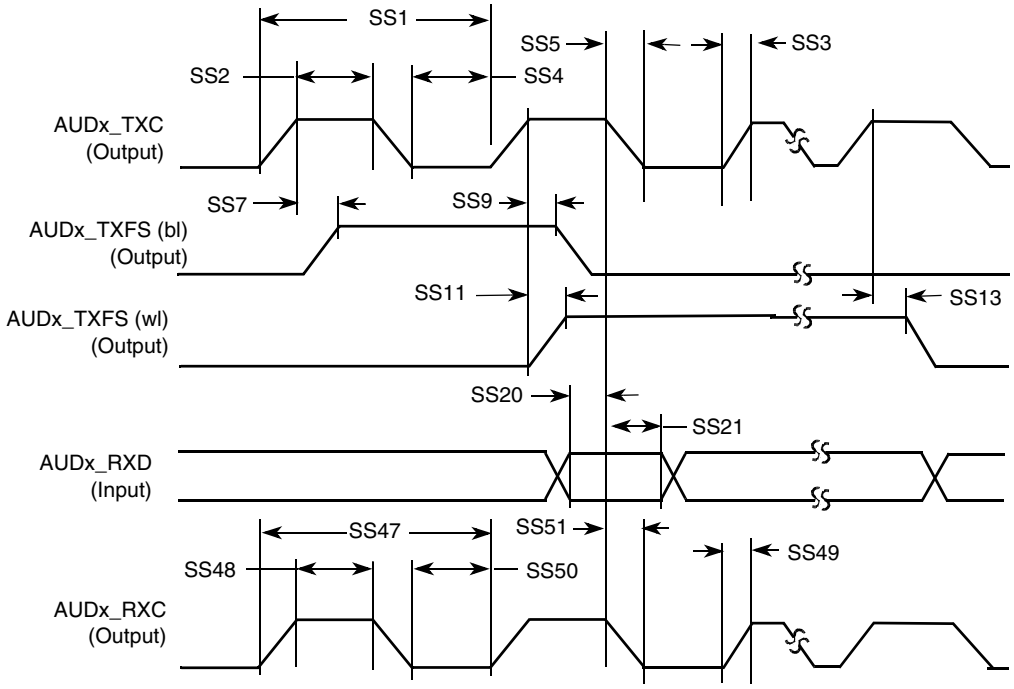

Figure 41. SSI Receiver Internal Clock Timing Diagram

Table 52. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

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Table 52. SSI Receiver with Internal Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.11.3 SSI Transmitter Timing with External Clock

Figure 42 depicts the SSI transmitter external clock timing and Table 53 lists the timing parameters for the transmitter timing with the external clock.

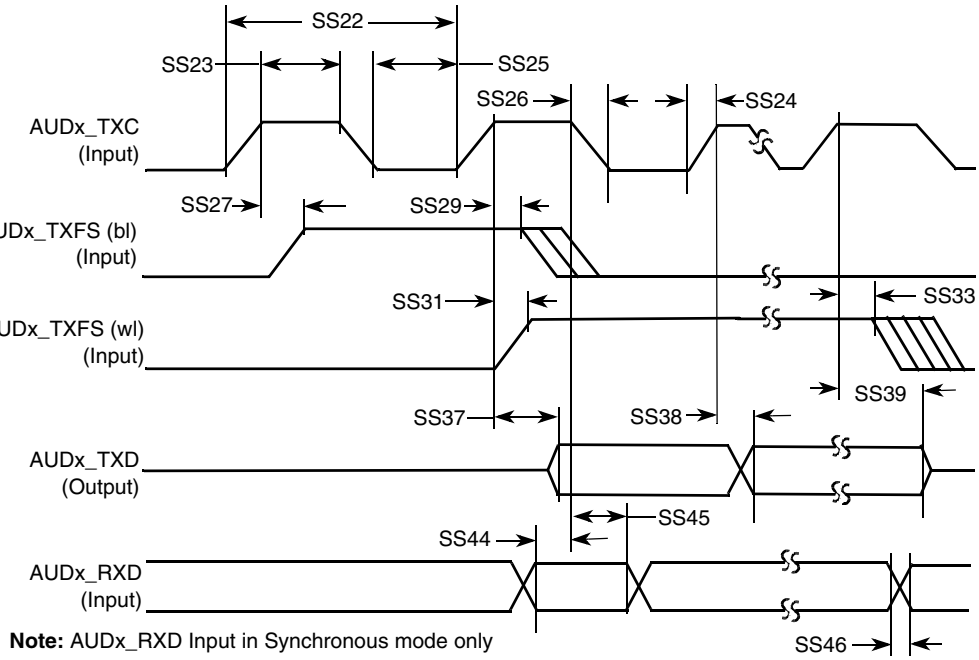

Figure 42. SSI Transmitter External Clock Timing Diagram

Table 53. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	–10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	–10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

Table 53. SSI Transmitter with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on AUDMUX Pads when SSI is used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.11.4 SSI Receiver Timing with External Clock

Figure 43 depicts the SSI receiver external clock timing and Table 54 lists the timing parameters for the receiver timing with the external clock.

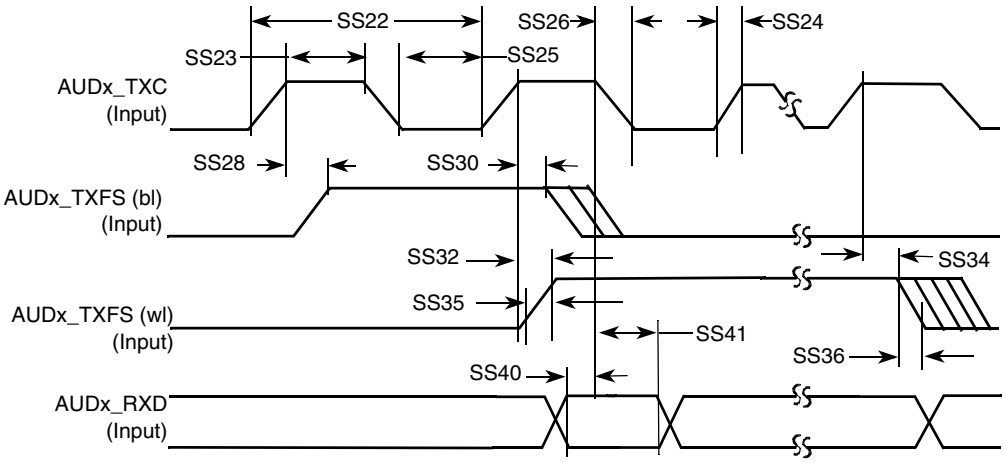

Figure 43. SSI Receiver External Clock Timing Diagram

Table 54. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	–10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	—	ns
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	–10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC=0) and a non-inverted frame sync (TXFS/RXFS=0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on AUDMUX Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.12 UART I/O Configuration and Timing Parameters

4.10.12.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6SoloLite UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 55 shows the UART I/O configuration based on the enabled mode.

Table 55. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UART_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UART_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UART_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UART_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UART_DCD_B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UART_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UART_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UART_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.10.12.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.10.12.2.1 UART Transmitter

Figure 44 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 56 lists the UART RS-232 serial mode transmit timing characteristics.

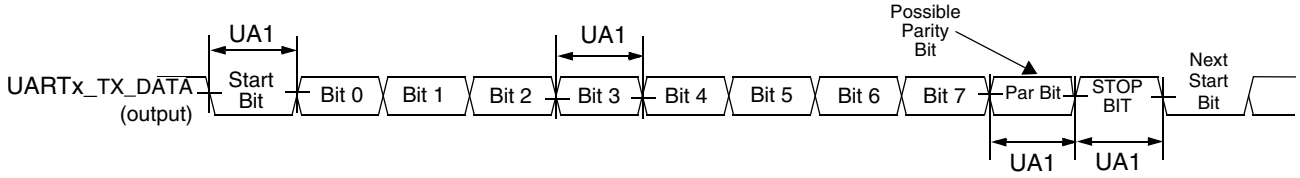

Figure 44. UART RS-232 Serial Mode Transmit Timing Diagram

Table 56. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud_rate} + T_{ref_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.10.12.2.2 UART Receiver

Figure 45 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 57 lists serial mode receive timing characteristics.

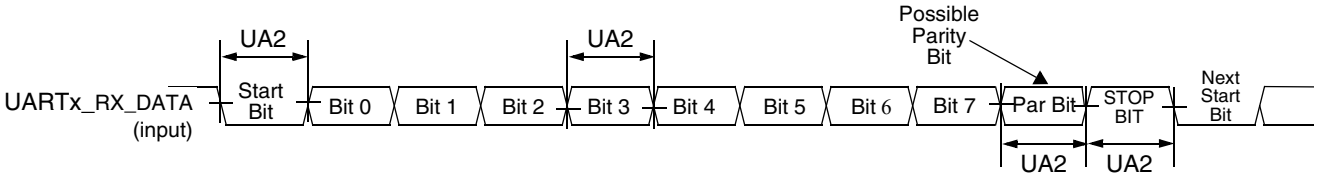

Figure 45. UART RS-232 Serial Mode Receive Timing Diagram

Table 57. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud_rate}$[2] – $1/(16 \times F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.12.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 46 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 58 lists the transmit timing characteristics.

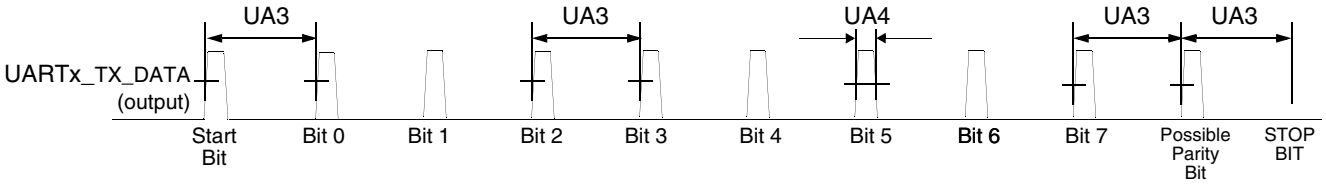

Figure 46. UART IrDA Mode Transmit Timing Diagram

Table 58. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud_rate} + T_{ref_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud_rate}) - T_{ref_clk}$	$(3/16) \times (1/F_{baud_rate}) + T_{ref_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 47 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 59 lists the receive timing characteristics.

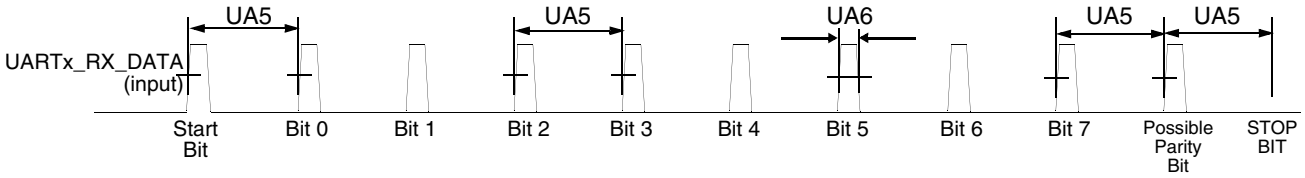

Figure 47. UART IrDA Mode Receive Timing Diagram

Table 59. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud_rate}$[2] – $1/(16 \times F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.13 USB HSIC Timing Parameters

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is the DDR signal, the following timing parameters are for both rising and falling edge.

4.10.13.1 Transmit Timing Parameters

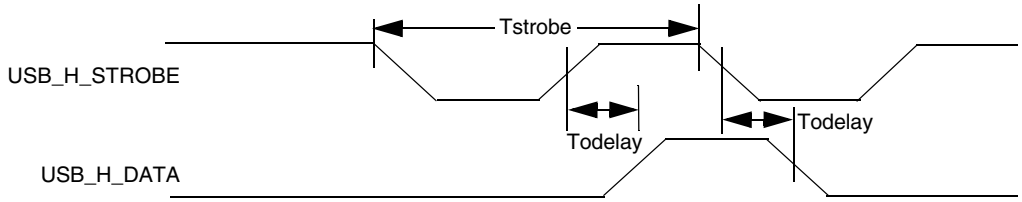

Figure 48. USB HSIC Transmit Timing Diagram

Table 60. USB HSIC Transmit Timing Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	Strobe period	4.166	4.167	ns	—
Todelay	Data output delay time	550	1350	ps	Measured at 50% point
Tslew	Strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

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4.10.13.2 Receive Timing Parameters

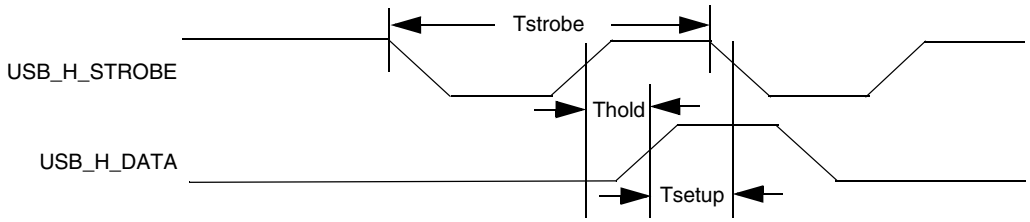

Figure 49. USB HSIC Receive Timing Diagram

Table 61. USB HSIC Receive Timing Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	Strobe period	4.166	4.167	ns	—
Thold	Data hold time	300	—	ps	Measured at 50% point
Tsetup	Data setup time	365	—	ps	Measured at 50% point
Tslew	Strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.10.14 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.
The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 62 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6SoloLite Fuse Map document and the System Boot chapter of the i.MX 6SoloLite reference manual.

Table 62. Fuses and Associated Pins Used for Boot

Ball Name	Direction at Reset	eFuse Name
Boot Mode Selection		
BOOT_MODE1	Input	Boot Mode Selection
BOOT_MODE0	Input	Boot Mode Selection
Boot Options[1]		
LCD_DAT0	Input	BOOT_CFG1[0]
LCD_DAT1	Input	BOOT_CFG1[1]
LCD_DAT2	Input	BOOT_CFG1[2]
LCD_DAT3	Input	BOOT_CFG1[3]
LCD_DAT4	Input	BOOT_CFG1[4]
LCD_DAT5	Input	BOOT_CFG1[5]
LCD_DAT6	Input	BOOT_CFG1[6]
LCD_DAT7	Input	BOOT_CFG1[7]
LCD_DAT8	Input	BOOT_CFG2[0]
LCD_DAT9	Input	BOOT_CFG2[1]
LCD_DAT10	Input	BOOT_CFG2[2]
LCD_DAT11	Input	BOOT_CFG2[3]
LCD_DAT12	Input	BOOT_CFG2[4]
LCD_DAT13	Input	BOOT_CFG2[5]
LCD_DAT14	Input	BOOT_CFG2[6]
LCD_DAT15	Input	BOOT_CFG2[7]
LCD_DAT16	Input	BOOT_CFG4[0]
LCD_DAT17	Input	BOOT_CFG4[1]
LCD_DAT18	Input	BOOT_CFG4[2]

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 62. Fuses and Associated Pins Used for Boot (continued)

Ball Name	Direction at Reset	eFuse Name
LCD_DAT19	Input	BOOT_CFG4[3]
LCD_DAT20	Input	BOOT_CFG4[4]
LCD_DAT21	Input	BOOT_CFG4[5]
LCD_DAT22	Input	BOOT_CFG4[6]
LCD_DAT23	Input	BOOT_CFG4[7]

1 Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 63 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 63. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Ball Names During Boot	Comment
SPI	ECSPI-1	ECSPI1_MISO, ECSPI1_MOSI, ECSPI1_SCLK, ECSPI1_SS0, I2C1_SCL, I2C1_SDA, ECSPI2_SS0	—
SPI	ECSPI-2	ECSPI2_MISO, ECSPI2_MOSI, ECSPI2_SCLK, ECSPI2_SS0, EPDC_SDCE0, EPDC_GDCLK, EPDC_GDOE	—
SPI	ECSPI-3	EPDC_D9, EPDC_D8, EPDC_D11, EPDC_D10, EPDC_D12, EPDC_D13, EPDC_D14	—
SPI	ECSPI-4	EPDC_D1, EPDC_D0, EPDC_D3, EPDC_D2, EPDC_D2, EPDC_D5, EPDC_D6	—
EIM	EIM	LCD_DAT[21:6], KEY_COL[7:0], KEY_ROW[7:0], EPDC_D[15:8], EPDC_VCOM0, EPDC_VCOM1, EPDC_BDR0, EPDC_PWRCTRL[2:0], EPDC_SDCE1	—
SD/MMC	USDHC-1	Refer to the table "SD/MMC IOMUX Pin Configuration" in the System Boot Chapter of the **i.MX 6SoloLite Applications Processor Reference Manual**	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-2	Refer to the table "SD/MMC IOMUX Pin Configuration" in the System Boot Chapter of the **i.MX 6SoloLite Applications Processor Reference Manual**	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-3	Refer to the table "SD/MMC IOMUX Pin Configuration" in the System Boot Chapter of the **i.MX 6SoloLite Applications Processor Reference Manual**	1, 4, or 8 bit Fastboot (UHSI not supported)
SD/MMC	USDHC-4	Refer to the table "SD/MMC IOMUX Pin Configuration" in the System Boot Chapter of the **i.MX 6SoloLite Applications Processor Reference Manual**	1, 4, or 8 bit Fastboot
I2C	I2C-1	I2C1_SCL, I2C1_SDA	—

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 63. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Ball Names During Boot	Comment
I2C	I2C-2	I2C2_SCL, I2C2_SDA	—
I2C	I2C-3	AUD_RXFS, AUD_RXC	—
USB	USB_OTG1_PHY	USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS USB_OTG1_CHD_B USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS	—

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 Updated Signal Naming Convention

The signal names of the i.MX6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

6.2 13 x 13mm Package Information

6.2.1 Case 2240, 13 x 13 mm, 0.5 mm Pitch, 24 x 24 Ball Matrix

Figure 50 shows the top, bottom, and side views of the 13×13 mm BGA package.

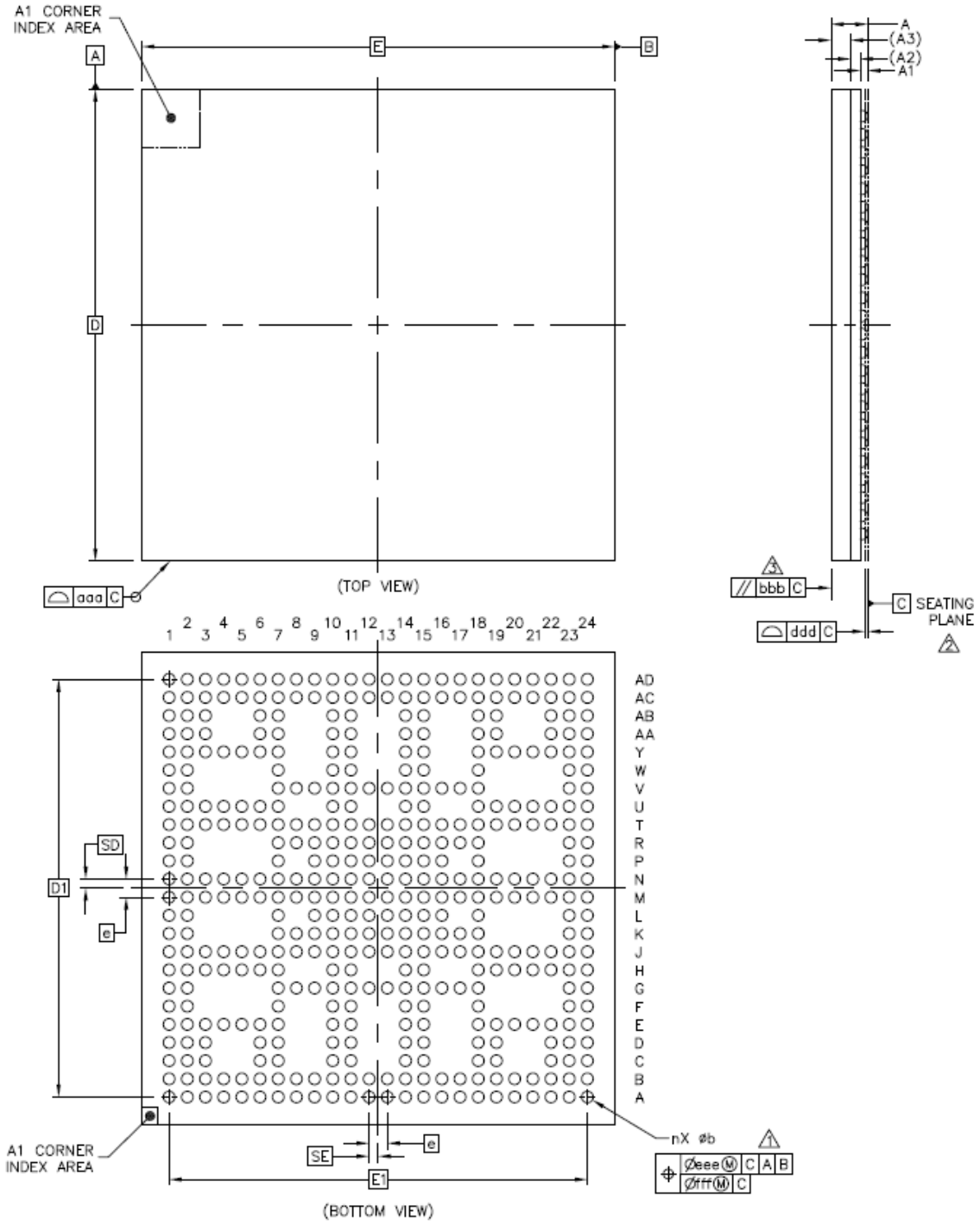

Figure 50. 13 x 13, 0.5 mm BGA Package Top, Bottom, and Side Views

Table 64 shows the 13 x 13 mm BGA package details.

Table 64. 13 x 13, 0.5 mm BGA Package Details

Parameter	Symbol	Common Dimensions		
		Minimum	Normal	Maximum
Total Thickness	A	0.88	—	1.1
Stand Off	A1	0.16	—	0.26
Substrate Thickness	A2	0.26 REF		
Mold Thickness	A3	0.54 REF		
Body Size	D	13 BSC		
	E	13 BSC		
Ball Diameter	—	0.3		
Ball Opening	—	0.275		
Ball Width	b	0.27	—	0.37
Ball Pitch	e	0.5 BSC		
Ball Count	n	432	—	—
Edge Ball Center to Center	D1	11.5 BSC		
	E1	11.5 BSC		
Body Center to Contact Ball	SD	0.25 BSC		
	SE	0.25 BSC		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.1		
Coplanarity	ddd	0.08		
Ball Offset (Package)	eee	0.15		
Ball Offset (Ball)	fff	0.05		

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

6.2.2 13 x 13 mm Ground, Power, Sense, Not Connected, and Reference Contact Assignments

Table 65 shows the device connection list for ground, power, sense, and reference contact signals.

Table 65. 13 x 13 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
DRAM_VREF	N5	—
GND	A1, A4, A7, A24, C6, C10, C14, C19, D1, D2, E5, G1, G8, G9, G10, G11, G13, G14, G15, G17, G18, H3, H7, H18, H22, J5, K1, L7, L9, L10, L11, L12, L13, L14, L15, L16, M5, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, N3, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, N22, P9, P10, P11, P12, P13, P14, P15, P16, R1, T5, U3, U7, U18, U22, V1, V8, V9, V10, V11, V12, V13, V14, V15, V16, V18, Y5, AA1, AA2, AB10, AB14, AB18, AC18, AD1, AD4, AD7, AD24	—
GND_KELVIN	V17	Must be connected
GPANAIO	AD22	Analog output for NXP use only. This output must remain unconnected.
NVCC_1P2V	W7	—
NVCC18_IO	E14, E15, M20, Y11	—
NVCC33_IO	H10, H11, H14, H15, L18, M18, T19, U10, U11	—
NVCC_DRAM	E6, Y6, G7, H6, J6, N6, P7, T6, U6, V7	Supply of the DDR Interface
NVCC_DRAM_2P5	M6	—
NVCC_PLL	Y19	—
VDD_ARM_CAP	J15, J16, J17, J18, K15, K16, K17, K18	Secondary Supply for the ARM0 and ARM1 Cores (internal regulator output—requires capacitor if internal regulator is used)
VDD_ARM_IN	J12, J13, J14, K12, K13, K14	Primary Supply, for the ARM0 and ARM1 Core' Regulator
VDD_HIGH_CAP	R14, R15, T14, T15	Secondary Supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDD_HIGH_IN	R12, R13, T12, T13	Primary Supply for the 2.5 V Regulator
VDD_PU_CAP	R7, R8, R9, T7, T8, T9	Secondary Supply for the VPU and GPU's (internal regulator output—requires capacitor if internal regulator is used)
VDD_PU_IN	R10, R11, T10, T11	—
VDD_SNVS_CAP	AD20	Secondary Supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)

Table 65. 13 x 13 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDD_SNVS_IN	AC20	Primary Supply, for the SNVS Regulator
VDD_SOC_CAP	J7, J8, J9, K7, K8, K9, N18, P18, R18	Secondary Supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDD_SOC_IN	J10, J11, K10, K11, R16, R17, T16, T17, T18	Primary Supply, for the SoC and PU Regulators
VDD_USB_CAP	U14	Secondary Supply for the 3V Domain (USBPHY, MLPBPHY, eFuse), internal regulator output, requires capacitor if internal regulator is used.
USB_OTG1_VBUS	AA18	—
USB_OTG2_VBUS	AD18	—
ZQPAD	H2	Connect ZQPAD to an external 240 ohm 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.
NC	C4, C5, C8, C9, C12, C13, C16, C17, C20, C21, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, E8, E9, E12, E13, E16, E17, F3, F4, F5, F6, F8, F9, F12, F13, F16, F17, F19, F20, F21, F22, G3, G4, G5, G6, G19, G20, G21, G22, H8, H9, H12, H13, H16, H17, K3, K4, K5, K6, K19, K20, K21, K22, L3, L4, L5, L6, L8, L17, L19, L20, L21, L22, P3, P4, P5, P6, P8, P17, P19, P20, P21, P22, R3, R4, R5, R6, R19, R20, R21, R22, U8, U9, U12, U13, U16, U17, V3, V4, V5, V6, V19, V20, V21, V22, W3, W4, W5, W6, W8, W9, W12, W13, W16, W17, W19, W20, W21, W22, Y8, Y9, Y12, Y13, Y16, Y17, AA4, AA5, AA8, AA9, AA12, AA13, AA16, AA17, AA20, AA21, AB4, AB5, AB8, AB9, AB12, AB13, AB16, AB17 AB20, AB21	No Connections.

Table 66 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 66. 13 x 13 mm Functional Contact Assignments

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
AUD_MCLK	H19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[6]	Input	Keeper
AUD_RXC	J21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[1]	Input	Keeper
AUD_RXD	J20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[2]	Input	Keeper

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
AUD_RXFS	J19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[0]	Input	Keeper
AUD_TXC	H20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[3]	Input	Keeper
AUD_TXD	J22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[5]	Input	Keeper
AUD_TXFS	H21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[4]	Input	Keeper
BOOT_MODE0	AC15	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	Keeper
BOOT_MODE1	AB15	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	Keeper
CLK1_N	AD23	VDDHIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	AC23	VDDHIGH_CAP	—	—	CLK1_P	—	—
DRAM_A0	U4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	0
DRAM_A1	U5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	0
DRAM_A10	J2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	0
DRAM_A11	T2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	0
DRAM_A12	U2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	0
DRAM_A13	H5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	0
DRAM_A14	R2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	0
DRAM_A15	K2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	0
DRAM_A2	T3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	0
DRAM_A3	T4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	0
DRAM_A4	N4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	0
DRAM_A5	M3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	0
DRAM_A6	M4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	0
DRAM_A7	H4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	0
DRAM_A8	J3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	0
DRAM_A9	J4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	0
DRAM_CAS_B	P1	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	0
DRAM_CS0_B	N2	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	0
DRAM_CS1_B	L2	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	0
DRAM_D0	AC2	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	PU (100K)
DRAM_D1	AC1	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	PU (100K)
DRAM_D10	E3	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	PU (100K)
DRAM_D11	D3	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	PU (100K)
DRAM_D12	C1	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	PU (100K)
DRAM_D13	C2	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	PU (100K)
DRAM_D14	B1	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	PU (100K)
DRAM_D15	B2	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	PU (100K)
DRAM_D16	AD8	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	PU (100K)

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
DRAM_D17	AC7	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	PU (100K)
DRAM_D18	AD6	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	PU (100K)
DRAM_D19	AC6	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	PU (100K)
DRAM_D2	AB2	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	PU (100K)
DRAM_D20	AD5	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	PU (100K)
DRAM_D21	AC5	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	PU (100K)
DRAM_D22	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	PU (100K)
DRAM_D23	AD3	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	PU (100K)
DRAM_D24	A3	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	PU (100K)
DRAM_D25	B4	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	PU (100K)
DRAM_D26	B5	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	PU (100K)
DRAM_D27	A5	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	PU (100K)
DRAM_D28	B6	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	PU (100K)
DRAM_D29	A6	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	PU (100K)
DRAM_D3	AB1	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	PU (100K)
DRAM_D30	B7	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	PU (100K)
DRAM_D31	A8	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	PU (100K)
DRAM_D4	AA3	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	PU (100K)
DRAM_D5	Y3	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	PU (100K)
DRAM_D6	Y1	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	PU (100K)
DRAM_D7	Y2	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	PU (100K)
DRAM_D8	E2	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	PU (100K)
DRAM_D9	E1	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	PU (100K)
DRAM_DQM0	V2	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	0
DRAM_DQM1	G2	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	0
DRAM_DQM2	AB3	NVCC_DRAM	DDR	ALT0	DRAM_DQM2	Output	0
DRAM_DQM3	C3	NVCC_DRAM	DDR	ALT0	DRAM_DQM3	Output	0
DRAM_RAS_B	N1	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	0
DRAM_RESET_B	D6	NVCC_DRAM	DDR	ALT0	DRAM_RESET_B	Output	0
DRAM_SDBA0	J1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	0
DRAM_SDBA1	T1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	0
DRAM_SDBA2	H1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	0
DRAM_SDCKE0	P2	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	0
DRAM_SDCKE1	M2	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	0
DRAM_SDCLK_0	L1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Output	0
DRAM_SDCLK_0_B	M1	NVCC_DRAM	DDRCLK	—	DRAM_SDCLK0_N	—	—
DRAM_SDODT0	Y4	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	0
DRAM_SDODT1	E4	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	0
DRAM_SDQS0	W2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	Hi-Z

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
DRAM_SDQS0_B	W1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS0_N	—	—
DRAM_SDQS1	F1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	Hi-Z
DRAM_SDQS1_B	F2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS1_N	—	—
DRAM_SDQS2	AC3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS2_P	Input	Hi-Z
DRAM_SDQS2_B	AD2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS2_N	—	—
DRAM_SDQS3	B3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS3_P	Input	Hi-Z
DRAM_SDQS3_B	A2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS3_N	—	—
DRAM_SDWE	U1	NVCC_DRAM	DDR	ALT0	DRAM_SDWE	Output	0
ECSPI1_MISO	M19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[10]	Input	Keeper
ECSPI1_MOSI	N20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[9]	Input	Keeper
ECSPI1_SCLK	N19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[8]	Input	Keeper
ECSPI1_SS0	M21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[11]	Input	Keeper
ECSPI2_MISO	T20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[14]	Input	Keeper
ECSPI2_MOSI	U20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[13]	Input	Keeper
ECSPI2_SCLK	U19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[12]	Input	Keeper
ECSPI2_SS0	T21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[15]	Input	Keeper
EPDC_BDR0	C18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[5]	Input	Keeper
EPDC_BDR1	B18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[6]	Input	Keeper
EPDC_D0	A18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[7]	Input	Keeper
EPDC_D1	A17	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[8]	Input	Keeper
EPDC_D10	G16	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[17]	Input	Keeper
EPDC_D11	F14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[18]	Input	Keeper
EPDC_D12	D14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[19]	Input	Keeper
EPDC_D13	B14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[20]	Input	Keeper
EPDC_D14	A14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[21]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
EPDC_D15	A13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[22]	Input	Keeper
EPDC_D2	B17	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[9]	Input	Keeper
EPDC_D3	A16	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[10]	Input	Keeper
EPDC_D4	B16	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[11]	Input	Keeper
EPDC_D5	A15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[12]	Input	Keeper
EPDC_D6	B15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[13]	Input	Keeper
EPDC_D7	C15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[14]	Input	Keeper
EPDC_D8	D15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[15]	Input	Keeper
EPDC_D9	F15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[16]	Input	Keeper
EPDC_GDCLK	A12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[31]	Input	Keeper
EPDC_GDOE	B13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[0]	Input	Keeper
EPDC_GDRL	B12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[1]	Input	Keeper
EPDC_GDSP	A11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[2]	Input	Keeper
EPDC_PWRCOM	B11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[11]	Input	Keeper
EPDC_PWRCTRL0	D11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[7]	Input	Keeper
EPDC_PWRCTRL1	E11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[8]	Input	Keeper
EPDC_PWRCTRL2	F11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[9]	Input	Keeper
EPDC_PWRCTRL3	G12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[10]	Input	Keeper
EPDC_PWRINT	F10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[12]	Input	Keeper
EPDC_PWRSTAT	E10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[13]	Input	Keeper
EPDC_PWRWAKEUP	D10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[14]	Input	Keeper
EPDC_SDCE0	C11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[27]	Input	Keeper

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
EPDC_SDCE1	A10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[28]	Input	Keeper
EPDC_SDCE2	B9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[29]	Input	Keeper
EPDC_SDCE3	A9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[30]	Input	Keeper
EPDC_SDCLK	B10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[23]	Input	Keeper
EPDC_SDLE	B8	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[24]	Input	Keeper
EPDC_SDOE	E7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[25]	Input	Keeper
EPDC_SDSHR	F7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[26]	Input	Keeper
EPDC_VCOM0	C7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[3]	Input	Keeper
EPDC_VCOM1	D7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[4]	Input	Keeper
FEC_CRS_DV	AC9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[25]	Input	Keeper
FEC_MDC	AA7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[23]	Input	Keeper
FEC_MDIO	AB7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[20]	Input	Keeper
FEC_REF_CLK	W10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[26]	Input	Keeper
FEC_RX_ER	AD9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[19]	Input	Keeper
FEC_RXD0	AA10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[17]	Input	Keeper
FEC_RXD1	AC10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[18]	Input	Keeper
FEC_TX_CLK	AC8	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[21]	Input	Keeper
FEC_TX_EN	AD10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[22]	Input	Keeper
FEC_TXD0	Y10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[24]	Input	Keeper
FEC_TXD1	W11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[16]	Input	Keeper
HSIC_DAT	AA6	NVCC_1P2V	DDR	—	USB_H_DATA	Input	PD (100K)
HSIC_STROBE	AB6	NVCC_1P25	DDR	—	USB_H_STROBE	Input	PD (100K)

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
I2C1_SCL	AC13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[12]	Input	Keeper
I2C1_SDA	AD13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[13]	Input	Keeper
I2C2_SCL	E18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[14]	Input	Keeper
I2C2_SDA	D18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[15]	Input	Keeper
JTAG_MOD	Y14	NVCC33_IO	GPIO	ALT5	JTAG_MODE	—	PU (100K)
JTAG_TCK	AA14	NVCC33_IO	GPIO	ALT5	JTAG_TCK	—	PU (47K)
JTAG_TDI	W14	NVCC33_IO	GPIO	ALT5	JTAG_TDI	—	PU (47K)
JTAG_TDO	W15	NVCC33_IO	GPIO	ALT5	JTAG_TDO	—	Keeper
JTAG_TMS	Y15	NVCC33_IO	GPIO	ALT5	JTAG_TMS	—	PU (47K)
JTAG_TRSTB	AA15	NVCC33_IO	GPIO	ALT5	JTAG_TRSTB	—	PU (47K)
KEY_COL0	G23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[24]	Input	Keeper
KEY_COL1	F23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[26]	Input	Keeper
KEY_COL2	E23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[28]	Input	Keeper
KEY_COL3	E22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[30]	Input	Keeper
KEY_COL4	E20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[0]	Input	Keeper
KEY_COL5	D24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[2]	Input	Keeper
KEY_COL6	D22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[4]	Input	Keeper
KEY_COL7	C23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[6]	Input	Keeper
KEY_ROW0	G24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[25]	Input	Keeper
KEY_ROW1	F24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[27]	Input	Keeper
KEY_ROW2	E24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[29]	Input	Keeper
KEY_ROW3	E21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[31]	Input	Keeper
KEY_ROW4	E19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[1]	Input	Keeper
KEY_ROW5	D23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[3]	Input	Keeper

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
KEY_ROW6	C24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[5]	Input	Keeper
KEY_ROW7	B24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[7]	Input	Keeper
LCD_CLK	T22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[15]	Input	Keeper
LCD_DAT0	Y24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[20]	Input	Keeper
LCD_DAT1	W23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[21]	Input	Keeper
LCD_DAT10	R23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[30]	Input	Keeper
LCD_DAT11	R24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[31]	Input	Keeper
LCD_DAT12	P23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[0]	Input	Keeper
LCD_DAT13	P24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[1]	Input	Keeper
LCD_DAT14	N21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[2]	Input	Keeper
LCD_DAT15	N23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[3]	Input	Keeper
LCD_DAT16	N24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[4]	Input	Keeper
LCD_DAT17	M22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[5]	Input	Keeper
LCD_DAT18	M23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[6]	Input	Keeper
LCD_DAT19	M24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[7]	Input	Keeper
LCD_DAT2	W24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[22]	Input	Keeper
LCD_DAT20	L23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[8]	Input	Keeper
LCD_DAT21	L24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[9]	Input	Keeper
LCD_DAT22	K23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[10]	Input	Keeper
LCD_DAT23	K24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[11]	Input	Keeper
LCD_DAT3	V23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[23]	Input	Keeper
LCD_DAT4	V24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[24]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
LCD_DAT5	U21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[25]	Input	Keeper
LCD_DAT6	U23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[26]	Input	Keeper
LCD_DAT7	U24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[27]	Input	Keeper
LCD_DAT8	T23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[28]	Input	Keeper
LCD_DAT9	T24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[29]	Input	Keeper
LCD_ENABLE	J24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[16]	Input	Keeper
LCD_HSYNC	H23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[17]	Input	Keeper
LCD_RESET	H24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[19]	Input	Keeper
LCD_VSYNC	J23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[18]	Input	Keeper
ONOFF	W18	VDD_SNVS_IN	GPIO		SRC_ONOFF	Input	PU (100K)
PMIC_ON_REQ	AD15	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	AD16	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	0
POR_B	AC16	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	PU (100K)
PWM1	Y7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[23]	Input	Keeper
REF_CLK_24M	AC14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[21]	Input	Keeper
REF_CLK_32K	AD14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[22]	Input	Keeper
RTC_XTALI	AB19	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	AA19	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD1_CLK	B20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[15]	Input	Keeper
SD1_CMD	B21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[14]	Input	Keeper
SD1_DAT0	B23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[11]	Input	Keeper
SD1_DAT1	A23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[8]	Input	Keeper
SD1_DAT2	C22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[13]	Input	Keeper

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
SD1_DAT3	B22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[6]	Input	Keeper
SD1_DAT4	A22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[12]	Input	Keeper
SD1_DAT5	A21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[9]	Input	Keeper
SD1_DAT6	A20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[7]	Input	Keeper
SD1_DAT7	A19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[10]	Input	Keeper
SD2_CLK	AC24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[5]	Input	Keeper
SD2_CMD	AB24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[4]	Input	Keeper
SD2_DAT0	AB22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[1]	Input	Keeper
SD2_DAT1	AB23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[30]	Input	Keeper
SD2_DAT2	AA22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[3]	Input	Keeper
SD2_DAT3	AA23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[28]	Input	Keeper
SD2_DAT4	AA24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[2]	Input	Keeper
SD2_DAT5	Y20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[31]	Input	Keeper
SD2_DAT6	Y21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[29]	Input	Keeper
SD2_DAT7	Y22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[0]	Input	Keeper
SD2_RST	Y23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[27]	Input	Keeper
SD3_CLK	AB11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[18]	Input	Keeper
SD3_CMD	AA11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[21]	Input	Keeper
SD3_DAT0	AC11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[19]	Input	Keeper
SD3_DAT1	AD11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[20]	Input	Keeper
SD3_DAT2	AC12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[16]	Input	Keeper
SD3_DAT3	AD12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[17]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
TAMPER	Y18	VDD_SNVS_IN	GPIO	ALT0	SNVS_TAMPER	Input	—
TEST_MODE	U15	VDD_SNVS_IN	GPIO	ALT0	TEST_MODE	Input	—
UART1_RXD	B19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[16]	Input	Keeper
UART1_TXD	D19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[17]	Input	Keeper
USB_OTG_CHD_B	AC22	VDD_USB_CAP	ANALOG	—	USB_OTG_CHD_B	—	—
USB_OTG1_DN	AD19	VDD_USB_CAP	ANALOG	—	USB_OTG1_DN	—	—
USB_OTG1_DP	AC19	VDD_USB_CAP	ANALOG	—	USB_OTG1_DP	—	—
USB_OTG2_DN	AD17	VDD_USB_CAP	ANALOG	—	USB_OTG2_DN	—	—
USB_OTG2_DP	AC17	VDD_USB_CAP	ANALOG	—	USB_OTG2_DP	—	—
WDOG_B	F18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[18]	Input	Keeper
XTALI	AD21	NVCC_PLL	ANALOG	—	XTALI	—	—
XTALO	AC21	NVCC_PLL	ANALOG	—	XTALO	—	—
ZQPAD	H2	NVCC_DRAM	ZQPAD	—	DRAM_ZQPAD	Input	Hi-Z

1 All balls marked Power Group NVCC33_IO or NVCC18_IO are dual-voltage IOs. The user supplies NVCC33_IO and NVCC18_IO. In the IOMUX for each ball, the user selects either 3.3 V or 1.8 V operation using the LVE field in the Pad Control Register for each ball.

2 The state immediately after reset and before ROM firmware or software has executed.

3 Variance of the pull-up and pull-down strengths are shown in the tables as follows:

- Table 21, "DVGPIO I/O DC Parameters," on page 33
- Table 22, "LPDDR2 I/O DC Electrical Parameters," on page 34
- Table 23, "DDR3 I/O DC Electrical Parameters," on page 34

For most of the signals, the state during reset is same as the state after reset, given in the *Out of Reset Condition* column of Table 66. However, there are some signals for which the state during reset is different from the state after reset. These signals along with their state during reset are given in Table 67.

Table 67. Signals with Differing Before Reset and After Reset States

Ball name	Before Reset State	
	Input/Output	Value
EIM_A16	**Input**	PD (100k)
EIM_A17	**Input**	PD (100k)
EIM_A18	**Input**	PD (100k)
EIM_A19	**Input**	PD (100k)
EIM_A20	**Input**	PD (100k)
EIM_A21	**Input**	PD (100k)

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 67. Signals with Differing Before Reset and After Reset States (continued)

Ball name	Before Reset State	
	Input/Output	Value
EIM_A22	**Input**	PD (100k)
EIM_A23	**Input**	PD (100k)
EIM_A24	**Input**	PD (100k)
EIM_EB0	**Input**	PD (100k)
EIM_EB1	**Input**	PD (100k)
EIM_LBA	**Input**	PD (100k)
EIM_RW	**Input**	PD (100k)
EIM_GPIO19	**Input**	PD (100k)
EIM_GPIO17	**Input**	PD (100k)
KEY_COL0	**Input**	PD (100k)

6.2.3 13 x 13 mm, 0.5 mm Pitch Ball Map

Table 68 shows the MAPBGA 13 x 13 mm, 0.5 mm pitch ball map.

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map

	17	18	19	20	21	22	23	24
A	EPDC_D1	EPDC_D0	SD1_DAT7	SD1_DAT6	SD1_DAT5	SD1_DAT4	SD1_DAT1	GND
B	EPDC_D2	EPDC_BDR1	UART1_RXD	SD1_CLK	SD1_CMD	SD1_DAT3	SD1_DAT0	KEY_ROW7
C	NC	EPDC_BDR0	GND	NC	NC	SD1_DAT2	KEY_COL7	KEY_ROW6
D	NC	I2C2_SDA	UART1_TXD	NC	NC	KEY_COL6	KEY_ROW5	KEY_COL5
E	NC	I2C2_SCL	KEY_ROW4	KEY_COL4	KEY_ROW3	KEY_COL3	KEY_COL2	KEY_ROW2
F	NC	WDOG_B	NC	NC	NC	NC	KEY_COL1	KEY_ROW1
G	GND	GND	NC	NC	NC	NC	KEY_COL0	KEY_ROW0
H	NC	GND	AUD_MCLK	AUD_TXC	AUD_TXFS	GND	LCD_HSYNC	LCD_RESET
J	VDD_ARM_CAP	VDD_ARM_CAP	AUD_RXFS	AUD_RXD	AUD_RXC	AUD_TXD	LCD_VSYNC	LCD_ENABLE
K	VDD_ARM_CAP	VDD_ARM_CAP	NC	NC	NC	NC	LCD_DAT22	LCD_DAT23
L	NC	NVCC33_IO	NC	NC	NC	NC	LCD_DAT20	LCD_DAT21
M	GND	NVCC33_IO	ECSPI1_MISO	NVCC18_IO	ECSPI1_SS0	LCD_DAT17	LCD_DAT18	LCD_DAT19
N	GND	VDD_SOC_CAP	ECSPI1_SCLK	ECSPI1_MOSI	LCD_DAT14	GND	LCD_DAT15	LCD_DAT16
P	NC	VDD_SOC_CAP	NC	NC	NC	NC	LCD_DAT12	LCD_DAT13
R	VDD_SOC_IN	VDD_SOC_CAP	NC	NC	NC	NC	LCD_DAT10	LCD_DAT11
T	VDD_SOC_IN	VDD_SOC_IN	NVCC33_IO	ECSPI2_MISO	ECSPI_SS0	LCD_CLK	LCD_DAT8	LCD_DAT9
U	NC	GND	ECSPI2_SCLK	ECSPI2_MOSI	LCD_DAT5	GND	LCD_DAT6	LCD_DAT7
V	GND_KELVIN	GND	NC	NC	NC	NC	LCD_DAT3	LCD_DAT4
W	NC	ONOFF	NC	NC	NC	NC	LCD_DAT1	LCD_DAT2
Y	NC	TAMPER	NVCC_PLL	SD2_DAT5	SD2_DAT6	SD2_DAT7	SD2_RST	LCD_DAT0
AA	NC	USB_OTG1_VBUS	RTC_XTALO	NC	NC	SD2_DAT2	SD2_DAT3	SD2_DAT4
AB	NC	GND	RTC_XTALI	NC	NC	SD2_DAt0	SD2_DAT1	SD2_CMD
AC	USB_OTG2_DP	GND	USB_OTG1_DP	VDD_SNVS_IN	XTALO	USB_OTG_CHD_B	CLK1_P	SD2_CLK
AD	USB_OTG2_DN	USB_OTG2_VBUS	USB_OTG1_DN	VDD_SNVS_CAP	XTALI	GPANAIO	CLK1_N	GND

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

	9	10	11	12	13	14	15	16
A	EPDC_SDCE3	EPDC_SDCE1	EPDC_GDSP	EPDC_GDCLK	EPDC_D15	EPDC_D14	EPDC_D5	EPDC_D3
B	EPDC_SDCE2	EPDC_SDCLK	EPDC_PRWCOM	EPDC_GDRL	EPDC_GDOE	EPDC_D13	EPDC_D6	EPDC_D4
C	**NC**	GND	EPDC_SDCE0	**NC**	**NC**	GND	EPDC_D7	**NC**
D	**NC**	EPDC_PWRWAKEUP	EPDC_PWRCTRL0	**NC**	**NC**	EPDC_D12	EPDC_D8	**NC**
E	**NC**	EPDC_PWRSTAT	EPDC_PWRCTRL1	**NC**	**NC**	NVCC18_IO	NVCC18_IO	**NC**
F	**NC**	EPDC_PWRINT	EPDC_PWRCTRL2	**NC**	**NC**	EPDC_D11	EPDC_D9	**NC**
G	GND	GND	GND	EPDC_PWRCTRL3	GND	GND	GND	EPDC_D10
H	**NC**	NVCC33_IO	NVCC33_IO	**NC**	**NC**	NVCC33_IO	NVCC33_IO	**NC**
J	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_CAP	VDD_ARM_CAP
K	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_CAP	VDD_ARM_CAP
L	GND	GND	GND	GND	GND	GND	GND	GND
M	GND	GND	GND	GND	GND	GND	GND	GND
N	GND	GND	GND	GND	GND	GND	GND	GND
P	GND	GND	GND	GND	GND	GND	GND	GND
R	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP	VDD_HIGH_CAP	VDD_SOC_IN
T	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP	VDD_HIGH_CAP	VDD_SOC_IN
U	**NC**	NVCC33_IO	NVCC33_IO	**NC**	**NC**	VDD_USB_CAP	TEST_MODE	**NC**
V	GND	GND	GND	GND	GND	GND	GND	GND
W	**NC**	FEC_REF_CLK	FEC_TXD1	**NC**	**NC**	JTAG_TDI	JTAG_TDO	**NC**
Y	**NC**	FEC_TXD0	NVCC18_IO	**NC**	**NC**	JTAG_MOD	JTAG_TMS	**NC**
AA	**NC**	FEC_RXD0	SD3_CMD	**NC**	**NC**	JTAG_TCK	JTAG_TRSTB	**NC**
AB	**NC**	GND	SD3_CLk	**NC**	**NC**	GND	BOOT_MODE1	**NC**
AC	FEC_CRS_DV	FEC_RXD1	SD3_DAT0	SD3_DAT2	I2C1_SCL	REF_CLK_24M	BOOT_MODE0	POR_B
AD	FEC_RX_ER	FEC_TX_EN	SD3_DAT1	SD3_DAT3	I2C1_SDA	REF_CLK_32K	PMIC_ON_REQ	PMIC_STBY_REQ

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8
A	GND	DRAM_SDQS3_B	DRAM_D24	GND	DRAM_D27	DRAM_D29	GND	DRAM_D31
B	DRAM_D14	DRAM_D15	DRAM_SDQS3	DRAM_D25	DRAM_D26	DRAM_D28	DRAM_D30	EPDC_SDLE
C	DRAM_D12	DRAM_D13	DRAM_DQM3	**NC**	**NC**	GND	EPDC_VCOM0	**NC**
D	GND	GND	DRAM_D11	**NC**	**NC**	DRAM_RESET	EPDC_VCOM1	**NC**
E	DRAM_D9	DRAM_D8	DRAM_D10	DRAM_SDODT1	GND	NVCC_DRAM	EPDC_SDOE	**NC**
F	DRAM_SDQS1	DRAM_SDQS1_B	**NC**	**NC**	**NC**	**NC**	EPDC_SDSHR	**NC**
G	GND	DRAM_DQM1	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
H	DRAM_SDBA2	ZQPAD	GND	DRAM_A7	DRAM_A13	NVCC_DRAM	GND	**NC**
J	DRAM_SDBA0	DRAM_A10	DRAM_A8	DRAM_A9	GND	NVCC_DRAM	VDD_SOC_CAP	VDD_SOC_CAP
K	GND	DRAM_A15	**NC**	**NC**	**NC**	**NC**	VDD_SOC_CAP	VDD_SOC_CAP
L	DRAM_SDCLK_0	DRAM_CS1	**NC**	**NC**	**NC**	**NC**	GND	**NC**
M	DRAM_SDCLK_0_B	DRAM_SDCKE1	DRAM_A5	DRAM_A6	GND	NVCC_DRAM_2P5	GND	GND
N	DRAM_RAS	DRAM_CS0	GND	DRAM_A4	DRAM_VREF	NVCC_DRAM	GND	GND
P	DRAM_CAS	SDCKE0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	**NC**
R	GND	DRAM_A14	**NC**	**NC**	**NC**	**NC**	VDD_PU_CAP	VDD_PU_CAP
T	DRAM_SDBA1	DRAM_A11	DRAM_A2	DRAM_A3	GND	NVCC_DRAM	VDD_PU_CAP	VDD_PU_CAP
U	DRAM_SDWE	DRAM_A12	GND	DRAM_A0	DRAM_A1	NVCC_DRAM	GND	**NC**
V	GND	DRAM_DQM0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
W	DRAM_SDQS0_B	DRAM_SDQS0	**NC**	**NC**	**NC**	**NC**	NVCC_1P2	**NC**
Y	DRAM_D6	DRAM_D7	DRAM_D5	DRAM_SDODT0	GND	NVCC_DRAM	PWM1	**NC**
AA	GND	GND	DRAM_D4	**NC**	**NC**	HSIC_DAT	FEC_MDC	**NC**
AB	DRAM_D3	DRAM_D2	DRAM_DQM2	**NC**	**NC**	HSIC_STROBE	FEC_MDIO	**NC**
AC	DRAM_D1	DRAM_D0	DRAm_SDQS2	DRAM_D22	DRAM_D21	DRAM_D19	DRAM_D17	FEC_TX_CLK
AD	GND	DRAM_SDQS2_B	DRAM_D23	GND	DRAM_D20	DRAM_D18	GND	DRAM_D16

MCIMX6L8DVN10AB NXP USA Inc. IC MPU I.MX6SL 1.0GHZ 432MAPBGA

7 Revision History

Table 70 provides the revision history for this data sheet.

Table 70. i.MX 6SoloLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
6	10/2018	Changes to this Revision: • Table 20, "XTALI and RTC_XTALI DC Parameters," on page 32, – Row: XTALI input leakage current at startup, $I_{XTALI_STARTUP}$: Changed from "... driven 24 MHz RTC clock @ 1.1V" to "...driven 24 MHz clock at 1.1V." • Table 42, "eMMC4.4/4.41 Interface Timing Parameters," on page 59, – Row: SD2, uSDHC Output Delay: Changed t_{OD} from 2.5ns minimum to 2.8ns and 7.1ns maximum to 6.8ns.
5	9/2017	• Figure 1, "Part Number Nomenclature—i.MX 6SoloLite" Updates to the Silicon Revision column to include Rev. 1.4, C. • Table 1, "Example Orderable Part Numbers" Added "C" suffix part numbers and descriptions. • Section 4.8.2, "DDR I/O Output Buffer Impedance" Cross-reference change from JEDEC standards to MMDC section. • Table 42, "eMMC4.4/4.41 Interface Timing Parameters," Corrected SD3 Minimum from 2.6 to 1.7 ns. • Table 42, "eMMC4.4/4.41 Interface Timing Parameters," Added footnote related to Clock duty Cycle range. • Figure 30, "HS200 Mode Timing Diagram" Updated figure to remove extraneous ID callouts.

(*Revision History table continued on next page*)

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4	11/2016	• Changed throughout: – Changed terminology from “floating” to “not connected.” – Removed references to DDR3 • Section 1, “Introduction,” *i.MX 6SoloLite processor features*” Removed “low voltage DDR3” from second paragraph. • Table 1, "Example Orderable Part Numbers": Added new footnote to Speed Grade heading. – Removed paragraph about selecting the right data sheet. – Removed silicon revision 1 part numbers ending in “AA”. • Figure 1, "Part Number Nomenclature—i.MX 6SoloLite": Added to Silicon revision block Rev 1.3 and associated footnote. • Section 1.2, “Features,” added new bullet under Expansion cards, “4-bit or 8-bit…” • Table 2, "i.MX 6SoloLite Modules List": UART1–5, UART Interface row: – Changed bullet about programmable baud rate to “up to 5 Mbps.” – Added new bullet at top: “Conforms to the SD Host Controller…” – Added version “4.5” to MMCS specifications listed in second bullet “Fully compliant with MMC…” – Added new bullet “4-bit or 8-bit transfer mode…” • Table 3, "Special Signal Considerations," Content changes in the following rows: – XTALOSC_CLK1_P/ XTALOSC_CLK1_N: changed “floating” to “unconnected”. – NC: changed “floating” to “remain unconnected”. – SRC_POR_B: removed second sentence “May be used…” – RTC_XTALI/ RTC_XTALO: changed “floating” to “unconnected”. – RTC_XTALI/ RTC_XTALO: changed “keep RTC_XTALO floating” to “leave RTC_XTALO unconnected”. – TEST_MODE: changed “float this signal” to “leave this signal unconnected”. – XTALI/ XTALO: changed “floated” to “remains unconnected”. – Separated paragraphs with bullets. • Table 5, "Recommended Connections for Unused Analog Interfaces": changed “Float” to “Leave unconnected” in both lines. • Section 4.1.1, “Absolute Maximum Ratings”: Added new CAUTION text. • Table 7, "Absolute Maximum Ratings,": – Updated the maximum voltage specifications to an increased of 100 mV. – NVCC_DRAM maximum value changed to 1.975 V. – Added footnote regarding NVCC_DRAM maximum voltage allowance. – Added row to Vin/Vout supply voltage, separating DDR pins and non-DDR pins and included footnote regarding maximum voltage allowance. • Section 4.1.2.1, “BGA Case 2240 Package Thermal Resistance” Added NOTE “Per JEDEC JESD51-2…”. • Table 9, "Operating Ranges," Changed within rows: – Backup battery supply range, minimum reduced (improved) from “2.8” to “2.7”. – Backup battery supply range, maximum increased (improved) from “3.3” to “3.6” – Removed from the GPIO supplies row; NVCC_1P2V row for DDR3L • Section 4.1.5, “Maximum Supply Currents,” Paragraph 3: changed “AN4715” to “AN4580”. • Section 4.2.1, “Power-Up Sequence,” Removed reference to external SRC_POR_B: – Bullet 3: Removed “If the external” and final sentence “In the absence of…” – Removed bullet 4. – Added third NOTE: “For customers starting new designs…” *Continued on next page*

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4 *Continued*	11/2016	• Section 4.2.2, “Power-Down Sequence,” Replaced contents of section with sentence: “There are no special requirements on the power-down sequence other than …”. • Section 4.5.2, “OSC32K”: Removed text regarding coin cell from third paragraph and removed second NOTE about third party coin cell manufacturer. • Section 4.6, “I/O DC Parameters”: Removed second bullet regarding single voltage GPIO cell set. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters” Added NOTE after table.Table 20, "XTALI and RTC_XTALI DC Parameters”: – Added parameter rows: Input capacitance; XTALI input leakage; and DC input current. – Added new footnote, “This voltage specification…” • Section 4.6.3, “*Single Voltage General Purpose I/O (GPIO) DC Parameters”* removed section. • Section 4.8, “Output Buffer Impedance Parameters”: Removed second bullet “Single voltage General Purpose I/O cell set …”. • Table 28, "DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)”: Changed all Typical values. • Table 29, "DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)”: Changed all Typical values. • Section 4.8.2, “*Single Voltage GPIO Output Buffer Impedance*”: removed section. • Table 34, "EIM Bus Timing Parameters, Updates throughout table to include min/max values. • Table 35, "EIM Asynchronous Timing Parameters Table Relative Chip Select, Updates throughout table to include min/max values. • Section 4.9.4, “Multi-Mode DDR Controller (MMDC),” created this new section. • Removed: Section 4.9.5, “DDR SDRAM Specific Parameters (DDR3 and LPDDR2),” Section 4.9.5.1, “DDR3 Parameters,” and Section 4.9.5.2, “LPDDR2 Parameters.” • Table 37, "CSI Gated Clock Mode Timing Parameters,” – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 reduced (improved) from 10ns to 7.5 ns. – Parameter P7 corrected to 66 MHz (no functional change). • Table 38, "CSI Ungated Clock Mode Timing Parameters,” – Parameter P4 reduced (improved) from 10ns to 7.5 ns. – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 corrected to 66 MHz (no functional change). • Section 4.10.3.1, “ECSPI Master Mode Timing,” Added new NOTE under Figure 25. • Section 4.10.3.2, “ECSPI Slave Mode Timing,” Added new NOTE under Figure 26. • Section 4.10.4.3, “SDR50/SDR104 AC Timing Parameters,” Figure 29 updated to correct SD5. • Table 43, "SDR50/SDR104 Interface Timing Parameters,” – SD2, changed minimum value to “0.46”, and changed maximum value to “0.54”. – SD3, changed minimum value to “0.46”, and changed maximum value to “0.54”. – SD2 (parameter Clock High Time), parameter name corrected to SD3. – SD5, changed maximum value to “0.74”. • Section 4.10.5, “HS200 Mode Timing Parameters,” Added this new section. • Section 4.10.14, “USB PHY Parameters,” Added new text to second paragraph “USB Host with the amendments below…” • Table 63, "Interfaces Allocation During Boot USDHC-1–USDHC-4 row, replaced existing text with “Refer to the table “SD/MMC…” • Table 65, "13 x 13 mm Supplies Contact Assignment,” – GPANAIO: changed remark from “Analog pad” to “Analog output for NXP use…” – ZQPAD: changed remark to “Connect ZQPAD to…” • Table 66, "13 x 13 mm Functional Contact Assignments,” DRAM_SDCLK_0, corrected “Input” to “Output” and Value to “0”. • Section 6.2.2, “13 x 13 mm Ground, Power, Sense, Not Connected, and Reference Contact Assignments,” Added new text “For most of the signals…” after Table 66. • Table 68, "13 x 13 mm, 0.5 mm Pitch Ball Map,” ball AD6 name corrected to “DRAM_D18”.

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 3	02/2014	• Section 1.2,Feature description for: - Camera sensors: Added to Parallel Camera port “and up to 66 MHz peak”. - Miscellaneous IPs and interfaces; Changed from: “Three I2S/SSI/AC97 supported,” to “SSI block is capable of supporting audio sample frequencies up to 192 kHZ stereo inputs and outputs with I2S mode.” • Table 2, Modules List: UART1–5, Brief Description; Changed bullet about programmable baud rate to “up to 5 MHz.” • Table 2, Modules List: uSDHC1–4, Brief Description; Changed bullet about Fully compliant with SD command/response to include “and SDXC cards up to 2TB.” • Table 9, operating range for GPIO supplies: Added NVCC_1P2V min/typ/max values for LPDDR2, DDR3L, DDR3. • Section 4.1.4, External Clock Sources; added Note, “The internal oscillator may run high …” • Table 11, Maximum Supply currents: Added row; NVCC_LVDS2P5. • Section 4.2.1, Power-Up Sequence: reworded third bulleted item regarding POR control. • Section 4.2.1, Power-Up Sequence: removed Note. • Section 4.5.1, OSC24K, first paragraph corrected ‘*powered from*’ signal from NVCC_1P2 to NVCC_1P2V. • Section 4.5.2, OSC32K, Changed second paragraph and added CAUTION. • Table 31 Reset Timing Parameters, changed Unit from XTALI cycle to XTALOSC_RTC_XTALI cycle. • Section 4.5.2, External Interface Module; enhanced wording to first paragraph to describe operating frequency for data transfers, and to explain register settings are valid for entire range of frequencies. • Table 34, EIM Bus Timing Parameters; reworded footnotes for clarity.
Rev. 3.0	02/2014	• Table 45, DDR3 Write Cycle; changed footnote 3, outputs from “DDR_VREF” to “DRAM_VREF”. • Figure 25, LPDDR2 Command and Address Timing Diagram; changed signal name from “DRAM_CAS_B” to “DRAM_ADDRxx”. • Table 47, LPDDR2 Timing Parameters; changed footnote 2, outputs from “DDR_VREF” to “DRAM_VREF”. • Table 48, LPDDR2 Write Cycle; changed footnote 3, outputs from “DDR_VREF” to “DRAM_VREF”. • Table 49, LPDDR2 Read Cycle; changed footnote 3, outputs from “DDR_VREF” to “DRAM_VREF”. • Table 65, 13x13mm Supplies Contact Assignment; changed Supply Rail Name “DDR_VREF” to “DRAM_VREF”. • Table 65, 13x13mm Supplies Contact Assignment; changed ZQPAD ball position from “AE17” to “H2”. • Table 68, 13x13mm Functional Contact Assignment; Changed the following signals to include active-low “_B” in the Default Function column: DRAM_CAS_B; DRAM_CS0_B; DRAM_CS1_B; DRAM_RAS_B; DRAM_RESET_B. • Table 68, 13x13mm Functional Contact Assignment; Changed the Ball Name of DRAM_WE_B to DRAM_SDWE. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; Y19, changed from “ON/OFF” to “NVCC_PLL. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; W18, changed from “TEST_MODE” to “ON/OFF”. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; U15, changed from “NVCC_PLL” to “TEST_MODE”. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; U11 & U10, changed from “NHVCC_3V3” to “NVCC33_IO”.
Rev. 2.2	8/2013	Substantive Changes are as follows: • Section 1.2, “Features,” corrected value of OCRAM from 256KB to 128KB: The SoC-level memory system consists of the following additional components: — Boot ROM, including HAB (96 KB) — Internal multimedia / shared, fast access RAM (OCRAM, 128 KB) • Removed parenthetical statement (input slope <= 5 ns) from Table 31, “Reset Timing Parameters” CC1: Duration of POR_B to be qualified as valid. The parenthetical statement was a typographical error and is not a specification requirement for this device.

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Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 2.1	05/2013	Substantive changes throughout this document are as follows: • Incorporated standardized signal names. This change is extensive throughout the document. • Added section Section 1.3, “Updated Signal Naming Convention”. • Added reference to EB792, i.MX Signal Name Mapping. • Figures updated to align to standardized signal names. • Updated references to eMMC standard to include 4.41. • References to Consumer and Extended consumer temperature grades changed to Commercial and Extended Commercial. • Figure 1 “Part Number Nomenclature—i.MX 6SoloLite,” updates to *Silicon Revision* section. • Table 1 “Orderable Part Numbers” part numbers updated and options updated accordingly. • Table 2 “i.MX 6SoloLite Modules List” Changed reference to Global Power Controller to read General Power Controller. • Table 12. “Stop Mode Current and Power Consumption” Added SNVS only mode information. • Table 39 “ECSPI Master Mode Timing Parameters,” updated CS5/CS6 Min to Half ECSPIx_SCLK period-4/Half ECSPIx_SCLK period-2. • Table 39 “ECSPI Master Mode Timing Parameters,” added to CS8 parameters slow group/fast group. • Table 41 “SD/eMMC4.3 Interface Timing Specification,” changed SD8 from 5.6ns to 1.5ns. • Table 66 “13 x 13 mm Functional Contact Assignments,” Changes throughout. NVCC_GPIO, NVCC_SD1, NVCC_SD2, NVCC_SD3, and NVCC_LCD entries in the Power Group column changed to NVCC33_IO or NVCC18_IO. • Table 66 “13 x 13 mm Functional Contact Assignments,” Added footnote to Value to include reference information to pull-up and pull-down strengths.
Rev. 2.1	05/2013	• Table 66: “13 x 13 mm Functional Contact Assignments,” for contact ECSPI_MOSI through ECSPI2_SCLK changed ball type from ALT5 to GPIO. • Section 1.2, “Features,” added bulleted items regarding the SOC-level memory system. • Renamed and updated Section 4.3.2, “Regulators for Analog Modules.” • Section 4.10.6, “FEC AC Timing Parameters,” removed FEC MII subsections and other references to MII—changed to RMII as applicable. • Removed section, “EIM Signal Cross Reference.” Signal names are now aligned between Reference Manual and Data Sheet.

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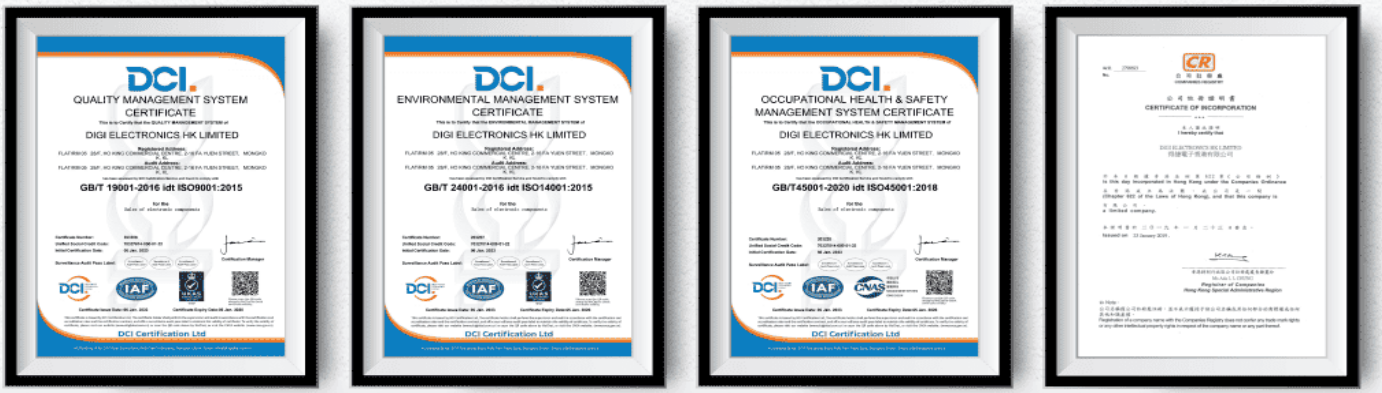

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