PTN3944EWY Datasheet

DiGi Electronics Part Number	PTN3944EWY-DG
Manufacturer	NXP Semiconductors
Manufacturer Product Number	PTN3944EWY
Description	PTN3944 - Multi-Channel PCIe Gen
Detailed Description	4 Channel 16Gbps 36-HWFLGA (2.1x6)

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
PTN3944EWY	NXP Semiconductors
Series:	Product Status:
-	Active
Type:	Applications:
-	PCIe
Input:	Output:
Differential	Differential
Data Rate (Max):	Number of Channels:
16Gbps	4
Delay Time:	Signal Conditioning:
70ps	Input Equalization
Capacitance - Input:	Voltage - Supply:
10 pF	1.7V ~ 1.9V
Current - Supply:	Operating Temperature:
250mA	-20°C ~ 85°C (TA)
Package / Case:	Supplier Device Package:
36-WFLGA Exposed Pad	36-HWFLGA (2.1x6)

PTN3944

Multi-channel PCIe 4.0 linear equalizer

Rev. 1.1 — 10 June 2021 Product data sheet

1 General description

PTN3944 is a high-performance multi-channel (x4) linear equalizer that is optimized for PCIe 4.0, UPI, and similar high-speed interfaces.

PTN3944 addresses high-speed signal quality enhancement requirements for implementation of PCIe and UPI interfaces[1].

The device provides programmable linear equalization, output swing linearity control by pin strapping or I^2C control to improve signal integrity and enable channel extension by reducing Inter-Symbol Interference (ISI). The equalizer supports use across a variety of channel conditions.

PTN3944 is powered from a 1.8 V supply. It is available in a small high performance HWFLGA36 package.

2 Features

- Supports PCIe Gen1 (2.5 Gbps) x4, Gen2 (5 Gbps) x4, Gen3 (8 Gbps) x4, and Gen4 (16 Gbps) x4
  - Peaking gain up to 18.3 dB at 8 GHz
  - Output swing linearity control: 500 mV_{ppd} to 950 mV_{ppd}
  - Flat gain of +0.7 dB or -0.7 dB
- Configurable via I^2C interface (supports 16 slave addresses)
- Supports maximum voltage limit ($V_{voltage\_jump}$) to align to the latest system platform capabilities
- Integrated termination resistors provide impedance matching on both transmit and receive sides
- RX equalizers on all high-speed channels to compensate for signal attenuation
- Good linearity over the frequency band (DC to Nyquist Frequency) and input voltage dynamic range
- Differential input/output return loss performance < -15 dB up to 8 GHz
- Flow-through pin-out to ease PCB layout and minimize crosstalk effects
  - Very low crosstalk: DDNEXT < -60 dB up to 8 GHz
  - Very low crosstalk: DDFEXT < -50 dB up to 8 GHz
- Low active current consumption for output swing linearity control of 950 mV_{ppd}
  - Single channel: 62 mA (typ)
  - Two channels: 125 mA (typ)
  - Four channels: 250 mA (typ)
- Power Supply 1.7 V to 1.9 V
- Small high performance HWFLGA36 package
- ESD HBM 1.5 kV, CDM 1 kV
- Operating temperature range -20 °C to +85 °C

3 Applications

- Servers
- Data centers
- AI/ML hardware accelerators
- Hub or dock devices
- Edge mobile computing devices

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PTN3944EW	44	HWFLGA36	plastic thermal enhanced very very thin fine-pitch land grid array package	SOT1948-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN3944EW	PTN3944EWY	HWFLGA36	REEL 13" Q1 DP	7000	T_{amb} = -20 °C to 85 °C

5 Functional diagram

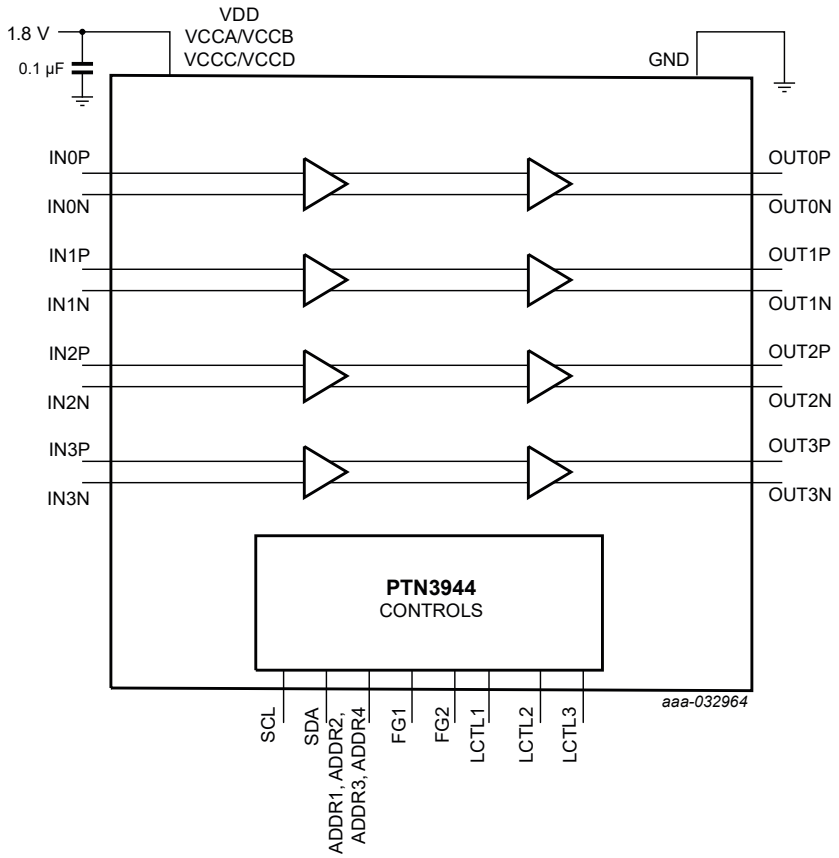


Figure 1. Functional diagram

6 Pinning information

6.1 Pinning

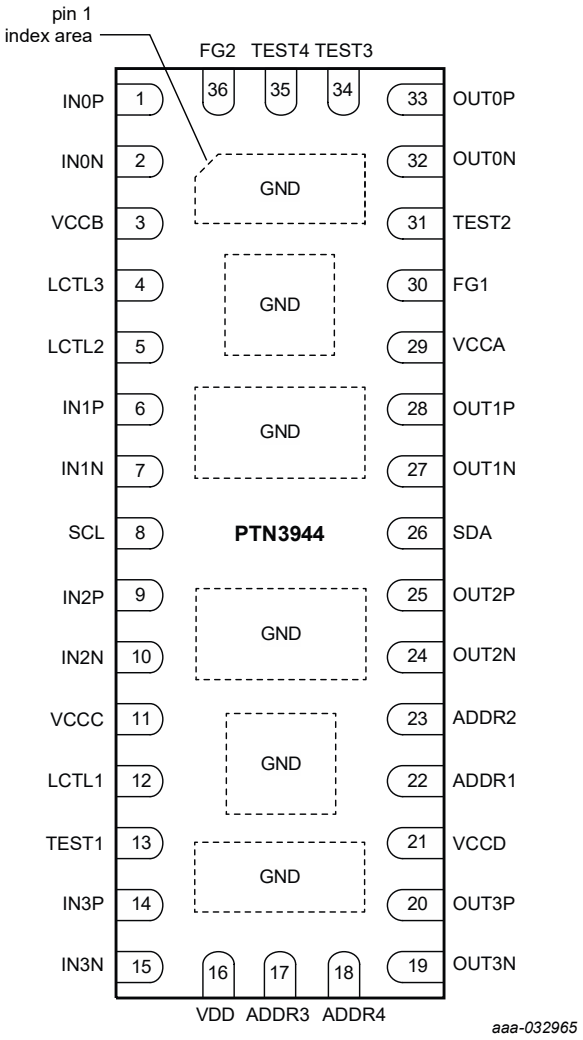


Figure 2. PTN3944 pinning (transparent top view)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
1	IN0P	Self-biasing differential input/ output	Differential signal high-speed input/output. IN0P makes a differential pair with IN0N. The associated output TX pair is OUT0P and OUT0N.
2	IN0N		
3	VCCB	Power pins for high-speed paths	These dedicated power pins for high-speed differential pairs provide good signal integrity and isolation
11	VCCC		
21	VCCD		
29	VCCA		

Table 3. Pin description*...continued*

Symbol	Pin	Type	Description
4	LCTL3	Ternary Input	Ternary Input for controlling Output Linear Swing on the downstream side of the chip. Refer to Table 6 for details
12	LCTL1	Ternary input	LCTL1 and LCTL2 are Peaking setting pins for inputs on upstream side of the chip. Refer to Table 4 and Table 5 for details
5	LCTL2		
6	IN1P	Self-biasing differential input	Differential signal from high-speed RX path. IN1P makes a differential pair with IN1N. The associated TX output pair is OUT1P and OUT1N
7	IN1N		
8	SCL	Open Drain input	When operating in I^2C mode, this pin is slave I^2C clock pin, and external pull-up resistor to I^2C supply (1.8 V or 3.3 V) is required. If I^2C is not used, then this pin could be connected to 1.8 V or to GND. Do not leave floating.
9	IN2P	Self-biasing differential input	Differential signal from high-speed RX path. IN2P makes a differential pair with IN2N. The associated TX output pair is OUT2P and OUT2N
10	IN2N		
13	TEST1	Reserved test pin	Reserved for test purpose only. Must be connected to GND in the system application
14	IN3P	Self-biasing differential input/ output	Differential signal high-speed input/output. IN3P makes a differential pair with IN3N. The associated output TX pair is OUT3P and OUT3N.
15	IN3N		
16	VDD	Power	1.8 V Supply for I^2C and digital blocks
17	ADDR3	Binary input	I^2C slave address selection pin in I^2C mode controls bit [4]
18	ADDR4	Binary input	I^2C slave address selection pin in I^2C mode controls bit [6]
19	OUT3N	Self-biasing differential input/ output	Differential signal high-speed input/output. OUT3P makes a differential pair with OUT3N. The associated output/ input pair is IN3P and IN3N.
20	OUT3P		
22	ADDR1	Quaternary Input	I^2C slave address selection pin in I^2C mode
23	ADDR2	Binary input	I^2C Slave address extension input
30	FG1	Ternary input	Flat Gain control static input 1
24	OUT2N	Self-biasing differential output	Differential signal of high-speed TX path. OUT2P makes a differential pair with OUT2N. The associated RX input pair is IN2N and IN2P
25	OUT2P		
26	SDA	Binary open drain input/ output	When PTN3944 is operating in I^2C mode, this pin is slave I^2C Data pin, and external pull-up resistor to I^2C supply (1.8 V or 3.3 V) is required. If I^2C is not used, then this pin could be connected to 1.8 V or to GND. Do not leave floating.
27	OUT1N	Self-biasing differential output	Differential signal of high-speed TX path. OUT1P makes a differential pair with OUT1N. The associated RX input pair is IN1P and IN1N
28	OUT1P		
31	TEST2	Reserved test pin	Reserved for test purpose only. Must be connected to GND in the system application
32	OUT0N	Self-biasing differential input/ output	Differential signal high-speed input/output. OUT0P makes a differential pair with OUT0N. The associated input pair is IN0P and IN0N.
33	OUT0P		
34	TEST3	Reserved test pin	Reserved for test purpose only. Must be connected to GND in the system application

Table 3. Pin description*...continued*

Symbol	Pin	Type	Description
35	TEST4	Reserved test pin	Reserved for test purpose only. Must be connected to GND in the system application
36	FG2	Ternary input	Flat Gain control static input 2
Center pads	GND		These six center pads must be connected to GND plane for both electrical grounding and thermal relief

7 Functional description

7.1 PCIe operation

PTN3944 supports PCIe speeds at 2.5 Gbps, 5 Gbps, 8 Gbps, and 16 Gbps with receiver equalization and linearity control. The receive equalization gain and linearity level are configured either via I^2C register settings or pin strapping (LCTL[3:1], FG[2:1]).

- Active state wherein device is fully operational. In this state, PCIe connection exists and the Receive Termination remains active. PTN3944 supports entering into Deep standby state using an I^2C register write.

PTN3944 uses lane count information for configuring the transmitters and receivers. It is possible that only a subset of lanes gets selected and remaining lanes are not active. Depending on the number of lanes selected, PTN3944 is configured to operate with the selected lane count thereby saving power consumption on unused lanes. This can be configured via I^2C.

7.2 Linear equalizer control

PTN3944 allows for programming of equalization and linearity levels on a per channel basis. Peaking gain is referenced to the maximum data rate (or Nyquist channel) in that channel. Linearity (Output swing control) is set based on selected input source signal amplitude, Tx preset, and expected channel attenuation.

7.2.1 Power-on operational mode

After Power On Reset (POR) initialization, the device goes into PCIe mode of operation.

7.2.2 Channel settings

PTN3944 can be configured via GPIO or using the I^2C interface. The I^2C interface allows many more settings to be configured. The ternary channel condition or GPIO inputs LCTL1, LCTL2, LCTL3, FG1 and FG2 are enabled and sampled at POR. The detected values from these ternary inputs are then used to initialize the I^2C registers. After entry into I^2C mode, changes to the ternary channel conditions are ignored and subsequent writes of I^2C values overwrite the sampled ternary input values. Once the ternary inputs have been sampled during Mode detection, there is no mechanism to reinitialize the I^2C registers to the sampled values except an I^2C write. When a software reset is issued, I^2C register values get reset to the stored value of the ternary inputs sampled at power-up.

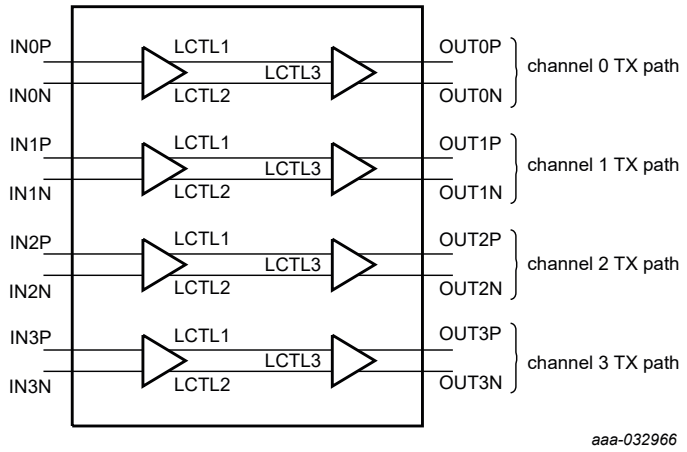


Figure 3. LCTL signals to corresponding transmitter or receiver

Table 4 and Table 5 will be expanded to cover gain values at different link rates of PCIe.

Table 4. LCTL[2:1] Channel configurations: Flat gain setting of 0.7 dB (typical)

Peaking Gain is the equalization gain at specific frequency relative to absolute gain at 10 MHz and for Flat Gain setting of 0.7 dB (typical)

I^2C register value <3:0>	LCTL2	LCTL1	Unit	Gain at 10 MHz	100 MHz	1.35 GHz	2.5 GHz	4 GHz	6.75 GH	8 GHz
0000	LOW	OPEN	dB	0.8	0	-0.3	-0.2	0.1	1.1	1.7
0001	OPEN	LOW	dB	0.8	0	-0.2	0.0	0.3	1.5	2.2
0010			dB	0.8	0	0	0.2	0.6	2.0	2.9
0011	HIGH	HIGH	dB	0.8	0.1	0.2	0.5	1.1	2.9	4.0
0100			dB	0.8	0.1	0.4	0.8	1.5	3.6	4.9
0101	HIGH	OPEN	dB	0.8	0.1	0.9	1.5	2.5	5.2	6.8
0110			dB	0.8	0.1	1.1	1.9	3.1	6.1	7.8
0111	HIGH	LOW	dB	0.8	0.1	1.7	2.7	4.3	7.8	9.7
1000			dB	0.8	0.2	2.3	3.6	5.5	9.5	11.6
1001	OPEN	HIGH	dB	0.8	0.2	2.6	4.0	6.1	10.3	12.4
1010			dB	0.8	0.1	3.1	4.8	7.1	11.6	13.9
1011	LOW	HIGH	dB	0.8	0.1	3.5	5.3	7.8	12.6	15.0
1100			dB	0.9	0.1	3.8	5.7	8.3	13.3	15.8
1101	OPEN	OPEN	dB	0.9	0.1	4.1	6.1	8.9	14.1	16.6
1110			dB	0.9	0.1	4.1	6.1	8.9	14.1	16.6
1111	LOW	LOW	dB	0.9	0.2	4.1	6.1	8.9	14.2	16.6

Table 5. LCTL[2:1] Channel configurations: Flat gain setting of -0.7 dB (typical)

Peaking Gain is the equalization gain at specific frequency relative to absolute gain at 10 MHz and for Flat Gain setting of -0.7 dB (typical)

I^2C register value <3:0>	LCTL2	LCTL1	Unit	Gain at 10 MHz	100 MHz	1.35 GHz	2.5 GHz	4 GHz	6.75 GH	8 GHz
0000	LOW	OPEN	dB	-0.7	0	-0.1	0.4	1.2	2.6	3.4
0001	OPEN	LOW	dB	-0.8	0	0.1	0.6	1.5	3.1	4.0
0010			dB	-0.8	0	0.3	0.9	1.8	3.7	4.7
0011	HIGH	HIGH	dB	-0.8	0.1	0.6	1.3	2.4	4.6	5.8
0100			dB	-0.8	0.1	0.8	1.7	2.9	5.3	6.6
0101	HIGH	OPEN	dB	-0.8	0.1	1.4	2.5	4.0	7.0	8.5
0110			dB	-0.9	0.1	1.7	3.0	4.7	7.9	9.6
0111	HIGH	LOW	dB	-0.9	0.2	2.5	3.9	5.9	9.6	11.5
1000			dB	-0.9	0.2	3.2	4.9	7.2	11.3	13.3
1001	OPEN	HIGH	dB	-0.9	0.2	3.5	5.3	7.8	12.0	14.2
1010			dB	-0.8	0.2	4.1	6.1	8.8	13.4	15.6
1011	LOW	HIGH	dB	-0.8	0.2	4.6	6.7	9.5	14.4	16.7
1100			dB	-0.8	0.2	4.9	7.2	10.0	15.1	17.5
1101	OPEN	OPEN	dB	-0.7	0.2	5.2	7.6	10.6	15.8	18.3
1110			dB	-0.7	0.2	5.2	7.6	10.6	15.8	18.3
1111	LOW	LOW	dB	-0.7	0.2	5.2	7.6	10.6	15.8	18.3

Table 6. LCTL3 channel configuration

I^2C Register Value	LCTL3	Output linear swing (OLS) -1 dB compression point
0		500 mV_{ppd}
1	OPEN	650 mV_{ppd}
2	LOW	800 mV_{ppd}
3	HIGH	950 mV_{ppd}

Table 7. Channel flat gain control using FG1 and FG2 pins

FG2	FG1	Flat gain in dB of individual channels - I^2C offset register 0x03, bits [3:0]			
		Ch0	Ch1	Ch2	Ch3
LOW	LOW	+0.7	+0.7	+0.7	+0.7
LOW	OPEN	+0.7	+0.7	+0.7	-0.7
LOW	HIGH	+0.7	+0.7	-0.7	+0.7
OPEN	LOW	+0.7	+0.7	-0.7	-0.7

Table 7. Channel flat gain control using FG1 and FG2 pins *...continued*

FG2	FG1	Flat gain in dB of individual channels - I²C offset register 0x03, bits [3:0]			
		Ch0	Ch1	Ch2	Ch3
OPEN	OPEN	+0.7	-0.7	+0.7	+0.7
OPEN	HIGH	+0.7	-0.7	-0.7	+0.7
HIGH	LOW	-0.7	+0.7	+0.7	+0.7
HIGH	OPEN	-0.7	-0.7	+0.7	+0.7
HIGH	HIGH	-0.7	-0.7	-0.7	-0.7

7.2.3 I²C configurability

PTN3944 has an I²C register interface that enables system integrator to program register settings suitable as per application needs. After power on reset, the device reads the ADDR1 and ADDR2 pins for determining the I²C Slave Address. PTN3944 provides up to eight I²C Slave address combinations based on Quaternary (ADDR1) and Binary (ADDR2) pin settings, and they are summarized in Table 8.

Table 8. I²C slave address options

ADDR4	ADDR3	ADDR2	ADDR1	7-Bit I²C Slave Address	Address (Hex)
Pin state	Pin state	Pin state	Pin state		
LOW	LOW	LOW	Connected to 1.8 V directly	0100011	0x23
LOW	LOW	LOW	Connected to 1.8 V with 56 kΩ (±10%) pull-up resistor	0100010	0x22
LOW	LOW	LOW	Connected to 1.8 V with 200 kΩ (±10%) pull-up resistor	0100001	0x21
LOW	LOW	LOW	Connected to GND directly	0100000	0x20
LOW	LOW	HIGH	Connected to 1.8 V directly	0101011	0x2B
LOW	LOW	HIGH	Connected to 1.8 V with 56 kΩ (±10%) pull-up resistor	0101010	0x2A
LOW	LOW	HIGH	Connected to 1.8 V with 200 kΩ (±10%) pull-up resistor	0101001	0x29
LOW	LOW	HIGH	Connected to GND directly	0101000	0x28
LOW	HIGH	LOW	Connected to 1.8 V directly	0110011	0x33
LOW	HIGH	LOW	Connected to 1.8 V with 56 kΩ (±10%) pull-up resistor	0110010	0x32
LOW	HIGH	LOW	Connected to 1.8 V with 200 kΩ (±10%) pull-up resistor	0110001	0x31
LOW	HIGH	LOW	Connected to GND directly	0110000	0x30
LOW	HIGH	HIGH	Connected to 1.8 V directly	0111011	0x3B
LOW	HIGH	HIGH	Connected to 1.8 V with 56 kΩ (±10%) pull-up resistor	0111010	0x3A
LOW	HIGH	HIGH	Connected to 1.8 V with 200 kΩ (±10%) pull-up resistor	0111001	0x39
LOW	HIGH	HIGH	Connected to GND directly	0111000	0x38
HIGH	LOW	LOW	Connected to 1.8 V directly	1100011	0x63
HIGH	LOW	LOW	Connected to 1.8 V with 56 kΩ (±10%) pull-up resistor	1100010	0x62
HIGH	LOW	LOW	Connected to 1.8 V with 200 kΩ (±10%) pull-up resistor	1100001	0x61
HIGH	LOW	LOW	Connected to GND directly	1100000	0x60
HIGH	LOW	HIGH	Connected to 1.8 V directly	1101011	0x6B

Table 8. I²C slave address options*...continued*

ADDR4	ADDR3	ADDR2	ADDR1	7-Bit I²C Slave Address	Address (Hex)
Pin state	Pin state	Pin state	Pin state		
HIGH	LOW	HIGH	Connected to 1.8 V with 56 kΩ (±10%) pull-up resistor	1101010	0x6A
HIGH	LOW	HIGH	Connected to 1.8 V with 200 kΩ (±10%) pull-up resistor	1101001	0x69
HIGH	LOW	HIGH	Connected to GND directly	1101000	0x68
HIGH	HIGH	LOW	Connected to 1.8 V directly	1110011	0x73 [1]
HIGH	HIGH	LOW	Connected to 1.8 V with 56 kΩ (±10%) pull-up resistor	1110010	0x72 [1]
HIGH	HIGH	LOW	Connected to 1.8 V with 200 kΩ (±10%) pull-up resistor	1110001	0x71 [1]
HIGH	HIGH	LOW	Connected to GND directly	1110000	0x70 [1]
HIGH	HIGH	HIGH	Connected to 1.8 V directly	1111011	0x7B [1]
HIGH	HIGH	HIGH	Connected to 1.8 V with 56 kΩ (±10%) pull-up resistor	1111010	0x7A [1]
HIGH	HIGH	HIGH	Connected to 1.8 V with 200 kΩ (±10%) pull-up resistor	1111001	0x79 [1]
HIGH	HIGH	HIGH	Connected to GND directly	1111000	0x78 [1]

[1] Reserved I²C address, not recommended for use.

7.2.4 I²C registers

The system integrator must program the registers of the device for proper operation. Further, it is expected that the system integrator performs I²C configuration after power-on and before data transport is initiated over the link. If such an operation is attempted during normal operation, the device may not behave as specified.

Table 9. I²C registers and description

Register offset	Register name	Bits	POR default value	Description
0x00 Read Only	Chip ID	7:0	b'00001111	Chip ID Number
0x01 Read Only	Chip Revision	7:4	b'1010	Chip base layer version
		3:0	b'0001	Chip metal layer version
0x02	Reserved	7:0	b'0000 0000	

Table 9. I²C registers and description*...continued*

Register offset	Register name	Bits	POR default value	Description
0x03	Flat gain control			Flat gain control setting for each high speed data channel. The flat gain is specified at 100 MHz
		7:6	b'00	Reserved
		5	b'0	Always set to 0
		4	b'0	Always set to 0
		3	based on FG1/ FG2	Channel 0 flat gain control 0 = flat gain of +0.7 dB 1 = flat gain of -0.7 dB
		2	based on FG1/ FG2	Channel 1 flat gain control 0 = flat gain of +0.7 dB 1 = flat gain of -0.7 dB
		1	based on FG1/ FG2	Channel 2 flat gain control 0 = flat gain of +0.7 dB 1 = flat gain of -0.7 dB
		0	based on FG1/ FG2	Channel 3 flat gain control 0 = flat gain of +0.7 dB 1 = flat gain of -0.7 dB
0x04 Read/Write	PCIe operation	7:3	b'00000	Always set to 0
		2:0	b' 011	000 = Enforce part to go into deep power saving state 011 = Enforce part to be active
0x05 Read/Write	Device reset	7:1	b'0001010	Reserved
		0	b'0	Device Reset bit. This is a self-clearing bit, and reading this register will always return 0. • Writing a '1' to this register will soft reset the device including I²C register contents and internal digital logic states, while the chip continuing to operate under I²C mode. After soft reset, chip will be in deep power saving state. • Writing a '0' does not have any effect.
0x06 Read/Write	link control and status	7:5	b'000	Reserved
		4	b'0	Always set to 0
		3:2	b'11	Operating channel count • 0: None • 1: one channel • 2: two channels • 3: four channels
		1:0	b'00	Always set to 00
0x07 Read/Write	Channel 0 Control_1 Register	7:4	b'00	Reserved
		3:0	LCTL1, LCTL2	Channel 0 link Equalization gain. Refer to Peaking gain settings (Table 4 and Table 5) in Section 7.2.2 and for more details.

Table 9. I^2C registers and description*...continued*

Register offset	Register name	Bits	POR default value	Description
0x08 Read/Write	Channel 0 Control_2 Register	7:2	b'0000 00	Reserved
		1:0	LCTL3	Channel 0 output signal swing linearity (-1 dB compression point) • 0: 500 mV_{ppd} • 1: 650 mV_{ppd} • 2: 800 mV_{ppd} • 3: 950 mV_{ppd}
0x09 Read/Write	Channel 1 Control_1 Register	7:4	b'0000	Reserved
		3:0	LCTL1, LCTL2	Channel 1 link Equalization gain. Refer to Peaking gain settings (Table 4 and Table 5) in Section 7.2.2 for more details.
0x0A Read/Write	Channel 1 Control_2 Register	7:2	b'0000 00	Reserved
		1:0	LCTL3	Channel 1 output signal swing linearity (-1 dB compression point) • 0: 500 mV_{ppd} • 1: 650 mV_{ppd} • 2: 800 mV_{ppd} • 3: 950 mV_{ppd}
0x0B Read/Write	Channel 2 Control_1 Register	7:4	b'0000	Reserved
		3:0	LCTL1, LCTL2	Channel 2 link Equalization gain. Refer to Peaking gain settings (Table 4 and Table 5) in Section 7.2.2 for more details.
0X0C Read/Write	Channel 2 Control_2 Register	7:2	b'0000 00	Reserved
		1:0	LCTL3	channel 2 output signal swing linearity (-1 dB compression point) • 0: 500 mV_{ppd} • 1: 650 mV_{ppd} • 2: 800 mV_{ppd} • 3: 950 mV_{ppd}
0x0D Read/Write	Channel 3 Control_1 Register	7:4	b'0000	Reserved
		3:0	LCTL1, LCTL2	Channel 3 link Equalization gain. Refer to Peaking gain settings (Table 4 and Table 5) in Section 7.2.2 for more details.
0x0E Read/Write	Channel 3 Control_2 Register	7:2	b'0000 00	Reserved
		1:0	LCTL3	channel 3 output signal swing linearity (-1 dB compression point) • 0: 500 mV_{ppd} • 1: 650 mV_{ppd} • 2: 800 mV_{ppd} • 3: 950 mV_{ppd}
0x0F to 0x18	Reserved	7:0	b'0000 0000	Always set to 0
0x19 to 0xFF	Reserved			Reserved for NXP Internal use only; Do not write to these registers

7.2.5 I²C read/write operations

PTN3944 supports programming of the registers through the I²C interface. Reading/writing the registers must be done according to protocols defined in UM10204[2].

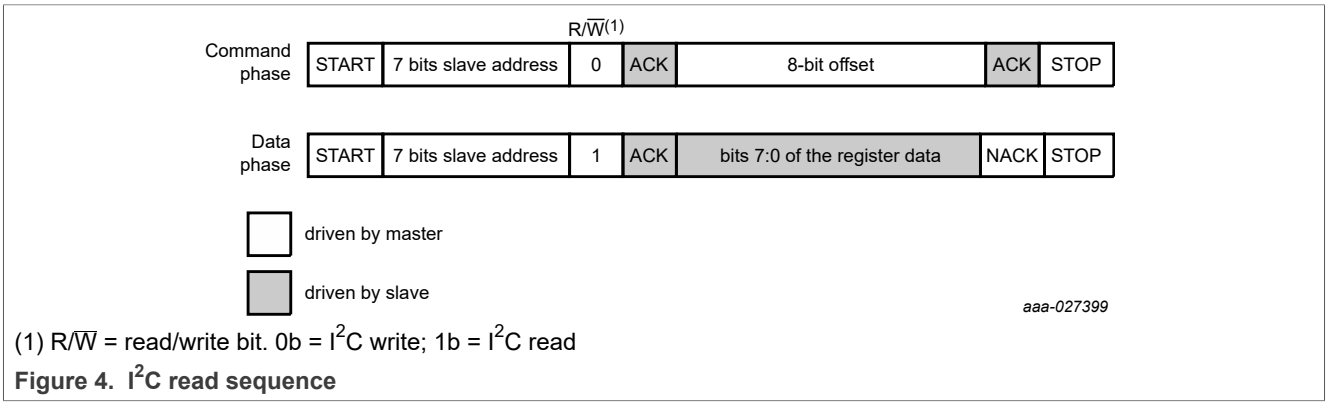
PTN3944 supports programming of the registers through the I²C interface. Reading/writing the registers must be done according to the following sequences.

The read sequence contains two phases:

- Command phase
- Data phase

7.2.5.1 Single byte register reads/writes

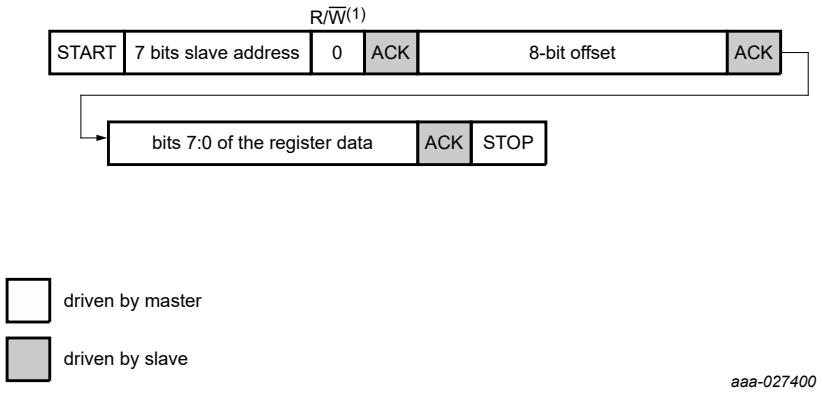
The command phase is an I²C write to PTN3944 that contains a single data byte. The LS bit indicates if the command that is being executed will read or write data from/to the device. The other 7 bits are the device slave address. The single data byte followed is the register offset that is used to indicate which register address is being accessed (read or written). The data phase is a second I²C transaction that starts with 7-bit slave address, with LS bit set to 1 indicating a read operation, followed by an 8-bit data read back from the device register address.



(1) R/W = read/write bit. 0b = I²C write; 1b = I²C read

Figure 4. I²C read sequence

The write sequence starts with 7-bit slave address, with LS bit set to 0 indicating a write access. The next byte is the register offset that is used to indicate which device register address is being written to. The last byte is the 8-bit register data that will be written to the device register address.



(1) R/$\overline{W}$ = read/write bit. 0b = I^2C write; 1b = I^2C read

Figure 5. I^2C write sequence

7.2.5.2 Multi-byte register reads/writes

Reading one or more registers

The slave recognizes the following procedure as a request to read one or more registers:

1. Master asserts START condition or repeated-START condition
2. Master addresses PTN3944's slave address with R/W bit set as "Write"
3. Slave acknowledges the request by asserting ACK
4. Master writes the desired starting register address
5. Slave acknowledges the register address with ACK, even if the register address is not part of the defined register map
6. Master issues a repeated-START condition
7. Master addresses PTN3944's slave address with R/W bit set as "Read"
8. In the following clock pulses, the slave clocks out the value of the requested register
9. If master wishes to read the next consecutive register, it issues an ACK and then provides another set of clock pulses, whereby the slave supplies the value of the next register. As long as the master continues to issue ACK and supplies additional clock pulses, the slave continues to supply the value of consecutive registers. If the master attempts to read consecutive registers that do not exist in the defined register space the slave returns undefined data value of 0xFF
10. When the master does not wish to read additional consecutive registers, it supplies a NACK in response to the final register value it wishes to read and then issues a STOP or repeated-START condition.

Figure 6 provides an illustrative example where the master chooses to read from two consecutive registers starting with register "R".

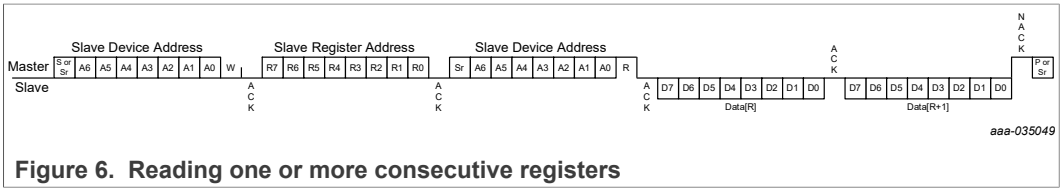


Figure 6. Reading one or more consecutive registers

Writing one or more registers

The slave recognizes the following procedure as a request to write to one or more registers.

1. Master asserts START condition or repeated-START condition
2. Master addresses PTN3944's slave address with R/W bit set as "Write"
3. Slave acknowledges the request by asserting ACK
4. Master writes the desired starting register address
5. Slave acknowledges the register address with ACK, even if register address is not part of the defined register map
6. Master writes the data for that register address. Slave updates the value of that register once all 8 bits of data have been written
7. Slave acknowledges the data with ACK
8. If the master wishes to write to the next consecutive register address, it supplies another data byte, which the slave ACKs. The master continues writing data bytes for consecutive registers. If the master writes to more consecutive registers than exist in the register map, the slave discards the extra data bytes, but ACKs each byte. When the master finishes writing the desired register(s), it issues either a STOP condition or a repeated-START condition

   Figure 7 provides an illustrative example where the master chooses to write to three consecutive registers starting with register "R".

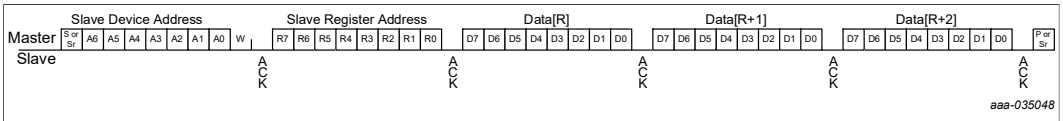


Figure 7. Writing one or more consecutive registers

8 Limiting values

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

In accordance with the Absolute Maximum Rating System (IEC 60134).

Table 10. Limiting values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{DD}[1]	Supply voltage	1.8 V digital supply voltage	-0.5		+2.2	V	LTC-VOL-PRIO1-001
V_{CCXX}[1]	Supply voltage for high-speed lanes	VCCA, VCCB, VCCC, VCCD	-0.5		+2.2	V	LTC-VOL-PRIO1-002
V_I[1]	Input voltage	SCL, SDA, LCTL1, LCTL2, LCTL3, FG1, FG2, ADDR1, ADDR2, ADDR3, and ADDR4 pins	-0.5		+3.6	V	LTC-VOL-PRIO1-005
		High-speed pins	-0.5		+2.5	V	LTC-VOL-PRIO1-006
T_{stg}	Storage temperature		-65		+150	°C	LTC-TMP-PRIO1-007
V_{esd}	Electro Static Discharge	HBM[2] for High-speed	1500			V	LTC-VOL-PRIO1-008
		HBM for other control pins	1500			V	LTC-VOL-PRIO1-009
		CDM[3] for High-speed	1000			V	LTC-VOL-PRIO1-010
		CDM for other control pins	1000			V	LTC-VOL-PRIO1-011
$R_{th(j-a)}$	Thermal resistance from junction to ambient environment	JEDEC still air test environment		40.6		°C/W	LTC-RES-PRIO2-012
$R_{th(j-c)}$	Thermal resistance from junction to case			16.8		°C/W	LTC-RES-PRIO2-013
$R_{th(j-b)}$	Thermal resistance from junction to board	FR4 PCB material and with center pad soldered with recommended solder pad structure		19.7		°C/W	LTC-RES-PRIO2-014

[1] All voltage values, except differential voltages, are with respect to network ground terminal.
[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model – Component level; Electrostatic Discharge Association, Rome, NY, USA.
[3] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model – Component level; Electrostatic Discharge Association, Rome, NY, USA

9 Recommended operating conditions

Over operating free-air temperature range (unless otherwise noted). Typical values are specified for 1.8 V and 25 °C operating temperature.

Table 11. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{DD}	Supply voltage	1.8 V Digital Supply voltage	1.7	1.8	1.9	V	ROC-VOL-PRIO1-001
V_{CC}	Supply voltage for high-speed lanes	VCCA, VCCB, VCCC, VCCD	1.7	1.8	1.9	V	ROC-VOL-PRIO1-002
V_I	Input voltage	SCL, SDA, LCTL1, LCTL2, LCTL3, FG1 and FG2 pins	-0.3		+3.6	V	ROC-VOL-PRIO1-003
		ADDR1, ADDR2, ADDR3, and ADDR4 pins	-0.3		V_{DD}	V	ROC-VOL-PRIO1-004
		High-speed Data pins	-0.3		V_{CC}+0.3	V	ROC-VOL-PRIO1-005
V_{SYS}	Power supply voltage for GPIO control signals		1.7		3.6	V	ROC-VOL-PRIO1-006
	Power supply voltage for I^2C signals		1.08		3.6	V	ROC-VOL-PRIO1-007
T_{amb}	Ambient temperature	Operating in free air	-20	-	+85	°C	ROC-TMP-PRIO1-008

10 Characteristics

10.1 Device characteristics

Table 12. Device characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{GND_VCC} noise	Noise voltage from DUT (50 Hz to 1 MHz) GND noise/bounce with VCC as the reference point	DUT only and No bypass cap during testing Test recommendations: Battery powered DUT with VCC pin as the reference power plan and measure the GND pin ground bounce. Measured by power rail probe.		18		mV_{PP}	DEV-VOL-PRIO2-001
	Noise voltage (1 MHz to 10 MHz)			18		mV_{PP}	DEV-VOL-PRIO2-002
	Noise voltage (10 MHz to 5 GHz)				10	mV_{PP}	DEV-VOL-PRIO1-003
CMRR	Common Mode Rejection Ratio Δ(Vcm,rx)/Δ(Vout_diff)	10 MHz to 1 GHz		30		dB	DEV-DB-PRIO2-004
PSRR	Power Supply Rejection Ratio Δ(VCC)/Δ(Vout_diff)	10 MHz to 200 MHz		41		dB	DEV-DB-PRIO2-005
$t_{Startup}$	Start-up time	Between supply voltage exceeding 1.4 V until sampling of channel configuration control pins	-		3	ms	DEV-TIM-PRIO1-006
t_{PD}	Differential Propagation Delay	Differential propagation delay between 50 % level at input and output pins		70	90	ps	DEV-TIM-PRIO1-011
Gp	Peaking gain (compensation at 8 GHz, with respect to gain at 10 MHz; sinusoidal input of 100 mVppd)	LCTL[2:1] = Open; Open; (Table 5)		18.3		dB	DEV-DB-PRIO2-075
Gp,var	Peaking gain variation over Gp at 8 GHz		-1.5		+1.5	dB	DEV-DB-PRIO1-076
Gf	Flat gain at 10 MHz	Flat gain disabled (Table 7)		-0.7		dB	DEV-DB-PRIO2-077
		Flat gain enabled (Table 7)		+0.7		dB	DEV-DB-PRIO2-078
Gf,var	Flat gain variation over Gf at 10 MHz		-1.2	-	+1.2	dB	DEV-DB-PRIO1-079
OLS_{10M}	-1 dB compression point of output linear swing at 10 MHz	LCTL3 = I^2C (based on I^2C register settings)		504		mV_{PP}	DEV-VOL-PRIO2-080
		LCTL3 = Open Table 6		646		mV_{PP}	DEV-VOL-PRIO2-081
		LCTL3 = 0 Table 6		810		mV_{PP}	DEV-VOL-PRIO2-082
		LCTL3 = 1 Table 6		923		mV_{PP}	DEV-VOL-PRIO2-083
OLS_{4G}	-1 dB compression point of output linear swing at 4 GHz	LCTL3 = I^2C (based on I^2C register settings)		458		mV_{PP}	DEV-VOL-PRIO2-084
		LCTL3 = Open (Table 6)		613		mV_{PP}	DEV-VOL-PRIO2-085
		LCTL3 = 0 (Table 6)		754		mV_{PP}	DEV-VOL-PRIO2-086
		LCTL3 = 1 (Table 6)		917		mV_{PP}	DEV-VOL-PRIO2-087
OLS_{8G}	-1 dB compression point of output linear swing at 8 GHz	LCTL3 = I^2C (based on I^2C register settings)		560		mV_{PP}	DEV-VOL-PRIO2-088
		LCTL3 = Open (Table 6)		712		mV_{PP}	DEV-VOL-PRIO2-089

Table 12. Device characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
		LCTL3 = 0 (Table 6)		860		mV_{PP}	DEV-VOL-PRIO2-090
		LCTL3 = 1 (Table 6)		1014		mV_{PP}	DEV-VOL-PRIO2-091
V_{noise_in}	Input referred noise	100 MHz to 15 GHz; Peaking gain of 8.4 dB (FGx =-0.7 dB) at 8 GHz and OLS 950 mV_{ppd}		0.8		mV_{rms}	DEV-VOL-PRIO2-035
		100 MHz to 15 GHz; Peaking gain of 14.7 dB (FGx =-0.7 dB) at 8 GHz and OLS 950 mV_{ppd}		1.0		mV_{rms}	DEV-VOL-PRIO2-036
V_{noise_out}	Output referred noise	100 MHz to 15 GHz; Peaking gain of 8.5 dB (FGx =-0.7 dB) at 8 GHz and OLS 950 mV_{ppd}		2.0		mV_{rms}	DEV-VOL-PRIO2-037
		100 MHz to 15 GHz; Peaking gain of 15.6 dB (FGx =-0.7 dB) at 8 GHz and OLS 950 mV_{ppd}		2.0		mV_{rms}	DEV-VOL-PRIO2-038
I_{DD}	Supply current All four channels are active	-1 dB compression point at 950 mV_{ppd}		250	270	mA	DEV-CUR-PRIO1-044
		-1 dB compression point at 800 mV_{ppd}		225	260	mA	DEV-CUR-PRIO1-045
		-1 dB compression point at 650 mV_{ppd}		200	240	mA	DEV-CUR-PRIO1-046
		-1 dB compression point at 500 mV_{ppd}		190	230	mA	DEV-CUR-PRIO1-047
	Supply current two channels are active	-1 dB compression point at 950 mV_{ppd}		125	140	mA	DEV-CUR-PRIO1-048
		-1 dB compression point at 800 mV_{ppd}		110	130	mA	DEV-CUR-PRIO1-049
		-1 dB compression point at 650 mV_{ppd}		115	120	mA	DEV-CUR-PRIO1-050
		-1 dB compression point at 500 mV_{ppd}		100	120	mA	DEV-CUR-PRIO1-051
	Supply current One channel is active	-1 dB compression point at 950 mV_{ppd}		62	75	mA	DEV-CUR-PRIO1-052
		-1 dB compression point at 800 mV_{ppd}		57	70	mA	DEV-CUR-PRIO1-053
		-1 dB compression point at 650 mV_{ppd}		52	65	mA	DEV-CUR-PRIO1-054
		-1 dB compression point at 500 mV_{ppd}		47	60	mA	DEV-CUR-PRIO1-055
DDNEXT	Near end cross talk for adjacent high-speed channels	at 8 GHz		-60		dB	DEV-DB-PRIO2-092
DDFEXT	Far end cross talk	at 8 GHz highest peaking gain			-50	dB	DEV-DB-PRIO2-093

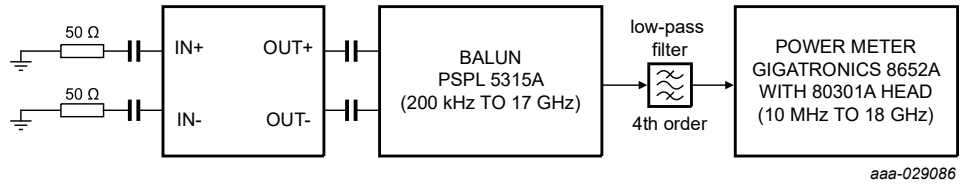


Figure 8. Noise test configuration

10.2 Input AC/DC characteristics

Table 13. Input AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
$C_{ac\_coupling}$	AC coupling capacitance		176		265	nF	INC-CAP-PRIO1-016
$T_{Discharge}$	Discharge time				250	ms	INC-TIM-PRIO1-003
R_{in-DC}	Input DC common mode impedance		21		34	Ω	INC-RES-PRIO1-004
$V_{RX-CM-AC-PP}$	RX AC common mode voltage tolerance	A single tone test at 120 MHz is deemed to be an adequate stress test			300	mV_{pp}	INC-VOL-PRIO1-005
$V_{RX-CM-PP1}$	RX AC common mode voltage tolerance	A single tone test at 400 MHz is deemed to be an adequate stress test			100	mV_{pp}	INC-VOL-PRIO1-006
$R_{IN-DIFF-DC}$	DC Differential Impedance		90		131	Ω	INC-RES-PRIO1-007
$V_{IP-DC-CM}$	DC biasing/common mode voltage	Biasing on all SuperSpeed pins		1.8		V	INC-VOL-PRIO2-008
$V_{voltage\_jump}$	Maximum voltage jump on left side pins (measured before AC coupling capacitors)	Applicable during power-on/power-off, transition from low power to active state and vice versa	-0.3		+1.0	V	INC-VOL-PRIO1-009
$Z_{IN-HIGH-IMP-DC-POS}$	DC Input High Impedance; V_{DD} > 0 during Reset or power down	DC common-mode input impedance when output of redriver is not terminated and V_{DD} between 1.7 V and 1.9 V.	10			kΩ	INC-RES-PRIO1-010
$V_{RX-DIFF-PP}$	Input voltage (peak to peak differential signal)		45		1200	mV_{ppd}	INC-VOL-PRIO1-012
$RL_{DD11, IN}$	Input differential mode Return Loss	10 MHz to 12 GHz		15		dB	INC-DB-PRIO2-014
$RL_{CC11, IN}$	Input common mode Return Loss	10 MHz to 12 GHz		12		dB	INC-DB-PRIO2-015

10.3 Output AC/DC characteristics

Table 14. Output AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
R_{OP-DC}	Output DC common mode Impedance		21		34	Ω	OUC-RES-PRIO1-001
$R_{OP-DIFF-DC}$	Output Differential Impedance		89		131	Ω	OUC-RES-PRIO1-002
$V_{OP-DC-CM}$	DC biasing/common mode voltage	1 dB Compression point at 950 mV		1.2		V	OUC-VOL-PRIO2-003
		1 dB Compression point at 800 mV		1.3		V	OUC-VOL-PRIO2-004
		1 dB Compression point at 650 mV		1.4		V	OUC-VOL-PRIO2-005
		1 dB Compression point at 500 mV		1.5		V	OUC-VOL-PRIO2-006
$V_{TX-CM-AC-PP\_ACTIVE}$	Output AC Common mode output voltage in active state	Device input fed with differential signal			20	mV_{pp}	OUC-VOL-PRIO1-007
$V_{TX-IDLE-DIFF-AC-pp}$	Output AC differential output voltage	When link is in electrical idle			10	mV_{ppd}	OUC-VOL-PRIO1-008
$V_{voltage\_jump}$	Maximum voltage jump on right side pins (measured after AC coupling capacitors)	Applicable during power-on/power-off, transition from low power to active state and vice versa	-0.3		1.0	V	OUC-VOL-PRIO1-009
V_{DETECT}	Voltage change allowed during USB receiver detection	Positive voltage swing to sense the receiver termination detection			600	mV	OUC-VOL-PRIO1-010
$RL_{DD11, OP}$	Output differential mode Return Loss	10 MHz to 12 GHz		18		dB	OUC-DB-PRIO2-011
$RL_{CC11, OP}$	Output common mode Return Loss	10 MHz to 12 GHz		12		dB	OUC-DB-PRIO2-012

All S-parameter measurements are with respect to 100 Ω differential impedance reference and 50 Ω single-ended impedance reference.

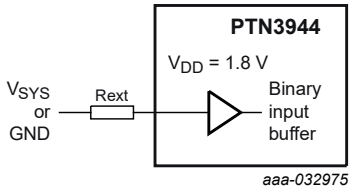


Figure 9. Binary GPIO input buffer setting

10.4 Ternary control characteristics for LCTL[1, 2, 3] and FG[2:1] pins

Table 15. Ternary control input characteristics (external system voltage V_{SYS}= 1.7 V to 3.6 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{IH}	High level voltage	External pull-up 1 kΩ resistor to V_{SYS}	0.8*V_{DD}		V_{SYS}	V	TER-VOL-PRIO1-001
V_{IM}	Unconnected or open condition		0.35*V_{DD}		0.45* V_{DD}	V	TER-VOL-PRIO1-002
V_{IL}	Low level voltage	External pull-down 1 kΩ resistor to GND			0.15* V_{DD}	V	TER-VOL-PRIO1-003
I_{IL}	Leakage current when pin is not active	VDD = 1.8 V, pull-up resistor connected to V_{SYS} = 3.6 V			15	µA	TER-CUR-PRIO1-004
		VDD = 1.8 V, pull-up resistor connected to V_{SYS} = 1.8 V			1	µA	TER-CUR-PRIO1-005
	Leakage current when pin is active	VDD = 1.8 V, pull-up resistor connected to V_{SYS} = 3.6 V			80	µA	TER-CUR-PRIO1-006
		VDD = 1.8 V, pull-up resistor connected to V_{SYS} = 1.8 V	-25		35	µA	TER-CUR-PRIO1-007
I_{bck}	Back current sunk from pin to powered down supply	V_{DD} = 0, V_{SYS} = 3.6 V			20	µA	TER-CUR-PRIO1-008
R_{pu}	Internal pull-up resistance			120		kΩ	TER-RES-PRIO2-009
R_{pd}	Internal pull-down resistance			80		kΩ	TER-RES-PRIO2-010
C_{pin}	Maximum allowed capacitance at the pin				10	pF	TER-CAP-PRIO1-011

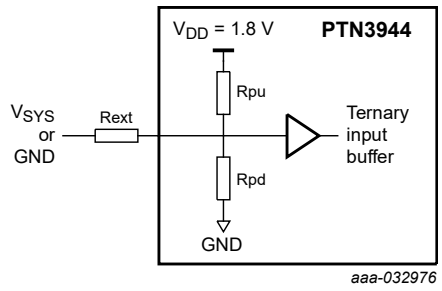


Figure 10. Ternary GPIO input buffer setting

10.5 Binary control characteristics ADDR2, ADDR3, and ADDR4 pins

Table 16. Binary control characteristics ADDR2, ADDR3, and ADDR4 pins (external system voltage V_{SYS} = 1.7 V to 3.6 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{IH}	High level voltage	ADDR3, ADDR4	$0.7*V_{DD}$	-	V_{SYS}	V	BIN-VOL-PRIO1-001
		ADDR2	$0.7*V_{DD}$	-	V_{SYS}	V	BIN-VOL-PRIO1-003
V_{IL}	Low level voltage	ADDR3, ADDR4			$0.3*V_{DD}$	V	BIN-VOL-PRIO1-002
		ADDR2			$0.22*V_{DD}$	v	BIN-VOL-PRIO1-004
I_{IL}	Leakage current		-1		+4	µA	BIN-CUR-PRIO1-007

10.6 Quaternary control characteristics for ADDR1 pin

Table 17. Quaternary control input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{IH1}	High level voltage	Pin connected to V_{DD}	0.9*V_{DD}		V_{DD}+ 0.3	V	QAT-VOL-PRIO1-001
V_{IH2}	High level voltage	R_{ext} = 56 kΩ (10 % resistor) pull-up to V_{DD}	0.575* V_{DD}		0.725* V_{DD}	V	QAT-VOL-PRIO1-002
V_{IM}	Voltage at unconnected/ open condition	R_{ext} = 200 kΩ (10 % resistor) pull-up to V_{DD}	0.275* V_{DD}		0.425* V_{DD}	V	QAT-VOL-PRIO1-003
V_{IL}	Low level voltage	Pin connected to GND			0.1* V_{DD}	V	QAT-VOL-PRIO1-004
I_{IL}	Leakage current at the pin	Pin voltage = 3.6 V			20	µA	QAT-CUR-PRIO1-005
I_{bck}	Back current sunk from pin to powered down supply	V_{DD} = 0; Pin voltage = 3.6 V			20	µA	QAT-CUR-PRIO1-006
R_{pd}	Internal pull-down resistance			105		kΩ	QAT-RES-PRIO2-007
C_{pin}	Maximum allowed capacitance at the pin				10	pF	QAT-CAP-PRIO1-008

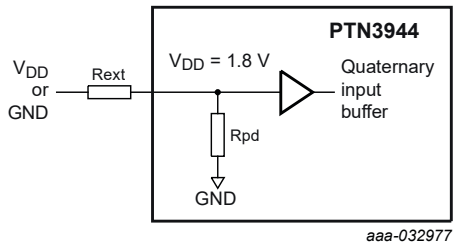


Figure 11. Quaternary input buffer setting

10.7 I^2C AC/DC characteristics

Table 18. I^2C interface; AC/DC characteristics for SCL and SDA pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
F_{I2C}	I^2C Clock frequency		0		1000	kHz	SER-FRQ-PRIO1-001
V_{IH}	HIGH-level Input voltage		1.19		3.6	V	SER-VOL-PRIO1-002
V_{IL}	LOW-level Input voltage				0.57	V	SER-VOL-PRIO1-003
V_{hys}	Hysteresis of Schmitt trigger inputs	V_{pullup} < 3.6 V	0.095			V	SER-VOL-PRIO1-004
V_{OL}	LOW-level output voltage at 2mA sink current	V_{pullup} < 3.6 V	0		0.4	V	SER-VOL-PRIO1-005
I_{OL}	LOW-level output current	VOL =0.4 V; Standard and Fast modes	3			mA	SER-CUR-PRIO1-006
		VOL =0.4 V; Fast mode plus	20			mA	SER-CUR-PRIO1-007
		VOL =0.6 V; Fast mode	6			mA	SER-CUR-PRIO1-008
I_{IL}	LOW-level input current	Pin voltage - 0.1* V_{pullup} to 0.9*$V_{pullup, max}$	-10		10	µA	SER-CUR-PRIO1-009
C_I	Capacitance of I/O pin				10	pF	SER-CAP-PRIO1-010
$t_{HD,STA}$	Hold time (repeated) START condition	Fast mode plus; After this period, the first clock pulse is generated	0.26			µs	SER-TIM-PRIO1-011
t_{LOW}	LOW period of I^2C clock	Fast mode plus	0.5			µs	SER-TIM-PRIO1-012
t_{HIGH}	HIGH period of I^2C clock	Fast mode plus	0.26			µs	SER-TIM-PRIO1-013
$T_{SU,STA}$	Setup time (repeated) START condition	Fast mode plus	0.26			µs	SER-TIM-PRIO1-014
$T_{HD,DAT}$	Data Hold time	Fast mode plus	0			µs	SER-TIM-PRIO1-015
$T_{SU,DAT}$	Data Setup time	Fast mode plus	50			ns	SER-TIM-PRIO1-016
T_r	Rise time of I^2C_SCL and I^2C_SDA signals	Fast mode plus	-		120	ns	SER-TIM-PRIO1-017
T_f	Fall time of I^2C_SCL and I^2C_SDA signals	Fast mode plus	-		120	ns	SER-TIM-PRIO1-018
$T_{SU,STO}$	Setup time for STOP condition	Fast mode plus	0.26			µs	SER-TIM-PRIO1-019
t_{BUF}	Bus free time between STOP and START condition	Fast mode plus	0.5			µs	SER-TIM-PRIO1-020
$t_{VD,DAT}$	Data valid time	Fast mode plus			0.45	µs	SER-TIM-PRIO1-021
$t_{VD,ACK}$	Data valid acknowledge time	Fast mode plus			0.45	µs	SER-TIM-PRIO1-022
t_{SP}	Pulse width of spikes that must be suppressed by input filter		0		50	ns	SER-TIM-PRIO1-023

Note: V_{pullup} is external pull-up voltage on SCL and SDA pins. The voltage can be up to 3.3 V from another power supply.

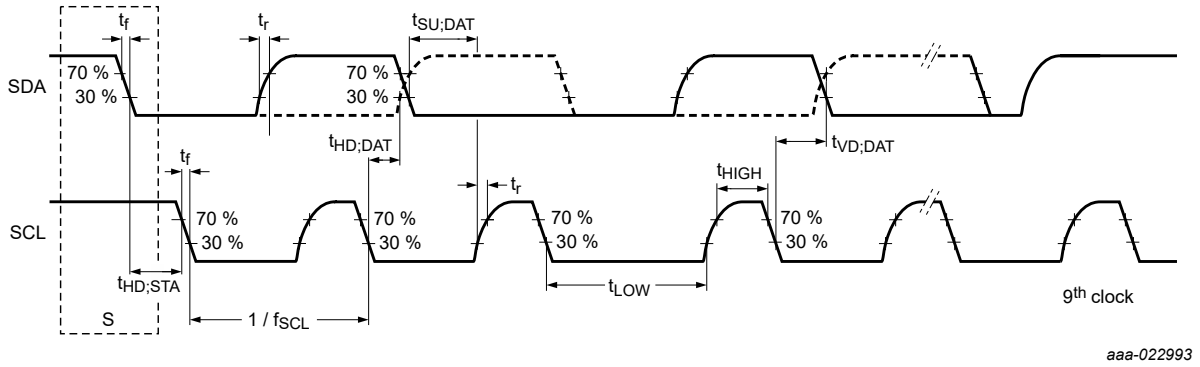


Figure 12. I^2C-bus timing diagram

11 Package outline

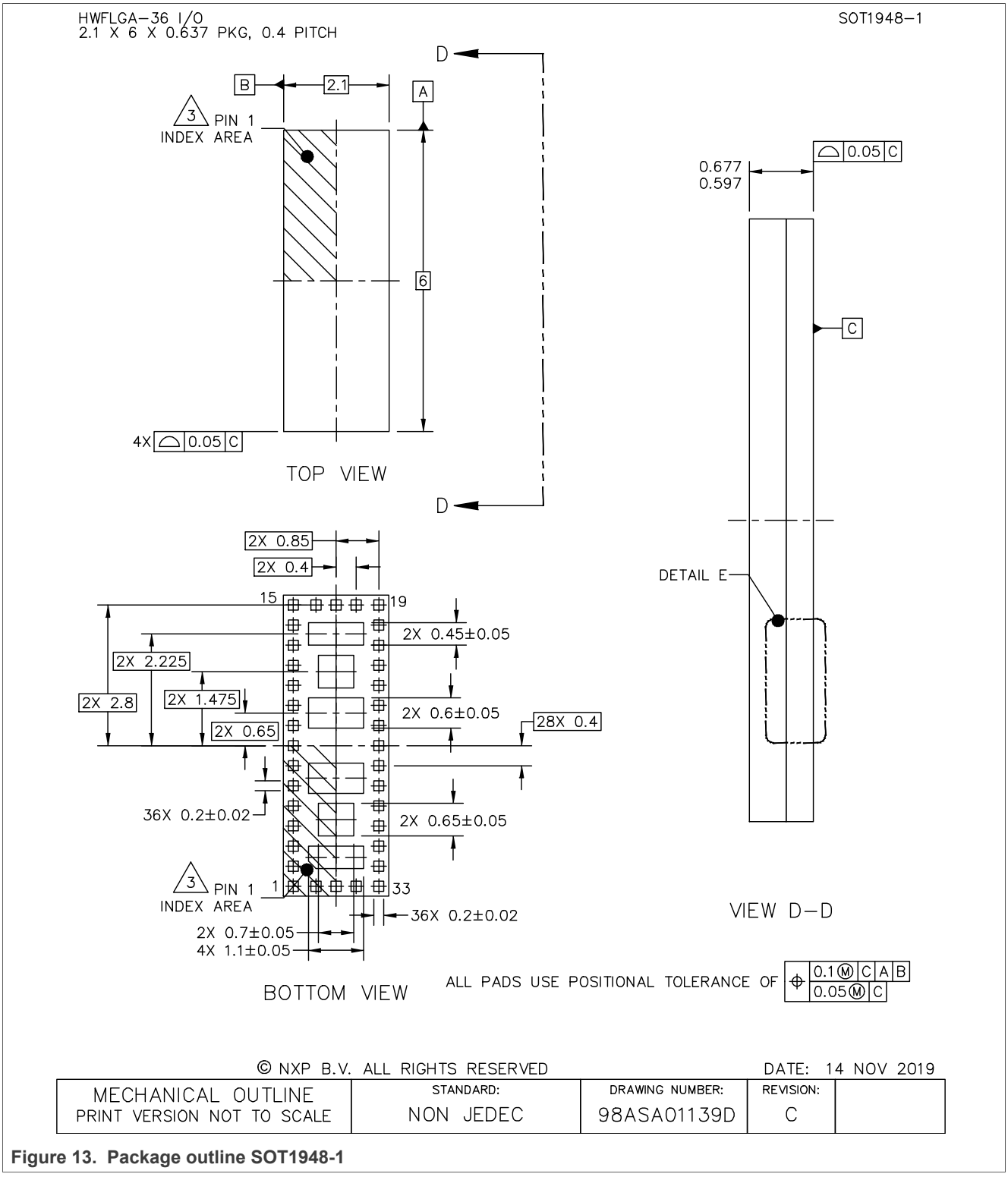


Figure 13. Package outline SOT1948-1

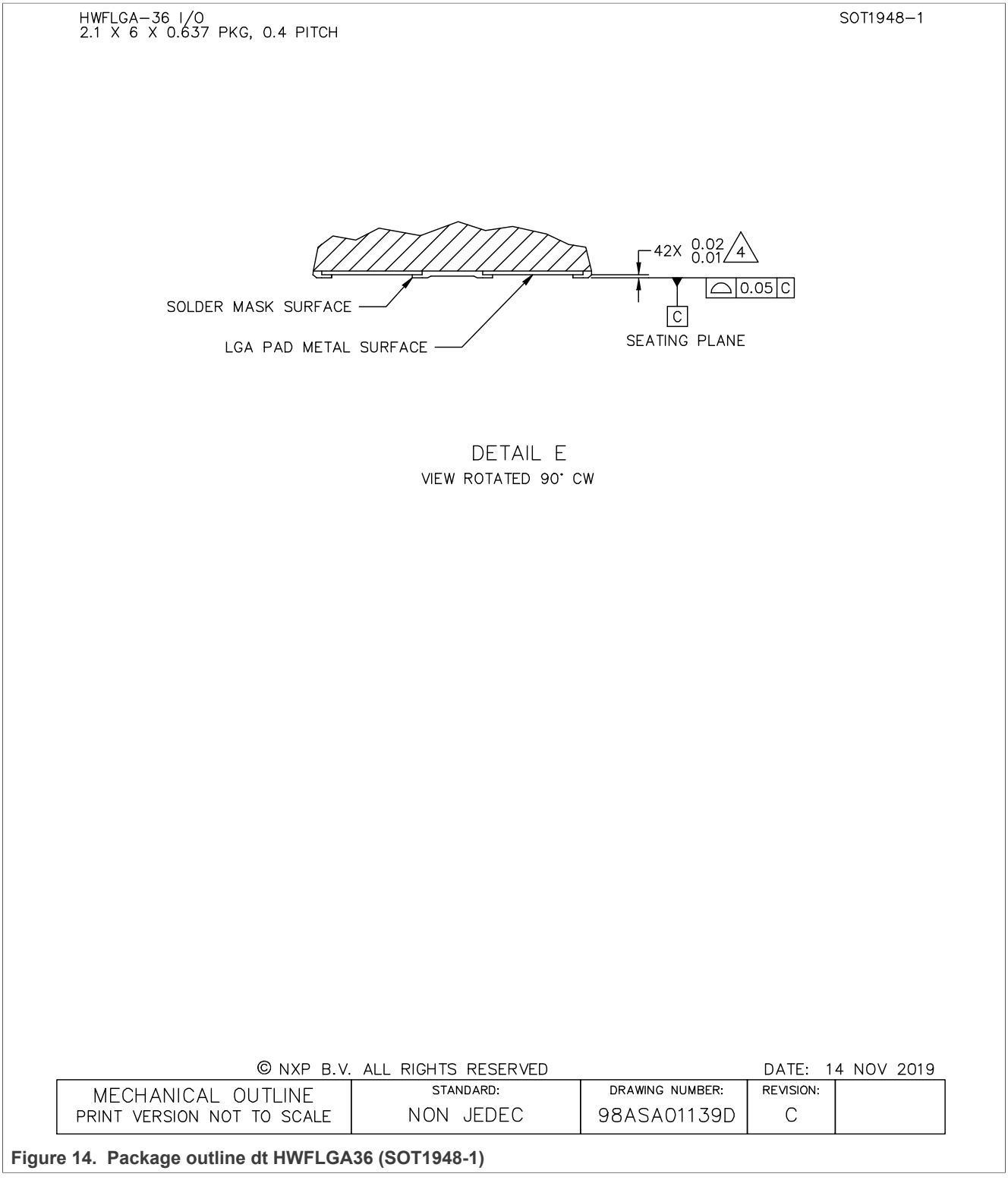


Figure 14. Package outline dt HWFLGA36 (SOT1948-1)

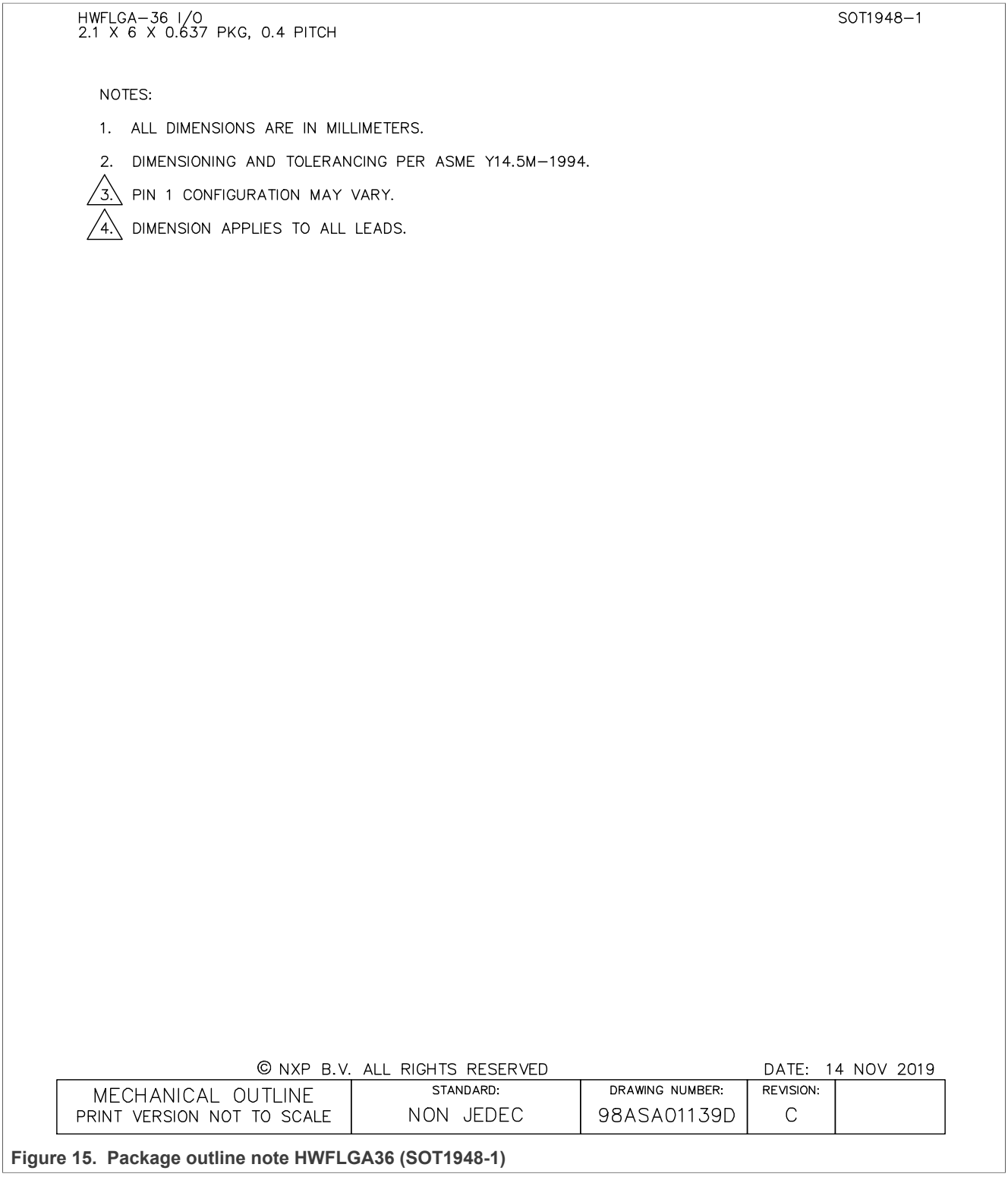


Figure 15. Package outline note HWFLGA36 (SOT1948-1)

12 Packing information

12.1 SOT1948-1; HWFLGA36; reel dry pack, SMD, 13" Q1 standard product orientation ordering code (12NC) ending 019

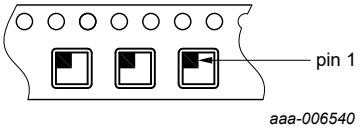
12.1.1 Dimensions and quantities

Table 19. Dimensions and quantities

Reel dimensions d × w (mm)[1]	SPQ/PQ (pcs)[2]	Reels per box
330 × 12	7000	1

[1] d = reel diameter; w = tape width.
[2] Packing quantity dependent on specific product type. View ordering and availability details at NXP order portal, or contact your local NXP representative.

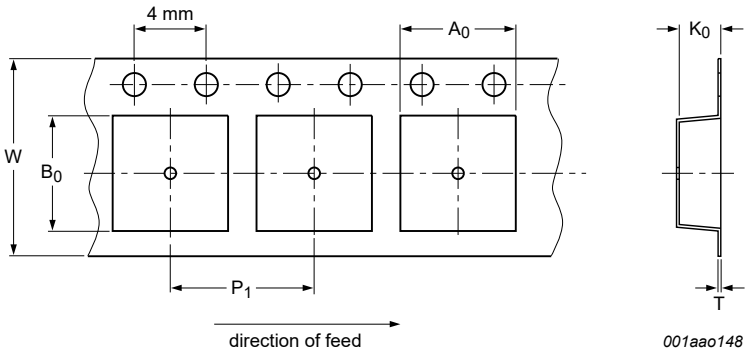
12.1.2 Product orientation



Pin 1 is in quadrant 1.

Figure 16. Product orientation in carrier tape

12.1.3 Carrier tape dimensions



Not drawn to scale.

Figure 17. Carrier tape dimensions

Table 20. Carrier tape dimensions

In accordance with IEC 60286-3/EIA-481.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
2.30 ± 0.05	6.30 ± 0.05	0.85 +.1/-.05	0.30 ± 0.05	8 ± 0.1	12 +0.3/-0.1

13 Soldering

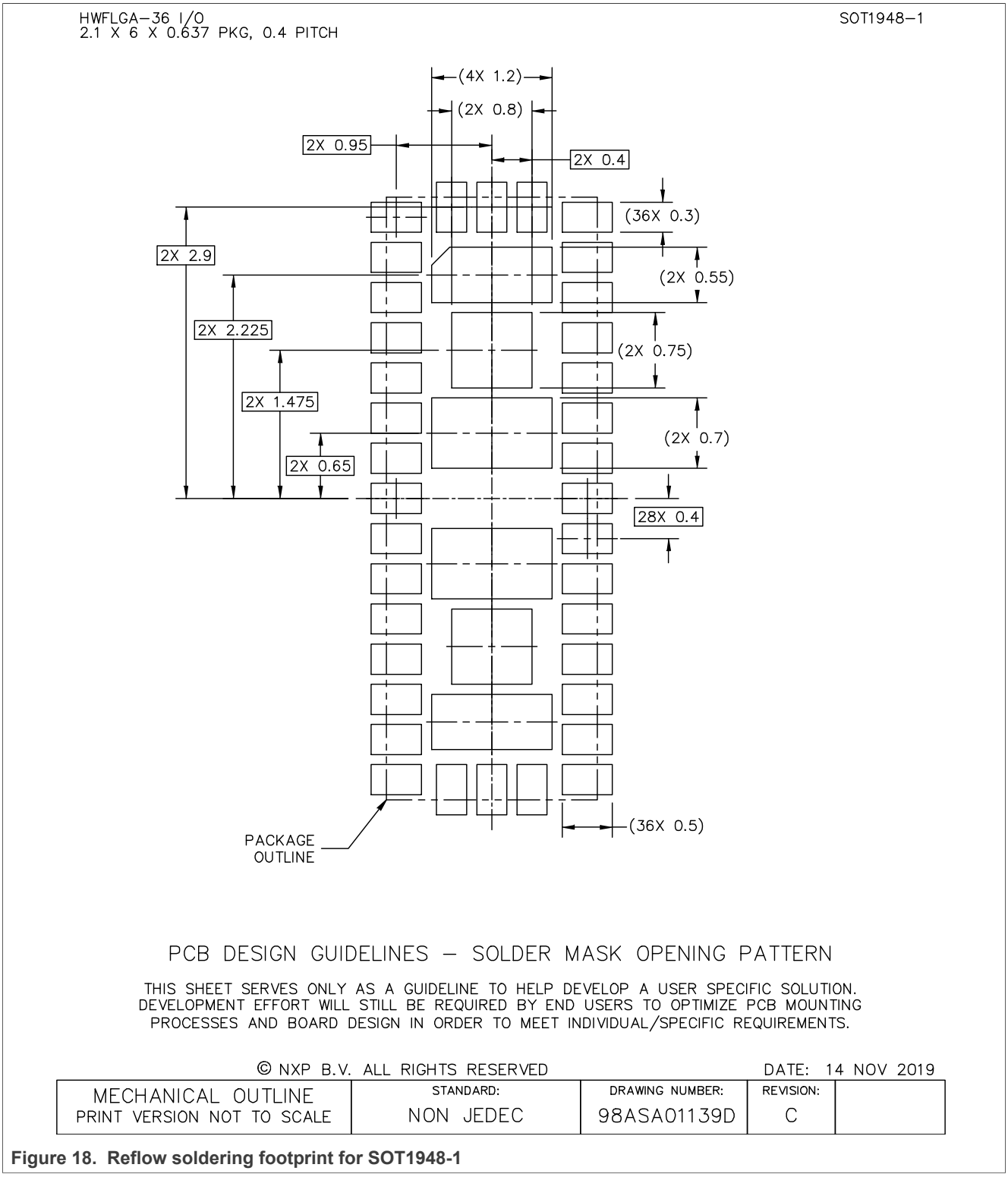


Figure 18. Reflow soldering footprint for SOT1948-1

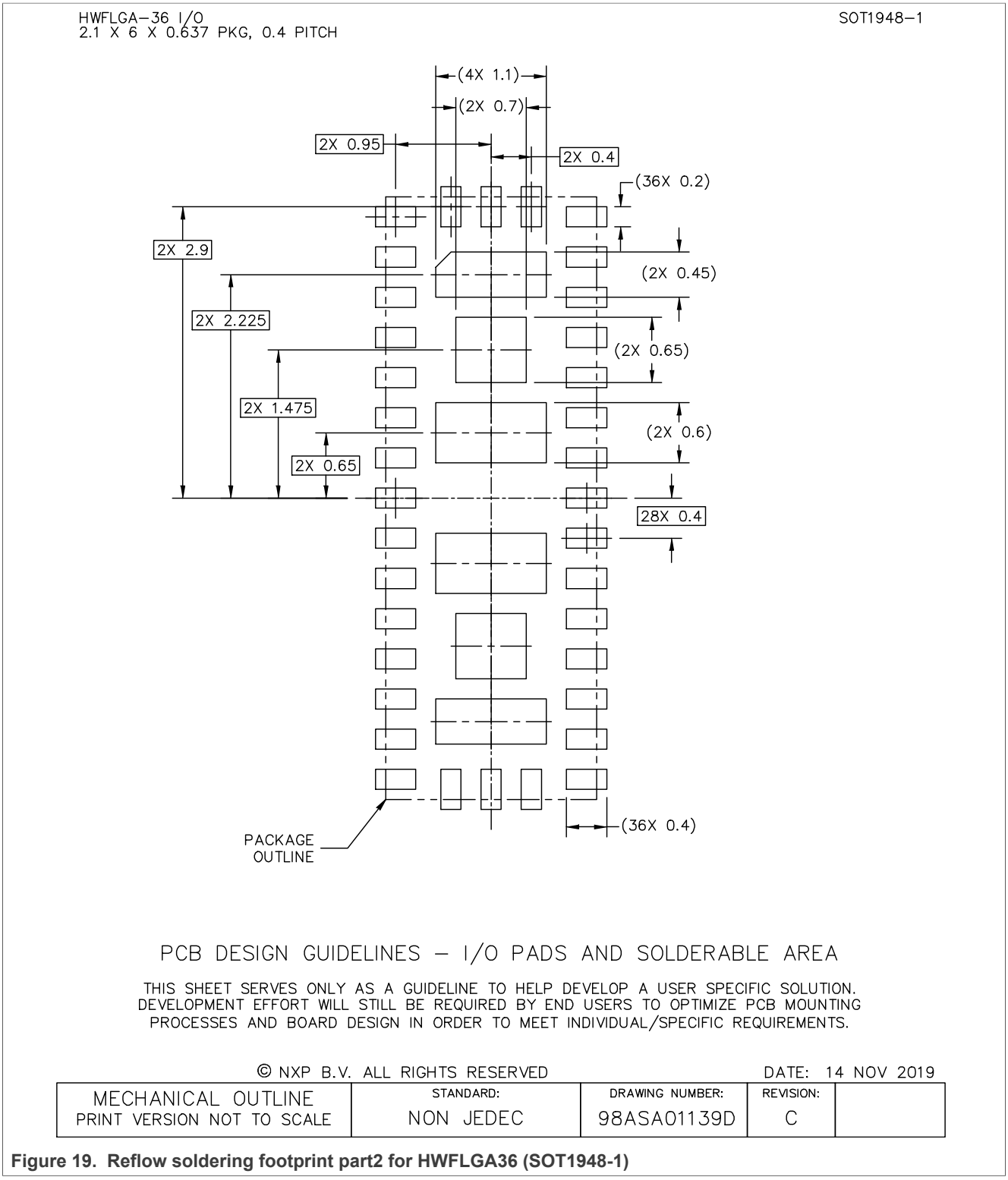
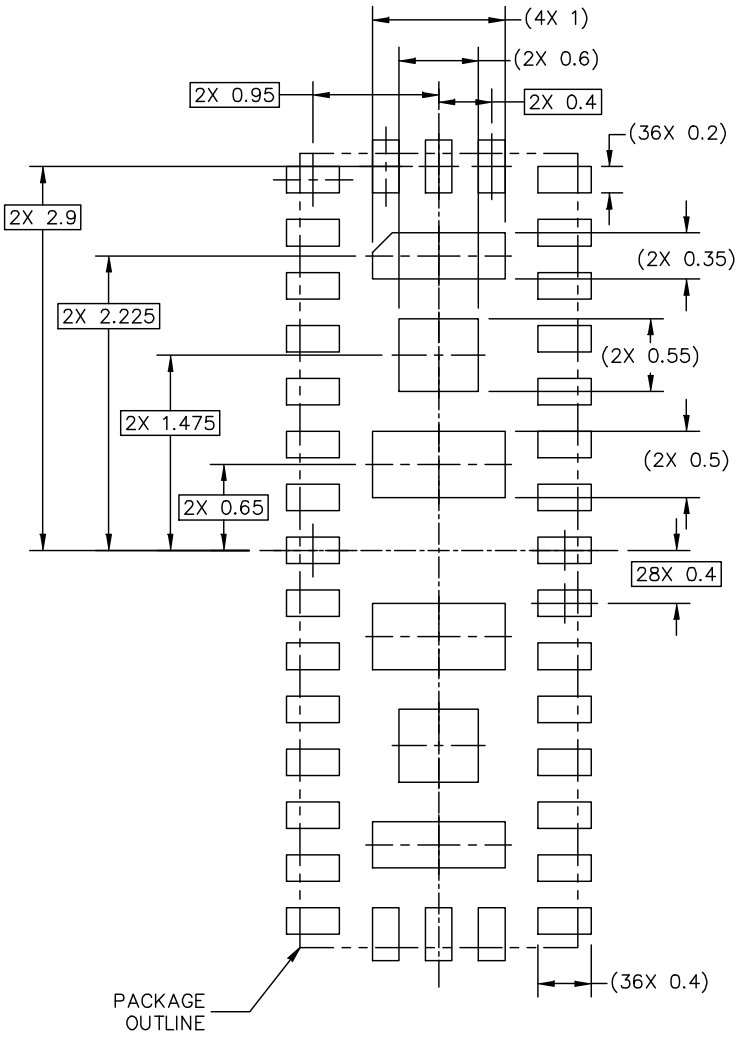


Figure 19. Reflow soldering footprint part2 for HWFLGA36 (SOT1948-1)



RECOMMENDED STENCIL THICKNESS 0.1

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DATE: 14 NOV 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01139D	REVISION: C	

Figure 20. Reflow soldering footprint part3 for HWFLGA36 (SOT1948-1)

14 Abbreviations

Table 21. Abbreviations

Acronym	Description
CDM	Charged Device Model
DS	Downstream
Gbps	Giga bits per second
HBM	Human Body Model
NC	No Connect
PCIe	Peripheral Component Interconnect Express
Rx	Receiver
SI	Signal Integrity
TX	Transmitter
UPI	Ultra Path Interconnect
US	Upstream

15 References

[1] PCI Express Base Specification, Revision 4.0 Version 1.0, Sep 27, 2017

[2] UM10204, "I^2C-bus specification and user manual"; NXP Semiconductors, Rev 6, April 4, 2014

16 Revision history

Table 22. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
PTN3944 v1.1	20210610	Product data sheet	-	PTN3944 v1.0
Modifications:	• Corrected Figure 1			
PTN3944 v1.0	20210607	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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