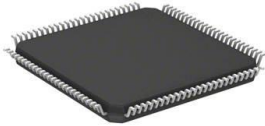


SPC5605BK0CLL6 Datasheet

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| | |
|------------------------------|---|
| DiGi Electronics Part Number | SPC5605BK0CLL6-DG |
| Manufacturer | NXP USA Inc. |
| Manufacturer Product Number | SPC5605BK0CLL6 |
| Description | IC MCU 32BIT 768KB FLASH 100LQFP |
| Detailed Description | e200z0h MPC56xx Qorivva Microcontroller IC 32-Bit Single-Core 64MHz 768KB (768K x 8) FLASH 100-LQFP (14x14) |

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Manufacturer Product Number:

SPC5605BK0CLL6

Series:

MPC56xx Qorivva

DiGi-Electronics Programmable:

Not Verified

Core Size:

32-Bit Single-Core

Connectivity:

CANbus, I2C, LINbus, SCI, SPI

Number of I/O:

77

Program Memory Type:

FLASH

RAM Size:

64K x 8

Data Converters:

A/D 7x10b, 5x12b

Operating Temperature:

-40°C ~ 85°C (TA)

Supplier Device Package:

100-LQFP (14x14)

Base Product Number:

SPC5605

Manufacturer:

NXP USA Inc.

Product Status:

Active

Core Processor:

e200z0h

Speed:

64MHz

Peripherals:

DMA, POR, PWM, WDT

Program Memory Size:

768KB (768K x 8)

EEPROM Size:

64K x 8

Voltage - Supply (Vcc/Vdd):

3V ~ 5.5V

Oscillator Type:

Internal

Mounting Type:

Surface Mount

Package / Case:

100-LQFP

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.31.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A991A2



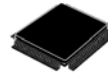
MPC5606BK



100 LQFP
14 mm x 14 mm



144 LQFP
20 mm x 20 mm



176 LQFP
24 mm x 24 mm

MPC5606BK Microcontroller Data Sheet

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

1.2 Description

This family of 32-bit system-on-chip (SoC) microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle.

The advanced and cost-efficient e200z0 host processor core of this automotive controller family complies with the Power Architecture® technology and only implements the VLE (variable-length encoding) APU (Auxiliary Processor Unit), providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

| | | |
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NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.



1.3 Device comparison

Table 1 summarizes the functions of the blocks present on the MPC5606BK.

Table 1. MPC5606BK family comparison¹

| Feature | MPC5605BK | | | MPC5606BK | | |
|---|------------------|------------------|------------------|------------------|------------------|------------------|
| | 100 LQFP | 144 LQFP | 176 LQFP | 100 LQFP | 144 LQFP | 176 LQFP |
| Package | 100 LQFP | 144 LQFP | 176 LQFP | 100 LQFP | 144 LQFP | 176 LQFP |
| CPU | e200z0h | | | | | |
| Execution speed ² | Up to 64 MHz | | | | | |
| Code flash memory | 768 KB | | | 1 MB | | |
| Data flash memory | 64 (4 x 16) KB | | | | | |
| SRAM | 64 KB | | | 80 KB | | |
| MPU | 8-entry | | | | | |
| eDMA | 16 ch | | | | | |
| 10-bit ADC | Yes | | | | | |
| dedicated ³ | 7 ch | 15 ch | 29 ch | 7 ch | 15 ch | 29 ch |
| shared with 12-bit ADC | 19 ch | | | | | |
| 12-bit ADC | Yes | | | | | |
| dedicated ⁴ | 5 ch | | | | | |
| shared with 10-bit ADC | 19 ch | | | | | |
| Total timer I/O ⁵ eMIOS | 37 ch, 16-bit | 64 ch, 16-bit | 37 ch, 16-bit | 64 ch, 16-bit | 37 ch, 16-bit | 64 ch, 16-bit |
| Counter / OPWM / ICOC ⁶ | 10 ch | | | | | |
| O(I)PWM / OPWFMB / OPWMCB / ICOC ⁷ | 7 ch | | | | | |
| O(I)PWM / ICOC ⁸ | 7 ch | 14 ch | | | | |
| OPWM / ICOC ⁹ | 13 ch | 33 ch | | | | |
| SCI (LINFlex) | 4 | 6 | 8 | 4 | 6 | 8 |
| SPI (DSPI) | 3 | 5 | 6 | 3 | 5 | 6 |
| CAN (FlexCAN) | 6 | | | | | |
| I ² C | 1 | | | | | |
| 32 KHz oscillator | Yes | | | | | |
| GPIO ¹⁰ | 77 | 121 | 149 | 77 | 121 | 149 |
| Debug | JTAG | | | | | |

¹ Feature set dependent on selected peripheral multiplexing; table shows example.

² Based on 125 °C ambient operating temperature.

³ Not shared with 12-bit ADC, but possibly shared with other alternate functions.

⁴ Not shared with 10-bit ADC, but possibly shared with other alternate functions.

⁵ Refer to eMIOS section of device reference manual for information on the channel configuration and functions.

⁶ Each channel supports a range of modes including Modulus counters, PWM generation, Input Capture, Output Compare.

⁷ Each channel supports a range of modes including PWM generation with dead time, Input Capture, Output Compare.

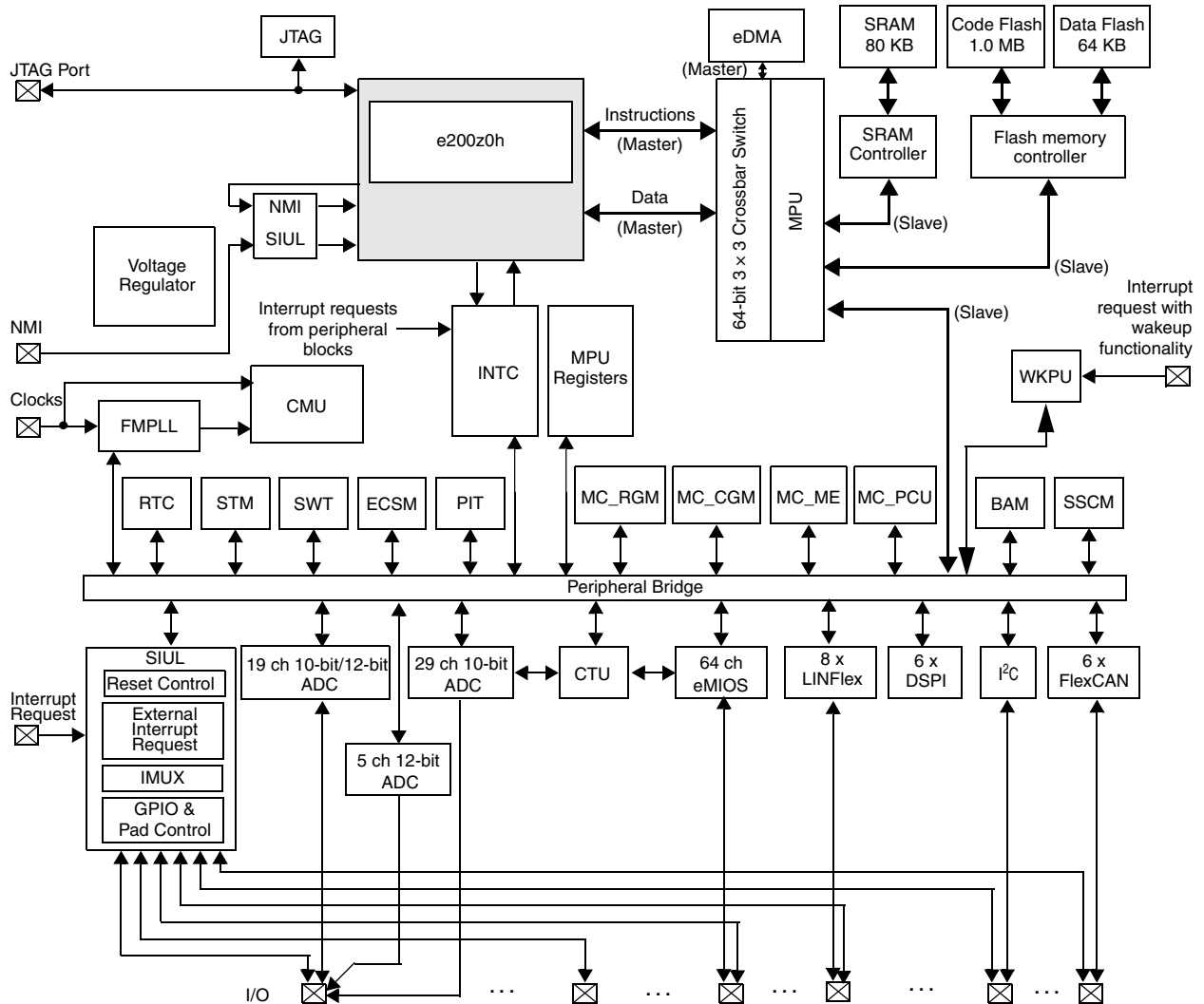
⁸ Each channel supports a range of modes including PWM generation, Input Capture, Output Compare, Period and Pulse width measurement.

⁹ Each channel supports a range of modes including PWM generation, Input Capture, and Output Compare.

¹⁰ Maximum I/O count based on multiplexing with peripherals.

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5606BK.



Legend:

| | | | |
|---------|---------------------------------------|---------|--|
| ADC | Analog-to-Digital Converter | LINFlex | Serial Communication Interface (LIN support) |
| BAM | Boot Assist Module | MC_CGM | Clock Generation Module |
| FlexCAN | Controller Area Network | MC_ME | Mode Entry Module |
| CFlash | Code flash memory | MPU | Memory Protection Unit |
| CMU | Clock Monitor Unit | NMI | Non-Maskable Interrupt |
| CTU | Cross Triggering Unit | MC_PCU | Power Control Unit |
| DFlash | Data flash memory | MC_RGM | Reset Generation Module |
| DSPI | Deserial Serial Peripheral Interface | PIT | Periodic Interrupt Timer |
| eDMA | Enhanced Direct Memory Access | RTC | Real-Time Clock |
| eMIOS | Enhanced Modular Input Output System | SIUL | System Integration Unit Lite |
| FMPLL | Frequency-Modulated Phase-Locked Loop | SRAM | Static Random-Access Memory |
| I2C | Inter-integrated Circuit Bus | SSCM | System Status Configuration Module |
| IMUX | Internal Multiplexer | STM | System Timer Module |
| INTC | Interrupt Controller | SWT | Software Watchdog Timer |
| JTAG | JTAG controller | WKPU | Wakeup Unit |

Figure 1. MPC5606BK block diagram

2 Package pinouts and signal descriptions

2.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions, please see [Table 2](#).

Figure 2 shows the MPC5606BK in the 176 LQFP package.

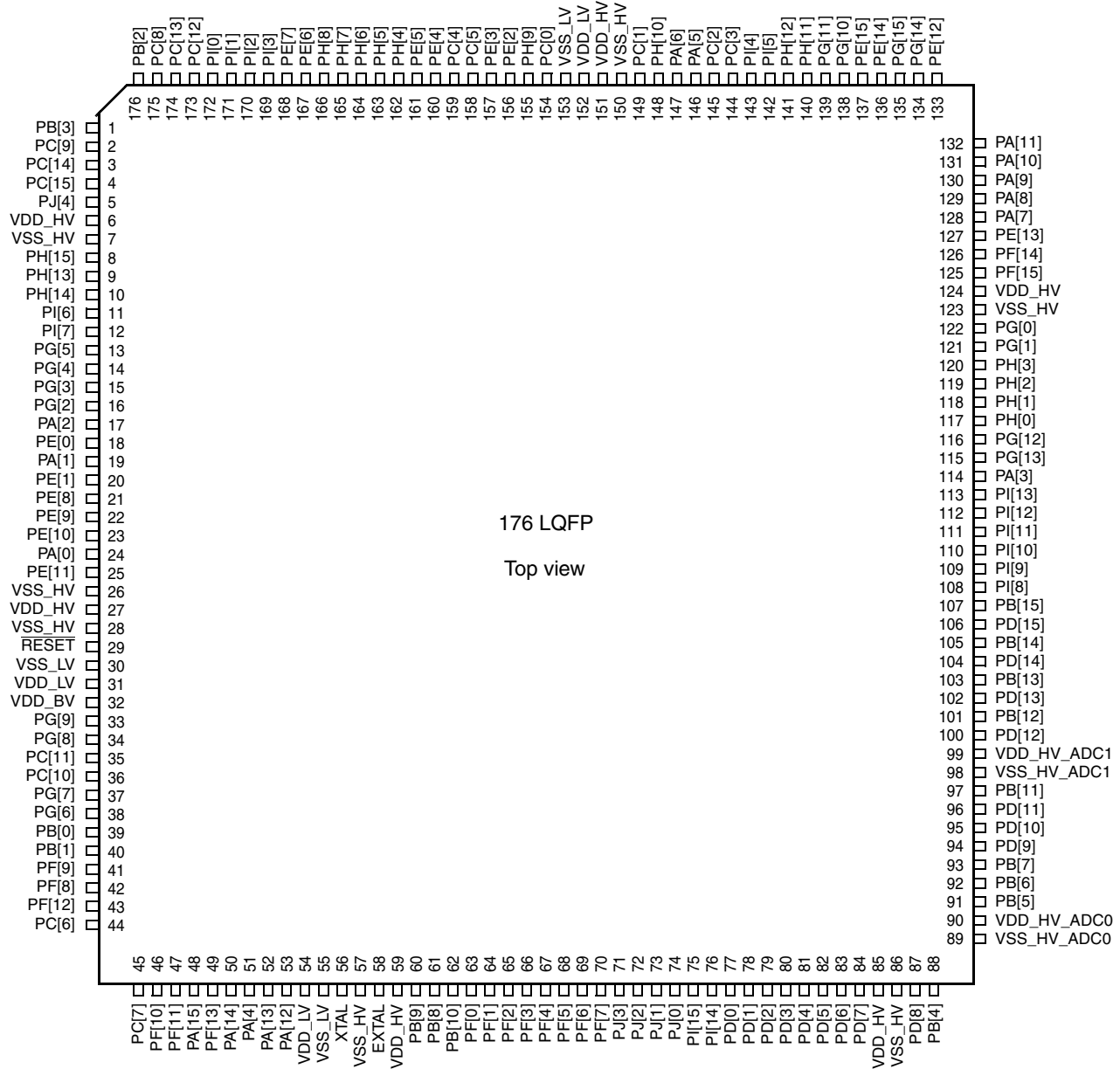


Figure 2. 176 LQFP pinout

Figure 3 shows the MPC5606BK in the 144 LQFP package.

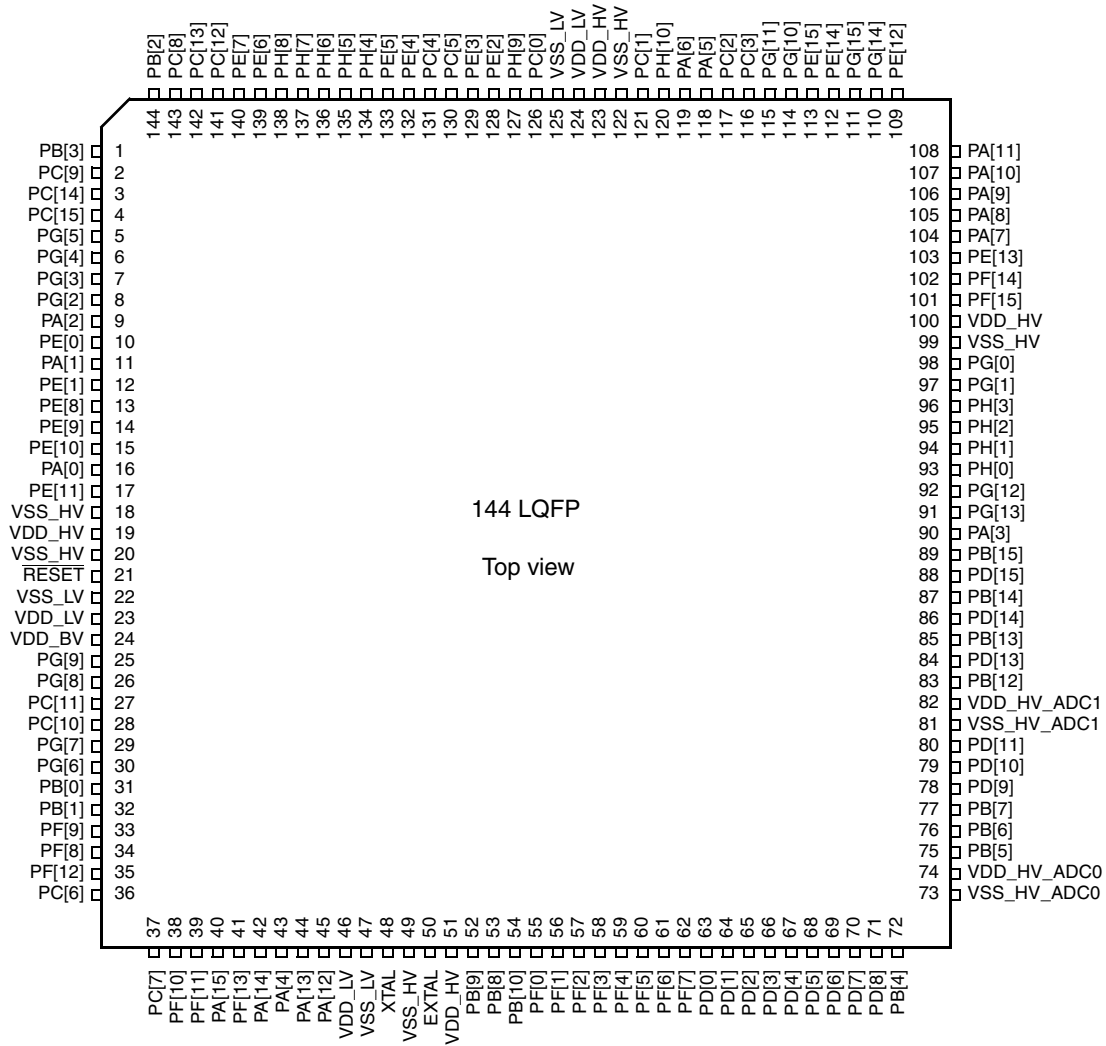


Figure 3. 144 LQFP pinout

2.2 Pin muxing

Table 2 defines the pin list and muxing for this device.

Each entry of Table 2 shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by AF0.

Table 2. Functional port pins

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------|--------------|------------------------------------|---|---|----------------------------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| Port A | | | | | | | | | | |
| PA[0] | PCR[0] | AF0 AF1 AF2 AF3 — | GPIO[0] E0UC[0] CLKOUT E0UC[13] WKUP[19] ⁴ | SIUL eMIOS_0 MC_CGM eMIOS_0 WKUP | I/O I/O O I/O I | M | Tristate | 12 | 16 | 24 |
| PA[1] | PCR[1] | AF0 AF1 AF2 AF3 — | GPIO[1] E0UC[1] NMI ⁵ — WKUP[2] ⁴ | SIUL eMIOS_0 WKUP — WKUP | I/O I/O I — I | S | Tristate | 7 | 11 | 19 |
| PA[2] | PCR[2] | AF0 AF1 AF2 AF3 — | GPIO[2] E0UC[2] — MA[2] WKUP[3] ⁴ | SIUL eMIOS_0 — ADC_0 WKUP | I/O I/O — O I | S | Tristate | 5 | 9 | 17 |
| PA[3] | PCR[3] | AF0 AF1 AF2 AF3 — — | GPIO[3] E0UC[3] LIN5TX CS4_1 EIRQ[0] ADC1_S[0] | SIUL eMIOS_0 LINFlex_5 DSPI_1 SIUL ADC_1 | I/O I/O O O I I | J | Tristate | 68 | 90 | 114 |
| PA[4] | PCR[4] | AF0 AF1 AF2 AF3 — — | GPIO[4] E0UC[4] — CS0_1 LIN5RX WKUP[9] ⁴ | SIUL eMIOS_0 — DSPI_1 LINFlex_5 WKUP | I/O I/O — I/O I I | S | Tristate | 29 | 43 | 51 |
| PA[5] | PCR[5] | AF0 AF1 AF2 AF3 | GPIO[5] E0UC[5] LIN4TX — | SIUL eMIOS_0 LINFlex_4 — | I/O I/O O — | M | Tristate | 79 | 118 | 146 |
| PA[6] | PCR[6] | AF0 AF1 AF2 AF3 — — | GPIO[6] E0UC[6] — CS1_1 EIRQ[1] LIN4RX | SIUL eMIOS_0 — DSPI_1 SIUL LINFlex_4 | I/O I/O — O I I | S | Tristate | 80 | 119 | 147 |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|----------|--------------|--|---|--|---------------------------------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PA[7] | PCR[7] | AF0 AF1 AF2 AF3 — — | GPIO[7] E0UC[7] LIN3TX — EIRQ[2] ADC1_S[1] | SIUL eMIOS_0 LINFlex_3 — SIUL ADC_1 | I/O I/O O — I I | J | Tristate | 71 | 104 | 128 |
| PA[8] | PCR[8] | AF0 AF1 AF2 AF3 — N/A ⁶ — | GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0] LIN3RX | SIUL eMIOS_0 eMIOS_0 — SIUL BAM LINFlex_3 | I/O I/O I/O — I I I | S | Input, weak pull-up | 72 | 105 | 129 |
| PA[9] | PCR[9] | AF0 AF1 AF2 AF3 N/A ⁶ | GPIO[9] E0UC[9] — CS2_1 FAB | SIUL eMIOS_0 — DSPI_1 BAM | I/O I/O — O I | S | Pull- down | 73 | 106 | 130 |
| PA[10] | PCR[10] | AF0 AF1 AF2 AF3 — | GPIO[10] E0UC[10] SDA LIN2TX ADC1_S[2] | SIUL eMIOS_0 I ² C_0 LINFlex_2 ADC_1 | I/O I/O I/O O I | J | Tristate | 74 | 107 | 131 |
| PA[11] | PCR[11] | AF0 AF1 AF2 AF3 — — — | GPIO[11] E0UC[11] SCL — EIRQ[16] LIN2RX ADC1_S[3] | SIUL eMIOS_0 I ² C_0 — SIUL LINFlex_2 ADC_1 | I/O I/O I/O — I I I | J | Tristate | 75 | 108 | 132 |
| PA[12] | PCR[12] | AF0 AF1 AF2 AF3 — — | GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0 | SIUL — eMIOS_0 DSPI_1 SIUL DSPI_0 | I/O — I/O O I I | S | Tristate | 31 | 45 | 53 |
| PA[13] | PCR[13] | AF0 AF1 AF2 AF3 | GPIO[13] SOUT_0 E0UC[29] — | SIUL DSPI_0 eMIOS_0 — | I/O O I/O — | M | Tristate | 30 | 44 | 52 |
| PA[14] | PCR[14] | AF0 AF1 AF2 AF3 — | GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4] | SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL | I/O I/O I/O I/O I | M | Tristate | 28 | 42 | 50 |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------|--------------|---------------------------------|-----------------------|--------------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PA[15] | PCR[15] | AF0 | GPIO[15] | SIUL | I/O | M | Tristate | 27 | 40 | 48 |
| | | AF1 | CS0_0 | DSPI_0 | I/O | | | | | |
| | | AF2 | SCK_0 | DSPI_0 | I/O | | | | | |
| | | AF3 | E0UC[1] | eMIOS_0 | I/O | | | | | |
| | | — | WKUP[10] ⁴ | WKUP | I | | | | | |
| Port B | | | | | | | | | | |
| PB[0] | PCR[16] | AF0 | GPIO[16] | SIUL | I/O | M | Tristate | 23 | 31 | 39 |
| | | AF1 | CAN0TX | FlexCAN_0 | O | | | | | |
| | | AF2 | E0UC[30] | eMIOS_0 | I/O | | | | | |
| | | AF3 | LIN0TX | LINFlex_0 | O | | | | | |
| PB[1] | PCR[17] | AF0 | GPIO[17] | SIUL | I/O | S | Tristate | 24 | 32 | 40 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | E0UC[31] | eMIOS_0 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[4] ⁴ | WKUP | I | | | | | |
| | | — | CAN0RX | FlexCAN_0 | I | | | | | |
| — | LIN0RX | LINFlex_0 | I | | | | | | | |
| PB[2] | PCR[18] | AF0 | GPIO[18] | SIUL | I/O | M | Tristate | 100 | 144 | 176 |
| | | AF1 | LIN0TX | LINFlex_0 | O | | | | | |
| | | AF2 | SDA | I ² C_0 | I/O | | | | | |
| | | AF3 | E0UC[30] | eMIOS_0 | I/O | | | | | |
| PB[3] | PCR[19] | AF0 | GPIO[19] | SIUL | I/O | S | Tristate | 1 | 1 | 1 |
| | | AF1 | E0UC[31] | eMIOS_0 | I/O | | | | | |
| | | AF2 | SCL | I ² C_0 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[11] ⁴ | WKUP | I | | | | | |
| | | — | LIN0RX | LINFlex_0 | I | | | | | |
| PB[4] | PCR[20] | AF0 | — | — | — | I | Tristate | 50 | 72 | 88 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[0] | ADC_0 | I | | | | | |
| | | — | ADC1_P[0] | ADC_1 | I | | | | | |
| | | — | GPIO[20] | SIUL | I | | | | | |
| PB[5] | PCR[21] | AF0 | — | — | — | I | Tristate | 53 | 75 | 91 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[1] | ADC_0 | I | | | | | |
| | | — | ADC1_P[1] | ADC_1 | I | | | | | |
| | | — | GPIO[21] | SIUL | I | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|----------|--------------|---------------------------------|---------------------------|------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PB[6] | PCR[22] | AF0 | — | — | — | I | Tristate | 54 | 76 | 92 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[2] | ADC_0 | I | | | | | |
| | | — | ADC1_P[2] | ADC_1 | I | | | | | |
| | | — | GPIO[22] | SIUL | I | | | | | |
| PB[7] | PCR[23] | AF0 | — | — | — | I | Tristate | 55 | 77 | 93 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[3] | ADC_0 | I | | | | | |
| | | — | ADC1_P[3] | ADC_1 | I | | | | | |
| | | — | GPIO[23] | SIUL | I | | | | | |
| PB[8] | PCR[24] | AF0 | GPIO[24] | SIUL | I | I | — | 39 | 53 | 61 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | OSC32K_XTAL ⁷ | OSC32K | — | | | | | |
| | | — | WKUP[25] | WKUP | I | | | | | |
| | | — | ADC0_S[0] | ADC_0 | I | | | | | |
| — | ADC1_S[4] | ADC_1 | I | | | | | | | |
| PB[9] | PCR[25] | AF0 | GPIO[25] | SIUL | I | I | — | 38 | 52 | 60 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | OSC32K_EXTAL ⁷ | OSC32K | — | | | | | |
| | | — | WKUP[26] | WKUP | I | | | | | |
| | | — | ADC0_S[1] | ADC_0 | I | | | | | |
| — | ADC1_S[5] | ADC_1 | I | | | | | | | |
| PB[10] | PCR[26] | AF0 | GPIO[26] | SIUL | I/O | J | Tristate | 40 | 54 | 62 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[8] ⁴ | WKUP | I | | | | | |
| | | — | ADC0_S[2] | ADC_0 | I | | | | | |
| | | — | ADC1_S[6] | ADC_1 | I | | | | | |
| PB[11] | PCR[27] | AF0 | GPIO[27] | SIUL | I/O | J | Tristate | — | — | 97 |
| | | AF1 | E0UC[3] | eMIOS_0 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | CS0_0 | DSPI_0 | I/O | | | | | |
| | | — | ADC0_S[3] | ADC_0 | I | | | | | |
| PB[12] | PCR[28] | AF0 | GPIO[28] | SIUL | I/O | J | Tristate | 61 | 83 | 101 |
| | | AF1 | E0UC[4] | eMIOS_0 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | CS1_0 | DSPI_0 | O | | | | | |
| | | — | ADC0_X[0] | ADC_0 | I | | | | | |
| | | — | — | — | — | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|--------------------|--------------|---|---|---|-------------------------------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PB[13] | PCR[29] | AF0 AF1 AF2 AF3 — | GPIO[29] E0UC[5] — CS2_0 ADC0_X[1] | SIUL eMIOS_0 — DSPI_0 ADC_0 | I/O I/O — O I | J | Tristate | 63 | 85 | 103 |
| PB[14] | PCR[30] | AF0 AF1 AF2 AF3 — | GPIO[30] E0UC[6] — CS3_0 ADC0_X[2] | SIUL eMIOS_0 — DSPI_0 ADC_0 | I/O I/O — O I | J | Tristate | 65 | 87 | 105 |
| PB[15] | PCR[31] | AF0 AF1 AF2 AF3 — | GPIO[31] E0UC[7] — CS4_0 ADC0_X[3] | SIUL eMIOS_0 — DSPI_0 ADC_0 | I/O I/O — O I | J | Tristate | 67 | 89 | 107 |
| Port C | | | | | | | | | | |
| PC[0] ⁸ | PCR[32] | AF0 AF1 AF2 AF3 | GPIO[32] — TDI — | SIUL — JTAGC — | I/O — I — | M | Input, weak pull-up | 87 | 126 | 154 |
| PC[1] ⁸ | PCR[33] | AF0 AF1 AF2 AF3 | GPIO[33] — TDO — | SIUL — JTAGC — | I/O — O — | F ⁹ | Tristate | 82 | 121 | 149 |
| PC[2] | PCR[34] | AF0 AF1 AF2 AF3 — | GPIO[34] SCK_1 CAN4TX DEBUG[0] EIRQ[5] | SIUL DSPI_1 FlexCAN_4 SSCM SIUL | I/O I/O O O I | M | Tristate | 78 | 117 | 145 |
| PC[3] | PCR[35] | AF0 AF1 AF2 AF3 — — — | GPIO[35] CS0_1 MA[0] DEBUG[1] EIRQ[6] CAN1RX CAN4RX | SIUL DSPI_1 ADC_0 SSCM SIUL FlexCAN_1 FlexCAN_4 | I/O I/O O O I I I | S | Tristate | 77 | 116 | 144 |
| PC[4] | PCR[36] | AF0 AF1 AF2 AF3 — — — | GPIO[36] E1UC[31] — DEBUG[2] EIRQ[18] SIN_1 CAN3RX | SIUL eMIOS_1 — SSCM SIUL DSPI_1 FlexCAN_3 | I/O I/O — O I I I | M | Tristate | 92 | 131 | 159 |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|----------|-----------------------|---------------------------------|-----------------------|------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PC[5] | PCR[37] | AF0 | GPIO[37] | SIUL | I/O | M | Tristate | 91 | 130 | 158 |
| | | AF1 | SOUT_1 | DSPI_1 | O | | | | | |
| | | AF2 | CAN3TX | FlexCAN_3 | O | | | | | |
| | | AF3 | DEBUG[3] | SSCM | O | | | | | |
| | | — | EIRQ[7] | SIUL | I | | | | | |
| PC[6] | PCR[38] | AF0 | GPIO[38] | SIUL | I/O | S | Tristate | 25 | 36 | 44 |
| | | AF1 | LIN1TX | LINFlex_1 | O | | | | | |
| | | AF2 | E1UC[28] | eMIOS_1 | I/O | | | | | |
| | | AF3 | DEBUG[4] | SSCM | O | | | | | |
| PC[7] | PCR[39] | AF0 | GPIO[39] | SIUL | I/O | S | Tristate | 26 | 37 | 45 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | E1UC[29] | eMIOS_1 | I/O | | | | | |
| | | AF3 | DEBUG[5] | SSCM | O | | | | | |
| | | — | LIN1RX | LINFlex_1 | I | | | | | |
| — | WKUP[12] ⁴ | WKUP | I | | | | | | | |
| PC[8] | PCR[40] | AF0 | GPIO[40] | SIUL | I/O | S | Tristate | 99 | 143 | 175 |
| | | AF1 | LIN2TX | LINFlex_2 | O | | | | | |
| | | AF2 | E0UC[3] | eMIOS_0 | I/O | | | | | |
| | | AF3 | DEBUG[6] | SSCM | O | | | | | |
| PC[9] | PCR[41] | AF0 | GPIO[41] | SIUL | I/O | S | Tristate | 2 | 2 | 2 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | E0UC[7] | eMIOS_0 | I/O | | | | | |
| | | AF3 | DEBUG[7] | SSCM | O | | | | | |
| | | — | WKUP[13] ⁴ | WKUP | I | | | | | |
| — | LIN2RX | LINFlex_2 | I | | | | | | | |
| PC[10] | PCR[42] | AF0 | GPIO[42] | SIUL | I/O | M | Tristate | 22 | 28 | 36 |
| | | AF1 | CAN1TX | FlexCAN_1 | O | | | | | |
| | | AF2 | CAN4TX | FlexCAN_4 | O | | | | | |
| | | AF3 | MA[1] | ADC_0 | O | | | | | |
| PC[11] | PCR[43] | AF0 | GPIO[43] | SIUL | I/O | S | Tristate | 21 | 27 | 35 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | MA[2] | ADC_0 | O | | | | | |
| | | — | WKUP[5] ⁴ | WKUP | I | | | | | |
| — | CAN1RX | FlexCAN_1 | I | | | | | | | |
| — | CAN4RX | FlexCAN_4 | I | | | | | | | |
| PC[12] | PCR[44] | AF0 | GPIO[44] | SIUL | I/O | M | Tristate | 97 | 141 | 173 |
| | | AF1 | E0UC[12] | eMIOS_0 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | EIRQ[19] | SIUL | I | | | | | |
| — | SIN_2 | DSPI_2 | I | | | | | | | |
| PC[13] | PCR[45] | AF0 | GPIO[45] | SIUL | I/O | S | Tristate | 98 | 142 | 174 |
| | | AF1 | E0UC[13] | eMIOS_0 | I/O | | | | | |
| | | AF2 | SOUT_2 | DSPI_2 | O | | | | | |
| | | AF3 | — | — | — | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------|--------------|---------------------------------|-----------|------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PC[14] | PCR[46] | AF0 | GPIO[46] | SIUL | I/O | S | Tristate | 3 | 3 | 3 |
| | | AF1 | E0UC[14] | eMIOS_0 | I/O | | | | | |
| | | AF2 | SCK_2 | DSPI_2 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | EIRQ[8] | SIUL | I | | | | | |
| PC[15] | PCR[47] | AF0 | GPIO[47] | SIUL | I/O | M | Tristate | 4 | 4 | 4 |
| | | AF1 | E0UC[15] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS0_2 | DSPI_2 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | EIRQ[20] | SIUL | I | | | | | |
| Port D | | | | | | | | | | |
| PD[0] | PCR[48] | AF0 | GPIO[48] | SIUL | I | I | Tristate | 41 | 63 | 77 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[27] | WKUP | I | | | | | |
| | | — | ADC0_P[4] | ADC_0 | I | | | | | |
| | | — | ADC1_P[4] | ADC_1 | I | | | | | |
| PD[1] | PCR[49] | AF0 | GPIO[49] | SIUL | I | I | Tristate | 42 | 64 | 78 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[28] | WKUP | I | | | | | |
| | | — | ADC0_P[5] | ADC_0 | I | | | | | |
| | | — | ADC1_P[5] | ADC_1 | I | | | | | |
| PD[2] | PCR[50] | AF0 | GPIO[50] | SIUL | I | I | Tristate | 43 | 65 | 79 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[6] | ADC_0 | I | | | | | |
| | | — | ADC1_P[6] | ADC_1 | I | | | | | |
| PD[3] | PCR[51] | AF0 | GPIO[51] | SIUL | I | I | Tristate | 44 | 66 | 80 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[7] | ADC_0 | I | | | | | |
| | | — | ADC1_P[7] | ADC_1 | I | | | | | |
| PD[4] | PCR[52] | AF0 | GPIO[52] | SIUL | I | I | Tristate | 45 | 67 | 81 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[8] | ADC_0 | I | | | | | |
| | | — | ADC1_P[8] | ADC_1 | I | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|----------|--------------|---------------------------------|--------------------------|----------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PD[5] | PCR[53] | AF0 | GPIO[53] | SIUL | I | I | Tristate | 46 | 68 | 82 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[9] ADC1_P[9] | ADC_0 ADC_1 | I I | | | | | |
| PD[6] | PCR[54] | AF0 | GPIO[54] | SIUL | I | I | Tristate | 47 | 69 | 83 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[10] ADC1_P[10] | ADC_0 ADC_1 | I I | | | | | |
| PD[7] | PCR[55] | AF0 | GPIO[55] | SIUL | I | I | Tristate | 48 | 70 | 84 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[11] ADC1_P[11] | ADC_0 ADC_1 | I I | | | | | |
| PD[8] | PCR[56] | AF0 | GPIO[56] | SIUL | I | I | Tristate | 49 | 71 | 87 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[12] ADC1_P[12] | ADC_0 ADC_1 | I I | | | | | |
| PD[9] | PCR[57] | AF0 | GPIO[57] | SIUL | I | I | Tristate | 56 | 78 | 94 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[13] ADC1_P[13] | ADC_0 ADC_1 | I I | | | | | |
| PD[10] | PCR[58] | AF0 | GPIO[58] | SIUL | I | I | Tristate | 57 | 79 | 95 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[14] ADC1_P[14] | ADC_0 ADC_1 | I I | | | | | |
| PD[11] | PCR[59] | AF0 | GPIO[59] | SIUL | I | I | Tristate | 58 | 80 | 96 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_P[15] ADC1_P[15] | ADC_0 ADC_1 | I I | | | | | |
| PD[12] | PCR[60] | AF0 | GPIO[60] | SIUL | I/O | J | Tristate | — | — | 100 |
| | | AF1 | CS5_0 | DSPI_0 | O | | | | | |
| | | AF2 | E0UC[24] | eMIOS_0 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[4] | ADC_0 | I | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------|--------------|---------------------------------|----------------------|------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PD[13] | PCR[61] | AF0 | GPIO[61] | SIUL | I/O | J | Tristate | 62 | 84 | 102 |
| | | AF1 | CS0_1 | DSPI_1 | I/O | | | | | |
| | | AF2 | E0UC[25] | eMIOS_0 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[5] | ADC_0 | I | | | | | |
| PD[14] | PCR[62] | AF0 | GPIO[62] | SIUL | I/O | J | Tristate | 64 | 86 | 104 |
| | | AF1 | CS1_1 | DSPI_1 | O | | | | | |
| | | AF2 | E0UC[26] | eMIOS_0 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[6] | ADC_0 | I | | | | | |
| PD[15] | PCR[63] | AF0 | GPIO[63] | SIUL | I/O | J | Tristate | 66 | 88 | 106 |
| | | AF1 | CS2_1 | DSPI_1 | O | | | | | |
| | | AF2 | E0UC[27] | eMIOS_0 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[7] | ADC_0 | I | | | | | |
| Port E | | | | | | | | | | |
| PE[0] | PCR[64] | AF0 | GPIO[64] | SIUL | I/O | S | Tristate | 6 | 10 | 18 |
| | | AF1 | E0UC[16] | eMIOS_0 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[6] ⁴ | WKUP | I | | | | | |
| — | CAN5RX | FlexCAN_5 | I | | | | | | | |
| PE[1] | PCR[65] | AF0 | GPIO[65] | SIUL | I/O | M | Tristate | 8 | 12 | 20 |
| | | AF1 | E0UC[17] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CAN5TX | FlexCAN_5 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | — | — | — | | | | | |
| PE[2] | PCR[66] | AF0 | GPIO[66] | SIUL | I/O | M | Tristate | 89 | 128 | 156 |
| | | AF1 | E0UC[18] | eMIOS_0 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | EIRQ[21] | SIUL | I | | | | | |
| — | SIN_1 | DSPI_1 | I | | | | | | | |
| PE[3] | PCR[67] | AF0 | GPIO[67] | SIUL | I/O | M | Tristate | 90 | 129 | 157 |
| | | AF1 | E0UC[19] | eMIOS_0 | I/O | | | | | |
| | | AF2 | SOUT_1 | DSPI_1 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | — | — | — | | | | | |
| PE[4] | PCR[68] | AF0 | GPIO[68] | SIUL | I/O | M | Tristate | 93 | 132 | 160 |
| | | AF1 | E0UC[20] | eMIOS_0 | I/O | | | | | |
| | | AF2 | SCK_1 | DSPI_1 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | EIRQ[9] | SIUL | I | | | | | |
| PE[5] | PCR[69] | AF0 | GPIO[69] | SIUL | I/O | M | Tristate | 94 | 133 | 161 |
| | | AF1 | E0UC[21] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS0_1 | DSPI_1 | I/O | | | | | |
| | | AF3 | MA[2] | ADC_0 | O | | | | | |
| | | — | — | — | — | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|----------|-----------------------|---------------------------------|------------------------|------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PE[6] | PCR[70] | AF0 | GPIO[70] | SIUL | I/O | M | Tristate | 95 | 139 | 167 |
| | | AF1 | E0UC[22] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS3_0 | DSPI_0 | O | | | | | |
| | | AF3 | MA[1] | ADC_0 | O | | | | | |
| | | — | EIRQ[22] | SIUL | I | | | | | |
| PE[7] | PCR[71] | AF0 | GPIO[71] | SIUL | I/O | M | Tristate | 96 | 140 | 168 |
| | | AF1 | E0UC[23] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS2_0 | DSPI_0 | O | | | | | |
| | | AF3 | MA[0] | ADC_0 | O | | | | | |
| | | — | EIRQ[23] | SIUL | I | | | | | |
| PE[8] | PCR[72] | AF0 | GPIO[72] | SIUL | I/O | M | Tristate | 9 | 13 | 21 |
| | | AF1 | CAN2TX | FlexCAN_2 | O | | | | | |
| | | AF2 | E0UC[22] | eMIOS_0 | I/O | | | | | |
| | | AF3 | CAN3TX | FlexCAN_3 | O | | | | | |
| PE[9] | PCR[73] | AF0 | GPIO[73] | SIUL | I/O | S | Tristate | 10 | 14 | 22 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | E0UC[23] | eMIOS_0 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[7] ⁴ | WKUP | I | | | | | |
| | | — | CAN2RX | FlexCAN_2 | I | | | | | |
| — | CAN3RX | FlexCAN_3 | I | | | | | | | |
| PE[10] | PCR[74] | AF0 | GPIO[74] | SIUL | I/O | S | Tristate | 11 | 15 | 23 |
| | | AF1 | LIN3TX | LINFlex_3 | O | | | | | |
| | | AF2 | CS3_1 | DSPI_1 | O | | | | | |
| | | AF3 | E1UC[30] | eMIOS_1 | I/O | | | | | |
| | | — | EIRQ[10] | SIUL | I | | | | | |
| PE[11] | PCR[75] | AF0 | GPIO[75] | SIUL | I/O | S | Tristate | 13 | 17 | 25 |
| | | AF1 | E0UC[24] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS4_1 | DSPI_1 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | LIN3RX | LINFlex_3 | I | | | | | |
| — | WKUP[14] ⁴ | WKUP | I | | | | | | | |
| PE[12] | PCR[76] | AF0 | GPIO[76] | SIUL | I/O | J | Tristate | 76 | 109 | 133 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | E1UC[19] ¹⁰ | eMIOS_1 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | EIRQ[11] | SIUL | I | | | | | |
| | | — | SIN_2 | DSPI_2 | I | | | | | |
| — | ADC1_S[7] | ADC_1 | I | | | | | | | |
| PE[13] | PCR[77] | AF0 | GPIO[77] | SIUL | I/O | S | Tristate | — | 103 | 127 |
| | | AF1 | SOUT_2 | DSPI_2 | O | | | | | |
| | | AF2 | E1UC[20] | eMIOS_1 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------|--------------|---------------------------------|------------|------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PE[14] | PCR[78] | AF0 | GPIO[78] | SIUL | I/O | S | Tristate | — | 112 | 136 |
| | | AF1 | SCK_2 | DSPI_2 | I/O | | | | | |
| | | AF2 | E1UC[21] | eMIOS_1 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | EIRQ[12] | SIUL | I | | | | | |
| PE[15] | PCR[79] | AF0 | GPIO[79] | SIUL | I/O | M | Tristate | — | 113 | 137 |
| | | AF1 | CS0_2 | DSPI_2 | I/O | | | | | |
| | | AF2 | E1UC[22] | eMIOS_1 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| Port F | | | | | | | | | | |
| PF[0] | PCR[80] | AF0 | GPIO[80] | SIUL | I/O | J | Tristate | — | 55 | 63 |
| | | AF1 | E0UC[10] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS3_1 | DSPI_1 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[8] | ADC_0 | I | | | | | |
| PF[1] | PCR[81] | AF0 | GPIO[81] | SIUL | I/O | J | Tristate | — | 56 | 64 |
| | | AF1 | E0UC[11] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS4_1 | DSPI_1 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[9] | ADC_0 | I | | | | | |
| PF[2] | PCR[82] | AF0 | GPIO[82] | SIUL | I/O | J | Tristate | — | 57 | 65 |
| | | AF1 | E0UC[12] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS0_2 | DSPI_2 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[10] | ADC_0 | I | | | | | |
| PF[3] | PCR[83] | AF0 | GPIO[83] | SIUL | I/O | J | Tristate | — | 58 | 66 |
| | | AF1 | E0UC[13] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS1_2 | DSPI_2 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[11] | ADC_0 | I | | | | | |
| PF[4] | PCR[84] | AF0 | GPIO[84] | SIUL | I/O | J | Tristate | — | 59 | 67 |
| | | AF1 | E0UC[14] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS2_2 | DSPI_2 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[12] | ADC_0 | I | | | | | |
| PF[5] | PCR[85] | AF0 | GPIO[85] | SIUL | I/O | J | Tristate | — | 60 | 68 |
| | | AF1 | E0UC[22] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS3_2 | DSPI_2 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[13] | ADC_0 | I | | | | | |
| PF[6] | PCR[86] | AF0 | GPIO[86] | SIUL | I/O | J | Tristate | — | 61 | 69 |
| | | AF1 | E0UC[23] | eMIOS_0 | I/O | | | | | |
| | | AF2 | CS1_1 | DSPI_1 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[14] | ADC_0 | I | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|----------|--------------|---------------------------------|-----------------------|------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PF[7] | PCR[87] | AF0 | GPIO[87] | SIUL | I/O | J | Tristate | — | 62 | 70 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | CS2_1 | DSPI_1 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[15] | ADC_0 | I | | | | | |
| PF[8] | PCR[88] | AF0 | GPIO[88] | SIUL | I/O | M | Tristate | — | 34 | 42 |
| | | AF1 | CAN3TX | FlexCAN_3 | O | | | | | |
| | | AF2 | CS4_0 | DSPI_0 | O | | | | | |
| | | AF3 | CAN2TX | FlexCAN_2 | O | | | | | |
| PF[9] | PCR[89] | AF0 | GPIO[89] | SIUL | I/O | S | Tristate | — | 33 | 41 |
| | | AF1 | E1UC[1] | eMIOS_1 | I/O | | | | | |
| | | AF2 | CS5_0 | DSPI_0 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[22] ⁴ | WKUP | I | | | | | |
| | | — | CAN2RX | FlexCAN_2 | I | | | | | |
| — | CAN3RX | FlexCAN_3 | I | | | | | | | |
| PF[10] | PCR[90] | AF0 | GPIO[90] | SIUL | I/O | M | Tristate | — | 38 | 46 |
| | | AF1 | CS1_0 | DSPI_0 | O | | | | | |
| | | AF2 | LIN4TX | LINFlex_4 | O | | | | | |
| | | AF3 | E1UC[2] | eMIOS_1 | I/O | | | | | |
| PF[11] | PCR[91] | AF0 | GPIO[91] | SIUL | I/O | S | Tristate | — | 39 | 47 |
| | | AF1 | CS2_0 | DSPI_0 | O | | | | | |
| | | AF2 | E1UC[3] | eMIOS_1 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[15] ⁴ | WKUP | I | | | | | |
| | | — | LIN4RX | LINFlex_4 | I | | | | | |
| PF[12] | PCR[92] | AF0 | GPIO[92] | SIUL | I/O | M | Tristate | — | 35 | 43 |
| | | AF1 | E1UC[25] | eMIOS_1 | I/O | | | | | |
| | | AF2 | LIN5TX | LINFlex_5 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| PF[13] | PCR[93] | AF0 | GPIO[93] | SIUL | I/O | S | Tristate | — | 41 | 49 |
| | | AF1 | E1UC[26] | eMIOS_1 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[16] ⁴ | WKUP | I | | | | | |
| | | — | LIN5RX | LINFlex_5 | I | | | | | |
| PF[14] | PCR[94] | AF0 | GPIO[94] | SIUL | I/O | M | Tristate | — | 102 | 126 |
| | | AF1 | CAN4TX | FlexCAN_4 | O | | | | | |
| | | AF2 | E1UC[27] | eMIOS_1 | I/O | | | | | |
| | | AF3 | CAN1TX | FlexCAN_1 | O | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------|--------------|---------------------------------|-----------------------|------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PF[15] | PCR[95] | AF0 | GPIO[95] | SIUL | I/O | S | Tristate | — | 101 | 125 |
| | | AF1 | E1UC[4] | eMIOS_1 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | EIRQ[13] | SIUL | I | | | | | |
| | | — | CAN1RX | FlexCAN_1 | I | | | | | |
| — | CAN4RX | FlexCAN_4 | I | | | | | | | |
| Port G | | | | | | | | | | |
| PG[0] | PCR[96] | AF0 | GPIO[96] | SIUL | I/O | M | Tristate | — | 98 | 122 |
| | | AF1 | CAN5TX | FlexCAN_5 | O | | | | | |
| | | AF2 | E1UC[23] | eMIOS_1 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| PG[1] | PCR[97] | AF0 | GPIO[97] | SIUL | I/O | S | Tristate | — | 97 | 121 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | E1UC[24] | eMIOS_1 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | EIRQ[14] | SIUL | I | | | | | |
| — | CAN5RX | FlexCAN_5 | I | | | | | | | |
| PG[2] | PCR[98] | AF0 | GPIO[98] | SIUL | I/O | M | Tristate | — | 8 | 16 |
| | | AF1 | E1UC[11] | eMIOS_1 | I/O | | | | | |
| | | AF2 | SOUT_3 | DSPI_3 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| PG[3] | PCR[99] | AF0 | GPIO[99] | SIUL | I/O | S | Tristate | — | 7 | 15 |
| | | AF1 | E1UC[12] | eMIOS_1 | I/O | | | | | |
| | | AF2 | CS0_3 | DSPI_3 | O | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[17] ⁴ | WKUP | I | | | | | |
| PG[4] | PCR[100] | AF0 | GPIO[100] | SIUL | I/O | M | Tristate | — | 6 | 14 |
| | | AF1 | E1UC[13] | eMIOS_1 | I/O | | | | | |
| | | AF2 | SCK_3 | DSPI_3 | I/O | | | | | |
| | | AF3 | — | — | — | | | | | |
| PG[5] | PCR[101] | AF0 | GPIO[101] | SIUL | I/O | S | Tristate | — | 5 | 13 |
| | | AF1 | E1UC[14] | eMIOS_1 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | WKUP[18] ⁴ | WKUP | I | | | | | |
| | | — | SIN_3 | DSPI_3 | I | | | | | |
| PG[6] | PCR[102] | AF0 | GPIO[102] | SIUL | I/O | M | Tristate | — | 30 | 38 |
| | | AF1 | E1UC[15] | eMIOS_1 | I/O | | | | | |
| | | AF2 | LIN6TX | LINFlex_6 | O | | | | | |
| | | AF3 | — | — | — | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------|--------------|------------------------------------|---|--|----------------------------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PG[7] | PCR[103] | AF0 AF1 AF2 AF3 — — | GPIO[103] E1UC[16] E1UC[30] — WKUP[20] ⁴ LIN6RX | SIUL eMIOS_1 eMIOS_1 — WKUP LINFlex_6 | I/O I/O I/O — I I | S | Tristate | — | 29 | 37 |
| PG[8] | PCR[104] | AF0 AF1 AF2 AF3 — | GPIO[104] E1UC[17] LIN7TX CS0_2 EIRQ[15] | SIUL eMIOS_1 LINFlex_7 DSPI_2 SIUL | I/O I/O O I/O I | S | Tristate | — | 26 | 34 |
| PG[9] | PCR[105] | AF0 AF1 AF2 AF3 — — | GPIO[105] E1UC[18] — SCK_2 WKUP[21] ⁴ LIN7RX | SIUL eMIOS_1 — DSPI_2 WKUP LINFlex_7 | I/O I/O — I/O I I | S | Tristate | — | 25 | 33 |
| PG[10] | PCR[106] | AF0 AF1 AF2 AF3 — | GPIO[106] E0UC[24] E1UC[31] — SIN_4 | SIUL eMIOS_0 eMIOS_1 — DSPI_4 | I/O I/O I/O — I | S | Tristate | — | 114 | 138 |
| PG[11] | PCR[107] | AF0 AF1 AF2 AF3 | GPIO[107] E0UC[25] CS0_4 — | SIUL eMIOS_0 DSPI_4 — | I/O I/O O — | M | Tristate | — | 115 | 139 |
| PG[12] | PCR[108] | AF0 AF1 AF2 AF3 | GPIO[108] E0UC[26] SOUT_4 — | SIUL eMIOS_0 DSPI_4 — | I/O I/O O — | M | Tristate | — | 92 | 116 |
| PG[13] | PCR[109] | AF0 AF1 AF2 AF3 | GPIO[109] E0UC[27] SCK_4 — | SIUL eMIOS_0 DSPI_4 — | I/O I/O I/O — | M | Tristate | — | 91 | 115 |
| PG[14] | PCR[110] | AF0 AF1 AF2 AF3 | GPIO[110] E1UC[0] — — | SIUL eMIOS_1 — — | I/O I/O — — | S | Tristate | — | 110 | 134 |
| PG[15] | PCR[111] | AF0 AF1 AF2 AF3 — | GPIO[111] E1UC[1] — — — | SIUL eMIOS_1 — — — | I/O I/O — — — | M | Tristate | — | 111 | 135 |
| Port H | | | | | | | | | | |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------------|--------------|---------------------------------|---|-------------------------------------|---------------------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PH[0] | PCR[112] | AF0 AF1 AF2 AF3 — | GPIO[112] E1UC[2] — — SIN_1 | SIUL eMIOS_1 — — DSPI_1 | I/O I/O — — I | M | Tristate | — | 93 | 117 |
| PH[1] | PCR[113] | AF0 AF1 AF2 AF3 | GPIO[113] E1UC[3] SOUT_1 — | SIUL eMIOS_1 DSPI_1 — | I/O I/O O — | M | Tristate | — | 94 | 118 |
| PH[2] | PCR[114] | AF0 AF1 AF2 AF3 | GPIO[114] E1UC[4] SCK_1 — | SIUL eMIOS_1 DSPI_1 — | I/O I/O I/O — | M | Tristate | — | 95 | 119 |
| PH[3] | PCR[115] | AF0 AF1 AF2 AF3 | GPIO[115] E1UC[5] CS0_1 — | SIUL eMIOS_1 DSPI_1 — | I/O I/O I/O — | M | Tristate | — | 96 | 120 |
| PH[4] | PCR[116] | AF0 AF1 AF2 AF3 | GPIO[116] E1UC[6] — — | SIUL eMIOS_1 — — | I/O I/O — — | M | Tristate | — | 134 | 162 |
| PH[5] | PCR[117] | AF0 AF1 AF2 AF3 | GPIO[117] E1UC[7] — — | SIUL eMIOS_1 — — | I/O I/O — — | S | Tristate | — | 135 | 163 |
| PH[6] | PCR[118] | AF0 AF1 AF2 AF3 | GPIO[118] E1UC[8] — MA[2] | SIUL eMIOS_1 — ADC_0 | I/O I/O — O | M | Tristate | — | 136 | 164 |
| PH[7] | PCR[119] | AF0 AF1 AF2 AF3 | GPIO[119] E1UC[9] CS3_2 MA[1] | SIUL eMIOS_1 DSPI_2 ADC_0 | I/O I/O O O | M | Tristate | — | 137 | 165 |
| PH[8] | PCR[120] | AF0 AF1 AF2 AF3 | GPIO[120] E1UC[10] CS2_2 MA[0] | SIUL eMIOS_1 DSPI_2 ADC_0 | I/O I/O O O | M | Tristate | — | 138 | 166 |
| PH[9] ⁸ | PCR[121] | AF0 AF1 AF2 AF3 | GPIO[121] — TCK — | SIUL — JTAGC — | I/O — I — | S | Input, weak pull-up | 88 | 127 | 155 |
| PH[10] ⁸ | PCR[122] | AF0 AF1 AF2 AF3 | GPIO[122] — TMS — | SIUL — JTAGC — | I/O — I — | M | Input, weak pull-up | 81 | 120 | 148 |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------|--------------|------------------------------------|---|--|--------------------------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PH[11] | PCR[123] | AF0 AF1 AF2 AF3 | GPIO[123] SOUT_3 CS0_4 E1UC[5] | SIUL DSPI_3 DSPI_4 eMIOS_1 | I/O O I/O I/O | M | Tristate | — | — | 140 |
| PH[12] | PCR[124] | AF0 AF1 AF2 AF3 | GPIO[124] SCK_3 CS1_4 E1UC[25] | SIUL DSPI_3 DSPI_4 eMIOS_1 | I/O I/O I/O — | M | Tristate | — | — | 141 |
| PH[13] | PCR[125] | AF0 AF1 AF2 AF3 | GPIO[125] SOUT_4 CS0_3 E1UC[26] | SIUL DSPI_4 DSPI_3 eMIOS_1 | I/O O I/O — | M | Tristate | — | — | 9 |
| PH[14] | PCR[126] | AF0 AF1 AF2 AF3 | GPIO[126] SCK_4 CS1_3 E1UC[27] | SIUL DSPI_4 DSPI_3 eMIOS_1 | I/O I/O I/O — | M | Tristate | — | — | 10 |
| PH[15] | PCR[127] | AF0 AF1 AF2 AF3 | GPIO[127] SOUT_5 — E1UC[17] | SIUL DSPI_5 — eMIOS_1 | I/O O — — | M | Tristate | — | — | 8 |
| Port I | | | | | | | | | | |
| PI[0] | PCR[128] | AF0 AF1 AF2 AF3 | GPIO[128] E0UC[28] — — | SIUL eMIOS_0 — — | I/O I/O — — | S | Tristate | — | — | 172 |
| PI[1] | PCR[129] | AF0 AF1 AF2 AF3 — — | GPIO[129] E0UC[29] — — WKUP[24] ⁴ — | SIUL eMIOS_0 — — WKUP — | I/O I/O — — I — | S | Tristate | — | — | 171 |
| PI[2] | PCR[130] | AF0 AF1 AF2 AF3 | GPIO[130] E0UC[30] — — | SIUL eMIOS_0 — — | I/O I/O — — | S | Tristate | — | — | 170 |
| PI[3] | PCR[131] | AF0 AF1 AF2 AF3 — — | GPIO[131] E0UC[31] — — WKUP[23] ⁴ — | SIUL eMIOS_0 — — WKUP — | I/O I/O — — I — | S | Tristate | — | — | 169 |
| PI[4] | PCR[132] | AF0 AF1 AF2 AF3 | GPIO[132] E1UC[28] SOUT_4 — | SIUL eMIOS_1 DSPI_4 — | I/O I/O O — | S | Tristate | — | — | 143 |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|----------|--------------|------------------------------------|---|--|------------------------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PI[5] | PCR[133] | AF0 AF1 AF2 AF3 | GPIO[133] E1UC[29] SCK_4 — | SIUL eMIOS_1 DSPI_4 — | I/O I/O I/O — | S | Tristate | — | — | 142 |
| PI[6] | PCR[134] | AF0 AF1 AF2 AF3 | GPIO[134] E1UC[30] CS0_4 — | SIUL eMIOS_1 DSPI_4 — | I/O I/O I/O — | S | Tristate | — | — | 11 |
| PI[7] | PCR[135] | AF0 AF1 AF2 AF3 | GPIO[135] E1UC[31] CS1_4 — | SIUL eMIOS_1 DSPI_4 — | I/O I/O I/O — | S | Tristate | — | — | 12 |
| PI[8] | PCR[136] | AF0 AF1 AF2 AF3 — | GPIO[136] — — — ADC0_S[16] | SIUL — — — ADC_0 | I/O — — — I | J | Tristate | — | — | 108 |
| PI[9] | PCR[137] | AF0 AF1 AF2 AF3 — | GPIO[137] — — — ADC0_S[17] | SIUL — — — ADC_0 | I/O — — — I | J | Tristate | — | — | 109 |
| PI[10] | PCR[138] | AF0 AF1 AF2 AF3 — | GPIO[138] — — — ADC0_S[18] | SIUL — — — ADC_0 | I/O — — — I | J | Tristate | — | — | 110 |
| PI[11] | PCR[139] | AF0 AF1 AF2 AF3 — — | GPIO[139] — — — ADC0_S[19] SIN_3 | SIUL — — — ADC_0 DSPI_3 | I/O — — — I I | J | Tristate | — | — | 111 |
| PI[12] | PCR[140] | AF0 AF1 AF2 AF3 — | GPIO[140] CS0_3 — — ADC0_S[20] | SIUL DSPI_3 — — ADC_0 | I/O I/O — — I | J | Tristate | — | — | 112 |
| PI[13] | PCR[141] | AF0 AF1 AF2 AF3 — | GPIO[141] CS1_3 — — ADC0_S[21] | SIUL DSPI_3 — — ADC_0 | I/O I/O — — I | J | Tristate | — | — | 113 |

Table 2. Functional port pins (continued)

| Port pin | PCR register | Alternate function ¹ | Function | Peripheral | I/O direction | Pad type ² | RESET config. ³ | Pin number | | |
|---------------|--------------|---------------------------------|---------------------|-----------------|---------------|-----------------------|----------------------------|------------|----------|----------|
| | | | | | | | | 100 LQFP | 144 LQFP | 176 LQFP |
| PI[14] | PCR[142] | AF0 | GPIO[142] | SIUL | I/O | J | Tristate | — | — | 76 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[22] SIN_4 | ADC_0 DSPI_4 | I I | | | | | |
| PI[15] | PCR[143] | AF0 | GPIO[143] | SIUL | I/O | J | Tristate | — | — | 75 |
| | | AF1 | CS0_4 | DSPI_4 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[23] | ADC_0 | I | | | | | |
| Port J | | | | | | | | | | |
| PJ[0] | PCR[144] | AF0 | GPIO[144] | SIUL | I/O | J | Tristate | — | — | 74 |
| | | AF1 | CS1_4 | DSPI_4 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[24] | ADC_0 | I | | | | | |
| PJ[1] | PCR[145] | AF0 | GPIO[145] | SIUL | I/O | J | Tristate | — | — | 73 |
| | | AF1 | — | — | — | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[25] SIN_5 | ADC_0 DSPI_5 | I I | | | | | |
| PJ[2] | PCR[146] | AF0 | GPIO[146] | SIUL | I/O | J | Tristate | — | — | 72 |
| | | AF1 | CS0_5 | DSPI_5 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[26] | ADC_0 | I | | | | | |
| PJ[3] | PCR[147] | AF0 | GPIO[147] | SIUL | I/O | J | Tristate | — | — | 71 |
| | | AF1 | CS1_5 | DSPI_5 | I/O | | | | | |
| | | AF2 | — | — | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | ADC0_S[27] | ADC_0 | I | | | | | |
| PJ[4] | PCR[148] | AF0 | GPIO[148] | SIUL | I/O | M | Tristate | — | — | 5 |
| | | AF1 | SCK_5 | DSPI_5 | I/O | | | | | |
| | | AF2 | E1UC[18] | eMIOS_1 | — | | | | | |
| | | AF3 | — | — | — | | | | | |
| | | — | — | — | — | | | | | |

¹ Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

² See Table 3.

³ The RESET configuration applies during and after reset.

- ⁴ All WKUP pins also support external interrupt capability. See the WKPU chapter of the *MPC5606BK Microcontroller Reference Manual* for further details.
- ⁵ NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.
- ⁶ “Not applicable” because these functions are available only while the device is booting. See the BAM chapter of the *MPC5606BK Microcontroller Reference Manual* for details.
- ⁷ Value of PCR.IBE bit must be 0.
- ⁸ Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO. PC[0:1] are available as JTAG pins (TDI and TDO respectively). PH[9:10] are available as JTAG pins (TCK and TMS respectively). It is up to the user to configure these pins as GPIO when needed.
- ⁹ PC[1] is a fast/medium pad but is in medium configuration by default. This pad is in Alternate Function 2 mode after reset which has TDO functionality. The reset value of PCR.OBE is 1, but this setting has no impact as long as this pad stays in AF2 mode. After configuring this pad as GPIO (PCR.PA = 0), output buffer is enabled as reset value of PCR.OBE = 1.
- ¹⁰ Not available in 100LQFP package.

Table 3. Pad types

| Type | Description |
|------|----------------------------------|
| F | Fast |
| I | Input only with analog feature |
| J | Input/output with analog feature |
| M | Medium |
| S | Slow |

3 Electrical characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in [Table 4](#) are used and the parameters are tagged accordingly in the tables where appropriate.

Table 4. Parameter classifications

| Classification tag | Tag description |
|--------------------|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Non-Volatile User Options Register (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the *MPC5606BK Microcontroller Reference Manual*.

3.2.1 NVUSRO[PAD3V5V] field description

Table 5 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 5. PAD3V5V field description¹

| Value ² | Description |
|--------------------|------------------------------|
| 0 | High voltage supply is 5.0 V |
| 1 | High voltage supply is 3.3 V |

¹ See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

² The default manufacturing value is ‘1’. This value can be programmed by the customer in Shadow Flash.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.2.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 6 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 6. OSCILLATOR_MARGIN field description¹

| Value ² | Description |
|--------------------|---|
| 0 | Low consumption configuration (4 MHz/8 MHz) |
| 1 | High margin configuration (4 MHz/16 MHz) |

¹ See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

² The default manufacturing value is ‘1’. This value can be programmed by the customer in Shadow Flash.

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

3.2.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. Table 7 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 7. WATCHDOG_EN field description¹

| Value ² | Description |
|--------------------|---------------------|
| 0 | Disable after reset |
| 1 | Enable after reset |

¹ See the MPC5606BK Microcontroller Reference Manual for more information on the NVUSRO register.

² The default manufacturing value is '1'. This value can be programmed by the customer in Shadow Flash.

3.3 Absolute maximum ratings

Table 8. Absolute maximum ratings

| Symbol | Parameter | Conditions | Value | | Unit | |
|----------------------|-----------|---|---|-----------------------|-----------------------|----|
| | | | Min | Max | | |
| V _{SS} | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| V _{DD} | SR | Voltage on VDD_HV pins with respect to ground (V _{SS}) | — | -0.3 | 6.0 | V |
| V _{SS_LV} | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V _{SS}) | — | V _{SS} - 0.1 | V _{SS} + 0.1 | V |
| V _{DD_BV} | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground (V _{SS}) | — | -0.3 | 6.0 | V |
| | | Relative to V _{DD} | — | -0.3 | V _{DD} + 0.3 | |
| V _{SS_ADC} | SR | Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V _{SS}) | — | V _{SS} - 0.1 | V _{SS} + 0.1 | V |
| V _{DD_ADC} | SR | Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V _{SS}) | — | -0.3 | 6.0 | V |
| | | Relative to V _{DD} | — | V _{DD} - 0.3 | V _{DD} + 0.3 | |
| V _{IN} | SR | Voltage on any GPIO pin with respect to ground (V _{SS}) | — | -0.3 | 6.0 | V |
| | | Relative to V _{DD} | — | — | V _{DD} + 0.3 | |
| I _{INJPAD} | SR | Injected input current on any pin during overload condition | — | -10 | 10 | mA |
| I _{INJSUM} | SR | Absolute sum of all injected input currents during overload condition | — | -50 | 50 | |
| I _{AVGSEG} | SR | Sum of all the static I/O current within a supply segment | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | 70 | mA |
| | | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | 64 | |
| T _{STORAGE} | SR | Storage temperature | — | -55 | 150 | °C |

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.4 Recommended operating conditions**Table 9. Recommended operating conditions (3.3 V)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|-----------------|----|---|----------------------|----------------|-----------------|------|
| | | | | Min | Max | |
| V_{SS} | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| V_{DD}^1 | SR | Voltage on VDD_HV pins with respect to ground (V_{SS}) | — | 3.0 | 3.6 | V |
| $V_{SS_LV}^2$ | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS}) | — | $V_{SS} - 0.1$ | $V_{SS} + 0.1$ | V |
| $V_{DD_BV}^3$ | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS}) | — | 3.0 | 3.6 | V |
| | | | Relative to V_{DD} | $V_{DD} - 0.1$ | $V_{DD} + 0.1$ | |
| V_{SS_ADC} | SR | Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS}) | — | $V_{SS} - 0.1$ | $V_{SS} + 0.1$ | V |
| $V_{DD_ADC}^4$ | SR | Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS}) | — | 3.0^5 | 3.6 | V |
| | | | Relative to V_{DD} | $V_{DD} - 0.1$ | $V_{DD} + 0.1$ | |
| V_{IN} | SR | Voltage on any GPIO pin with respect to ground (V_{SS}) | — | $V_{SS} - 0.1$ | — | V |
| | | | Relative to V_{DD} | — | $V_{DD} + 0.1$ | |
| I_{INPAD} | SR | Injected input current on any pin during overload condition | — | -5 | 5 | mA |
| I_{INJSUM} | SR | Absolute sum of all injected input currents during overload condition | — | -50 | 50 | |
| TV_{DD} | SR | V_{DD} slope to ensure correct power up ⁶ | — | 3.0^7 | 0.25 V/ μ s | V/s |

Table 9. Recommended operating conditions (3.3 V) (continued)

| Symbol | | Parameter | Conditions | Value | | Unit |
|-----------------------------|----|---------------------------------|------------------------------------|-------|-----|------|
| | | | | Min | Max | |
| $T_{A\text{ C-Grade Part}}$ | SR | Ambient temperature under bias | $f_{\text{CPU}} < 64\text{ MHz}^8$ | -40 | 85 | °C |
| $T_{J\text{ C-Grade Part}}$ | SR | Junction temperature under bias | — | -40 | 110 | |
| $T_{A\text{ V-Grade Part}}$ | SR | Ambient temperature under bias | $f_{\text{CPU}} < 64\text{ MHz}^8$ | -40 | 105 | |
| $T_{J\text{ V-Grade Part}}$ | SR | Junction temperature under bias | — | -40 | 130 | |
| $T_{A\text{ M-Grade Part}}$ | SR | Ambient temperature under bias | $f_{\text{CPU}} < 64\text{ MHz}^8$ | -40 | 125 | |
| $T_{J\text{ M-Grade Part}}$ | SR | Junction temperature under bias | — | -40 | 150 | |

¹ 100 nF capacitance needs to be provided between each $V_{\text{DD}}/V_{\text{SS}}$ pair.

² 330 nF capacitance needs to be provided between each $V_{\text{DD_LV}}/V_{\text{SS_LV}}$ supply pair.

³ 470 nF capacitance needs to be provided between $V_{\text{DD_BV}}$ and the nearest $V_{\text{SS_LV}}$ (higher value may be needed depending on external regulator characteristics). Supply ramp slope on $V_{\text{DD_BV}}$ should always be faster or equal to slope of $V_{\text{DD_HV}}$. Otherwise, device may enter regulator bypass mode if slope on $V_{\text{DD_BV}}$ is slower.

⁴ 100 nF capacitance needs to be provided between $V_{\text{DD_ADC}}/V_{\text{SS_ADC}}$ pair.

⁵ Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/O DC electrical specification may not be guaranteed. When voltage drops below V_{LVdHVL} , the device is reset.

⁶ Guaranteed by device validation

⁷ Minimum value of T_{VDD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH}).

⁸ This frequency includes the 4% frequency modulation guard band.

Table 10. Recommended operating conditions (5.0 V)

| Symbol | | Parameter | Conditions | Value | | Unit |
|-----------------------|----|---|-----------------------------|-----------------------|-----------------------|------|
| | | | | Min | Max | |
| V_{SS} | SR | Digital ground on $V_{\text{SS_HV}}$ pins | — | 0 | 0 | V |
| V_{DD}^1 | SR | Voltage on $V_{\text{DD_HV}}$ pins with respect to ground (V_{SS}) | — | 4.5 | 5.5 | V |
| | | | Voltage drop ² | 3.0 | 5.5 | |
| $V_{\text{SS_LV}}^3$ | SR | Voltage on $V_{\text{SS_LV}}$ (low voltage digital supply) pins with respect to ground (V_{SS}) | — | $V_{\text{SS}} - 0.1$ | $V_{\text{SS}} + 0.1$ | V |
| $V_{\text{DD_BV}}^4$ | SR | Voltage on $V_{\text{DD_BV}}$ pin (regulator supply) with respect to ground (V_{SS}) | — | 4.5 | 5.5 | V |
| | | | Voltage drop ² | 3.0 | 5.5 | |
| | | | Relative to V_{DD} | 3.0 | $V_{\text{DD}} + 0.1$ | |
| $V_{\text{SS_ADC}}$ | SR | Voltage on $V_{\text{SS_HV_ADC0}}$, $V_{\text{SS_HV_ADC1}}$ (ADC reference) pin with respect to ground (V_{SS}) | — | $V_{\text{SS}} - 0.1$ | $V_{\text{SS}} + 0.1$ | V |

Table 10. Recommended operating conditions (5.0 V) (continued)

| Symbol | Parameter | Conditions | Value | | Unit | |
|----------------------------|-----------|---|----------------------------------|------------------|-----------------|-----|
| | | | Min | Max | | |
| V_{DD_ADC} ⁵ | SR | Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS}) | — | 4.5 | 5.5 | V |
| | | | Voltage drop ² | 3.0 | 5.5 | |
| | | | Relative to V_{DD} | $V_{DD} - 0.1$ | $V_{DD} + 0.1$ | |
| V_{IN} | SR | Voltage on any GPIO pin with respect to ground (V_{SS}) | — | $V_{SS} - 0.1$ | — | V |
| | | | Relative to V_{DD} | — | $V_{DD} + 0.1$ | |
| I_{INJPAD} | SR | Injected input current on any pin during overload condition | — | -5 | 5 | mA |
| I_{INJSUM} | SR | Absolute sum of all injected input currents during overload condition | — | -50 | 50 | |
| TV_{DD} | SR | V_{DD} slope to ensure correct power up ⁶ | — | 3.0 ⁷ | 0.25 V/ μ s | V/s |
| $T_{A\ C-Grade\ Part}$ | SR | Ambient temperature under bias | $f_{CPU} < 64\ MHz$ ⁸ | -40 | 85 | °C |
| $T_{J\ C-Grade\ Part}$ | SR | Junction temperature under bias | — | -40 | 110 | |
| $T_{A\ V-Grade\ Part}$ | SR | Ambient temperature under bias | $f_{CPU} < 64\ MHz$ ⁸ | -40 | 105 | |
| $T_{J\ V-Grade\ Part}$ | SR | Junction temperature under bias | — | -40 | 130 | |
| $T_{A\ M-Grade\ Part}$ | SR | Ambient temperature under bias | $f_{CPU} < 64\ MHz$ ⁸ | -40 | 125 | |
| $T_{J\ M-Grade\ Part}$ | SR | Junction temperature under bias | — | -40 | 150 | |

¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

² Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

³ 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

⁴ 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). While the supply voltage ramps up, the slope on V_{DD_BV} should be less than $0.9V_{DD_HV}$ in order to ensure the device does not enter regulator bypass mode.

⁵ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

⁶ Guaranteed by device validation. Please refer to [Section 3.5.1, External ballast resistor recommendations](#) for minimum V_{DD} slope to be guaranteed to ensure correct power up in case of external resistor usage.

⁷ Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH}).

⁸ This frequency includes the 4% frequency modulation guard band.

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

3.5 Thermal characteristics

3.5.1 External ballast resistor recommendations

External ballast resistor on V_{DD_BV} pin helps in reducing the overall power dissipation inside the device. This resistor is required only when maximum power consumption exceeds the limit imposed by package thermal characteristics.

As stated in [Table 11](#) LQFP thermal characteristics, considering a thermal resistance of 144 LQFP as 48.3 °C/W, at ambient temperature $T_A = 125$ °C, the junction temperature T_j will cross 150 °C if the total power dissipation is greater than $(150 - 125)/48.3 = 517$ mW. Therefore, the total device current I_{DDMAX} at 125 °C/5.5 V must not exceed 94.1 mA (i.e., PD/VDD). Assuming an average $I_{DD}(V_{DD_HV})$ of 15–20 mA consumption typically during device RUN mode, the LV domain consumption $I_{DD}(V_{DD_BV})$ is thus limited to $I_{DDMAX} - I_{DD}(V_{DD_HV})$, i.e., 80 mA.

Therefore, respecting the maximum power allowed as explained in [Section 3.5.2, Package thermal characteristics](#), it is recommended to use this resistor only in the 125 °C/5.5 V operating corner as per the following guidelines:

- If $I_{DD}(V_{DD_BV}) < 80$ mA, then no resistor is required.
- If $80 \text{ mA} < I_{DD}(V_{DD_BV}) < 90$ mA, then 4 Ω resistor can be used.
- If $I_{DD}(V_{DD_BV}) > 90$ mA, then 8 Ω resistor can be used.

Using resistance in the range of 4–8 Ω, the gain will be around 10–20% of total consumption on V_{DD_BV} . For example, if 8 Ω resistor is used, then power consumption when $I_{DD}(V_{DD_BV})$ is 110 mA is equivalent to power consumption when $I_{DD}(V_{DD_BV})$ is 90 mA (approximately) when resistor not used.

In order to ensure correct power up, the minimum V_{DD_BV} to be guaranteed is 30 mV. If the supply ramp is slower than this value, then LVDHV3B monitoring ballast supply V_{DD_BV} pin gets triggered leading to device reset. Until the supply reaches certain threshold, this low voltage monitor generates destructive reset event in the system. This threshold depends on the maximum $I_{DD}(V_{DD_BV})$ possible across the external resistor.

3.5.2 Package thermal characteristics

Table 11. LQFP thermal characteristics¹

| Symbol | C | Parameter | Conditions ² | Pin count | Value | | | Unit |
|-----------------|----|---|-------------------------|-----------|-------|-----|------|------|
| | | | | | Min | Typ | Max | |
| $R_{\theta JA}$ | CC | Thermal resistance, junction-to-ambient natural convection ³ | Single-layer board — 1s | 100 | — | — | 64 | °C/W |
| | | | | 144 | — | — | 64 | |
| | | | | 176 | — | — | 64 | |
| | | | Four-layer board — 2s2p | 100 | — | — | 49.7 | |
| | | | | 144 | — | — | 48.3 | |
| | | | | 176 | — | — | 47.3 | |
| $R_{\theta JB}$ | CC | Thermal resistance, junction-to-board ⁴ | Single-layer board — 1s | 100 | — | — | 36 | °C/W |
| | | | | 144 | — | — | 38 | |
| | | | | 176 | — | — | 38 | |
| | | | Four-layer board — 2s2p | 100 | — | — | 33.6 | |
| | | | | 144 | — | — | 33.4 | |
| | | | | 176 | — | — | 33.4 | |

Table 11. LQFP thermal characteristics¹ (continued)

| Symbol | C | Parameter | Conditions ² | Pin count | Value | | | Unit |
|------------------|----|---|-------------------------|-----------|-------|-----|------|------|
| | | | | | Min | Typ | Max | |
| R _{θJC} | CC | Thermal resistance, junction-to-case ⁵ | Single-layer board — 1s | 100 | — | — | 23 | °C/W |
| | | | | 144 | — | — | 23 | |
| | | | | 176 | — | — | 23 | |
| | | | Four-layer board — 2s2p | 100 | — | — | 19.8 | |
| | | | | 144 | — | — | 19.2 | |
| | | | | 176 | — | — | 18.8 | |

¹ Thermal characteristics are targets based on simulation.

² V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C.

³ Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.

⁴ Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB}.

⁵ Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC}.

3.5.3 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using [Equation 1](#):

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \text{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

R_{θJA} is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and P_{I/O} (P_D = P_{INT} + P_{I/O}).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

P_{I/O} represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, P_{I/O} < P_{INT} and may be neglected. On the other hand, P_{I/O} may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if P_{I/O} is neglected) is given by:

$$P_D = K / (T_J + 273 \text{ °C}) \quad \text{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273 \text{ °C}) + R_{\theta JA} \times P_D^2 \quad \text{Eqn. 3}$$

Where:

Table 12. I/O input DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-------------------------------|----|-----------|---|------------------------------|-------------------------|-----------------------|------|------|----|
| | | | | Min | Typ | Max | | | |
| V _{IH} | SR | P | Input high level CMOS (Schmitt Trigger) | — | — | V _{DD} + 0.4 | V | | |
| V _{IL} | SR | P | Input low level CMOS (Schmitt Trigger) | — | — | 0.35V _{DD} | | | |
| V _{HYS} | CC | C | Input hysteresis CMOS (Schmitt Trigger) | — | — | — | | | |
| I _{LKG} | CC | P | Digital input leakage | No injection on adjacent pin | T _A = -40 °C | — | 2 | — | nA |
| | | | | | T _A = 25 °C | — | 2 | — | |
| | | | | | T _A = 85 °C | — | 5 | 300 | |
| | | | | | T _A = 105 °C | — | 12 | 500 | |
| | | | | | T _A = 125 °C | — | 70 | 1000 | |
| W _{FI} ² | SR | P | Wakeup input filtered pulse | — | — | 40 | ns | | |
| W _{NFI} ² | SR | P | Wakeup input not filtered pulse | — | — | — | ns | | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

3.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 13 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 14 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 15 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 16 provides output driver characteristics for I/O pads when in FAST configuration.

Table 13. I/O pull-up/pull-down DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|------------------|----|-----------|---------------------------------------|---|--------------------------|-----|------|-----|----|
| | | | | Min | Typ | Max | | | |
| I _{WPU} | CC | P | Weak pull-up current absolute value | V _{IN} = V _{IL} , V _{DD} = 5.0 V ± 10% | PAD3V5V = 0 | 10 | — | 150 | μA |
| | | | | | PAD3V5V = 1 ² | 10 | — | 250 | |
| | | | | V _{IN} = V _{IL} , V _{DD} = 3.3 V ± 10% | PAD3V5V = 1 | 10 | — | 150 | |
| I _{WPD} | CC | P | Weak pull-down current absolute value | V _{IN} = V _{IH} , V _{DD} = 5.0 V ± 10% | PAD3V5V = 0 | 10 | — | 150 | μA |
| | | | | | PAD3V5V = 1 | 10 | — | 250 | |
| | | | | V _{IN} = V _{IH} , V _{DD} = 3.3 V ± 10% | PAD3V5V = 1 | 10 | — | 150 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 14. SLOW configuration output buffer electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-----------------|----|-----------|--------------------------------------|-----------|--|-----------------------|------|--------------------|---|
| | | | | Min | Typ | Max | | | |
| V _{OH} | CC | P | Output high level SLOW configuration | Push Pull | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8V _{DD} | — | — | V |
| | | | | | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | 0.8V _{DD} | — | — | |
| | | | | | I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | V _{DD} - 0.8 | — | — | |
| V _{OL} | CC | P | Output low level SLOW configuration | Push Pull | I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | 0.1V _{DD} | V |
| | | | | | I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | — | — | 0.1V _{DD} | |
| | | | | | I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 15. MEDIUM configuration output buffer electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-----------------|----|-----------|--|-----------|---|-----------------------|------|---|---|
| | | | | Min | Typ | Max | | | |
| V _{OH} | CC | C | Output high level MEDIUM configuration | Push Pull | I _{OH} = -3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 0.8V _{DD} | — | — | V |
| | | | | | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8V _{DD} | — | — | |
| | | | | | I _{OH} = -1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | 0.8V _{DD} | — | — | |
| | | | | | I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | V _{DD} - 0.8 | — | — | |
| | | | | | I _{OH} = -100 μA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 0.8V _{DD} | — | — | |
| | | P | | | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8V _{DD} | — | — | |
| | | C | | | I _{OH} = -1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | 0.8V _{DD} | — | — | |
| | | C | | | I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | V _{DD} - 0.8 | — | — | |
| | | C | | | I _{OH} = -100 μA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 0.8V _{DD} | — | — | |

Table 15. MEDIUM configuration output buffer electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-----------------|----|-----------|--|-----------|--|-----|------|--------------------|---|
| | | | | Min | Typ | Max | | | |
| V _{OL} | CC | C | Output low level MEDIUM configuration | Push Pull | I _{OL} = 3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 0.2V _{DD} | V |
| | | | | | I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | 0.1V _{DD} | |
| | | | | | I _{OL} = 1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | — | — | 0.1V _{DD} | |
| | | | | | I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |
| | | | | | I _{OL} = 100 µA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 0.1V _{DD} | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 16. FAST configuration output buffer electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-----------------|----|-----------|---|-----------|---|-----------------------|------|--------------------|---|
| | | | | Min | Typ | Max | | | |
| V _{OH} | CC | P | Output high level FAST configuration | Push Pull | I _{OH} = -14 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8V _{DD} | — | — | V |
| | | | | | I _{OH} = -7 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | 0.8V _{DD} | — | — | |
| | | | | | I _{OH} = -11 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | V _{DD} - 0.8 | — | — | |
| V _{OL} | CC | P | Output low level FAST configuration | Push Pull | I _{OL} = 14 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | 0.1V _{DD} | V |
| | | | | | I _{OL} = 7 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | — | — | 0.1V _{DD} | |
| | | | | | I _{OL} = 11 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when $V_{DD} = 5\text{ V}$ is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

3.6.4 Output pin transition times

Table 17. Output pin transition times

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|----------|----|--|-------------------------|--|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| T_{tr} | CC | Output transition time output pin ² SLOW configuration | $C_L = 25\text{ pF}$ | $V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 0 | — | — | 50 | ns |
| | | | $C_L = 50\text{ pF}$ | | — | — | 100 | |
| | | | $C_L = 100\text{ pF}$ | | — | — | 125 | |
| | | | $C_L = 25\text{ pF}$ | $V_{DD} = 3.3\text{ V} \pm 10\%$, PAD3V5V = 1 | — | — | 50 | |
| | | | $C_L = 50\text{ pF}$ | | — | — | 100 | |
| | | | $C_L = 100\text{ pF}$ | | — | — | 125 | |
| T_{tr} | CC | Output transition time output pin ² MEDIUM configuration | $C_L = 25\text{ pF}$ | $V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 0 SIUL.PCRx.SRC = 1 | — | — | 10 | ns |
| | | | $C_L = 50\text{ pF}$ | | — | — | 20 | |
| | | | $C_L = 100\text{ pF}$ | | — | — | 40 | |
| | | | $C_L = 25\text{ pF}$ | $V_{DD} = 3.3\text{ V} \pm 10\%$, PAD3V5V = 1 SIUL.PCRx.SRC = 1 | — | — | 12 | |
| | | | $C_L = 50\text{ pF}$ | | — | — | 25 | |
| | | | $C_L = 100\text{ pF}$ | | — | — | 40 | |
| T_{tr} | CC | Output transition time output pin ² FAST configuration | $C_L = 25\text{ pF}$ | $V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 0 | — | — | 4 | ns |
| | | | $C_L = 50\text{ pF}$ | | — | — | 6 | |
| | | | $C_L = 100\text{ pF}$ | | — | — | 12 | |
| | | | $C_L = 25\text{ pF}$ | $V_{DD} = 3.3\text{ V} \pm 10\%$, PAD3V5V = 1 | — | — | 4 | |
| | | | $C_L = 50\text{ pF}$ | | — | — | 7 | |
| | | | $C_L = 100\text{ pF}$ | | — | — | 12 | |

¹ $V_{DD} = 3.3\text{ V} \pm 10\%$ / $5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^\circ\text{C}$, unless otherwise specified

² C_L includes device and package capacitances ($C_{PKG} < 5\text{ pF}$).

3.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in [Table 18](#).

[Table 19](#) provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 18. I/O supply segments

| Package | Supply segment | | | | | | | |
|----------|----------------|---------------|-----------------|-----------------|-----------------|---------------|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 176 LQFP | pin7 – pin27 | pin28 – pin57 | pin59 – pin85 | pin86 – pin123 | pin124 – pin150 | pin151 – pin6 | — | — |
| 144 LQFP | pin20 – pin49 | pin51 – pin99 | pin100 – pin122 | pin 123 – pin19 | — | — | — | — |
| 100 LQFP | pin16 – pin35 | pin37 – pin69 | pin70 – pin83 | pin84 – pin15 | — | — | — | — |

Table 19. I/O consumption

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|----------------------------------|----|-----------|---|---------------------------------|---|-----|------|------|----|
| | | | | Min | Typ | Max | | | |
| I _{SWTSLW} ² | CC | D | Dynamic I/O current for SLOW configuration | C _L = 25 pF | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 20 | mA |
| | | | | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 16 | |
| I _{SWTMED} ² | CC | D | Dynamic I/O current for MEDIUM configuration | C _L = 25 pF | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 29 | mA |
| | | | | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 17 | |
| I _{SWTFST} ² | CC | D | Dynamic I/O current for FAST configuration | C _L = 25 pF | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 110 | mA |
| | | | | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 50 | |
| I _{RMSLW} | CC | D | Root medium square I/O current for SLOW configuration | C _L = 25 pF, 2 MHz | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 2.3 | mA |
| | | | | C _L = 25 pF, 4 MHz | | — | — | 3.2 | |
| | | | | C _L = 100 pF, 2 MHz | | — | — | 6.6 | |
| | | | | C _L = 25 pF, 2 MHz | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 1.6 | |
| | | | | C _L = 25 pF, 4 MHz | | — | — | 2.3 | |
| | | | | C _L = 100 pF, 2 MHz | | — | — | 4.7 | |
| I _{RMSMED} | CC | D | Root medium square I/O current for MEDIUM configuration | C _L = 25 pF, 13 MHz | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 6.6 | mA |
| | | | | C _L = 25 pF, 40 MHz | | — | — | 13.4 | |
| | | | | C _L = 100 pF, 13 MHz | | — | — | 18.3 | |
| | | | | C _L = 25 pF, 13 MHz | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 5 | |
| | | | | C _L = 25 pF, 40 MHz | | — | — | 8.5 | |
| | | | | C _L = 100 pF, 13 MHz | | — | — | 11 | |

Table 19. I/O consumption (continued)

| Symbol | C | Parameter | Conditions ¹ | | Value | | | Unit | |
|---------------------|----|---|--|---|---------------------------------|-----|-----|------|----|
| | | | | | Min | Typ | Max | | |
| I _{RMSFST} | CC | D Root medium square I/O current for FAST configuration | C _L = 25 pF, 40 MHz | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 22 | mA | |
| | | | | | C _L = 25 pF, 64 MHz | — | — | | 33 |
| | | | | | C _L = 100 pF, 40 MHz | — | — | | 56 |
| | | | C _L = 25 pF, 40 MHz | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 14 | | |
| | | | | | C _L = 25 pF, 64 MHz | — | — | | 20 |
| | | | | | C _L = 100 pF, 40 MHz | — | — | | 35 |
| I _{AVGSEG} | SR | D Sum of all the static I/O current within a supply segment | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | — | — | 70 | mA | |
| | | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | — | — | 65 | | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 20 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below the 100%.

Table 20. I/O weight¹

| Supply segment | | | Pad | 176 LQFP | | | | 144/100 LQFP | | | |
|----------------|----------|----------|--------|----------------------|---------|--------------|---------|--------------|---------|--------------|---------|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | |
| 176 LQFP | 144 LQFP | 100 LQFP | | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| 6 | 4 | 4 | PB[3] | 5% | — | 6% | — | 13% | — | 15% | — |
| | | | PC[9] | 4% | — | 5% | — | 13% | — | 15% | — |
| | | | PC[14] | 4% | — | 4% | — | 13% | — | 15% | — |
| | | | PC[15] | 3% | 4% | 4% | 4% | 12% | 18% | 15% | 16% |
| | | | — | — | PJ[4] | 3% | 4% | 3% | 3% | — | — |

Table 20. I/O weight¹ (continued)

| Supply segment | | | Pad | 176 LQFP | | | | 144/100 LQFP | | | | |
|----------------|----------|----------|--------|----------------------|---------|--------------|---------|--------------|---------|--------------|---------|----|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | | |
| 176 LQFP | 144 LQFP | 100 LQFP | | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | |
| 1 | — | — | PH[15] | 2% | 3% | 3% | 3% | — | — | — | — | |
| | — | — | PH[13] | 3% | 4% | 3% | 4% | — | — | — | — | |
| | — | — | PH[14] | 3% | 4% | 4% | 4% | — | — | — | — | |
| | — | — | PI[6] | 4% | — | 4% | — | — | — | — | — | |
| | — | — | PI[7] | 4% | — | 4% | — | — | — | — | — | |
| | — | 4 | PG[5] | 4% | — | 5% | — | 10% | — | 12% | — | |
| | — | | PG[4] | 4% | 6% | 5% | 5% | 9% | 13% | 11% | 12% | |
| | — | | PG[3] | 4% | — | 5% | — | 9% | — | 11% | — | |
| | — | | PG[2] | 4% | 6% | 5% | 5% | 9% | 12% | 10% | 11% | |
| | — | | 4 | PA[2] | 4% | — | 5% | — | 8% | — | 10% | — |
| | — | | | PE[0] | 4% | — | 5% | — | 8% | — | 9% | — |
| | — | | | PA[1] | 4% | — | 5% | — | 8% | — | 9% | — |
| | — | | | PE[1] | 4% | 6% | 5% | 6% | 7% | 10% | 9% | 9% |
| | — | | | PE[8] | 4% | 6% | 5% | 6% | 7% | 10% | 8% | 9% |
| | — | | | PE[9] | 4% | — | 5% | — | 6% | — | 8% | — |
| | — | PE[10] | | 4% | — | 5% | — | 6% | — | 7% | — | |
| — | PA[0] | 4% | | 6% | 5% | 5% | 6% | 8% | 7% | 7% | | |
| — | PE[11] | 4% | — | 5% | — | 5% | — | 6% | — | | | |

Table 20. I/O weight¹ (continued)

| Supply segment | | | Pad | 176 LQFP | | | | 144/100 LQFP | | | |
|----------------|----------|----------|--------|----------------------|---------|--------------|---------|--------------|---------|--------------|---------|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | |
| 176 LQFP | 144 LQFP | 100 LQFP | | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| 2 | 1 | — | PG[9] | 9% | — | 10% | — | 9% | — | 10% | — |
| | | — | PG[8] | 9% | — | 11% | — | 9% | — | 11% | — |
| | | 1 | PC[11] | 9% | — | 11% | — | 9% | — | 11% | — |
| | | | PC[10] | 9% | 13% | 11% | 12% | 9% | 13% | 11% | 12% |
| | | — | PG[7] | 9% | — | 11% | — | 9% | — | 11% | — |
| | | — | PG[6] | 10% | 14% | 11% | 12% | 10% | 14% | 11% | 12% |
| | | 1 | PB[0] | 10% | 14% | 12% | 12% | 10% | 14% | 12% | 12% |
| | | | PB[1] | 10% | — | 12% | — | 10% | — | 12% | — |
| | | — | PF[9] | 10% | — | 12% | — | 10% | — | 12% | — |
| | | — | PF[8] | 10% | 14% | 12% | 13% | 10% | 14% | 12% | 13% |
| | | — | PF[12] | 10% | 15% | 12% | 13% | 10% | 15% | 12% | 13% |
| | | 1 | PC[6] | 10% | — | 12% | — | 10% | — | 12% | — |
| | | | PC[7] | 10% | — | 12% | — | 10% | — | 12% | — |
| | | — | PF[10] | 10% | 14% | 11% | 12% | 10% | 14% | 11% | 12% |
| | | — | PF[11] | 9% | — | 11% | — | 9% | — | 11% | — |
| | | 1 | PA[15] | 8% | 12% | 10% | 10% | 8% | 12% | 10% | 10% |
| | | — | PF[13] | 8% | — | 10% | — | 8% | — | 10% | — |
| | | 1 | PA[14] | 8% | 11% | 9% | 10% | 8% | 11% | 9% | 10% |
| | | | PA[4] | 7% | — | 9% | — | 7% | — | 9% | — |
| | | | PA[13] | 7% | 10% | 8% | 9% | 7% | 10% | 8% | 9% |
| PA[12] | 7% | | — | 8% | — | 7% | — | 8% | — | | |

Table 20. I/O weight¹ (continued)

| Supply segment | | | Pad | 176 LQFP | | | | 144/100 LQFP | | | | | |
|----------------|----------|----------|--------|----------------------|---------|--------------|---------|--------------|---------|--------------|---------|-----|---|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | | | |
| 176 LQFP | 144 LQFP | 100 LQFP | | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | | |
| 3 | 2 | 2 | PB[9] | 1% | — | 1% | — | 1% | — | 1% | — | | |
| | | | PB[8] | 1% | — | 1% | — | 1% | — | 1% | — | | |
| | | | PB[10] | 5% | — | 6% | — | 6% | — | 7% | — | | |
| | | — | — | — | PF[0] | 5% | — | 6% | — | 6% | — | 8% | — |
| | | — | — | — | PF[1] | 5% | — | 6% | — | 7% | — | 8% | — |
| | | — | — | — | PF[2] | 6% | — | 7% | — | 7% | — | 9% | — |
| | | — | — | — | PF[3] | 6% | — | 7% | — | 8% | — | 9% | — |
| | | — | — | — | PF[4] | 6% | — | 7% | — | 8% | — | 10% | — |
| | | — | — | — | PF[5] | 6% | — | 7% | — | 9% | — | 10% | — |
| | | — | — | — | PF[6] | 6% | — | 7% | — | 9% | — | 11% | — |
| | — | — | — | PF[7] | 6% | — | 7% | — | 9% | — | 11% | — | |
| | — | — | — | PJ[3] | 6% | — | 7% | — | — | — | — | — | |
| | — | — | — | PJ[2] | 6% | — | 7% | — | — | — | — | — | |
| | — | — | — | PJ[1] | 6% | — | 7% | — | — | — | — | — | |
| | — | — | — | PJ[0] | 6% | — | 7% | — | — | — | — | — | |
| | — | — | — | PI[15] | 6% | — | 7% | — | — | — | — | — | |
| | — | — | — | PI[14] | 6% | — | 7% | — | — | — | — | — | |
| | — | 2 | 2 | PD[0] | 1% | — | 1% | — | 1% | — | 1% | — | |
| | — | — | — | PD[1] | 1% | — | 1% | — | 1% | — | 1% | — | |
| | — | — | — | PD[2] | 1% | — | 1% | — | 1% | — | 1% | — | |
| — | — | — | PD[3] | 1% | — | 1% | — | 1% | — | 1% | — | | |
| — | — | — | PD[4] | 1% | — | 1% | — | 1% | — | 1% | — | | |
| — | — | — | PD[5] | 1% | — | 1% | — | 1% | — | 1% | — | | |
| — | — | — | PD[6] | 1% | — | 1% | — | 1% | — | 2% | — | | |
| — | — | — | PD[7] | 1% | — | 1% | — | 1% | — | 2% | — | | |

Table 20. I/O weight¹ (continued)

| Supply segment | | | Pad | 176 LQFP | | | | 144/100 LQFP | | | |
|----------------|----------|----------|--------|----------------------|---------|--------------|---------|--------------|---------|--------------|---------|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | |
| 176 LQFP | 144 LQFP | 100 LQFP | | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| 4 | 2 | 2 | PD[8] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | | PB[4] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | | PB[5] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | | PB[6] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | | PB[7] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | | PD[9] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | | PD[10] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | | PD[11] | 1% | — | 1% | — | 1% | — | 2% | — |
| 4 | — | — | PB[11] | 1% | — | 1% | — | — | — | — | — |
| | — | — | PD[12] | 11% | — | 13% | — | — | — | — | — |
| | 2 | 2 | PB[12] | 11% | — | 13% | — | 15% | — | 17% | — |
| | | | PD[13] | 11% | — | 13% | — | 14% | — | 17% | — |
| | | | PB[13] | 11% | — | 13% | — | 14% | — | 17% | — |
| | | | PD[14] | 11% | — | 13% | — | 14% | — | 17% | — |
| | | | PB[14] | 11% | — | 13% | — | 14% | — | 16% | — |
| | | | PD[15] | 11% | — | 13% | — | 13% | — | 16% | — |
| | | | PB[15] | 11% | — | 13% | — | 13% | — | 15% | — |
| | — | — | PI[8] | 10% | — | 12% | — | — | — | — | — |
| | — | — | PI[9] | 10% | — | 12% | — | — | — | — | — |
| | — | — | PI[10] | 10% | — | 12% | — | — | — | — | — |
| | — | — | PI[11] | 10% | — | 12% | — | — | — | — | — |
| | — | — | PI[12] | 10% | — | 12% | — | — | — | — | — |
| | — | — | PI[13] | 10% | — | 11% | — | — | — | — | — |
| | 2 | 2 | PA[3] | 9% | — | 11% | — | 11% | — | 13% | — |
| | | | PG[13] | 9% | 13% | 11% | 11% | 10% | 14% | 12% | 13% |
| | | | PG[12] | 9% | 13% | 10% | 11% | 10% | 14% | 12% | 12% |
| | | | PH[0] | 6% | 8% | 7% | 7% | 6% | 9% | 7% | 8% |
| | | | PH[1] | 6% | 8% | 7% | 7% | 6% | 8% | 7% | 7% |
| PH[2] | | | 5% | 7% | 6% | 6% | 5% | 7% | 6% | 7% | |
| PH[3] | | | 5% | 7% | 5% | 6% | 5% | 7% | 6% | 6% | |
| PG[1] | | | 4% | — | 5% | — | 4% | — | 5% | — | |
| — | — | PG[0] | 4% | 5% | 4% | 5% | 4% | 5% | 4% | 5% | |

Table 20. I/O weight¹ (continued)

| Supply segment | | | Pad | 176 LQFP | | | | 144/100 LQFP | | | |
|----------------|----------|----------|--------|----------------------|---------|--------------|---------|--------------|---------|--------------|---------|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | |
| 176 LQFP | 144 LQFP | 100 LQFP | | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| 5 | 3 | — | PF[15] | 4% | — | 4% | — | 4% | — | 4% | — |
| | | — | PF[14] | 4% | 6% | 5% | 5% | 4% | 6% | 5% | 5% |
| | | — | PE[13] | 4% | — | 5% | — | 4% | — | 5% | — |
| | | 3 | PA[7] | 5% | — | 6% | — | 5% | — | 6% | — |
| | | | PA[8] | 5% | — | 6% | — | 5% | — | 6% | — |
| | | | PA[9] | 6% | — | 7% | — | 6% | — | 7% | — |
| | | | PA[10] | 6% | — | 8% | — | 6% | — | 8% | — |
| | | | PA[11] | 8% | — | 9% | — | 8% | — | 9% | — |
| | | | PE[12] | 8% | — | 9% | — | 8% | — | 9% | — |
| | | | — | PG[14] | 8% | — | 9% | — | 8% | — | 9% |
| | | — | PG[15] | 8% | 11% | 9% | 10% | 8% | 11% | 9% | 10% |
| | | — | PE[14] | 8% | — | 9% | — | 8% | — | 9% | — |
| | | — | PE[15] | 8% | 11% | 9% | 10% | 8% | 11% | 9% | 10% |
| | | — | PG[10] | 8% | — | 9% | — | 8% | — | 9% | — |
| | — | PG[11] | 7% | 11% | 9% | 9% | 7% | 11% | 9% | 9% | |
| | — | — | — | PH[11] | 7% | 10% | 9% | 9% | — | — | — |
| | — | — | — | PH[12] | 7% | 10% | 8% | 9% | — | — | — |
| | — | — | — | PI[5] | 7% | — | 8% | — | — | — | — |
| | — | — | — | PI[4] | 7% | — | 8% | — | — | — | — |
| | 3 | 3 | PC[3] | 6% | — | 8% | — | 6% | — | 8% | — |
| PC[2] | | | 6% | 8% | 7% | 7% | 6% | 8% | 7% | 7% | |
| PA[5] | | | 6% | 8% | 7% | 7% | 6% | 8% | 7% | 7% | |
| PA[6] | | | 5% | — | 6% | — | 5% | — | 6% | — | |
| PH[10] | | | 5% | 7% | 6% | 6% | 5% | 7% | 6% | 6% | |
| PC[1] | | | 5% | 19% | 5% | 13% | 5% | 19% | 5% | 13% | |

Table 20. I/O weight¹ (continued)

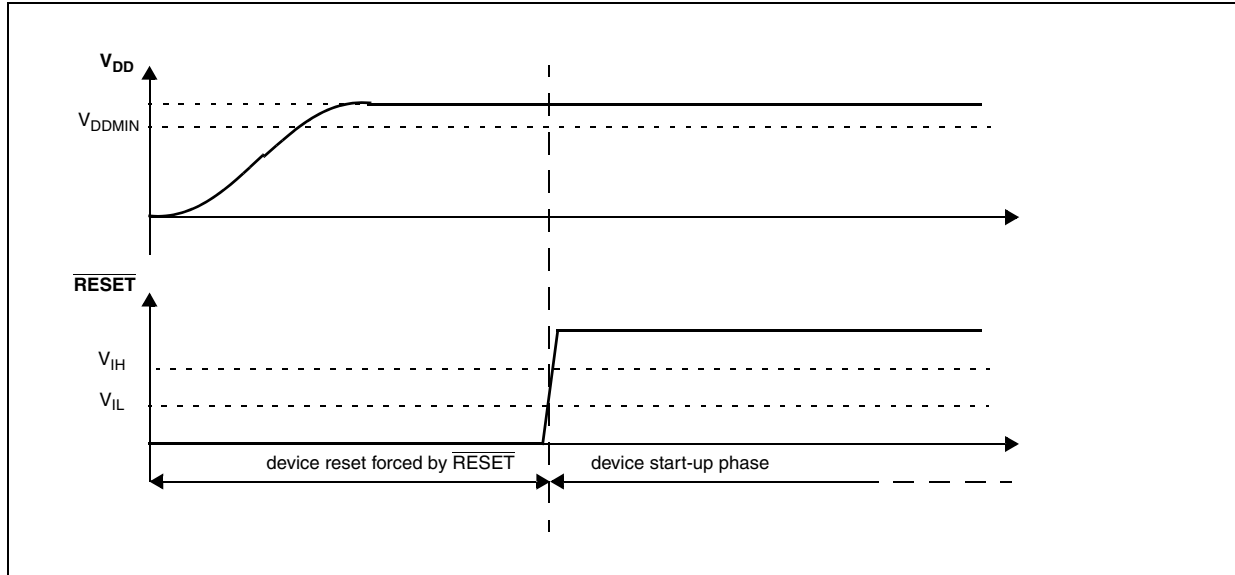
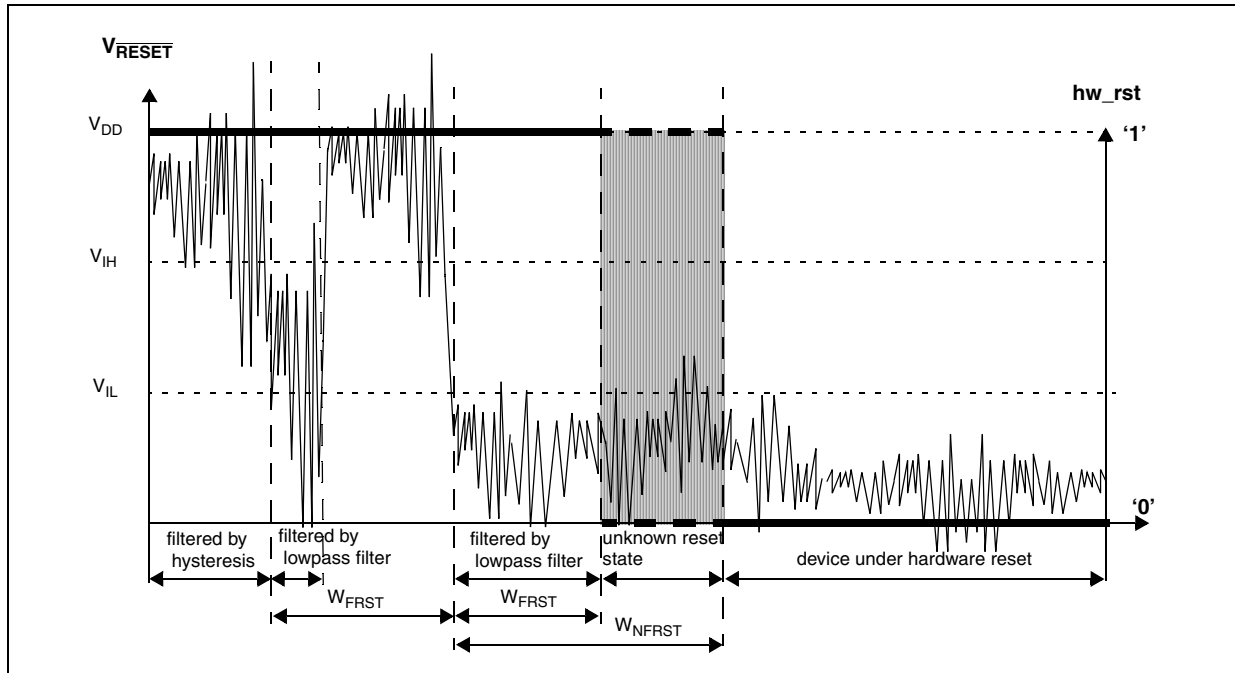
| Supply segment | | | Pad | 176 LQFP | | | | 144/100 LQFP | | | | | |
|----------------|----------|----------|--------|----------------------|---------|--------------|---------|--------------|---------|--------------|---------|-----|-----|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | | | |
| 176 LQFP | 144 LQFP | 100 LQFP | | SRC ² = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | | |
| 6 | 4 | 4 | PC[0] | 6% | 9% | 7% | 8% | 7% | 10% | 8% | 8% | | |
| | | | PH[9] | 7% | — | 8% | — | 7% | — | 9% | — | | |
| | | | PE[2] | 7% | 10% | 8% | 9% | 8% | 11% | 9% | 10% | | |
| | | | PE[3] | 7% | 10% | 9% | 9% | 8% | 12% | 10% | 10% | | |
| | | | PC[5] | 7% | 11% | 9% | 9% | 8% | 12% | 10% | 11% | | |
| | | | PC[4] | 8% | 11% | 9% | 10% | 9% | 13% | 10% | 11% | | |
| | | | PE[4] | 8% | 11% | 9% | 10% | 9% | 13% | 11% | 12% | | |
| | | | PE[5] | 8% | 11% | 10% | 10% | 9% | 14% | 11% | 12% | | |
| | | — | — | — | PH[4] | 8% | 12% | 10% | 10% | 10% | 14% | 12% | 12% |
| | | — | — | — | PH[5] | 8% | — | 10% | — | 10% | — | 12% | — |
| | | — | — | — | PH[6] | 8% | 12% | 10% | 11% | 10% | 15% | 12% | 13% |
| | | — | — | — | PH[7] | 9% | 12% | 10% | 11% | 11% | 15% | 13% | 13% |
| | | — | — | — | PH[8] | 9% | 12% | 10% | 11% | 11% | 16% | 13% | 14% |
| | | — | — | 4 | PE[6] | 9% | 12% | 10% | 11% | 11% | 16% | 13% | 14% |
| | | — | — | — | PE[7] | 9% | 12% | 10% | 11% | 11% | 16% | 14% | 14% |
| | | — | — | — | PI[3] | 9% | — | 10% | — | — | — | — | — |
| | | — | — | — | PI[2] | 9% | — | 10% | — | — | — | — | — |
| | | — | — | — | PI[1] | 9% | — | 10% | — | — | — | — | — |
| | | — | — | — | PI[0] | 9% | — | 10% | — | — | — | — | — |
| | | — | 4 | 4 | PC[12] | 8% | 12% | 10% | 11% | 12% | 18% | 15% | 16% |
| — | — | — | PC[13] | 8% | — | 10% | — | 13% | — | 15% | — | | |
| — | — | — | PC[8] | 8% | — | 10% | — | 13% | — | 15% | — | | |
| — | — | — | PB[2] | 8% | 11% | 9% | 10% | 13% | 18% | 15% | 16% | | |

¹ $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^\circ\text{C}$, unless otherwise specified

² SRC is the Slew Rate Control bit in SIU_PCRx

3.7 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.


Figure 6. Start-up reset requirements

Figure 7. Noise filtering on reset signal
Table 21. Reset electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|----------|----|-----------|---|--------------|-----|----------------|------|
| | | | | Min | Typ | Max | |
| V_{IH} | SR | P | Input High Level CMOS (Schmitt Trigger) | $0.65V_{DD}$ | — | $V_{DD} + 0.4$ | V |

Table 21. Reset electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|--------------------|----|-----------|---|---|------|---------------------|--------------------|----|
| | | | | Min | Typ | Max | | |
| V _{IL} | SR | P | Input low Level CMOS (Schmitt Trigger) | — | — | 0.35V _{DD} | V | |
| V _{HYS} | CC | C | Input hysteresis CMOS (Schmitt Trigger) | — | — | 0.1V _{DD} | V | |
| V _{OL} | CC | P | Output low level | Push Pull, I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | 0.1V _{DD} | V |
| | | | | Push Pull, I _{OL} = 1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | — | — | 0.1V _{DD} | |
| | | | | Push Pull, I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |
| T _{tr} | CC | D | Output transition time output pin ³ MEDIUM configuration | C _L = 25 pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 10 | ns |
| | | | | C _L = 50 pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 20 | |
| | | | | C _L = 100 pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 40 | |
| | | | | C _L = 25 pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 12 | |
| | | | | C _L = 50 pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 25 | |
| | | | | C _L = 100 pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 40 | |
| W _{FRST} | SR | P | $\overline{\text{RESET}}$ input filtered pulse | — | — | 40 | ns | |
| W _{NFRST} | SR | P | $\overline{\text{RESET}}$ input not filtered pulse | — | 1000 | — | ns | |
| I _{WPU} | CC | P | Weak pull-up current absolute value | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | 10 | — | 150 | μA |
| | | | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 10 | — | 150 | |
| | | | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁴ | 10 | — | 250 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to the MC_RGM chapter of the MPC5606BK Microcontroller Reference Manual).

³ C_L includes device and package capacitance (C_{PKG} < 5 pF).

⁴ The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV} . The regulator itself is supplied by the common I/O supply V_{DD} . The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD} .
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
 - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
 - LV_CFLA: Low voltage supply for code Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
 - LV_DFLA: Low voltage supply for data Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
 - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

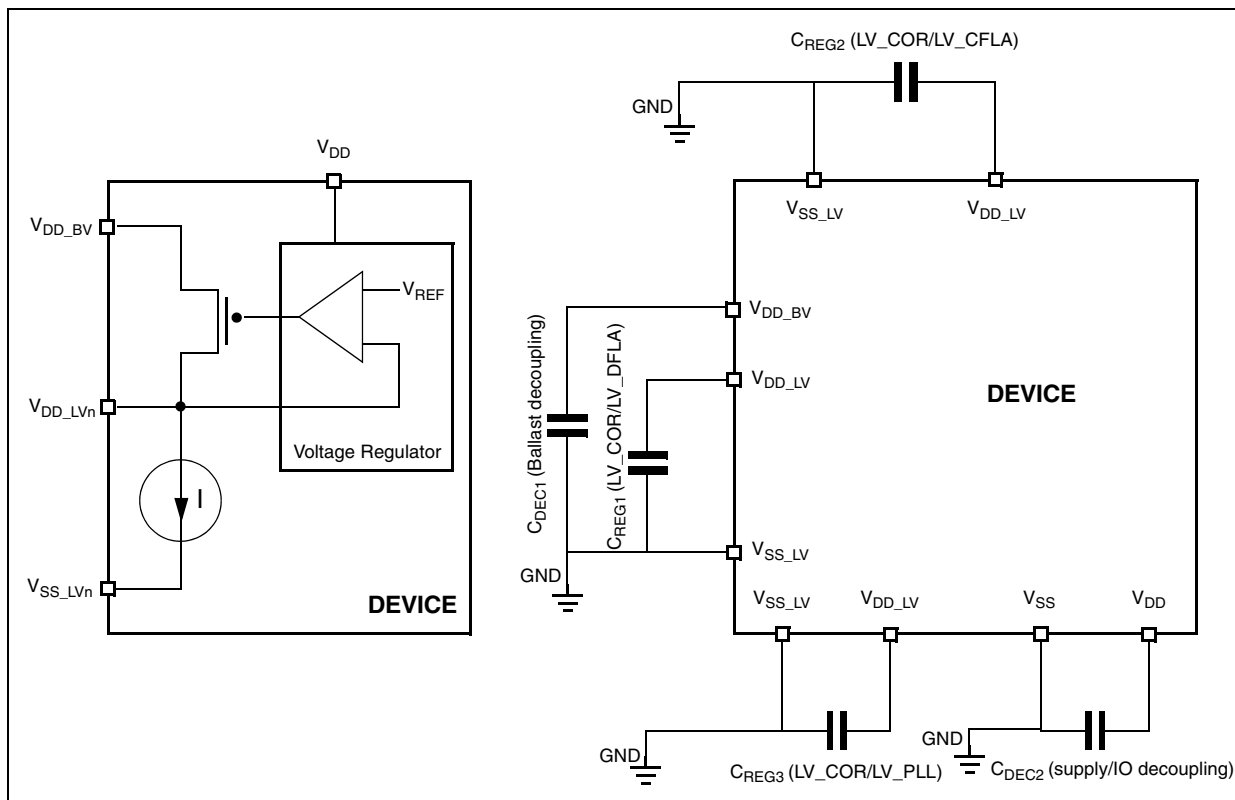


Figure 8. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see [Section 3.4, Recommended operating conditions](#)).

The internal voltage regulator requires controlled slew rate of V_{DD}/V_{DD_BV} as described in [Figure 9](#).

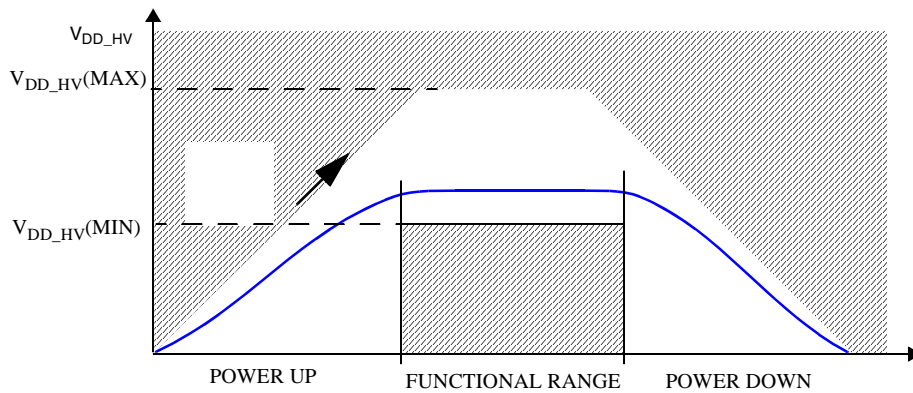


Figure 9. V_{DD} and V_{DD_BV} maximum slope

When STANDBY mode is used, further constraints apply to the V_{DD}/V_{DD_BV} in order to guarantee correct regulator functionality during STANDBY exit. This is described in [Figure 10](#).

STANDBY regulator constraints should normally be guaranteed by implementing equivalent of C_{STDBY} capacitance on application board (capacitance and ESR typical values), but would actually depend on the exact characteristics of the application's external regulator.

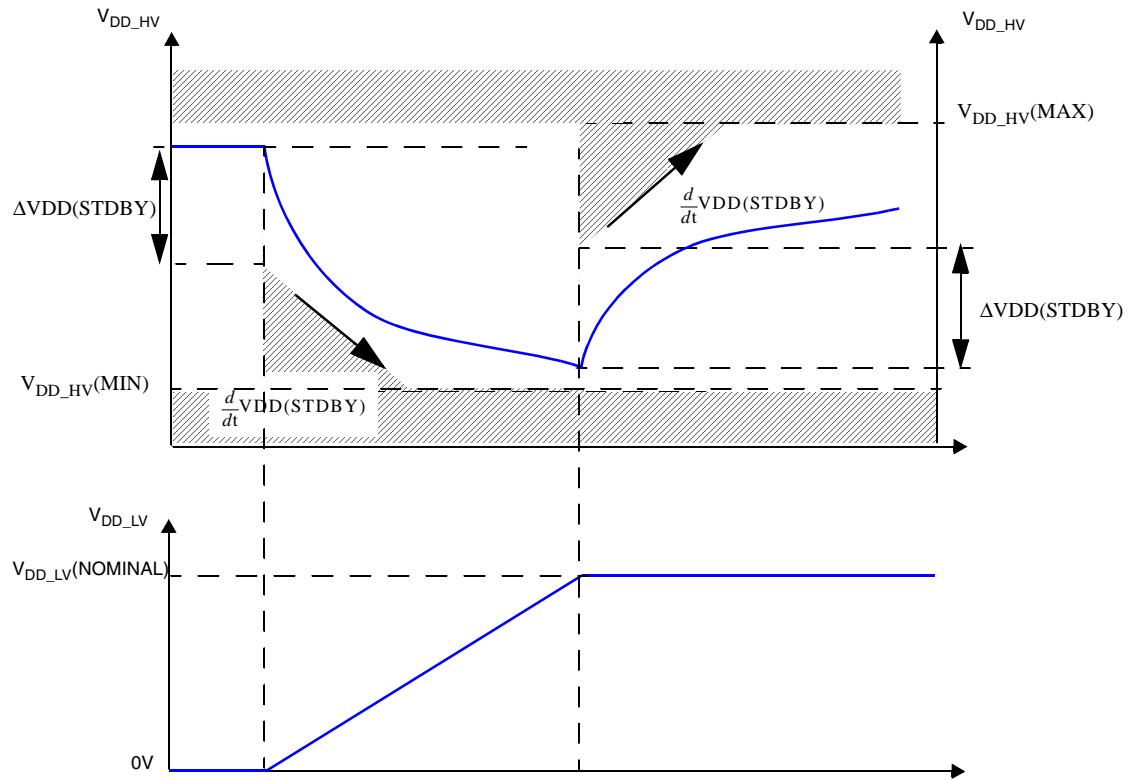

 Figure 10. V_{DD} and V_{DD_BV} supply constraints during STANDBY mode exit

Table 22. Voltage regulator electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|------------|----|--|--|---------------------------|------------------|------|----------|---|
| | | | | Min | Typ | Max | | |
| C_{REGn} | SR | Internal voltage regulator external capacitance | — | 200 | — | 500 | nF | |
| R_{REG} | SR | Stability capacitor equivalent serial resistance | — | — | — | 0.2 | Ω | |
| C_{DEC1} | SR | Decoupling capacitance ² ballast | V_{DD_BV}/V_{SS_LV} pair: $V_{DD_BV} = 4.5\text{ V to }5.5\text{ V}$ | 100 ³ | 470 ⁴ | — | nF | |
| | | | V_{DD_BV}/V_{SS_LV} pair: $V_{DD_BV} = 3\text{ V to }3.6\text{ V}$ | 400 | — | — | | |
| C_{DEC2} | SR | Decoupling capacitance regulator supply | V_{DD}/V_{SS} pair | 10 | 100 | — | nF | |
| V_{MREG} | CC | P | Main regulator output voltage | Before exiting from reset | — | 1.32 | — | V |
| | | | After trimming | 1.15 | 1.28 | 1.32 | | |
| I_{MREG} | SR | Main regulator current provided to V_{DD_LV} domain | — | — | — | 150 | mA | |

Table 22. Voltage regulator electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|---|----|-----------|---|---|------|------|------------------|-------|
| | | | | Min | Typ | Max | | |
| I _{MREGINT} | CC | D | Main regulator module current consumption | I _{MREG} = 200 mA | — | — | 2 | mA |
| | | | | I _{MREG} = 0 mA | — | — | 1 | |
| V _{LPREG} | CC | P | Low power regulator output voltage | After trimming | 1.15 | 1.23 | 1.32 | V |
| I _{LPREG} | SR | — | Low power regulator current provided to V _{DD_LV} domain | — | — | — | 15 | mA |
| I _{LPREGINT} | CC | D | Low power regulator module current consumption | I _{LPREG} = 15 mA; T _A = 55 °C | — | — | 600 | μA |
| | | | | I _{LPREG} = 0 mA; T _A = 55 °C | — | 5 | — | |
| V _{ULPREG} | CC | P | Ultra low power regulator output voltage | After trimming | 1.15 | 1.23 | 1.32 | V |
| I _{ULPREG} | SR | — | Ultra low power regulator current provided to V _{DD_LV} domain | — | — | — | 5 | mA |
| I _{ULPREGINT} | CC | D | Ultra low power regulator module current consumption | I _{ULPREG} = 5 mA; T _A = 55 °C | — | — | 100 | μA |
| | | | | I _{ULPREG} = 0 mA; T _A = 55 °C | — | 2 | — | |
| I _{DD_BV} | CC | D | Inrush average current on V _{DD_BV} during power-up ⁵ | — | — | — | 300 ⁶ | mA |
| $\left \frac{d}{dt} V_{DD} \right $ | SR | — | Maximum slope on VDD | — | — | — | 250 | mV/μs |
| ΔV _{VDD(STDBY)} | SR | — | Maximum instant variation on VDD during STANDBY exit | — | — | — | 30 | mV |
| $\left \frac{d}{dt} V_{DD}(STDBY) \right $ | SR | — | Maximum slope on VDD during STANDBY exit | — | — | — | 15 | mV/μs |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

³ This value is acceptable to guarantee operation from 4.5 V to 5.5 V

⁴ External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

⁵ Inrush current is seen only for short time during power-up and on standby exit (max 20 μs, depending on external capacitances to be load).

⁶ The duration of the inrush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

3.8.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV3B monitors V_{DD_BV} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the $5.0\text{ V} \pm 10\%$ range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

NOTE

When enabled, power domain No. 2 is monitored through LVDLVBKP.

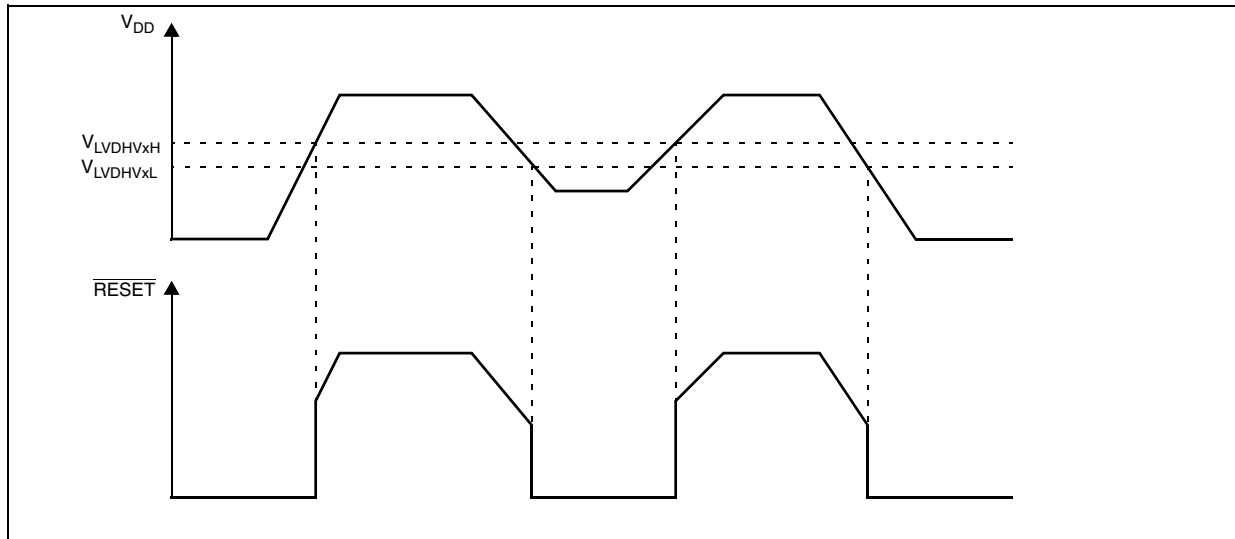


Figure 11. Low voltage monitor vs. reset

Table 23. Low voltage monitor electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|-----------------|----|-----------|---|-------|-----|------|------|
| | | | | Min | Typ | Max | |
| V_{PORUP} | SR | D | Supply for functional POR module | 1.0 | — | 5.5 | V |
| V_{PORH} | CC | P | Power-on reset threshold | 1.5 | — | 2.6 | |
| $V_{LVDHV3H}$ | CC | T | LVDHV3 low voltage detector high threshold | — | — | 2.95 | |
| $V_{LVDHV3L}$ | CC | P | LVDHV3 low voltage detector low threshold | 2.6 | — | 2.9 | |
| $V_{LVDHV3BH}$ | CC | T | LVDHV3B low voltage detector high threshold | — | — | 2.95 | |
| $V_{LVDHV3BL}$ | CC | P | LVDHV3BL low voltage detector low threshold | 2.6 | — | 2.9 | |
| $V_{LVDHV5H}$ | CC | T | LVDHV5 low voltage detector high threshold | — | — | 4.5 | |
| $V_{LVDHV5L}$ | CC | P | LVDHV5 low voltage detector low threshold | 3.8 | — | 4.4 | |
| $V_{LVDLVCORL}$ | CC | P | LVDLVCOR low voltage detector low threshold | 1.08 | — | — | |
| $V_{LVDLVBKPL}$ | CC | P | LVDLVBKP low voltage detector low threshold | 1.08 | — | 1.14 | |

¹ $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^\circ\text{C}$, unless otherwise specified

3.9 Power consumption in different application modes

Table 24 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 24. Electrical characteristics in different application modes¹

| Symbol | C | Parameter | Conditions ² | Value | | | Unit | | |
|----------------|----|-----------|---|---|------------------------------------|------------------|------|------|---------------|
| | | | | Min | Typ | Max | | | |
| I_{DDMAX}^3 | CC | C | RUN mode maximum average current | — | 81 | 130 ⁴ | mA | | |
| I_{DDRUN}^5 | CC | T | RUN mode typical average current ⁶ | $f_{CPU} = 8 \text{ MHz}$ | — | 12 | — | mA | |
| | | T | | $f_{CPU} = 16 \text{ MHz}$ | — | 27 | — | | |
| | | C | | $f_{CPU} = 32 \text{ MHz}$ | — | 40 | — | | |
| | | P | | $f_{CPU} = 48 \text{ MHz}$ | — | 54 | 95 | | |
| | | P | | $f_{CPU} = 64 \text{ MHz}$ | — | 67 | 120 | | |
| I_{DDHALT} | CC | C | HALT mode current ⁷ | Slow internal RC oscillator (128 kHz) running | $T_A = 25 \text{ }^\circ\text{C}$ | — | 10 | 15 | mA |
| | | P | | $T_A = 125 \text{ }^\circ\text{C}$ | — | 15 | 28 | | |
| I_{DDSTOP} | CC | P | STOP mode current ⁸ | Slow internal RC oscillator (128 kHz) running | $T_A = 25 \text{ }^\circ\text{C}$ | — | 130 | 500 | μA |
| | | D | | | $T_A = 55 \text{ }^\circ\text{C}$ | — | 180 | — | |
| | | D | | | $T_A = 85 \text{ }^\circ\text{C}$ | — | 1 | 5 | mA |
| | | D | | | $T_A = 105 \text{ }^\circ\text{C}$ | — | 3 | 9 | |
| | | P | | | $T_A = 125 \text{ }^\circ\text{C}$ | — | 5 | 14 | |
| $I_{DDSTDBY2}$ | CC | P | STANDBY2 mode current ⁹ | Slow internal RC oscillator (128 kHz) running | $T_A = 25 \text{ }^\circ\text{C}$ | — | 17 | 80 | μA |
| | | C | | | $T_A = 55 \text{ }^\circ\text{C}$ | — | 30 | — | |
| | | C | | | $T_A = 85 \text{ }^\circ\text{C}$ | — | 110 | — | |
| | | C | | | $T_A = 105 \text{ }^\circ\text{C}$ | — | 280 | 950 | |
| | | C | | | $T_A = 125 \text{ }^\circ\text{C}$ | — | 460 | 1700 | |
| $I_{DDSTDBY1}$ | CC | C | STANDBY1 mode current ¹⁰ | Slow internal RC oscillator (128 kHz) running | $T_A = 25 \text{ }^\circ\text{C}$ | — | 12 | 50 | μA |
| | | C | | | $T_A = 55 \text{ }^\circ\text{C}$ | — | 24 | — | |
| | | C | | | $T_A = 85 \text{ }^\circ\text{C}$ | — | 48 | — | |
| | | C | | | $T_A = 105 \text{ }^\circ\text{C}$ | — | 150 | 500 | |
| | | C | | | $T_A = 125 \text{ }^\circ\text{C}$ | — | 260 | — | |

¹ Except for I_{DDMAX} , all consumptions in this table apply to V_{DD_BV} only and do not include V_{DD_HV} .

² $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40 \text{ to } 125 \text{ }^\circ\text{C}$, unless otherwise specified

³ Running consumption is given on voltage regulator supply (V_{DDREG}). I_{DDMAX} is composed of three components: $I_{DDMAX} = I_{DD}(V_{DD_BV}) + I_{DD}(V_{DD_HV}) + I_{DD}(V_{DD_HV_ADC})$. It does not include a fourth component linked to I/Os toggling which is **highly** dependent on the application. The given value is thought to be a **worst case value** (64 MHz at 125 °C) with all peripherals running, and code fetched from code flash while modify operation on-going on data flash. Note that this value can be significantly reduced by the application: switch off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

- ⁴ Higher current may be sunk by device during power-up and standby exit. Please refer to inrush current in [Table 22](#).
- ⁵ RUN current measured with typical application with accesses on both Flash and RAM.
- ⁶ Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.
- ⁷ Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 to 9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication), instance: 1 to 5 clocks gated. RTC/API ON. PIT ON. STM ON. ADC1 OFF. ADC0 ON but no conversion except two analog watchdogs.
- ⁸ Only for the “P” classification: No clock, FIRC 16 MHz off, SIRC 128 kHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.
- ⁹ Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.
- ¹⁰ ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

3.10 Flash memory electrical characteristics

3.10.1 Program/erase characteristics

[Table 25](#) shows the program and erase characteristics.

Table 25. Program and erase specifications

| Symbol | C | Parameter | Conditions | Value | | | | Unit | |
|--------------------------|----|-----------|--|------------|------------------|--------------------------|------------------|-------|----|
| | | | | Min | Typ ¹ | Initial max ² | Max ³ | | |
| T _{dwprogram} | CC | C | Double word (64 bits) program time ⁴ | Code Flash | — | 18 | 50 | 500 | μs |
| | | | Data Flash | — | 22 | | | | |
| T _{16Kpperase} | | | 16 KB block preprogram and erase time | Code Flash | — | 200 | 500 | 5000 | ms |
| | | | Data Flash | — | 300 | | | | |
| T _{32Kpperase} | | | 32 KB block preprogram and erase time | Code Flash | — | 300 | 600 | 5000 | ms |
| | | | Data Flash | — | 400 | | | | |
| T _{32Kpperase} | | | 32 KB block preprogram and erase time for sector B0F4 | Code Flash | — | 600 | 1200 | 10000 | ms |
| T _{128Kpperase} | | | 128 KB block preprogram and erase time | Code Flash | — | 600 | 1300 | 7500 | ms |
| | | | Data Flash | — | 800 | | | | |
| T _{128Kpperase} | | | 128 KB block preprogram and erase time for sector B0F5 | Code Flash | — | 1200 | 2600 | 15000 | ms |
| T _{eslat} | | D | Erase Suspend Latency | — | — | — | 30 | 30 | μs |
| T _{ESRT} | | C | Erase Suspend Request Rate | Code Flash | 20 | — | — | — | ms |
| | | | Data Flash | 10 | — | — | — | | |

- ¹ Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
- ² Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
- ³ The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
- ⁴ Actual hardware programming times. This does not include software overhead.

Table 26. Flash module life

| Symbol | | C | Parameter | Conditions | Value | | | Unit |
|-----------|----|---|---|---------------------------------------|--------|--------|-----|--------|
| | | | | | Min | Typ | Max | |
| P/E | CC | C | Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T _J) | — | 100000 | — | — | cycles |
| P/E | CC | C | Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T _J) | — | 10000 | 100000 | — | cycles |
| P/E | CC | C | Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T _J) | — | 1000 | 100000 | — | cycles |
| Retention | CC | C | Minimum data retention at 85 °C average ambient temperature ¹ | Blocks with 0–1,000 P/E cycles | 20 | — | — | years |
| | | | | Blocks with 1,001–10,000 P/E cycles | 10 | — | — | years |
| | | | | Blocks with 10,001–100,000 P/E cycles | 5 | — | — | years |

¹ Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 27. Flash read access timing

| Symbol | | C | Parameter | Conditions ¹ | Max | Unit |
|-------------------|----|---|-------------------------------------|-------------------------|-----|------|
| f _{READ} | CC | P | Maximum frequency for Flash reading | 2 wait states | 64 | MHz |
| | | C | | 1 wait state | 40 | |
| | | C | | 0 wait states | 20 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

3.10.2 Flash power supply DC characteristics

Table 28 shows the power supply DC characteristics on external supply.

Table 28. Flash power supply DC electrical characteristics

| Symbol | Parameter | Conditions ¹ | Value | | | Unit | |
|---------------------|--|---|------------|-----|-----|------|----|
| | | | Min | Typ | Max | | |
| I _{CFREAD} | Sum of the current consumption on V _{DDHV} and V _{DDBV} on read access | Flash module read f _{CPU} = 64 MHz ² | Code Flash | — | — | 33 | mA |
| I _{DFREAD} | | | Data Flash | — | — | 33 | |
| I _{CFMOD} | Sum of the current consumption on V _{DDHV} and V _{DDBV} on matrix modification (program/erase) | Program /Erase on-going while reading Flash registers f _{CPU} = 64 MHz ² | Code Flash | — | — | 52 | mA |
| I _{DFMOD} | | | Data Flash | — | — | 33 | |
| I _{CFLPW} | Sum of the current consumption on V _{DDHV} and V _{DDBV} during Flash low power mode | — | Code Flash | — | — | 1.1 | mA |
| I _{DFLPW} | | | Data Flash | — | — | 900 | |
| I _{CFPWD} | Sum of the current consumption on V _{DDHV} and V _{DDBV} during Flash power down mode | — | Code Flash | — | — | 150 | μA |
| I _{DFPWD} | | | Data Flash | — | — | 150 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² f_{CPU} 64 MHz can be achieved at up to 125 °C.

3.10.3 Start-up/Switch-off timings

Table 29. Start-up time/Switch-off time

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|-------------------------|----|-----------|---|-------|-----|-----|------|
| | | | | Min | Typ | Max | |
| T _{FLARSTEXIT} | CC | T | Delay for Flash module to exit reset mode | — | — | 125 | μs |
| T _{FLALPEXIT} | CC | T | Delay for Flash module to exit low-power mode | — | — | 0.5 | |
| T _{FLAPDEXIT} | CC | T | Delay for Flash module to exit power-down mode | — | — | 30 | |
| T _{FLALPENTRY} | CC | T | Delay for Flash module to enter low-power mode | — | — | 0.5 | |
| T _{FLAPDENTRY} | CC | T | Delay for Flash module to enter power-down mode | — | — | 1.5 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

3.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
 - Corrupted program counter
 - Unexpected reset
 - Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.
To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

3.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 30. EMI radiated emission measurement^{1,2}

| Symbol | C | Parameter | Conditions | Value | | | Unit | | |
|--------------------|----|-----------|-----------------------|--|--------------------------------|------|------|------|------|
| | | | | Min | Typ | Max | | | |
| — | SR | — | Scan range | — | — | 1000 | MHz | | |
| f _{CPU} | SR | — | Operating frequency | — | 64 | — | MHz | | |
| V _{DD_LV} | SR | — | LV operating voltages | — | 1.28 | — | V | | |
| S _{EMI} | CC | T | Peak level | V _{DD} = 5 V, T _A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f _{OSC} = 8 MHz/f _{CPU} = 64 MHz | No PLL frequency modulation | — | — | 18 | dBμV |
| | | | | ± 2% PLL frequency modulation | — | — | 14 | dBμV | |

¹ EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

² For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

3.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts×(n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 31. ESD absolute maximum ratings^{1,2}

| Symbol | Ratings | Conditions | Class | Max value ³ | Unit |
|-----------------------|--|---|-------|------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (Human Body Model) | T _A = 25 °C conforming to AEC-Q100-002 | H1C | 2000 | V |
| V _{ESD(MM)} | Electrostatic discharge voltage (Machine Model) | T _A = 25 °C conforming to AEC-Q100-003 | M2 | 200 | |
| V _{ESD(CDM)} | Electrostatic discharge voltage (Charged Device Model) | T _A = 25 °C conforming to AEC-Q100-011 | C3A | 500 750 (corners) | |

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

³ Data based on characterization results, not tested in production

3.11.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

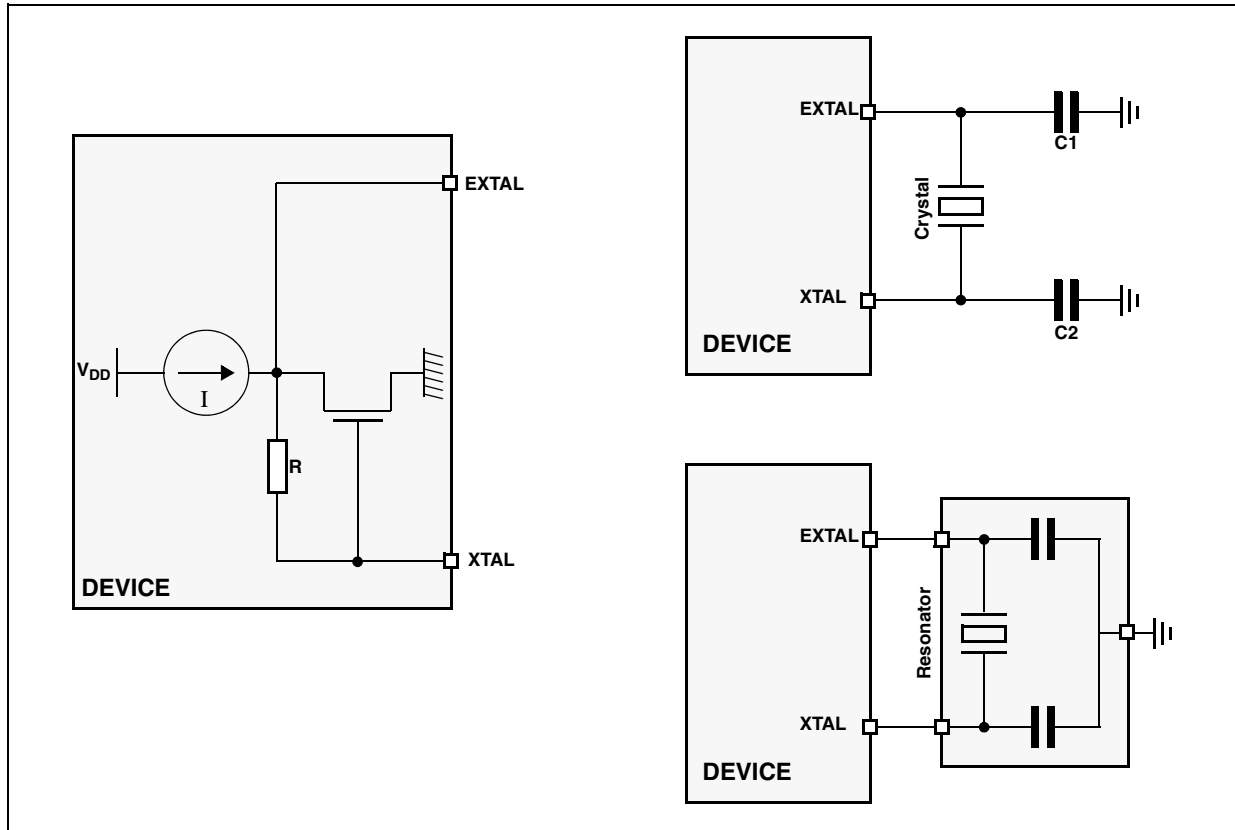
Table 32. Latch-up results

| Symbol | Parameter | Conditions | Class |
|--------|-----------------------|---|------------|
| LU | Static latch-up class | T _A = 125 °C conforming to JESD 78 | II level A |

3.12 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. [Figure 12](#) describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

[Table 33](#) provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.


Figure 12. Crystal oscillator and resonator connection scheme
NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 33. Crystal description

| Nominal frequency (MHz) | NDK crystal reference | Crystal equivalent series resistance ESR Ω | Crystal motional capacitance (C_m) fF | Crystal motional inductance (L_m) mH | Load on xtalin/xtalout $C1 = C2$ (pF) ¹ | Shunt capacitance between xtalout and xtal in $C0^2$ (pF) |
|-------------------------|-----------------------|---|---|--|--|---|
| 4 | NX8045GB | 300 | 2.68 | 591.0 | 21 | 2.93 |
| 8 | NX5032GA | 300 | 2.46 | 160.7 | 17 | 3.01 |
| 10 | | 150 | 2.93 | 86.6 | 15 | 2.91 |
| 12 | | 120 | 3.11 | 56.5 | 15 | 2.93 |
| 16 | | 120 | 3.90 | 25.3 | 10 | 3.00 |

¹ The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

² The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

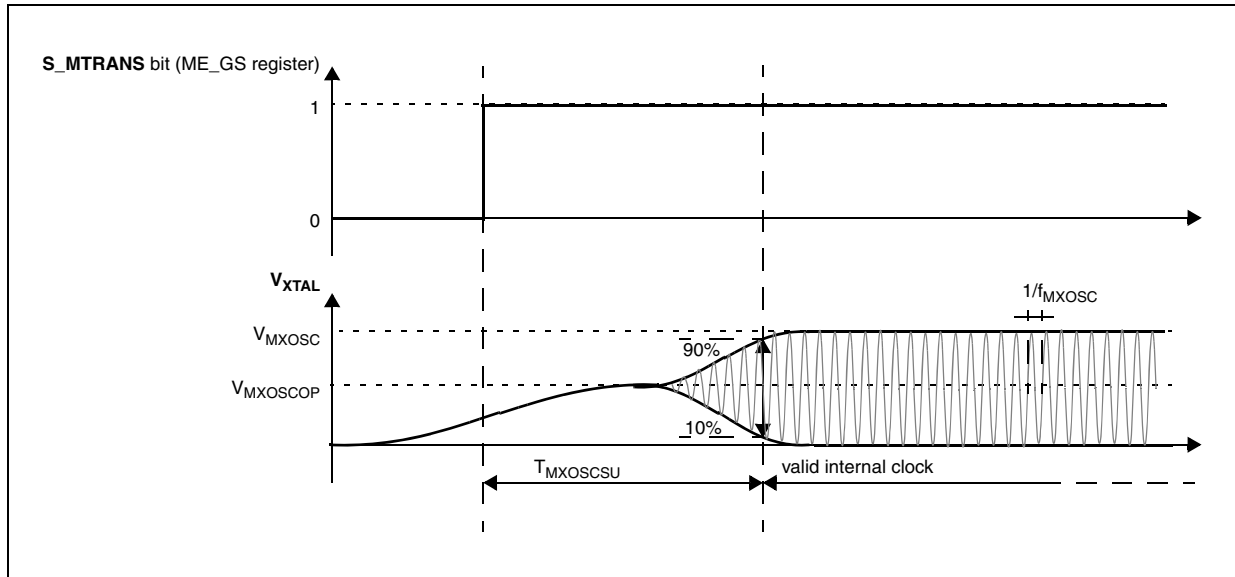


Figure 13. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Table 34. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|---------------------------------|----|-----------|---|--|------|------|------|------|
| | | | | Min | Typ | Max | | |
| f _{FXOSC} | SR | — | Fast external crystal oscillator frequency | 4.0 | — | 16.0 | MHz | |
| g _{mFXOSC} | CC | C | Fast external crystal oscillator transconductance | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0 | 2.2 | — | 8.2 | mA/V |
| | CC | P | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0 | 2.0 | — | 7.4 | |
| | CC | C | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1 | 2.7 | — | 9.7 | |
| | CC | C | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1 | 2.5 | — | 9.2 | |
| V _{FXOSC} | CC | T | Oscillation amplitude at EXTAL | f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0 | 1.3 | — | — | V |
| | | | | f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1 | 1.3 | — | — | |
| V _{FXOSCOIP} | CC | P | Oscillation operating point | — | 0.95 | — | V | |
| I _{FXOSC} ² | CC | T | Fast external crystal oscillator consumption | — | 2 | 3 | mA | |

Table 34. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics (continued)

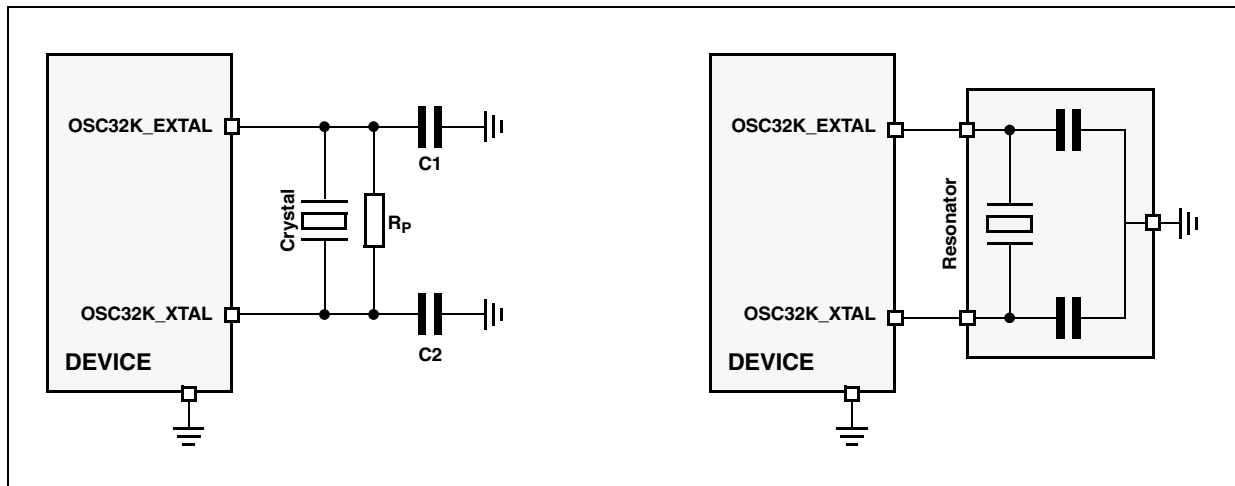
| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|----------------------|----|--|---|---------------------|-----|-----------------------|------|
| | | | | Min | Typ | Max | |
| T _{FXOSCSU} | CC | Fast external crystal oscillator start-up time | f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0 | — | — | 6 | ms |
| | | | f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1 | — | — | 1.8 | |
| V _{IH} | SR | Input high level CMOS (Schmitt Trigger) | Oscillator bypass mode | 0.65V _{DD} | — | V _{DD} + 0.4 | V |
| V _{IL} | SR | Input low level CMOS (Schmitt Trigger) | Oscillator bypass mode | -0.4 | — | 0.35V _{DD} | V |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

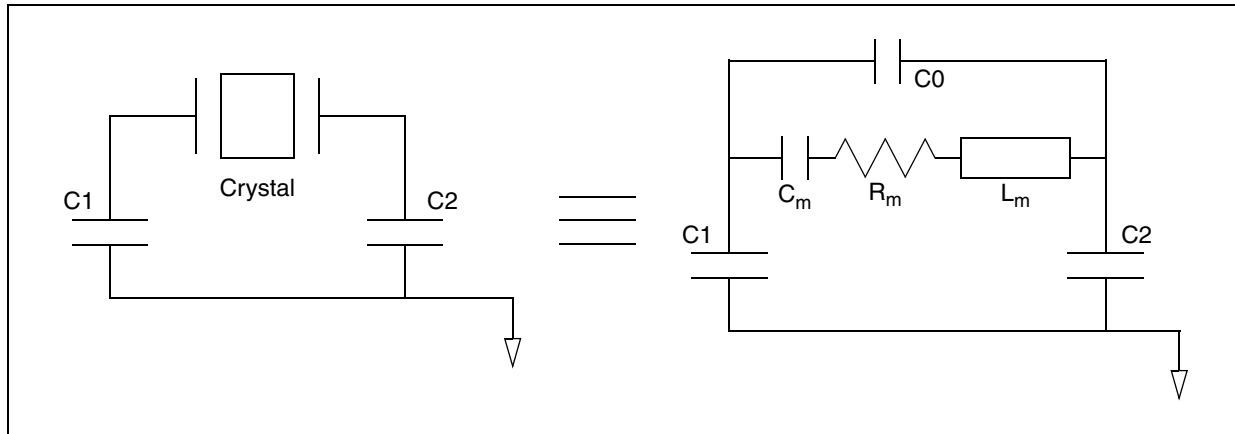
3.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.


Figure 14. Crystal oscillator and resonator connection scheme

NOTE

OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.


Figure 15. Equivalent circuit of a quartz crystal
Table 35. Crystal motional characteristics¹

| Symbol | Parameter | Conditions | Value | | | Unit |
|---------|--|---|-------|--------|-----|------------|
| | | | Min | Typ | Max | |
| L_m | Motional inductance | — | — | 11.796 | — | KH |
| C_m | Motional capacitance | — | — | 2 | — | fF |
| C1/C2 | Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground ² | — | 18 | — | 28 | pF |
| R_m^3 | Motional resistance | AC coupled at $C_0 = 2.85 \text{ pF}^4$ | — | — | 65 | k Ω |
| | | AC coupled at $C_0 = 4.9 \text{ pF}^4$ | — | — | 50 | |
| | | AC coupled at $C_0 = 7.0 \text{ pF}^4$ | — | — | 35 | |
| | | AC coupled at $C_0 = 9.0 \text{ pF}^4$ | — | — | 30 | |

¹ The crystal used is Epson Toyocom MC306.

² This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

³ Maximum ESR (R_m) of the crystal is 50 k Ω

⁴ C_0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

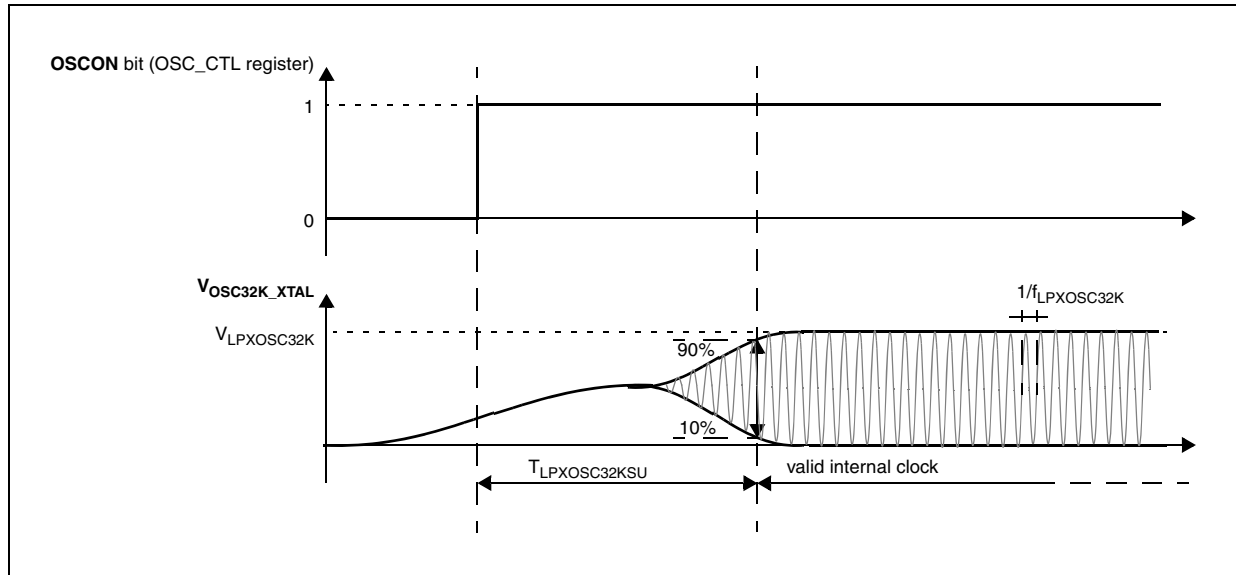


Figure 16. Slow external crystal oscillator (32 kHz) electrical characteristics

Table 36. Slow external crystal oscillator (32 kHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|------------------------|----|-----------|--|-------|--------|----------------|------|
| | | | | Min | Typ | Max | |
| f _{SXOSC} | SR | — | Slow external crystal oscillator frequency | 32 | 32.768 | 40 | kHz |
| V _{SXOSC} | CC | T | Oscillation amplitude | — | 2.1 | — | V |
| I _{SXOSCBIAS} | CC | T | Oscillation bias current | — | 2.5 | | μA |
| I _{SXOSC} | CC | T | Slow external crystal oscillator consumption | — | — | 8 | μA |
| T _{SXOSCSU} | CC | T | Slow external crystal oscillator start-up time | — | — | 2 ² | s |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.14 FMPLL electrical characteristics

The device provides a frequency modulated phase locked loop (FMPLL) module to generate a fast system clock from the FXOSC or FIRC sources.

Table 37. FMPLL electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|--------------------|----|-----------|---|-------|-----|-----|------|
| | | | | Min | Typ | Max | |
| f _{PLLIN} | SR | — | FMPLL reference clock ² | 4 | — | 64 | MHz |
| Δ _{PLLIN} | SR | — | FMPLL reference clock duty cycle ² | 40 | — | 60 | % |

Table 37. FMPLL electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|-------------------------------|----|-----------|--|---|--------|-----------------|------|----|
| | | | | Min | Typ | Max | | |
| f _{PLLOUT} | CC | P | FMPLL output clock frequency | — | 16 | 64 | MHz | |
| f _{VCO} ³ | CC | P | VCO frequency without frequency modulation | — | 256 | 512 | MHz | |
| | | P | VCO frequency with frequency modulation | — | 245.76 | 532.48 | | |
| f _{CPU} | SR | — | System clock frequency | — | — | 64 ⁴ | MHz | |
| f _{FREE} | CC | P | Free-running frequency | — | 20 | 150 | MHz | |
| t _{LOCK} | CC | P | FMPLL lock time | Stable oscillator (f _{PLLIN} = 16 MHz) | | 40 | 100 | μs |
| Δt _{STJIT} | CC | — | FMPLL short term jitter ⁵ | f _{sys} maximum | | -4 | 4 | % |
| Δt _{LTJIT} | CC | — | FMPLL long term jitter | f _{PLLCLK} at 64 MHz, 4000 cycles | | — | 10 | ns |
| I _{PLL} | CC | C | FMPLL consumption | T _A = 25 °C | | — | 4 | mA |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

³ Frequency modulation is considered ± 4%.

⁴ f_{CPU} 64 MHz can be achieved only at up to 105 °C.

⁵ Short term jitter is measured on the clock rising edge at cycle *n* and *n* + 4.

3.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|------------------------------------|----|-----------|--|---------------------------------|-----------------|-----|------|-----|
| | | | | Min | Typ | Max | | |
| f _{FIRC} | CC | P | Fast internal RC oscillator high frequency | T _A = 25 °C, trimmed | | — | 16 | MHz |
| | SR | | | — | 12 | 20 | | |
| I _{FIRC RUN} ² | CC | T | Fast internal RC oscillator high frequency current in running mode | T _A = 25 °C, trimmed | | — | 200 | μA |
| I _{FIRC PWD} | CC | D | Fast internal RC oscillator high frequency current in power down mode | T _A = 25 °C | | — | 10 | μA |
| I _{FIRC STOP} | CC | T | Fast internal RC oscillator high frequency and system clock current in stop mode | T _A = 25 °C | sysclk = off | — | 500 | μA |
| | | | | | sysclk = 2 MHz | — | 600 | |
| | | | | | sysclk = 4 MHz | — | 700 | |
| | | | | | sysclk = 8 MHz | — | 900 | |
| | | | | | sysclk = 16 MHz | — | 1250 | |

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|----------------------|----|-----------|---|-------------------------------|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| T _{FIRCSU} | CC | C | Fast internal RC oscillator start-up time | V _{DD} = 5.0 V ± 10% | — | 1.1 | 2.0 | μs |
| Δ _{FIRCPRE} | CC | C | Fast internal RC oscillator precision after software trimming of f _{FIRC} | T _A = 25 °C | -1 | — | 1 | % |
| Δ _{FIRCTRM} | CC | C | Fast internal RC oscillator trimming step | T _A = 25 °C | — | 1.6 | — | % |
| Δ _{FIRCVAR} | CC | C | Fast internal RC oscillator variation over temperature and supply with respect to f _{FIRC} at T _A = 25 °C in high-frequency configuration | — | -5 | — | 5 | % |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz low power internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 39. Slow internal RC oscillator (128 kHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|--------------------------------|----|-----------|---|---|-----|-----|------|-----|
| | | | | Min | Typ | Max | | |
| f _{SIRC} | CC | P | Slow internal RC oscillator low frequency | T _A = 25 °C, trimmed | — | 128 | — | kHz |
| | SR | | | — | 100 | — | 150 | |
| I _{SIRC} ² | CC | C | Slow internal RC oscillator low frequency current | T _A = 25 °C, trimmed | — | — | 5 | μA |
| T _{SIRCSU} | CC | P | Slow internal RC oscillator start-up time | T _A = 25 °C, V _{DD} = 5.0 V ± 10% | — | 8 | 12 | μs |
| Δ _{SIRCPRE} | CC | C | Slow internal RC oscillator precision after software trimming of f _{SIRC} | T _A = 25 °C | -2 | — | 2 | % |
| Δ _{SIRCTRM} | CC | C | Slow internal RC oscillator trimming step | — | — | 2.7 | — | % |
| Δ _{SIRCVAR} | CC | C | Slow internal RC oscillator variation in temperature and supply with respect to f _{SIRC} at T _A = 55 °C in high frequency configuration | High frequency configuration | -10 | — | 10 | % |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.17 ADC electrical characteristics

3.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

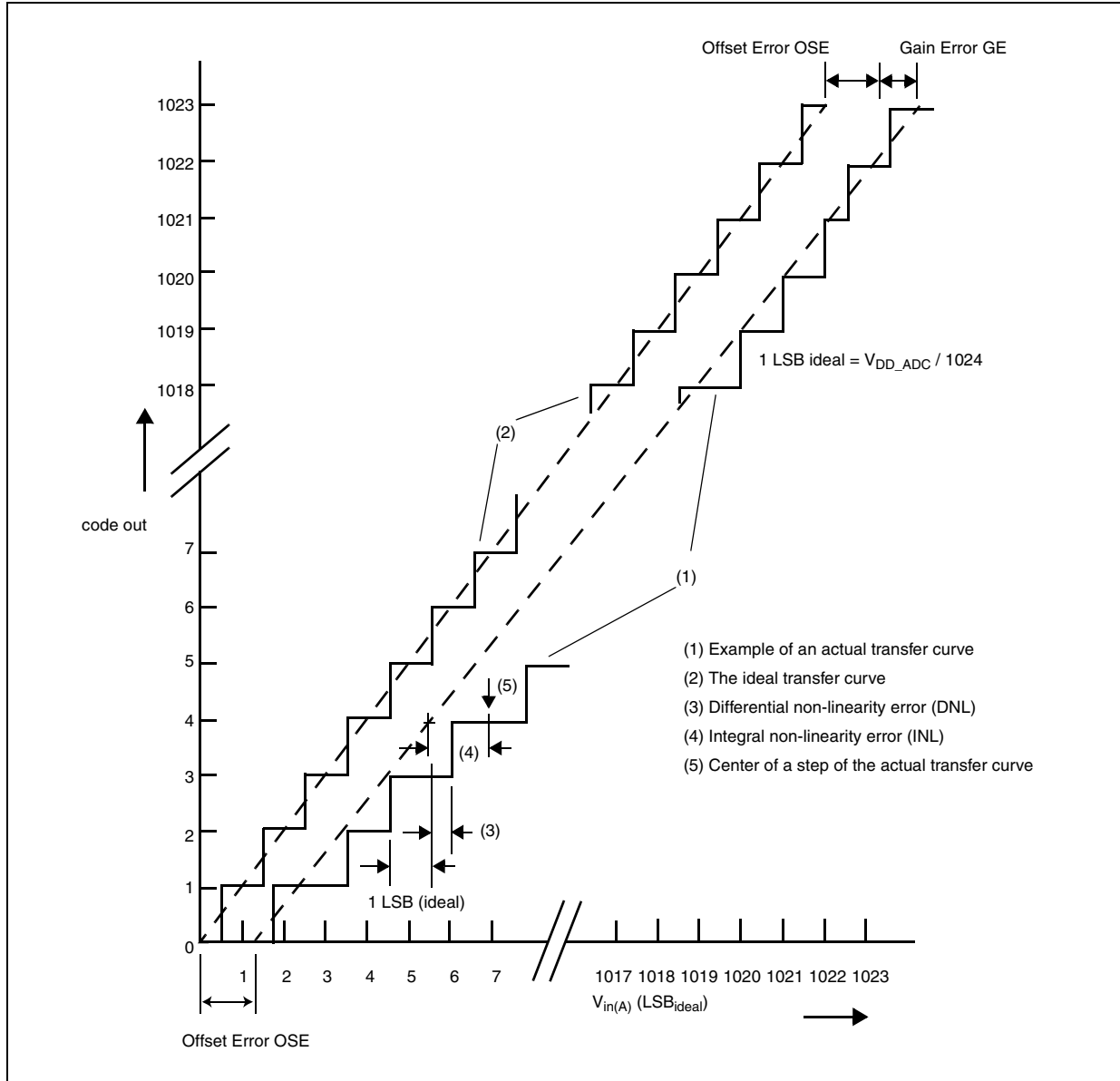


Figure 17. ADC_0 characteristic and error definitions

3.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as

possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 k Ω is obtained ($R_{EQ} = 1 / (fc \times C_S)$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the [Equation 4](#):

Eqn. 4

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} \text{LSB}$$

[Equation 4](#) generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

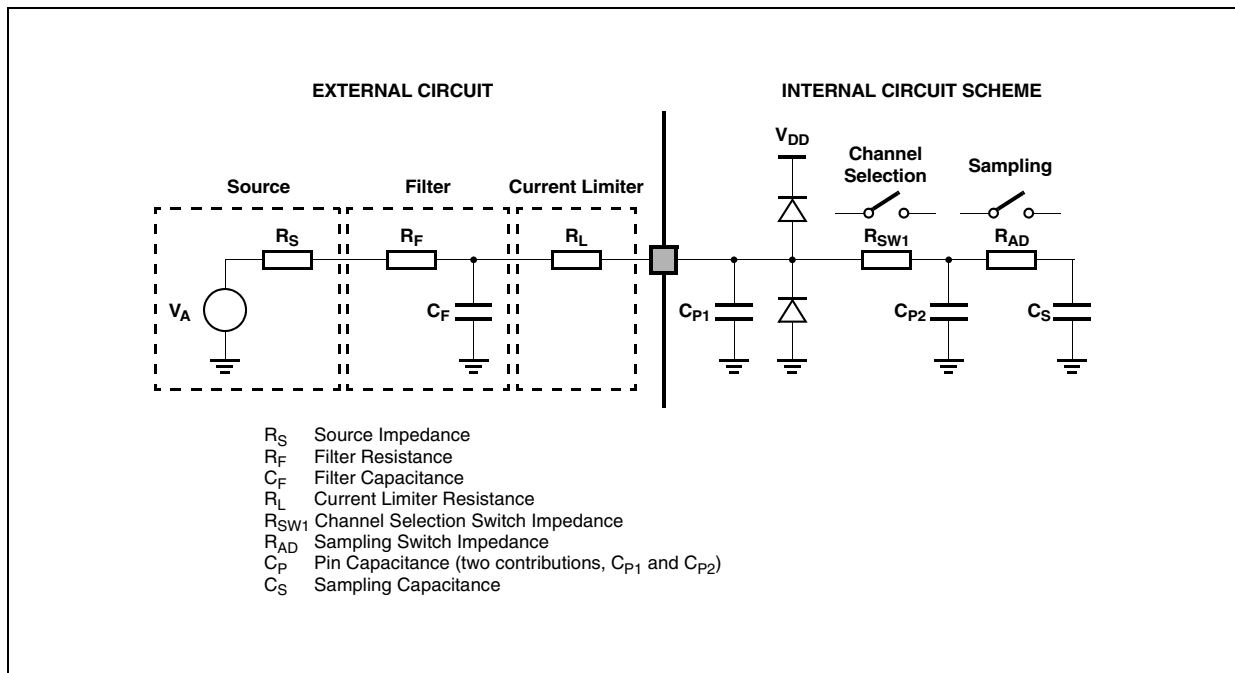


Figure 18. Input equivalent circuit (precise channels)

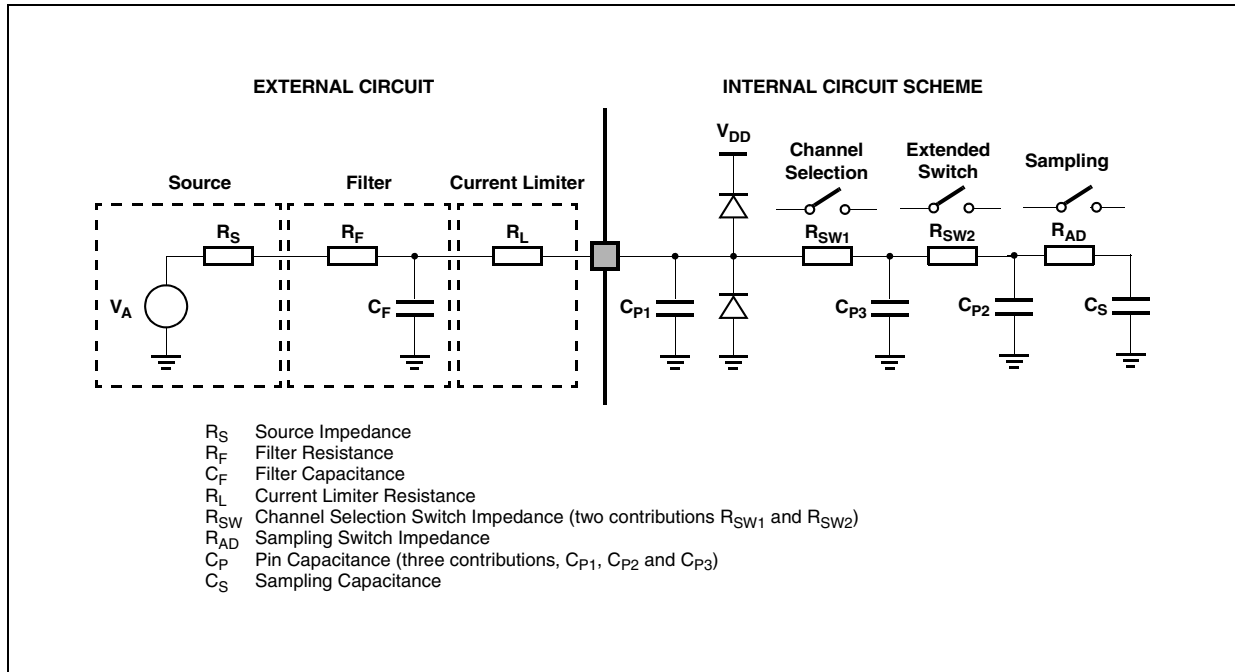


Figure 19. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F , C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 18): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

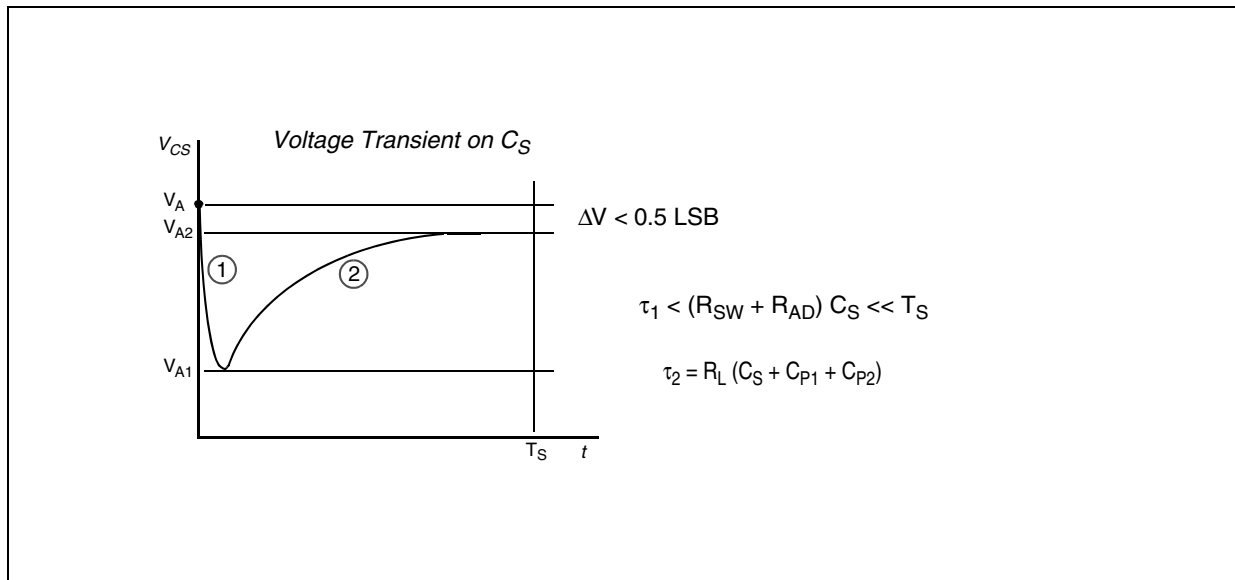


Figure 20. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S , determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L : again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S , a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1} , C_{P2} and C_S , then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1} . Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A ; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as antialiasing.

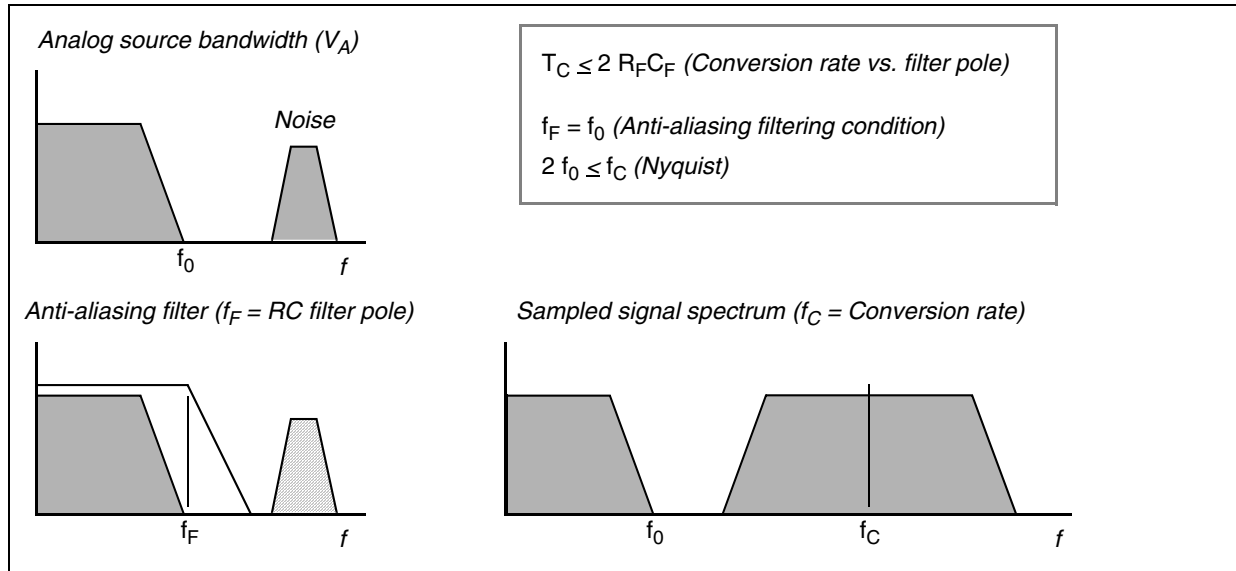


Figure 21. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the antialiasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S , which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S , so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S ; from the two charge balance equations above, it is simple to derive [Equation 11](#) between the ideal and real sampled voltage on C_S :

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

Eqn. 11

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

ADC_0 (10-bit)

$$C_F > 2048 \cdot C_S$$

Eqn. 12

ADC_1 (12-bit)

$$C_F > 8192 \cdot C_S$$

Eqn. 13

3.17.3 ADC electrical characteristics

Table 40. ADC input leakage current

| Symbol | C | Parameter | Conditions | Value | | | Unit | |
|------------------|----|-----------------------|-------------------------|--------------------------------------|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| I _{LKG} | CC | Input leakage current | T _A = -40 °C | No current injection on adjacent pin | — | 1 | — | nA |
| | | | T _A = 25 °C | | — | 1 | — | |
| | | | T _A = 85 °C | | | 3 | 100 | |
| | | | T _A = 105 °C | | — | 8 | 200 | |
| | | | T _A = 125 °C | | — | 45 | 400 | |

Table 41. ADC_0 conversion characteristics (10-bit ADC_0)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|-----------------------|----|-----------|---|---|-------|----------------------------|------|
| | | | | Min | Typ | Max | |
| V _{SS_ADC0} | SR | — | Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V _{SS}) ² | — | — | 0.1 | V |
| V _{DD_ADC0} | SR | — | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS}) | — | — | V _{DD} + 0.1 | V |
| V _{AINx} | SR | — | Analog input voltage ³ | — | — | V _{DD_ADC0} + 0.1 | V |
| I _{ADC0pwd} | SR | — | ADC_0 consumption in power down mode | — | — | 50 | μA |
| I _{ADC0run} | SR | — | ADC_0 consumption in running mode | — | — | 5 | mA |
| f _{ADC0} | SR | — | ADC_0 analog frequency | — | — | 32 + 4% | MHz |
| Δ _{ADC0_SYS} | SR | — | ADC_0 digital clock duty cycle (ipg_clk) | ADCLKSEL = 1 ⁴ | 45 | 55 | % |
| t _{ADC0_PU} | SR | — | ADC_0 power up delay | — | — | 1.5 | μs |
| t _{ADC0_S} | CC | T | Sample time ⁵ | f _{ADC} = 32 MHz, ADC0_conf_sample_input = 17 | 0.5 | — | μs |
| | | | | f _{ADC} = 6 MHz, INPSAMP = 255 | — | — | |
| t _{ADC0_C} | CC | P | Conversion time ⁶ | f _{ADC} = 32 MHz, ADC_conf_comp = 2 | 0.625 | — | μs |
| C _S | CC | D | ADC_0 input sampling capacitance | — | — | 3 | pF |
| C _{P1} | CC | D | ADC_0 input pin capacitance 1 | — | — | 3 | pF |
| C _{P2} | CC | D | ADC_0 input pin capacitance 2 | — | — | 1 | pF |
| C _{P3} | CC | D | ADC_0 input pin capacitance 3 | — | — | 1 | pF |

Table 41. ADC_0 conversion characteristics (10-bit ADC_0) (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|------------------|----|-----------|---|-------------------------------|-----|-----|------|-----|
| | | | | Min | Typ | Max | | |
| R _{SW1} | CC | D | Internal resistance of analog source | — | — | 3 | kΩ | |
| R _{SW2} | CC | D | Internal resistance of analog source | — | — | 2 | kΩ | |
| R _{AD} | CC | D | Internal resistance of analog source | — | — | 2 | kΩ | |
| I _{INJ} | SR | — | Input current Injection Current injection on one ADC_0 input, different from the converted one | V _{DD} = 3.3 V ± 10% | —5 | — | 5 | mA |
| | | | | V _{DD} = 5.0 V ± 10% | —5 | — | 5 | |
| INL | CC | T | Absolute value for integral nonlinearity | No overload | — | 0.5 | 1.5 | LSB |
| DNL | CC | T | Absolute differential nonlinearity | No overload | — | 0.5 | 1.0 | LSB |
| OFS | CC | T | Absolute offset error | — | — | 0.5 | — | LSB |
| GNE | CC | T | Absolute gain error | — | — | 0.6 | — | LSB |
| TUEP | CC | P | Total unadjusted error ⁷ for precise channels, input only pins | Without current injection | —2 | 0.6 | 2 | LSB |
| | | T | | With current injection | —3 | — | 3 | |
| TUEx | CC | T | Total unadjusted error ⁷ for extended channel | Without current injection | —3 | 1 | 3 | LSB |
| | | T | | With current injection | —4 | — | 4 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² Analog and digital V_{SS} **must** be common (to be tied together externally).

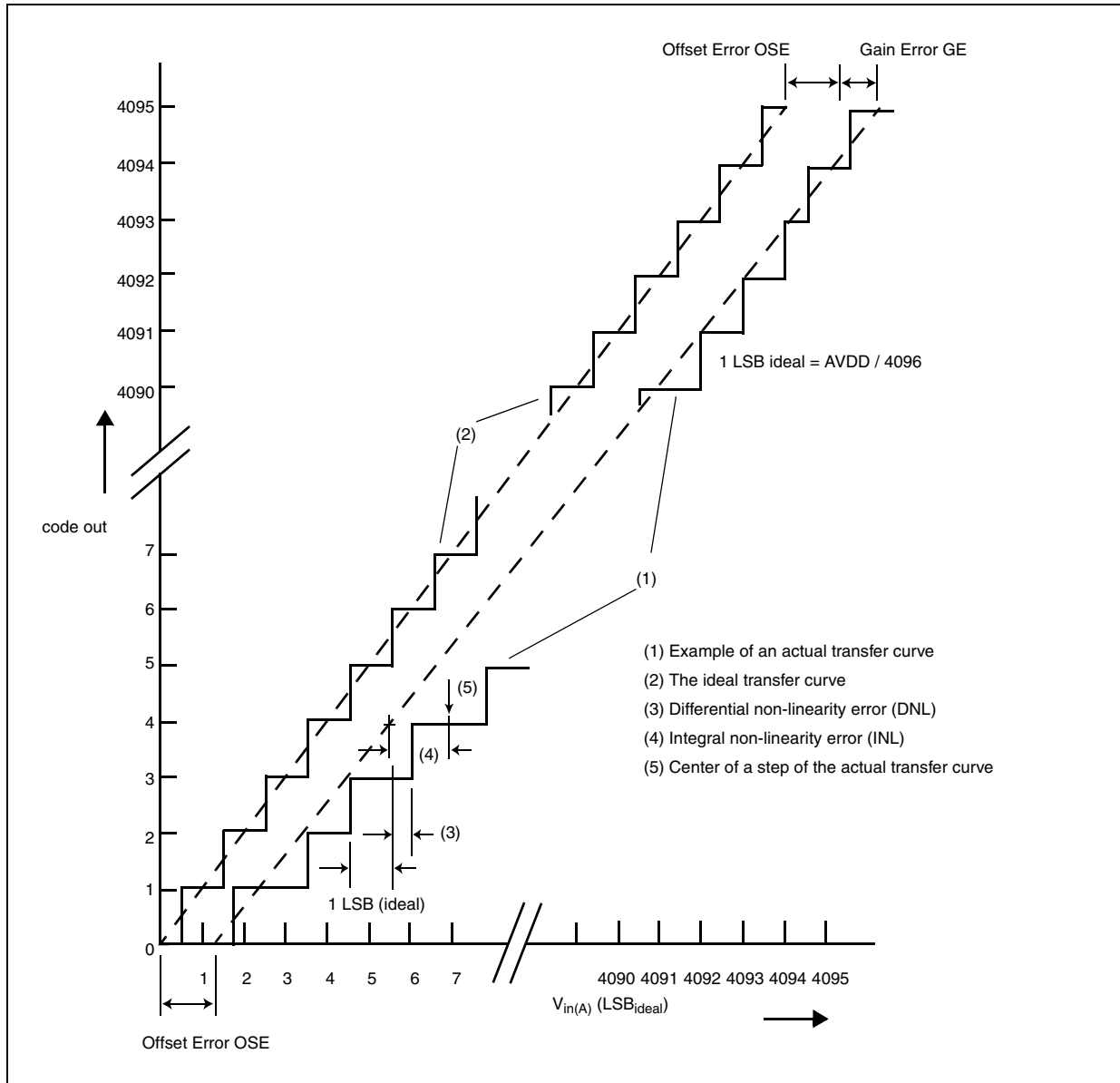
³ V_{AINx} may exceed V_{SS_ADC0} and V_{DD_ADC0} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

⁴ Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

⁵ During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC0_S}. After the end of the sample time t_{ADC0_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC0_S} depend on programming.

⁶ This parameter does not include the sample time t_{ADC0_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

⁷ Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.


Figure 22. ADC_1 characteristic and error definitions
Table 42. ADC_1 conversion characteristics (12-bit ADC_1)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|----------------|----|-----------|-------------------------|----------------|-----|----------------|------|
| | | | | Min | Typ | Max | |
| V_{SS_ADC1} | SR | — | — | -0.1 | — | 0.1 | V |
| V_{DD_ADC1} | SR | — | — | $V_{DD} - 0.1$ | — | $V_{DD} + 0.1$ | V |

Table 42. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|-----------------------|----|-----------|---|---|------|-----|---------|-----|
| | | | | Min | Typ | Max | | |
| V _{AINx} | SR | — | Analog input voltage ³ | — | | | V | |
| I _{ADC1pwd} | SR | — | ADC_1 consumption in power down mode | — | — | 50 | μA | |
| I _{ADC1run} | SR | — | ADC_1 consumption in running mode | — | — | 6 | mA | |
| f _{ADC1} | SR | — | ADC_1 analog frequency | V _{DD} = 3.3 V | 3.33 | — | 20 + 4% | MHz |
| | | | | V _{DD} = 5 V | 3.33 | — | 32 + 4% | |
| t _{ADC1_PU} | SR | — | ADC_1 power up delay | — | — | 1.5 | μs | |
| t _{ADC1_S} | CC | T | Sample time ⁴ VDD = 3.3 V | f _{ADC1} = 20 MHz, ADC1_conf_sample_input = 12 | 600 | — | — | ns |
| | | | Sample time ⁴ VDD = 5.0 V | f _{ADC1} = 32 MHz, ADC1_conf_sample_input = 17 | 500 | — | — | |
| | | | Sample time ⁴ VDD = 3.3 V | f _{ADC1} = 3.33 MHz, ADC1_conf_sample_input = 255 | — | — | 76.2 | μs |
| | | | Sample time ⁴ VDD = 5.0 V | f _{ADC1} = 3.33 MHz, ADC1_conf_sample_input = 255 | — | — | 76.2 | |
| t _{ADC1_C} | CC | P | Conversion time ⁵ VDD = 3.3 V | f _{ADC1} = 20MHz, ADC1_conf_comp = 0 | 2.4 | — | — | μs |
| | | | Conversion time ⁵ VDD = 5.0 V | f _{ADC1} = 32 MHz, ADC1_conf_comp = 0 | 1.5 | — | — | μs |
| | | | Conversion time ⁵ VDD = 3.3 V | f _{ADC1} = 13.33 MHz, ADC1_conf_comp = 0 | — | — | 3.6 | μs |
| | | | Conversion time ⁵ VDD = 5.0 V | f _{ADC1} = 13.33 MHz, ADC1_conf_comp = 0 | — | — | 3.6 | μs |
| Δ _{ADC1_SYS} | SR | — | ADC_1 digital clock duty cycle | ADCLKSEL = 1 ⁶ | 45 | — | 55 | % |
| C _S | CC | D | ADC_1 input sampling capacitance | — | — | — | 5 | pF |
| C _{P1} | CC | D | ADC_1 input pin capacitance 1 | — | — | — | 3 | pF |
| C _{P2} | CC | D | ADC_1 input pin capacitance 2 | — | — | — | 1 | pF |
| C _{P3} | CC | D | ADC_1 input pin capacitance 3 | — | — | — | 1.5 | pF |
| R _{SW1} | CC | D | Internal resistance of analog source | — | — | — | 1 | kΩ |
| R _{SW2} | CC | D | Internal resistance of analog source | — | — | — | 2 | kΩ |
| R _{AD} | CC | D | Internal resistance of analog source | — | — | — | 0.3 | kΩ |

Table 42. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-------------------|----|-----------|--|--|-------------------------------|-----|------|-----|----|
| | | | | Min | Typ | Max | | | |
| I _{INJ} | SR | — | Input current Injection | Current injection on one ADC_1 input, different from the converted one | V _{DD} = 3.3 V ± 10% | −5 | — | 5 | mA |
| | | | | | V _{DD} = 5.0 V ± 10% | −5 | — | 5 | |
| INLP | CC | T | Absolute Integral non-linearity-Precise channels | No overload | — | 1 | 3 | LSB | |
| INLX | CC | T | Absolute Integral non-linearity-Extended channels | No overload | — | 1.5 | 5 | LSB | |
| DNL | CC | T | Absolute Differential non-linearity | No overload | — | 0.5 | 1 | LSB | |
| OFS | CC | T | Absolute Offset error | — | — | 2 | — | LSB | |
| GNE | CC | T | Absolute Gain error | — | — | 2 | — | LSB | |
| TUEP ⁷ | CC | P | Total Unadjusted Error for precise channels, input only pins | Without current injection | −6 | — | 6 | LSB | |
| | | T | | With current injection | −8 | — | 8 | | |
| TUEX ⁷ | CC | T | Total Unadjusted Error for extended channel | Without current injection | −10 | — | 10 | LSB | |
| | | T | | With current injection | −12 | — | 12 | | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

² Analog and digital V_{SS} **must** be common (to be tied together externally).

³ V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFFF.

⁴ During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sample time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC1_S} depend on programming.

⁵ This parameter does not include the sample time t_{ADC1_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

⁶ Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

⁷ Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

3.18 On-chip peripherals

3.18.1 Current consumption

Table 43. On-chip peripherals current consumption¹

| Symbol | C | Parameter | Conditions | | Value | Unit |
|-------------------------------------|----|--|---|---|------------------------------|------|
| | | | | | Typ | |
| I _{DD_BV(CAN)} | CC | T CAN (FlexCAN) supply current on V _{DD_BV} | Bit rate = 500 KB/s | Total (static + dynamic) consumption: <ul style="list-style-type: none"> FlexCAN in loop-back mode XTAL at 8 MHz used as CAN engine clock source Message sending period is 580 μs | 8 * f _{periph} + 85 | μA |
| | | | Bit rate = 125 KB/s | | 8 * f _{periph} + 27 | |
| I _{DD_BV(eMIOS)} | CC | T eMIOS supply current on V _{DD_BV} | Static consumption: <ul style="list-style-type: none"> eMIOS channel OFF Global prescaler enabled | | 29 * f _{periph} | |
| | | | Dynamic consumption: <ul style="list-style-type: none"> It does not change varying the frequency (0.003 mA) | | 3 | |
| I _{DD_BV(SCI)} | CC | T SCI (LINFlex) supply current on V _{DD_BV} | Total (static + dynamic) consumption: <ul style="list-style-type: none"> LIN mode Baud rate: 20 KB/s | | 5 * f _{periph} + 31 | |
| I _{DD_BV(SPI)} | CC | T SPI (DSPI) supply current on V _{DD_BV} | Ballast static consumption (only clocked) | | 1 | |
| | | | Ballast dynamic consumption (continuous communication): <ul style="list-style-type: none"> Baud rate: 2 Mb/s Transmission every 8 μs Frame: 16 bits | | 16 * f _{periph} | |
| I _{DD_BV} (ADC_0/ADC_1) | CC | T ADC_0/ADC_1 supply current on V _{DD_BV} | V _{DD} = 5.5 V | Ballast static consumption (no conversion) | 41 * f _{periph} | μA |
| | | | V _{DD} = 5.5 V | Ballast dynamic consumption (continuous conversion) | 46 * f _{periph} | |
| I _{DD_HV_ADC0} | CC | T ADC_0 supply current on V _{DD_HV_ADC0} | V _{DD} = 5.5 V | Analog static consumption (no conversion) | 200 | mA |
| | | | V _{DD} = 5.5 V | Analog dynamic consumption (continuous conversion) | 3 | |

Table 43. On-chip peripherals current consumption¹ (continued)

| Symbol | C | Parameter | Conditions | | Value | Unit |
|---------------------------|----|--|-------------------------|--|---------------------------|------|
| | | | | | Typ | |
| I _{DD_HV_ADC1} | CC | ADC_1 supply current on V _{DD_HV_ADC1} | V _{DD} = 5.5 V | Analog static consumption (no conversion) | 300 * f _{periph} | μA |
| | | | V _{DD} = 5.5 V | Analog dynamic consumption (continuous conversion) | 4 | mA |
| I _{DD_HV(FLASH)} | CC | CFlash + DFlash supply current on V _{DD_HV} | V _{DD} = 5.5 V | — | 12 | mA |
| I _{DD_BV(PLL)} | CC | PLL supply current on V _{DD_BV} | V _{DD} = 5.5 V | — | 2.5 | mA |

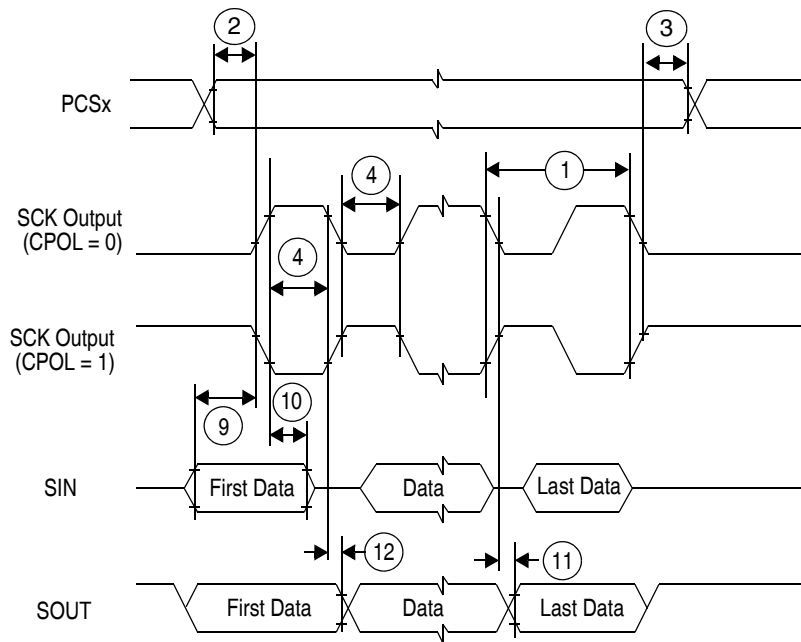
¹ Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 64 MHz

3.18.2 DSPI characteristics

Table 44. DSPI characteristics¹

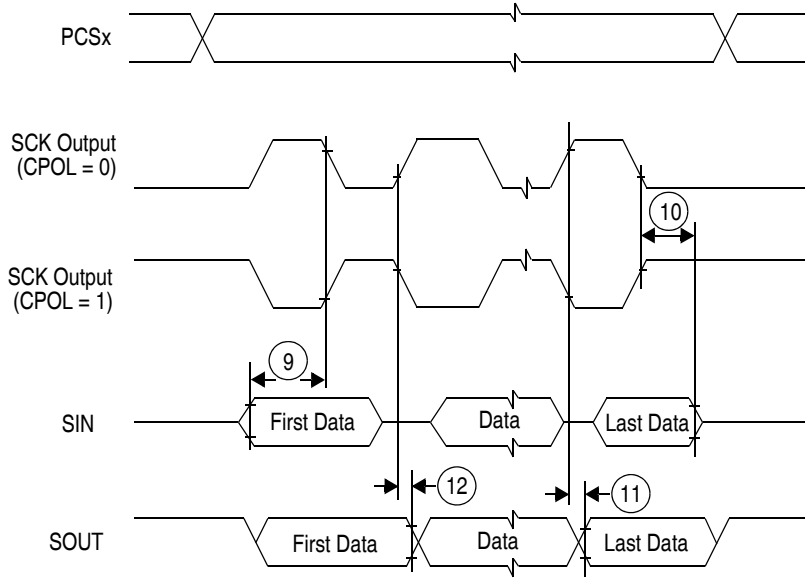
| No. | Symbol | C | D | Parameter | DSPI0/DSPI1/DSPI5/DSPI6 | | | DSPI2/DSPI4 | | | Unit | |
|-----|----------------|----|---|-----------------------------------|---------------------------|------------------|-------------|-------------------|------------------|-------------|--------------------|----|
| | | | | | Min | Typ | Max | Min | Typ | Max | | |
| 1 | t_{SCK} | SR | D | SCK cycle time | Master mode (MTFE = 0) | 125 | — | — | 333^2 | — | — | ns |
| | | | D | | Slave mode (MTFE = 0) | 125 | — | — | 333 | — | — | |
| | | | D | | Master mode (MTFE = 1) | 83 | — | — | 145 | — | — | |
| | | | D | | Slave mode (MTFE = 1) | 83 | — | — | 145 | — | — | |
| — | f_{DSPI} | SR | D | DSPI digital controller frequency | — | — | f_{CPU} | — | — | f_{CPU} | MHz | |
| 2 | t_{CSCext}^3 | SR | D | CS to SCK delay | Slave mode | 32 | — | — | 32 | — | — | ns |
| 3 | t_{ASCext}^4 | SR | D | After SCK delay | Slave mode | $1/f_{DSPI} + 5$ | — | — | $1/f_{DSPI} + 5$ | — | — | ns |
| 4 | t_{SDC} | CC | D | SCK duty cycle | Master mode | — | $t_{SCK}/2$ | — | — | $t_{SCK}/2$ | — | ns |
| | | | D | | Slave mode | $t_{SCK}/2$ | — | — | $t_{SCK}/2$ | — | — | |
| 5 | t_A | SR | D | Slave access time | Slave mode | — | — | $1/f_{DSPI} + 70$ | — | — | $1/f_{DSPI} + 130$ | ns |
| 6 | t_{DI} | SR | D | Slave SOUT disable time | Slave mode | 7 | — | — | 7 | — | — | ns |
| 7 | t_{PCSC} | CC | D | PCSx to \overline{PCSS} time | — | 13^5 | — | — | 13^5 | — | — | |
| 8 | t_{PASC} | CC | D | \overline{PCSS} to PCSx time | — | 13^5 | — | — | 13^5 | — | — | |
| 9 | t_{SUI} | SR | D | Data setup time for inputs | Master mode | 43 | — | — | 145 | — | — | ns |
| | | | | | Slave mode | 5 | — | — | 5 | — | — | |
| 10 | t_{HI} | SR | D | Data hold time for inputs | Master mode | 0 | — | — | 0 | — | — | ns |
| | | | | | Slave mode | 2^6 | — | — | 2^6 | — | — | |
| 11 | t_{SUO}^7 | CC | D | Data valid after SCK edge | Master mode | — | — | 32 | — | — | 50 | ns |
| | | | | | Slave mode | — | — | 52 | — | — | 160 | |
| 12 | t_{HO}^7 | CC | D | Data hold time for outputs | Master mode | 0 | — | — | 0 | — | — | ns |
| | | | | | Slave mode | 8 | — | — | 13 | — | — | |

- 1 Operating conditions: $C_{out} = 10$ to 50 pF, $Slew_{IN} = 3.5$ to 15 ns.
- 2 For DSPI4, if SOUT is mapped to a SLOW pad while SCK is mapped to a MEDIUM pad (or vice versa), the minimum cycle time for SCK should be calculated based on the rise and fall times of the SLOW pad. For MTFE=1, SOUT must not be mapped to a SLOW pad while SCK is mapped to a MEDIUM pad.
- 3 The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext} .
- 4 The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext} .
- 5 For $DSPIx_CTARn[PCSSCK] = 11$.
- 6 This delay value corresponds to $SMPL_PT = 00b$ which is bit field 9 and 8 of DSPI_MCR register.
- 7 SCK and SOUT are configured as MEDIUM pad.



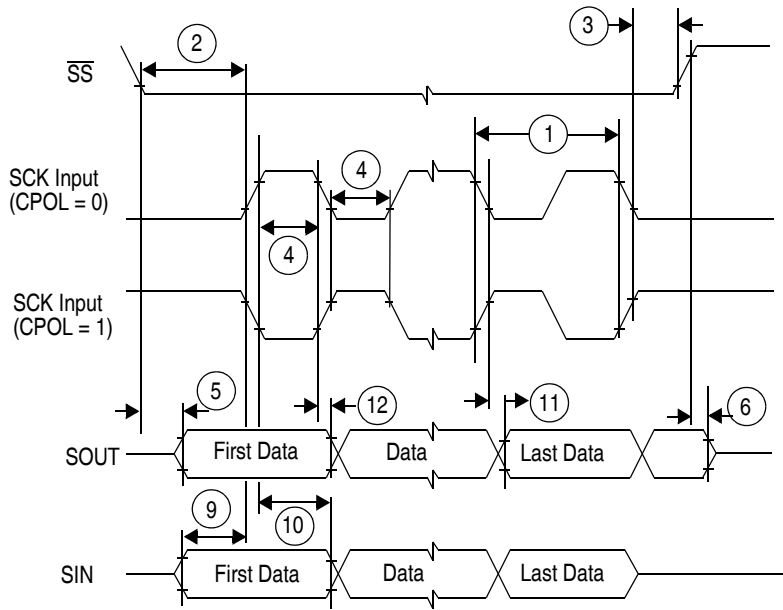
Note: Numbers shown reference [Table 44](#).

Figure 23. DSPI classic SPI timing — master, CPHA = 0



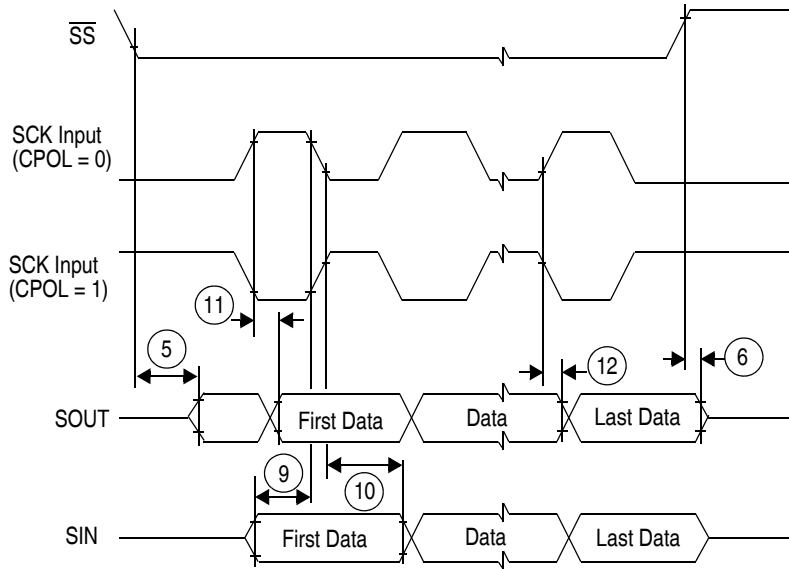
Note: Numbers shown reference [Table 44](#).

Figure 24. DSPI classic SPI timing — master, CPHA = 1



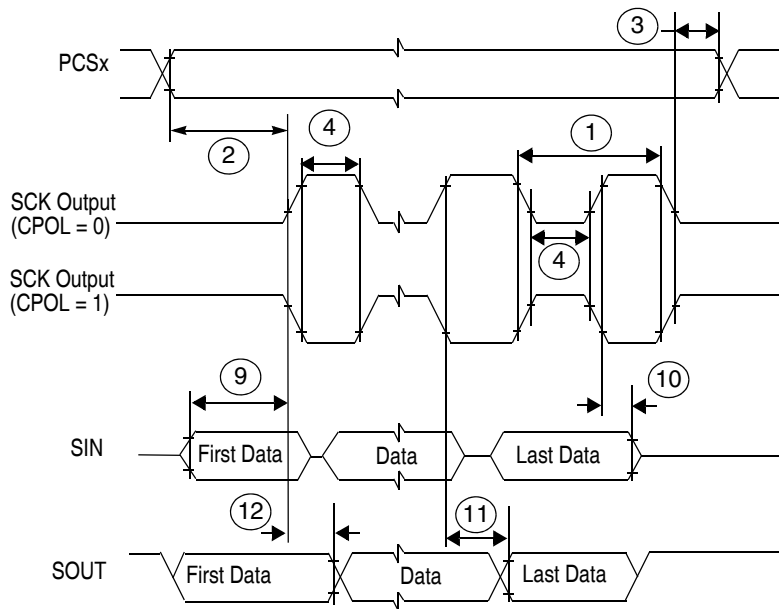
Note: Numbers shown reference [Table 44](#).

Figure 25. DSPI classic SPI timing — slave, CPHA = 0



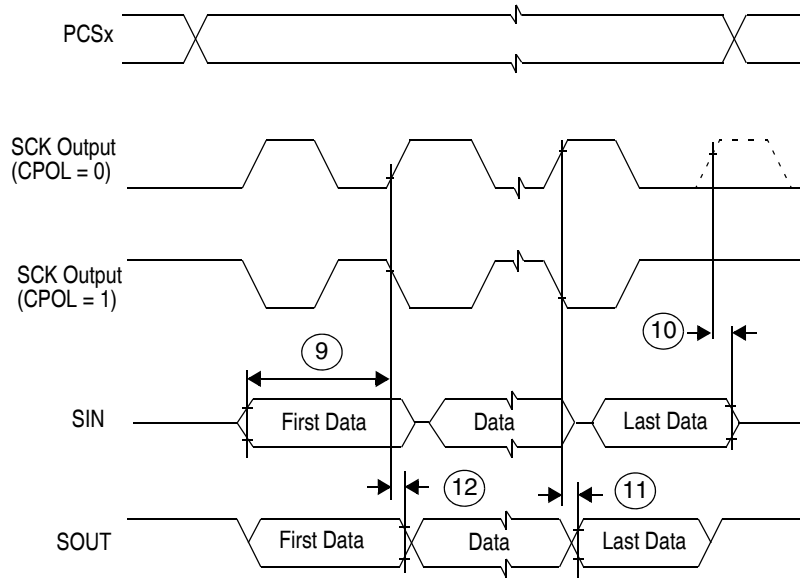
Note: Numbers shown reference [Table 44](#).

Figure 26. DSPI classic SPI timing — slave, CPHA = 1



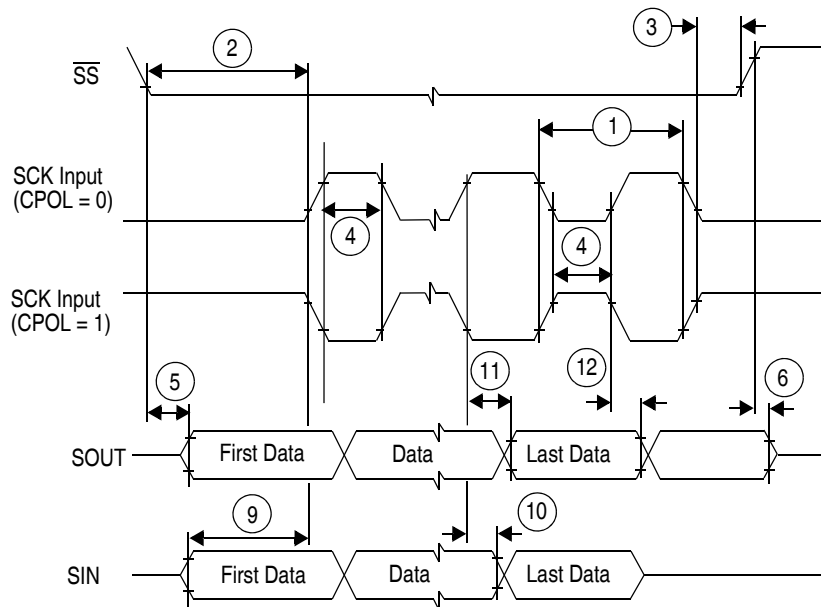
Note: Numbers shown reference [Table 44](#).

Figure 27. DSPI modified transfer format timing — master, CPHA = 0



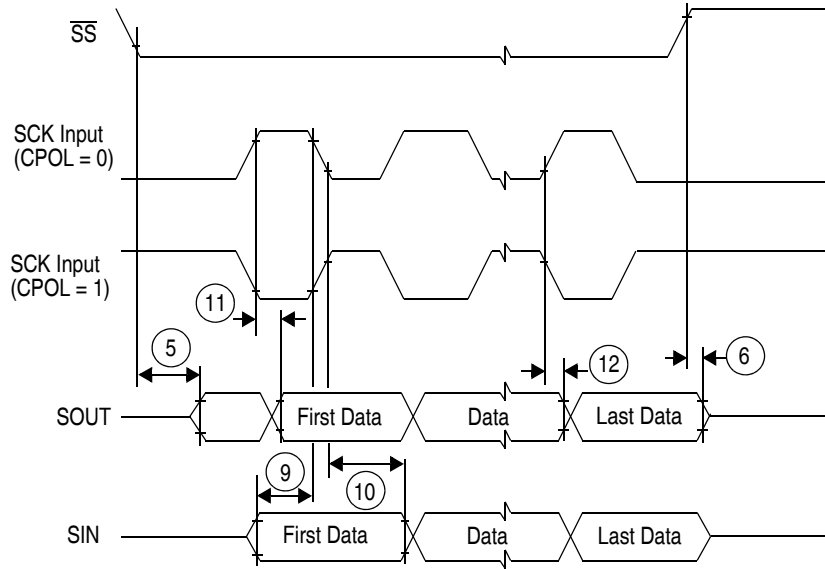
Note: Numbers shown reference [Table 44](#).

Figure 28. DSPI modified transfer format timing — master, CPHA = 1



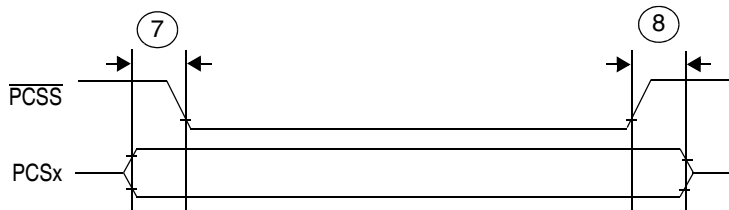
Note: Numbers shown reference [Table 44](#).

Figure 29. DSPI modified transfer format timing — slave, CPHA = 0



Note: Numbers shown reference [Table 44](#).

Figure 30. DSPI modified transfer format timing — slave, CPHA = 1



Note: Numbers shown reference [Table 44](#).

Figure 31. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.18.3 JTAG characteristics

Table 45. JTAG characteristics

| No. | Symbol | C | Parameter | Value | | | Unit | |
|-----|-------------------|----|-----------|----------------|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| 1 | t_{JCYC} | CC | D | TCK cycle time | 64 | — | — | ns |
| 2 | t_{TDIS} | CC | D | TDI setup time | 15 | — | — | ns |
| 3 | t_{TDIH} | CC | D | TDI hold time | 5 | — | — | ns |

Table 45. JTAG characteristics (continued)

| No. | Symbol | C | Parameter | Value | | | Unit | |
|-----|------------|----|-----------|------------------------|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| 4 | t_{TMSS} | CC | D | TMS setup time | 15 | — | — | ns |
| 5 | t_{TMSH} | CC | D | TMS hold time | 5 | — | — | ns |
| 6 | t_{TDOV} | CC | D | TCK low to TDO valid | — | — | 33 | ns |
| 7 | t_{TDOI} | CC | D | TCK low to TDO invalid | 6 | — | — | ns |

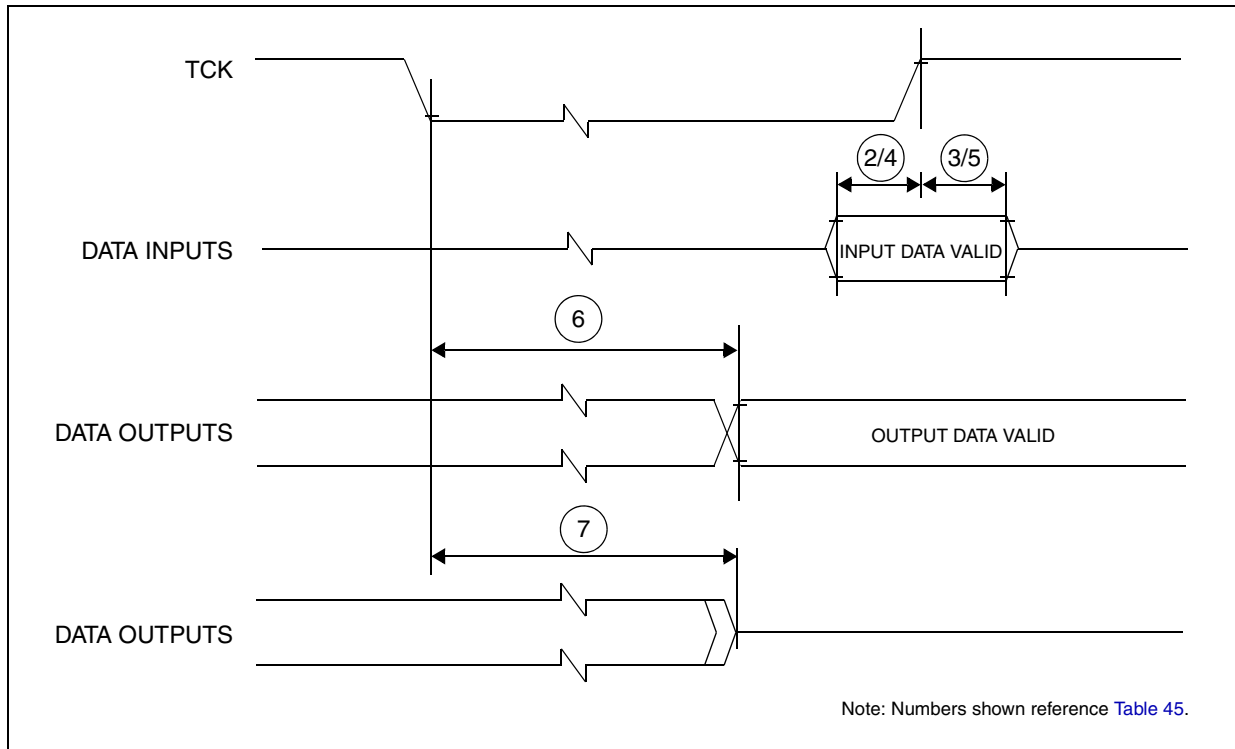


Figure 32. Timing diagram — JTAG boundary scan

4 Package characteristics

4.1 Package mechanical data

4.1.1 176 LQFP

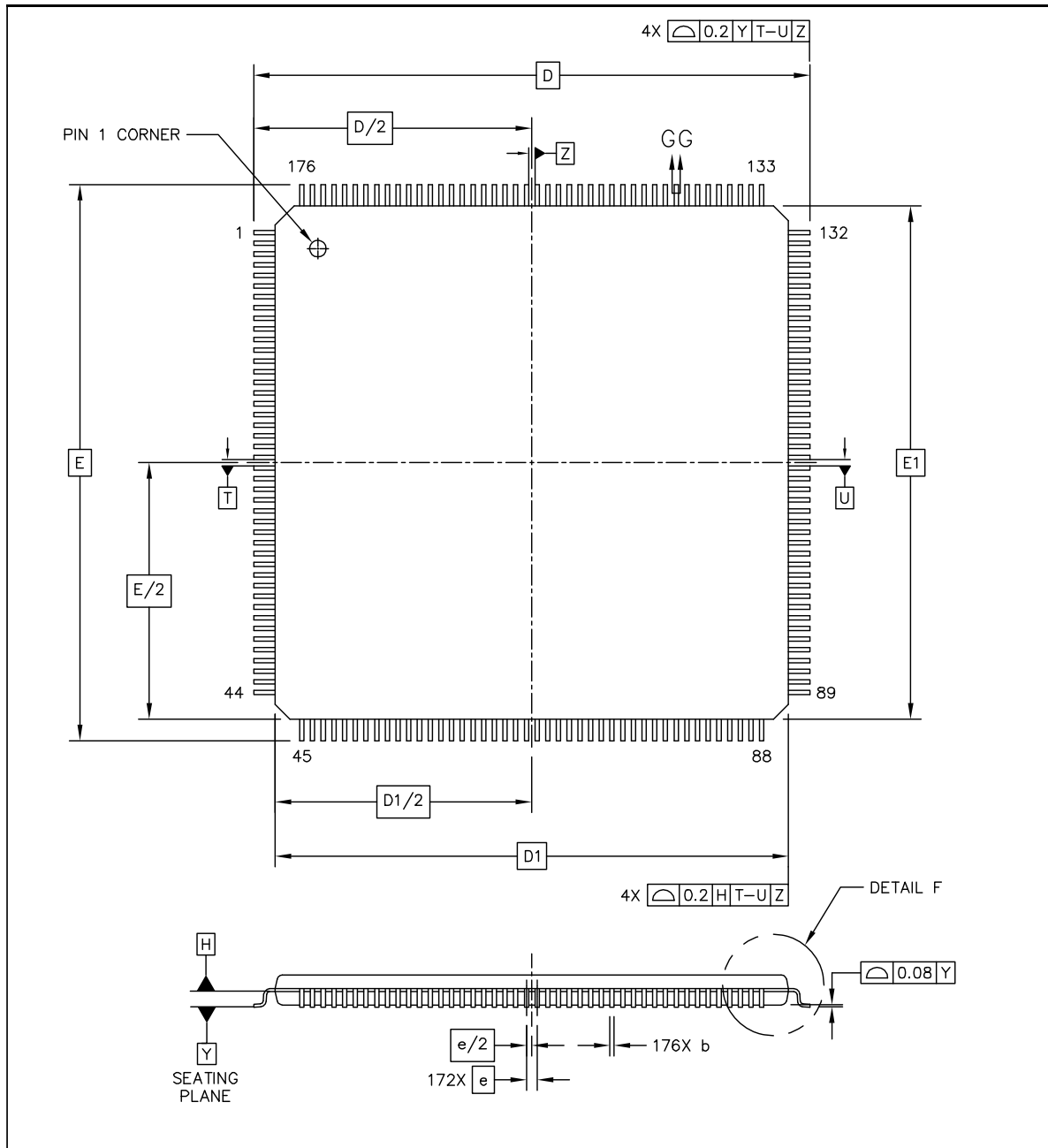


Figure 33. 176 LQFP package mechanical drawing (Part 1 of 3)

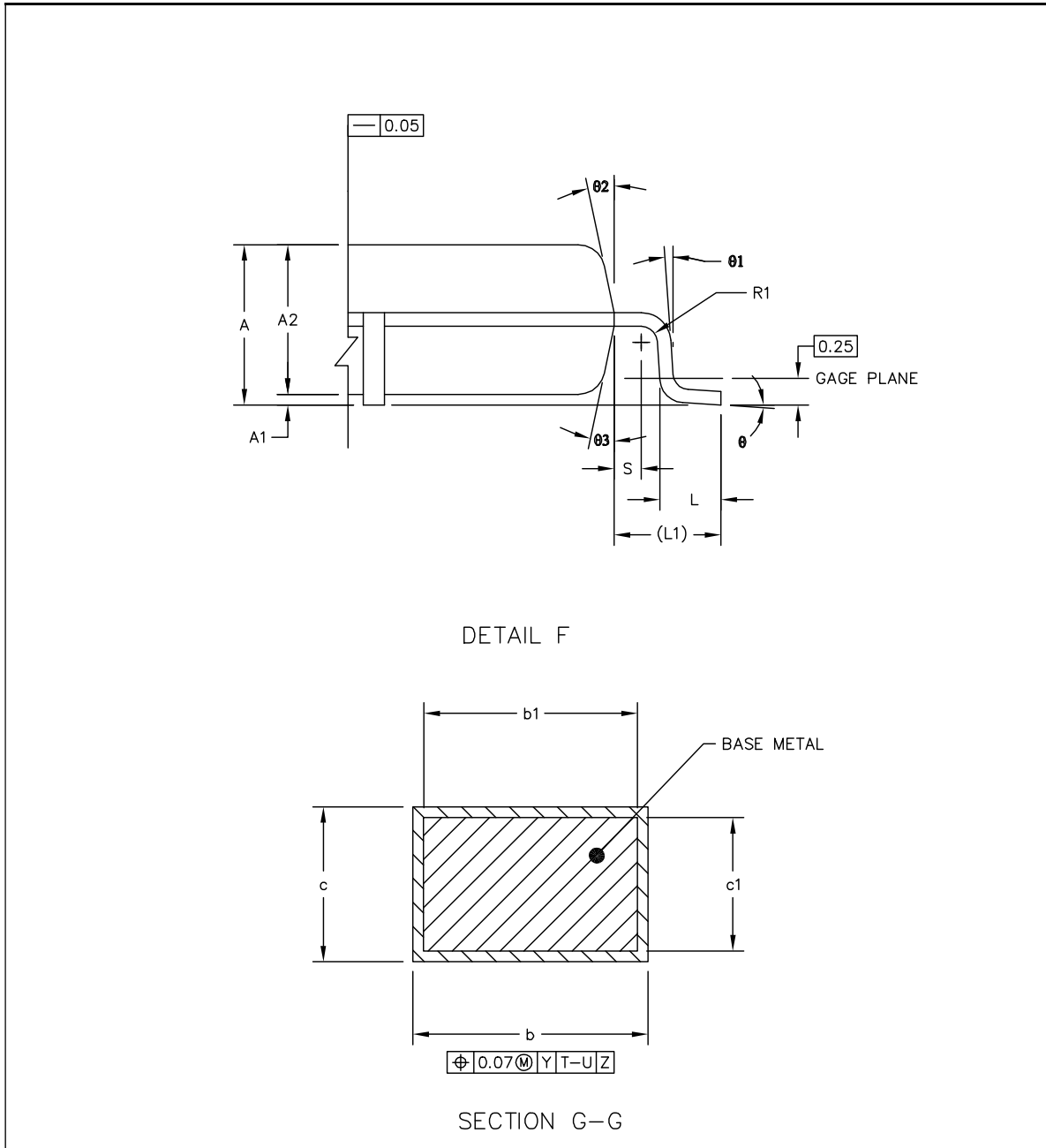


Figure 34. 176 LQFP package mechanical drawing (Part 2 of 3)

| NOTES: | | | | | | | | | | | |
|--|------|---------|------|------------|------|--------------------------|-----|-----|--------------------|-----|-----|
| <p>1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.</p> <p>2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.</p> | | | | | | | | | | | |
| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
| A | --- | | 1.6 | L1 | | 1 REF | | | | | |
| A1 | 0.05 | | 0.15 | R1 | 0.08 | | --- | | | | |
| A2 | 1.35 | 1.4 | 1.45 | R2 | 0.08 | | 0.2 | | | | |
| b | 0.17 | 0.22 | 0.27 | S | | 0.2 REF | | | | | |
| b1 | 0.17 | 0.2 | 0.23 | θ | 0° | 3.5° | 7° | | | | |
| c | 0.09 | | 0.2 | $\theta 1$ | 0° | | --- | | | | |
| c1 | 0.09 | | 0.16 | $\theta 2$ | 11° | 12° | 13° | | | | |
| D | | 26 BSC | | $\theta 3$ | 11° | 12° | 13° | | | | |
| D1 | | 24 BSC | | | | | | | | | |
| e | | 0.5 BSC | | | | | | | | | |
| E | | 26 BSC | | | | | | | | | |
| E1 | | 24 BSC | | | | | | | | | |
| L | 0.45 | 0.6 | 0.75 | | | | | | | | |
| | | | | | UNIT | DIMENSION AND TOLERANCES | | | REFERANCE DOCUMENT | | |
| | | | | | MM | ASME Y14.5M | | | 64-06-280-1392 | | |

Figure 35. 176 LQFP package mechanical drawing (Part 3 of 3)

4.1.2 144 LQFP

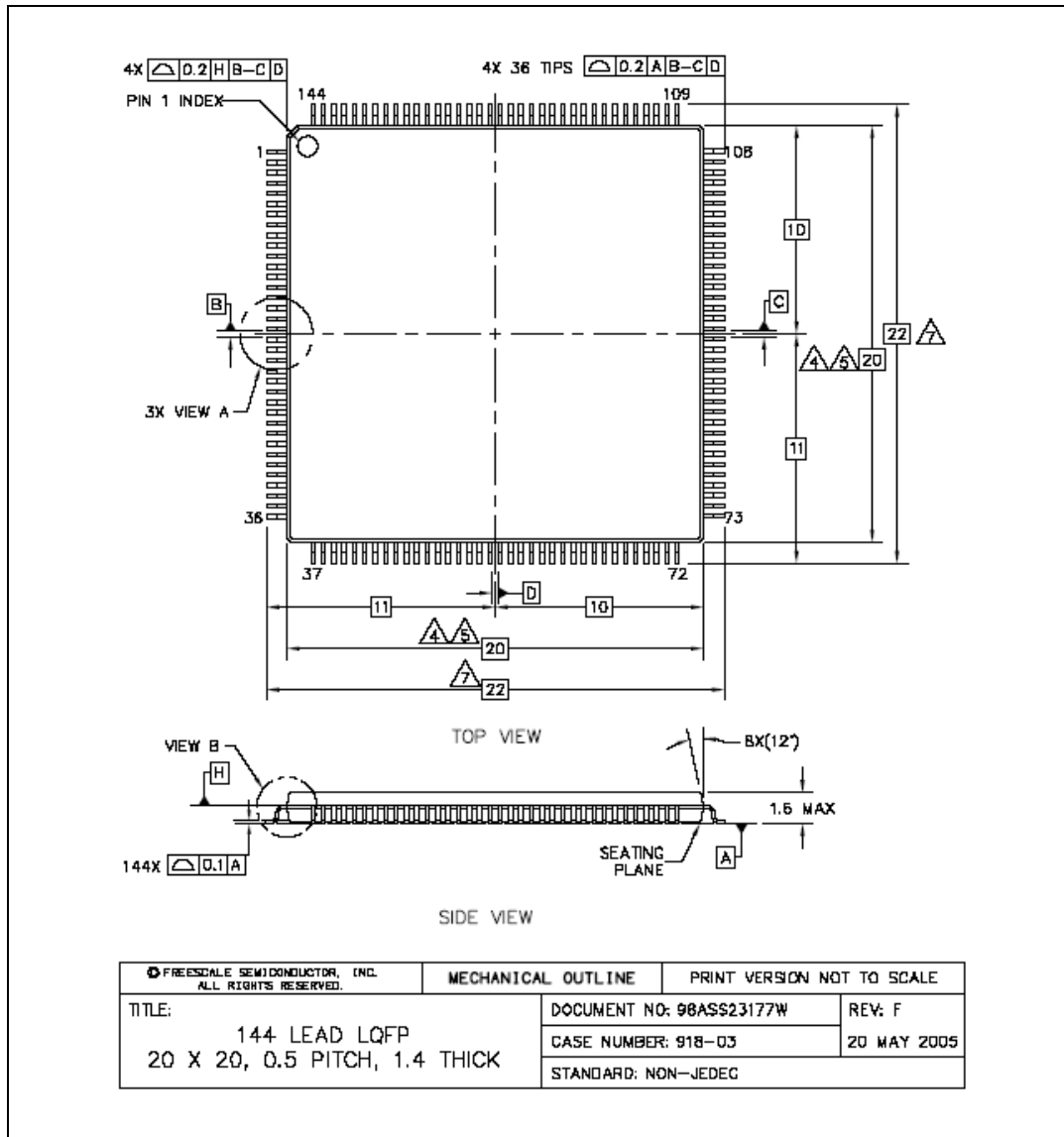


Figure 36. 144 LQFP package mechanical drawing (Part 1 of 2)

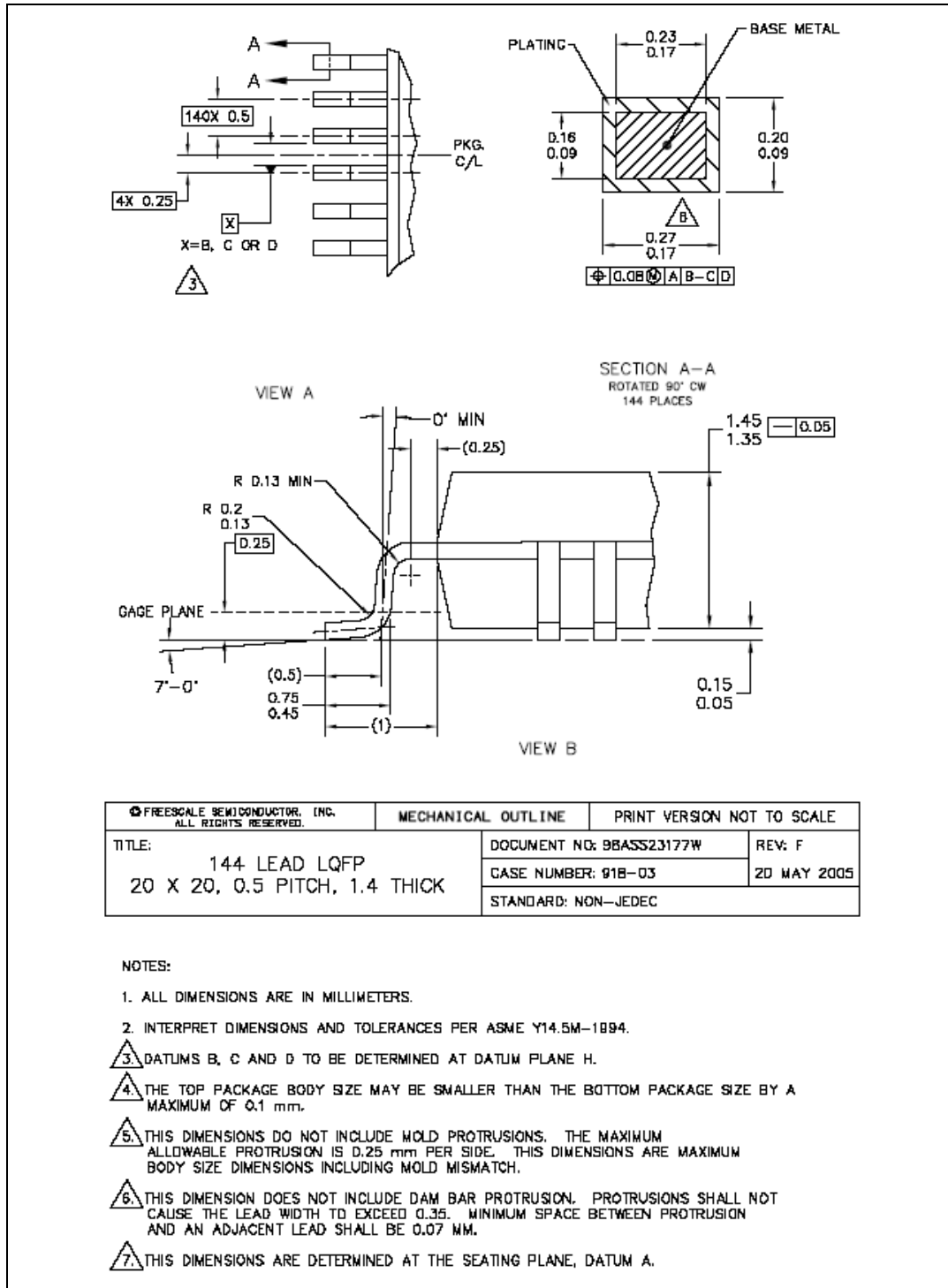


Figure 37. 144 LQFP package mechanical drawing (Part 2 of 2)

4.1.3 100 LQFP

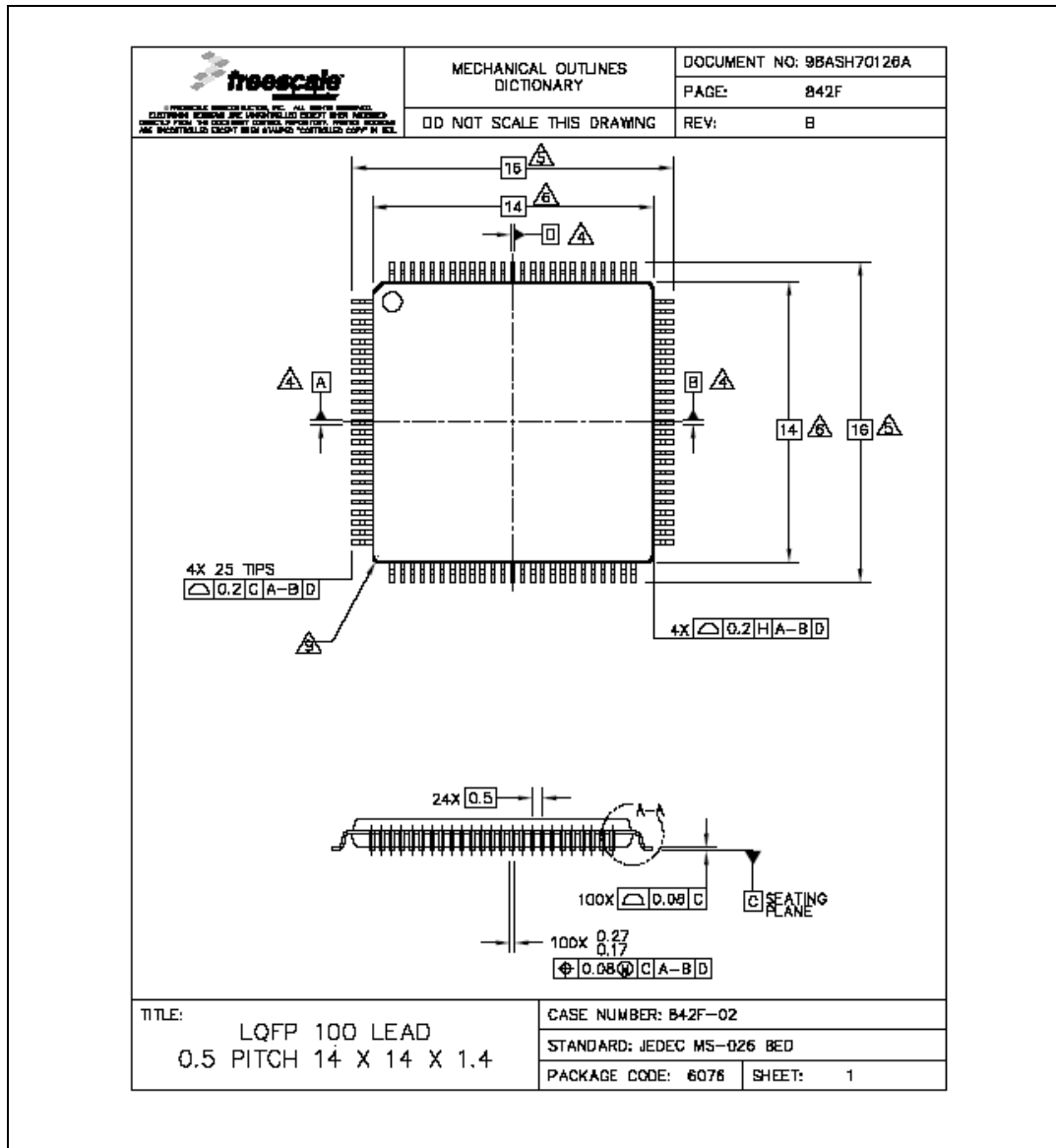


Figure 38. 100 LQFP package mechanical drawing (Part 1 of 3)

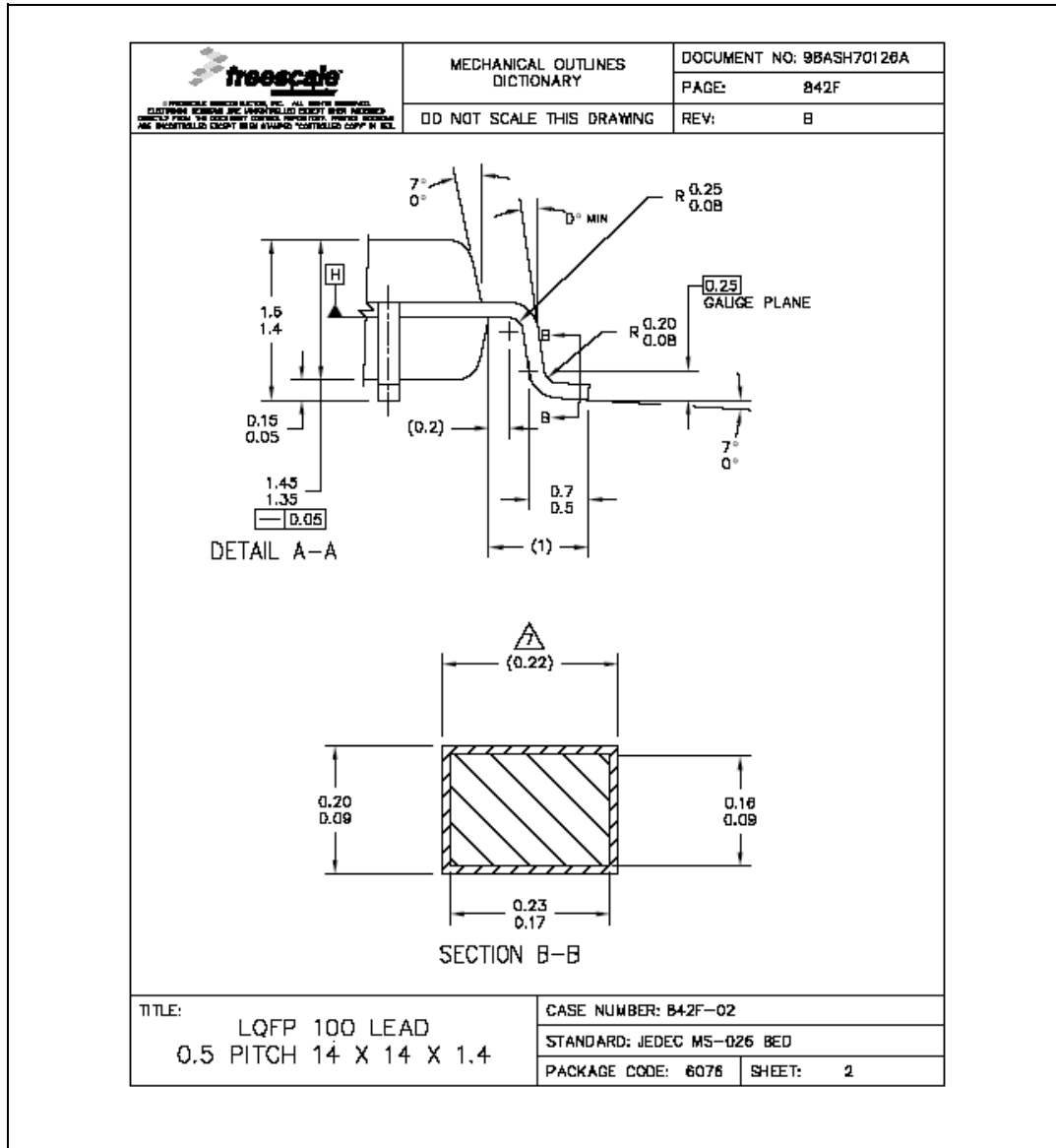


Figure 39. 100 LQFP package mechanical drawing (Part 2 of 3)


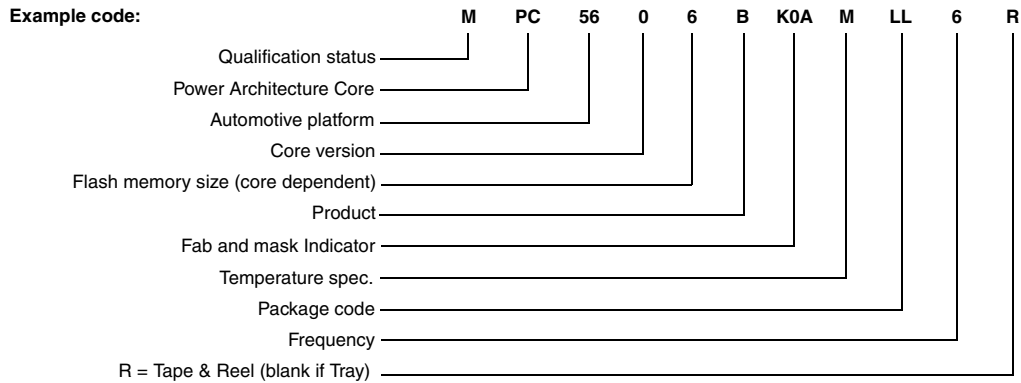
| | | |
|---|-----------------------------------|---|
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| | DO NOT SCALE THIS DRAWING | PAGE: 842F REV: B |
| <p>1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.</p> <p>2. CONTROLLING DIMENSION: MILLIMETER</p> <p>3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.</p> <p>4. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.</p> <p>5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM C.</p> <p>6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.</p> <p>7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07.</p> <p>8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.</p> <p>9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.</p> | | |
| TITLE: LQFP 100 LEAD 0.5 PITCH 14 X 14 X 1.4 | | CASE NUMBER: 842F-02 STANDARD: JEDEC MS-026 B02 PACKAGE CODE: 6076 SHEET: 3 |

Figure 40. 100 LQFP package mechanical drawing (Part 3 of 3)

5 Ordering information



Qualification status

M = General market qualified
 S = Automotive qualified
 P = Engineering samples

Automotive Platform

56 = Power Architecture in 90nm

Core version

0 = e200z0

Flash memory size (for z0 core)

5 = 768 KB
 6 = 1024 KB

Product

B = Body

Fab and mask Indicator

K = TSMC Fab
 0 = Version of the maskset
 A = Mask set indicator (Blank = 1st production maskset, A = 2nd, B = 3rd, etc)

Temperature spec.

C = -40 to 85 °C
 V = -40 to 105 °C
 M = -40 to 125 °C

Package code

LL = 100 LQFP
 LQ = 144 LQFP
 LU = 176 LQFP

Frequency

4 = Up to 48 MHz
 6 = Up to 64 MHz

Note: Not all options are available on all devices.

Figure 41. Commercial product code structure

6 Revision history

Table 46. Revision history

| Revision | Date | Description of changes |
|----------|-------------|---|
| 1 | 22 Apr 2011 | Initial release. |
| 2 | 15 May 2013 | <p>Changed device number to MPC5606BK.</p> <p>In Table 2 (Functional port pins), updated PA[11] AF2, PD[13] AF2, and PH[11] AF3 I/O direction to "I/O".</p> <p>In Table 3 (Pad types), corrected "Fast" in the "S" row to "Slow."</p> <p>In Table 5 (PAD3V5V field description), updated footnote 2.</p> <p>In Table 6 (OSCILLATOR_MARGIN field description), updated footnote 2.</p> <p>Inserted Section 3.2.3, NVUSRO[WATCHDOG_EN] field description.</p> <p>In Table 8 (Absolute maximum ratings), Table 9 (Recommended operating conditions (3.3 V)), and Table 10 (Recommended operating conditions (5.0 V)), corrected the parameter description for V_{DD_ADC} to "Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})"</p> <p>In Section 3.6.1, I/O pad types bullet item, removed Nexus reference.</p> <p>In Table 12 (I/O input DC electrical characteristics), added specifications for 85 °C.</p> <p>In Table 13 (I/O pull-up/pull-down DC electrical characteristics), Table 14 (SLOW configuration output buffer electrical characteristics), Table 15 (MEDIUM configuration output buffer electrical characteristics), and Table 16 (FAST configuration output buffer electrical characteristics), changed sentence in footnote 2 to "All pads but RESET are configured in input or in high impedance state."</p> <p>In Table 15 (MEDIUM configuration output buffer electrical characteristics), for V_{OL}, changed I_{OH} to I_{OL}.</p> <p>Updated Table 20 (I/O weight).</p> <p>In Table 21 (Reset electrical characteristics) changed sentence in footnote 4 to "All pads but RESET are configured in input or in high impedance state."</p> <p>In Table 22 (Voltage regulator electrical characteristics), corrected the maximum value for I_{DD_BV} in Table 22 (Voltage regulator electrical characteristics) to 300 mA.</p> <p>In Table 23 (Low voltage monitor electrical characteristics), changed V_{PORUP} classification tag from "P" (Production testing guaranteed) to "D" (Design simulation). Changed $V_{LVDHV3BH}$ classification tag from "P" (Production testing guaranteed) to "T" (Design characterization).</p> <p>In Table 23 (Low voltage monitor electrical characteristics), changed $V_{LVDHV3L}$, $V_{LVDHV3BL}$ minimums from 2.7 V to 2.6 V.</p> |

Table 46. Revision history (continued)

| Revision | Date | Description of changes |
|--------------|-------------|---|
| 2 (cont.) | 15 May 2013 | <p>In Table 24 (Electrical characteristics in different application modes),</p> <ul style="list-style-type: none"> — Changed I_{DDMAX} Typ to 81 mA and I_{DDMAX} Typ to 130 mA. — Changed I_{DDRUN} Typ for fCPU = 32 MHz to 40 mA. — Changed I_{DDRUN} Typ for fCPU = 48 MHz to 54 mA. Added I_{DDRUN} Max of 96 mA. — Changed I_{DDRUN} Typ for fCPU = 64 MHz to 67 mA. Added I_{DDRUN} Max of 120 mA. — Changed I_{DDHALT} at $T_A = 25\text{ °C}$ Typ to 10 mA and I_{DDHALT} Max to 15 mA. — Changed I_{DDHALT} at $T_A = 125\text{ °C}$ Typ to 15 mA and I_{DDHALT} Max to 28 mA. — Changed I_{DDSTOP} T_A temperature from -40 °C to 25 °C. — Changed I_{DDSTOP} at $T_A = 25\text{ °C}$ Typ to 130 μA and I_{DDSTOP} Max to 500 μA. — Changed I_{DDSTOP} at $T_A = 55\text{ °C}$ Typ to 180 μA. — Changed I_{DDSTOP} at $T_A = 85\text{ °C}$ Typ to 1 mA and I_{DDSTOP} Max to 5 mA. — Changed I_{DDSTOP} at $T_A = 105\text{ °C}$ Typ to 3 mA and I_{DDSTOP} Max to 9 mA. — Changed I_{DDSTOP} at $T_A = 125\text{ °C}$ Typ to 5 mA and I_{DDSTOP} Max to 14 mA. — Changed $I_{DDSTBY2}$ at $T_A = 25\text{ °C}$ Typ to 17 μA and Max to 80 μA. — Changed $I_{DDSTBY2}$ at $T_A = 55\text{ °C}$ Typ to 30 μA. — Changed $I_{DDSTBY2}$ at $T_A = 85\text{ °C}$ Typ to 100 μA. — Changed $I_{DDSTBY2}$ at $T_A = 105\text{ °C}$ Typ to 280 μA and Max to 950 μA. — Changed $I_{DDSTBY2}$ at $T_A = 125\text{ °C}$ Typ to 460 μA and Max to 1700 μA. — Changed the parameter classification for $I_{DDSTANDBY2}$ ($T_A = 125\text{ °C}$) — Changed $I_{DDSTBY1}$ at $T_A = 25\text{ °C}$ Typ to 12 μA and Max to 50 μA. — Changed $I_{DDSTBY1}$ at $T_A = 55\text{ °C}$ Typ to 24 μA. — Changed $I_{DDSTBY1}$ at $T_A = 85\text{ °C}$ Typ to 48 μA. — Changed $I_{DDSTBY1}$ at $T_A = 105\text{ °C}$ Typ to 150 μA and Max to 500 μA. — Changed $I_{DDSTBY1}$ at $T_A = 125\text{ °C}$ Typ to 260 μA. — Changed the third sentence of Footnote 3 to begin with “The given value is thought to be a worst case value (64 MHz at 125 °C) with all peripherals running.” — Removed footnotes 8 and 9 regarding I_{DDHALT} and I_{DDSTOP} — Corrected “C” characteristics to reflect testing status. <p>In Section 3.10, Flash memory electrical characteristics, removed the "FLASH_BIU settings vs. frequency of operation" table.</p> <p>In Table 28 (Flash power supply DC electrical characteristics), corrected Footnote 2 to specify 125 °C.</p> <p>In Section 3.14, FMPLL electrical characteristics, changed the text “the main oscillator driver” to “the FXOSC or FIRC sources.”</p> <p>In Table 40 (ADC input leakage current), added specifications for 85 °C.</p> <p>In Table 44 (DSPI characteristics), added t_{SCK} specifications for MTFE=1.</p> <p>In Table 44 (DSPI characteristics), updated specifications 7 and 8 to 13 ns, all DSPIs.</p> <p>in ADC section, corrected Equation 11.</p> <p>In Figure 41 (Commercial product code structure), added “Note: Not all options are available on all devices.”</p> <p>Removed Section 6, Abbreviations.</p> |
| 3 | 11 Sep 2013 | Updated the temperature in table note 2 in Table 1 (MPC5606BK family comparison) from 105 °C to 125 °C. |
| 4 | 25 Nov 2015 | Updated the Max value current for $I_{ADC0run}$ from 40 mA to 5 mA in Table 41 (ADC_0 conversion characteristics (10-bit ADC_0)) . |
| 5 | 7 Nov 2017 | <p>In Table 9 (Recommended operating conditions (3.3 V)) added Min value for TV_{DD}.</p> <p>In Table 10 (Recommended operating conditions (5.0 V)) added Min value for TV_{DD}.</p> <p>In Table 44 (DSPI characteristics) changed the for DSPI 2 and 4, in MTFE=1 mode from 125 to 145.</p> |

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