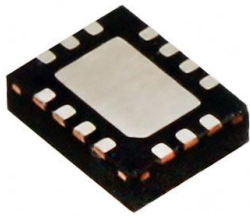


AB-557-03-HCLV-F-L-C-T3 Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|---|
| DiGi Electronics Part Number | AB-557-03-HCLV-F-L-C-T3-DG |
| Manufacturer | Abracon LLC |
| Manufacturer Product Number | AB-557-03-HCLV-F-L-C-T3 |
| Description | IC PCIE CLOCK GEN 100MHZ 14QFN |
| Detailed Description | PCI Express (PCIe), Clock Generator Clock/Frequency Generator IC 460MHz 1 Output 14-QFN (3.2x2.5) |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

AB-557-03-HCLV-F-L-C-T3

Series:

Pure Silicon™

DiGi-Electronics Programmable:

Not Verified

Main Purpose:

PCI Express (PCIe), Clock Generator

Output:

HCSL, LVDS

Ratio - Input:Output:

0:2

Frequency - Max:

460MHz

Operating Temperature:

-40°C ~ 85°C

Package / Case:

14-VFQFN Exposed Pad

Manufacturer:

Abracon LLC

Product Status:

Active

PLL:

Yes

Input:

-

Number of Circuits:

1

Differential - Input:Output:

No/Yes

Voltage - Supply:

2.25V ~ 3.6V

Mounting Type:

Surface Mount

Supplier Device Package:

14-QFN (3.2x2.5)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

AB-557-03 Series

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3.2 x 2.5 x .85 mm (14 pin QFN)

RoHS/RoHS II Compliant

MSL Level = 1

Features

- Meets PCIe Gen1, Gen2, & Gen3 specs.
- High Performance MEMS Technology by Discera
- Available Mixed Output Formats: HCSL, LVPECL, LVDS or LVC MOS
- Wide Temperature Range: -40° to 105° C
- Wide Supply Range: 2.25V to 3.6 V
- Low Power Consumption
- Excellent Shock & Vibration Immunity

Applications

- Solid State Storage
- Storage Area Networks
- Passive Optical Networks
- Ethernet: 1G, 10GBASE-T/KR/LR/SR, and FCoE
- TV and other Consumer Electronics
- Industrial and Medical
- Scanner, Printer

Key Electrical Specifications

| Parameters | | Minimum | Typical | Maximum | Units | Notes |
|---|---------------------|---|---------|---------|-------------------|--|
| Frequency | f ₀ | 2.3 | 100 | 460*1 | MHz | |
| Operating Temperature | | -20 | | +70 | °C | See options |
| Storage Temperature | | -55 | | +150 | °C | |
| Overall Freq. Stability*2 | Δf | -100 | | +100 | ppm | See options |
| Supply Voltage | V _{DD} | +2.25 | | +3.6 | V | |
| Supply Current- Enabled | I _{DD} | | 60 | | mA | R _L =50Ω, |
| Supply Current- Disabled | I _{DD} | | 21 | 23 | mA | |
| Startup Time | t _{su} | | | 5 | ms | |
| Enable Time | t _{EN} | | | 20 | ns | |
| Disable Time | t _{DA} | | | 5 | ns | |
| Tri-state Function (Standby/Disable) | | "1" (V _{IH} ≥0.75*V _{dd}) or Open: | | | V | 40kΩ pull-up |
| Aging | | -5.0 | | +5.0 | ppm | First year |
| Output Offset Voltage | V _{OH} | 0.725 | | | V | R _L =50 Ω |
| | V _{OL} | | | 0.10 | | |
| Peak to Peak Output Swing | | | 750 | | mV | Single-Ended |
| Rise Time | t _r | 200 | | 400 | ps | R _L =50 Ω, C _L =2pF |
| Fall Time | t _f | 200 | | 400 | ps | 20% to 80% |
| Duty Cycle | SYM | 48 | | 52 | % | Differential |
| Period Jitter | J _{PER} | | 2.5 | | ps _{RMS} | F ₀₁ =F ₀₂ =100.00MHz |
| Integrated Phase Noise (Common Clock Architecture) | R _J | | 0.540 | | ps _{RMS} | PCIe Gen 1.1 T _J = D _J + 14.069 x R _J (BER 10-12) |
| | D _J | | 0.832 | 41.9 | ps _{P-P} | |
| | T _J | | 8.536 | 86.0 | | |
| | J _{RMS-} | | 0.458 | 3.1 | ps _{RMS} | PCIe Gen 2.1 |
| | J _{RMS-} | | 0.030 | 3.0 | | PCIe Gen 2.1 |
| | J _{RMS-CC} | | 0.165 | 1.0 | | PCIe Gen 3.0 |
| Integrated Phase Noise (Data Clock Architecture) | J _{RMS-} | | 0.561 | 4.0 | ps _{RMS} | PCIe Gen 2.1 |
| | J _{RMS-} | | 1.778 | 7.5 | | PCIe Gen 2.1 |
| | J _{RMS-CC} | | 0.147 | 1.0 | | PCIe Gen 3.0 |

*1. For frequency other than 100MHz, please contact ABRACON or consider using ASEMDxx series

2. Frequency stability includes frequency variations due to initial tolerance, temp. and power supply voltage



CRYSTAL-LESS PCI EXPRESS DUAL OUTPUT ULTRA MINIATURE PURE SILICON™ SMD CLOCK GENERATOR

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3.2 x 2.5 x .85 mm (14 pin QFN)

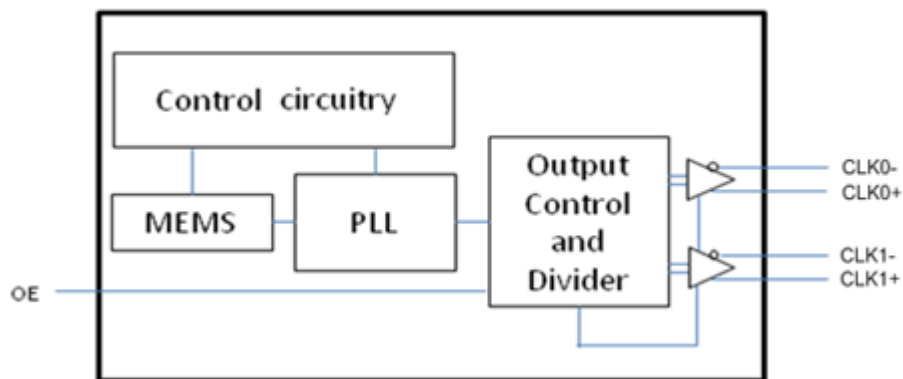
RoHS/RoHS II Compliant

MSL Level = 1

Absolute Maximum Ratings

| Item | Minimum | Maximum | Unit | Condition |
|-----------------|---------|----------------------|------|-----------|
| Supply Voltage | -0.3 | +4.0 | V | |
| Input Voltage | -0.3 | V _{dd} +0.3 | V | |
| Junction Temp. | | +150 | °C | |
| Storage Temp. | -55 | +150 | °C | |
| Soldering Temp. | | +260 | °C | 40sec max |
| ESD | | | | |
| HBM | | 4,000 | V | |
| MM | | 400 | | |
| CDM | | 1,500 | | |

Block Diagram



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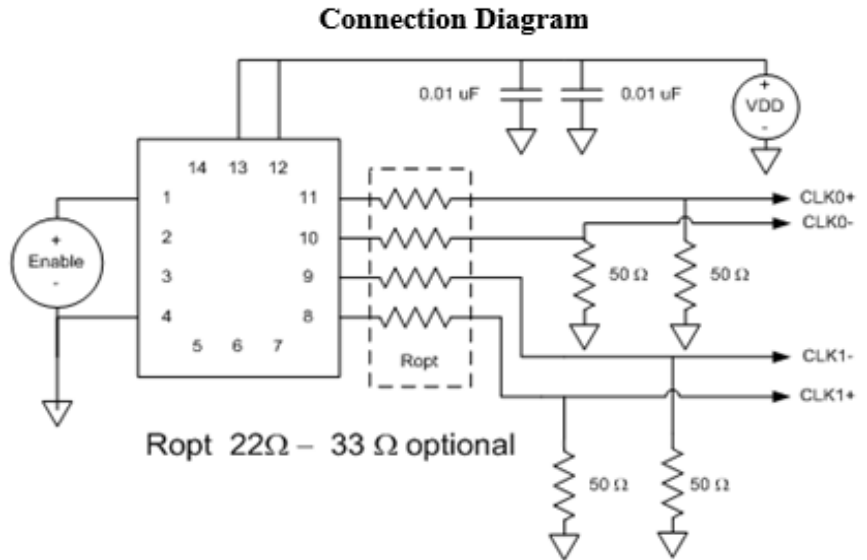
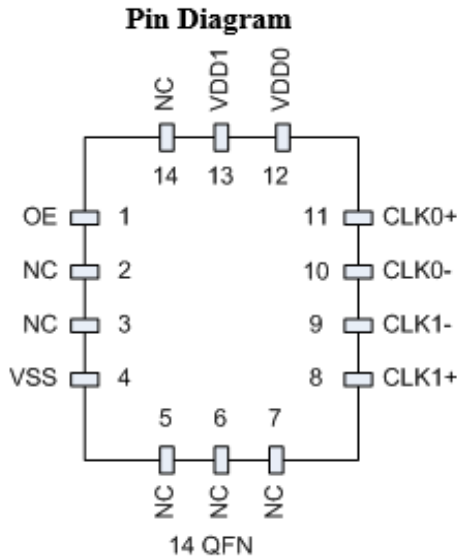
3.2 x 2.5 x .85 mm (14 pin QFN)

RoHS/RoHS II Compliant

MSL Level = 1

Pin Layout:

14 Pin QFN:



| Pin No. | Pin Name | Pin Type | Description |
|---------|----------|----------|--|
| 1 | OE | I | Output Enable; active high |
| 2 | NC | NA | Ground Connected or Leave Unconnected |
| 3 | NC | NA | Ground Connected or Leave Unconnected |
| 4 | VSS | Power | Ground |
| 5 | NC | NA | Ground Connected or Leave Unconnected |
| 6 | NC | NA | Ground Connected or Leave Unconnected |
| 7 | NC | NA | Ground Connected or Leave Unconnected |
| 8 | CLK1+ | O | True output of differential pair |
| 9 | CLK1- | O | Complement output of differential pair |
| 10 | CLK0- | O | Complement output of differential pair |
| 11 | CLK0+ | O | True output of differential pair |
| 12 | VDD0 | Power | Power Supply for Output 0 (CLK+/- 0) |
| 13 | VDD1 | Power | Power Supply for Core and Output 1 (CLK +/- 1) |
| 14 | NC | NA | Ground Connected or Leave Unconnected |



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3.2 x 2.5 x .85 mm (14 pin QFN)

RoHS/RoHS II Compliant

MSL Level = 1

Options and Part Identification (left blank if standard):

AB-557-03-□□-□-□-□-□

| Output Format, Clk1 |
|---------------------|
| C: LVCMOS |
| LP: LVPECL |
| LV:LVDS |
| HC:HCSL |

| Packaging |
|------------------------------|
| Blank: Bulk |
| T: Tape & Reel(1kpcs / reel) |
| T3: Tape & Reel(3kpcs/reel) |

| Overall Freq. Stability |
|-------------------------|
| Blank: ±100ppm |
| C: ±50ppm |

| Output Format, Clk0 |
|---------------------|
| C: LVCMOS |
| LP: LVPECL |
| LV:LVDS |
| HC:HCSL |

| Package Type |
|--------------|
| F: 14-QFN |

| Operating Temp. |
|-------------------|
| E: -20°C ~ +70°C |
| L: -40°C ~ +85°C |
| X: -40°C ~ +105°C |

Note: For frequency other than 100MHz, please contact ABRACON or consider using ASEMDxx series



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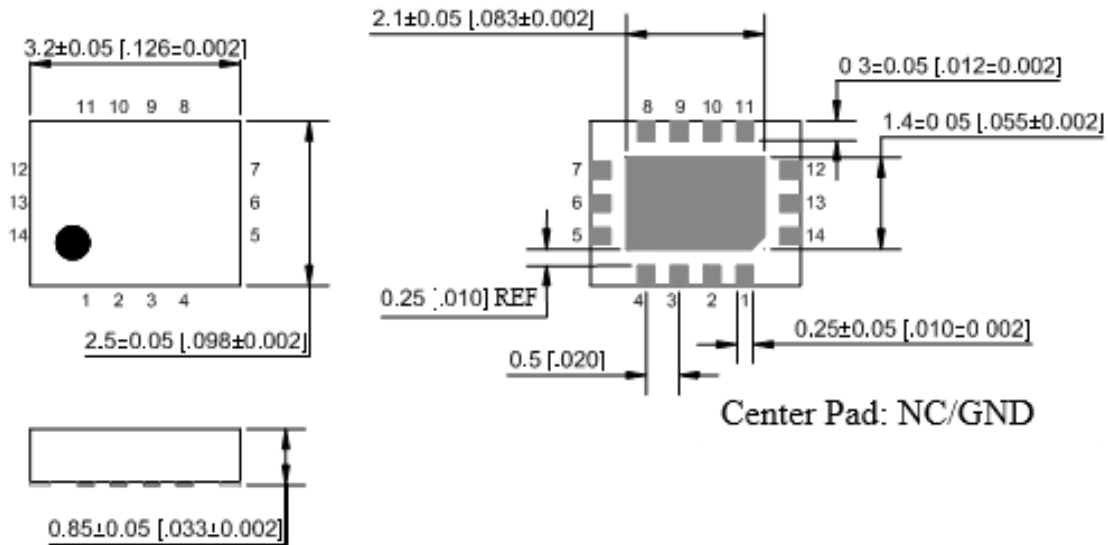
3.2 x 2.5 x .85 mm (14 pin QFN)

RoHS/RoHS II Compliant

MSL Level = 1

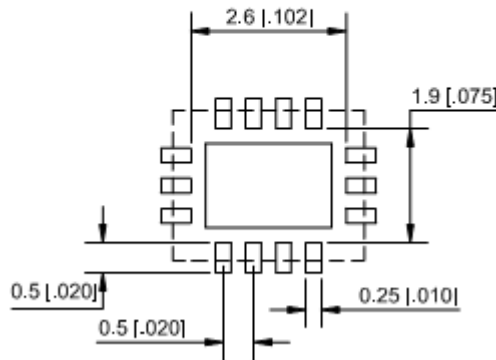
Mechanical Dimensions:

14 pin QFN:



Center Pad: NC/GND

Recommended Solder Pad Layout



Dimensions: mm [inches]



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RoHS/RoHS II Compliant

MSL Level = 1

Reflow Profile [JEDEC J-STD-020]

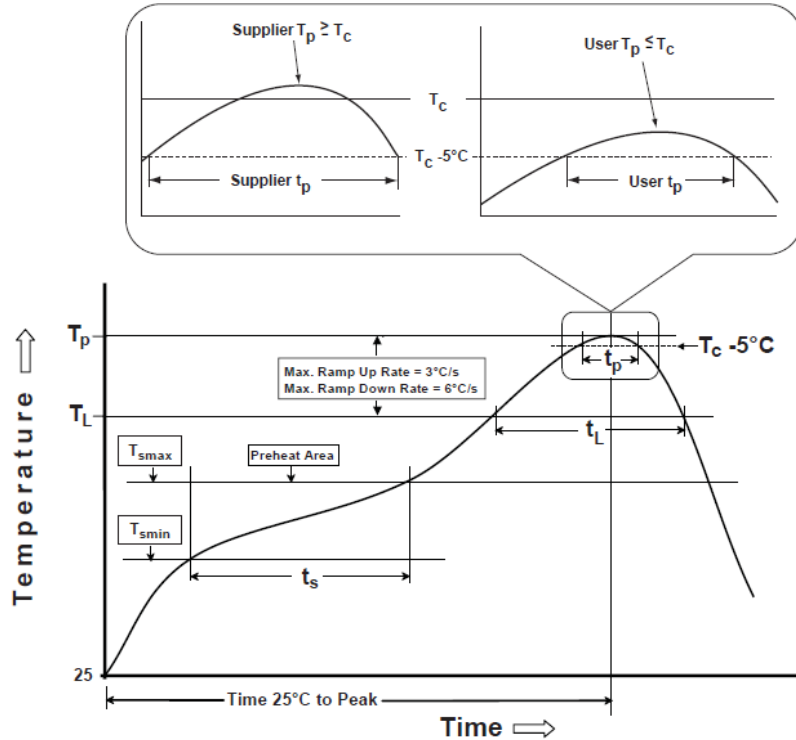


Table 1

SnPb Eutectic Process Classification Temperatures (Tc)

| Package Thickness | Volume mm ³ <350 | Volume mm ³ ≥350 |
|-------------------|-----------------------------|-----------------------------|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2

Pb-Free Process Classification Temperatures (Tc)

| Package Thickness | Volume mm ³ <350 | Volume mm ³ 350-2000 | Volume mm ³ >2000 |
|-------------------|-----------------------------|---------------------------------|------------------------------|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm - 2.5 mm | 260 °C | 250 °C | 245 °C |
| >2.5 mm | 250 °C | 245 °C | 245 °C |

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|-------------------------|------------------|
| Preheat / soak | | |
| Temperature minimum (T _{smin}) | 100°C | 150°C |
| Temperature maximum (T _{smax}) | 150°C | 200°C |
| Time (T _{smin} to T _{smax}) (t _s) | 60 - 120 sec. | 60 - 120 sec. |
| Average ramp-up rate (T _{smax} to T _p) | 3°C/sec. max | 3°C/sec. max |
| Liquidous temperature (T _L) | 183°C | 217°C |
| Time at liquidous (t _L) | 60 - 150 sec. | 60 - 150 sec. |
| Peak package body temperature (T _p)* | see Table 1 | see Table 2 |
| Time (t _p)** within 5°C of the specified classification temperature (T _c) | 20 sec. | 30 sec. |
| Ramp-down rate (T _p to T _{smax}) | 6°C/sec. max | 6°C/sec. max |
| Time 25°C to peak temperature | 6 min. max | 8 min. max |
| Reflow cycles | 2 max | 2 max |

*Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.



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RoHS/RoHS II Compliant

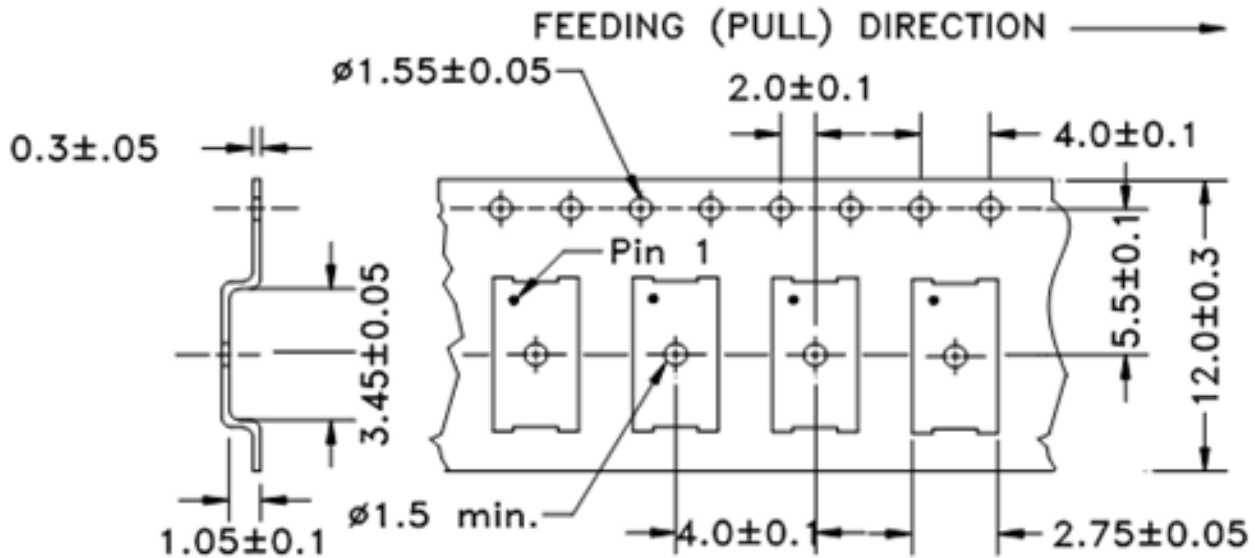
MSL Level = 1

Packaging

14 Pin QFN Tape Drawing:

T= 1,000pcs/reel
T3= 3,000pcs/reel

Reel Size = 7" diameter



Dimensions: mm



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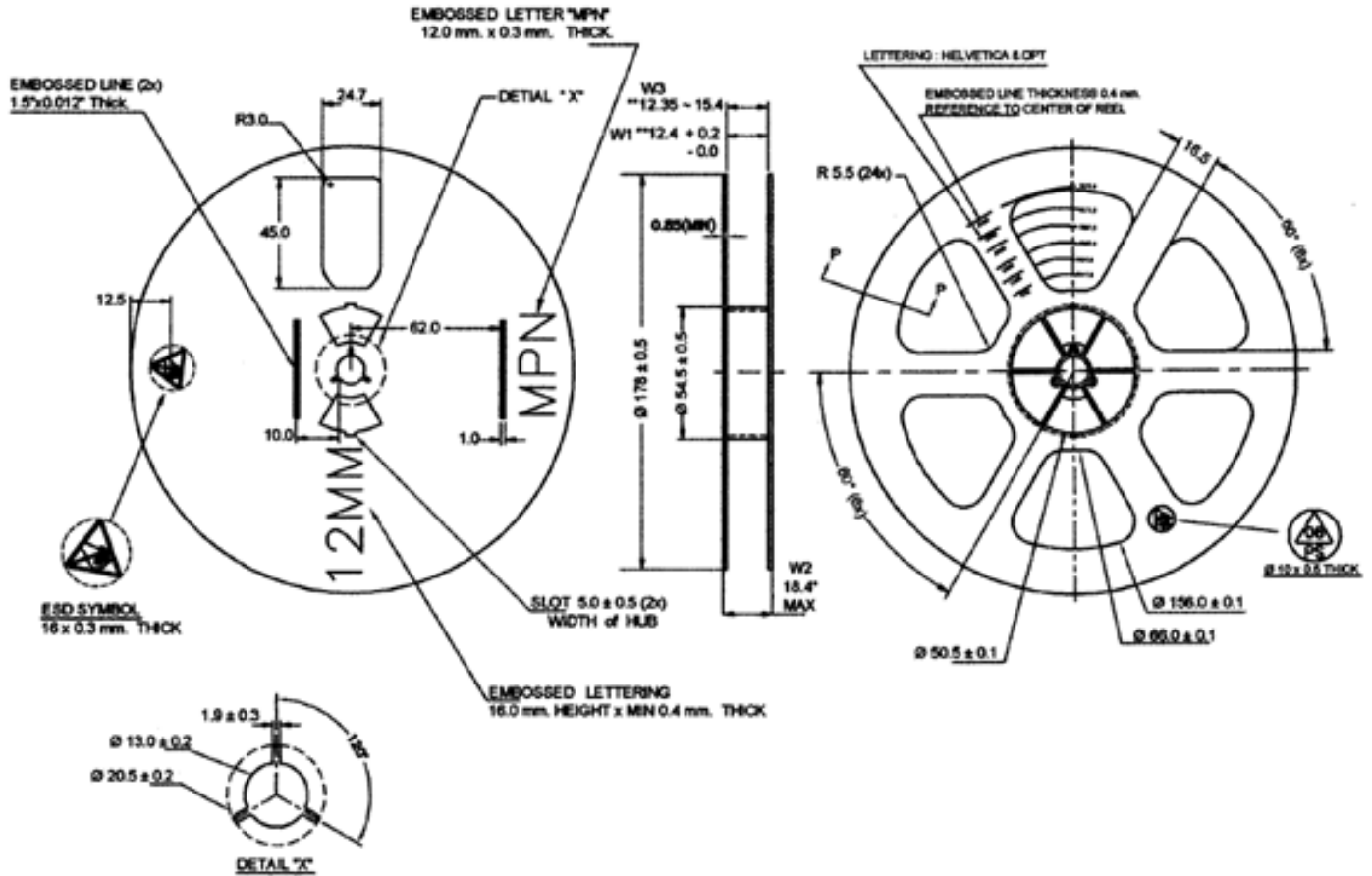


ESD Sensitive



3.2 x 2.5 x .85 mm (14 pin QFN)
RoHS/RoHS II Compliant
 MSL Level = 1

7" Reel Drawing (1000pcs/reel):



Dimensions: mm



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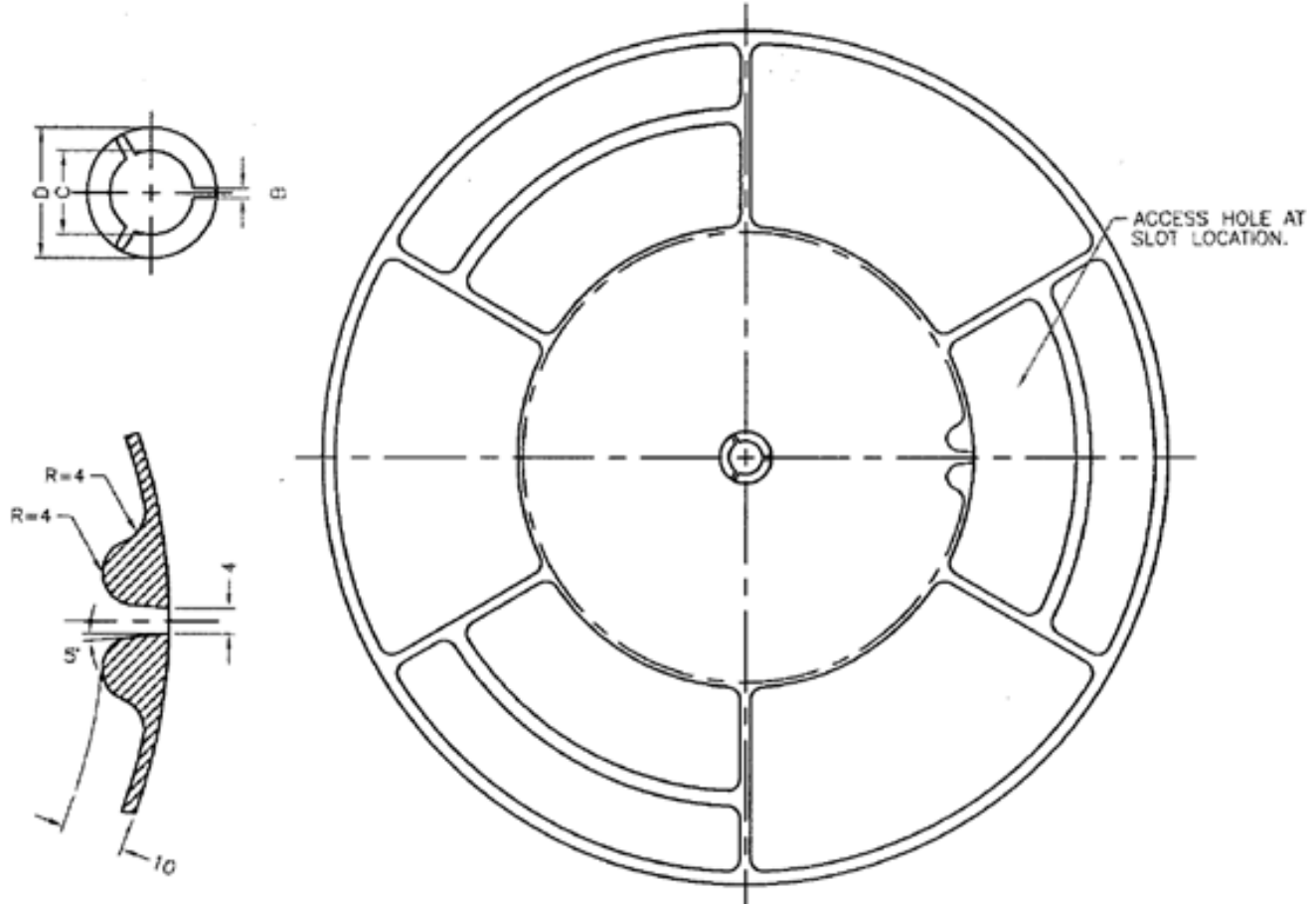


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3.2 x 2.5 x .85 mm (14 pin QFN)
RoHS/RoHS II Compliant
 MSL Level = 1

13" Reel Drawing (3000pcs/reel):



| A | N | W1 | W2 | W3 | D | B | C | Tape Width |
|-----------|---------------|-----------|-----------|--------------------------|-----------|---------|---------------|------------|
| 330 (13") | 178 (7") max. | 12.4+2/-0 | 18.4 max. | 12.35 min. 15.40 max. | 20.2 min. | 1.5 min | 13.0+0.5/-0.2 | 12 |

Dimensions: mm

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