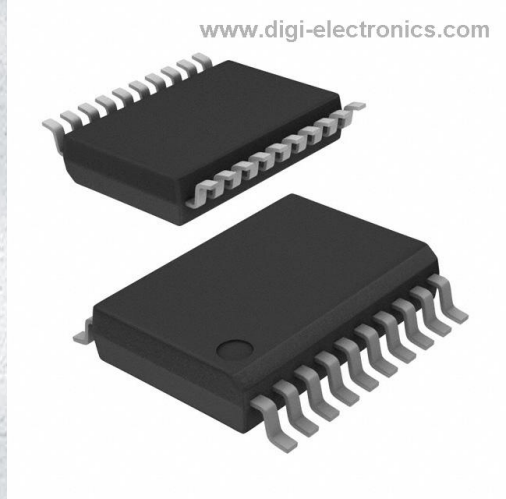
650R-21LF Datasheet



DiGi Electronics Part Number	650R-21LF-DG
Manufacturer	Renesas Electronics Corporation
Manufacturer Product Number	650R-21LF
Description	IC CLK/FREQ SYNTH 20QSOP
Detailed Description	Clock/Frequency Synthesizer IC 66.67MHz 1 20-SSOP (0.154", 3.90mm Width)

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RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
650R-21LF	Renesas Electronics Corporation
Series:	Product Status:
-	Obsolete
DiGi-Electronics Programmable:	Type:
Not Verified	Clock/Frequency Synthesizer
PLL:	Input:
Yes	Clock, Crystal
Output:	Number of Circuits:
CMOS	1
Ratio - Input:Output:	Differential - Input:Output:
1:8	No/No
Frequency - Max:	Divider/Multiplier:
66.67MHz	No/No
Voltage - Supply:	Operating Temperature:
3V ~ 5.5V	0°C ~ 70°C
Mounting Type:	Package / Case:
Surface Mount	20-SSOP (0.154", 3.90mm Width)
Supplier Device Package:	Base Product Number:
20-QSOP	650R

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

SYSTEM PERIPHERAL CLOCK SOURCE ICS650-21

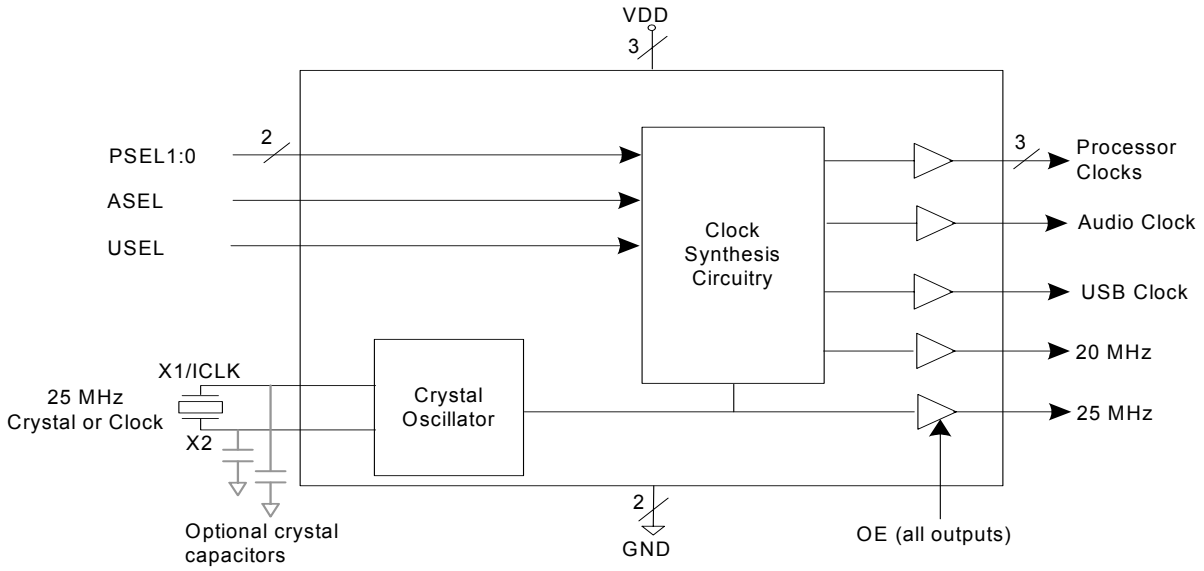
Description

The ICS650-21 is a low cost, low-jitter, high-performance clock synthesizer for system peripheral applications. Using analog/digital Phase Locked Loop (PLL) techniques, the device accepts a parallel resonant 25 MHz crystal input to produce up to eight output clocks. The device provides clocks for PCI, SCSI, Fast Ethernet, Ethernet, USB, and AC97. The user can select one of three USB frequencies and also one of two AC97 audio frequencies. The OE pin puts all outputs into a high-impedance state for board level testing. All frequencies are generated with less than one ppm error, meeting the demands of SCSI and Ethernet clocking.

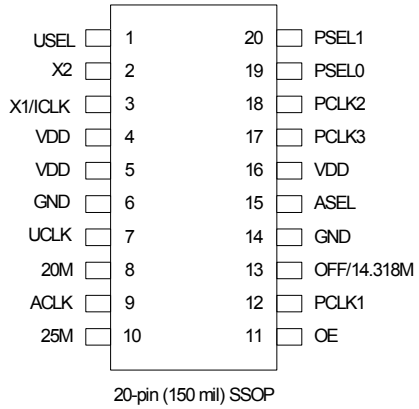
Features

- Packaged in 20-pin SSOP (QSOP)
- Pb (lead) free package, RoHS compliant
- Lower jitter version of ICS650-01
- Operating voltage of 3.3 V or 5 V
- Zero ppm synthesis error in all clocks
- Inexpensive 25 MHz crystal or clock input
- Provides Ethernet and Fast Ethernet clocks
- Provides SCSI clocks
- Provides PCI clocks
- Selectable AC97 audio clock
- Selectable USB clock
- OE pin tri-states the outputs for testing
- Selectable frequencies on three clocks
- Duty cycle of 45/55 for Processor clock and Audio clock
- Advanced, low-power CMOS process
- Industrial temperature range available

Block Diagram



Pin Assignment



20-pin (150 mil) SSOP

Processor Clock (MHz)

PSEL1	PSEL0	PCLK1	PCLK2, 3
0	0	25	50
0	M	TEST MODE	
0	1	TEST MODE	
M	0	40	80
M	M	33.3333	66.6667
M	1	20	40
1	0	20	33.3333
1	M	20	66.6667
1	1	50	100

USB Clock (MHz)

USEL	UCLK
0	12
M	24
1	48

Audio Clock (MHz)

ASEL	ACLK
0	49.152
M	24.576
1	14.318

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	USEL	Input	UCLK select pin. Determines frequency of USB clock per table above.
2	X2	XO	Crystal connection. Connect to parallel mode 25 MHz crystal. Leave open for clock.
3	X1/ICLK	XI	Crystal connection. Connect to parallel mode 25 MHz crystal or clock.
4	VDD	Power	Connect to VDD. Must be same value as other VDD. Decouple with pin 6.
5	VDD	Power	Connect to VDD. Must be same value as other VDD.
6	GND	Power	Connect to ground.
7	UCLK	Output	USB clock output per table above.
8	20M	Output	Fixed 20 MHz output for Ethernet.
9	ACLK	Output	AC97 audio clock output per table above.
10	25M	Output	Fixed 25 MHz reference output for Fast Ethernet.
11	OE	Input	Output enable. Tri-states all outputs when low.
12	PCLK1	Output	PCLK output number 1 per table above.

Pin Number	Pin Name	Pin Type	Pin Description
13	OFF/14.318M	Output	14.31818 MHz clock output only when ASEL = VDD.
14	GND	Power	Connect to ground.
15	ASEL	Input	ACLK select pin. Determines frequency of audio clock per table above.
16	VDD	Power	Connect to VDD. Must be same value as other VDD. Decouple with pin 14.
17	PCLK3	Output	PCLK output number 3 per table above.
18	PCLK2	Output	PCLK output number 2 per table above.
19	PSEL0	Input	Processor select pin #0. Determines frequencies on PCLKs 1-3 per table above.
20	PSEL1	Input	Processor select pin #1. Determines frequencies on PCLKs 1-3 per table above.

External Components

The ICS650-21 requires a minimum number of external components for proper operation.

Decoupling Capacitor

Decoupling capacitors of 0.01µF must be connected between each VDD and GND (pins 4 and 6, pins 16 and 14), as close to the device as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. So, for a crystal with a 16pF load capacitance, two 20 pF [(16-6) x 2] capacitors should be used.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-21. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.0	+3.3	+5.5	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Supply Current	IDD	No load, Note 1		30		mA
Input High Voltage	V_{IH}	Select inputs, OE	2			V
Input Low Voltage	V_{IL}	Select inputs, OE			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Short Circuit Current	I_{OS}	CLK output		±50		mA
Input Capacitance, inputs		Except X1		5		pF

Note 1: With all clocks at highest frequencies.

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Clocks Accuracy (synthesis error)		All clocks			1	ppm
Output Rise Time	t_{OR}	0.8 to 2.0 V, Note 2		1.5		ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, Note 2		1.5		ns
Output Clock Duty Cycle		UCLK, at VDD/2	40	50	60	%
		PCLCK, ACLCK, at VDD/2	45	50	55	%
One Sigma Jitter		Except ACLK		75		ps
		ACLK		120		ps
Absolute Clock Period Jitter		UCLK, 20M	-500		500	ps
Power-up Time		PLL lock time from power-up to 1% of final value		1	4	ms

Note 1: Values dependent on programming.

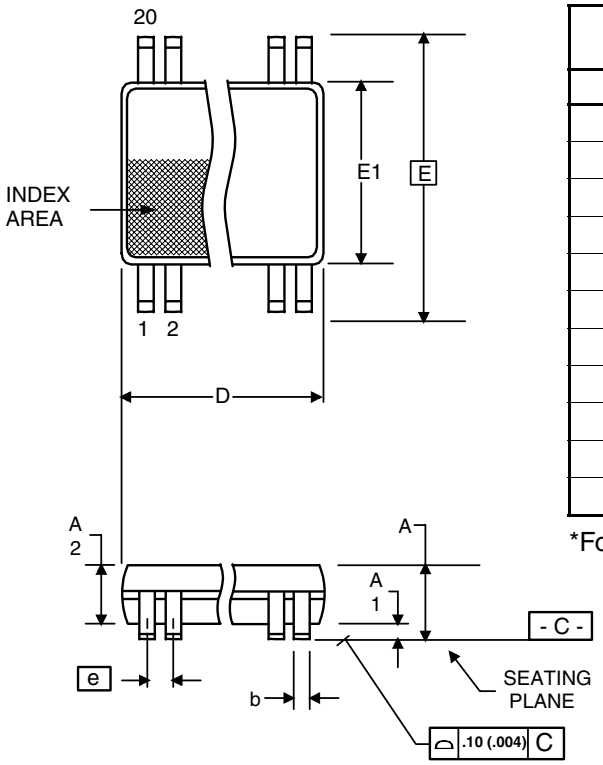
Note 2: Measured with 15 pF load.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		135		°C/W
	θ_{JA}	1 m/s air flow		93		°C/W
	θ_{JA}	3 m/s air flow		78		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

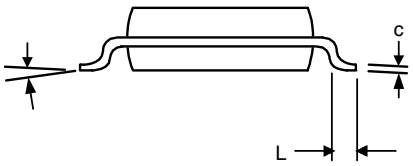
Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	0.008	0.012
C	0.18	0.25	.007	.010
D	8.55	8.75	.337	.344
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650R-21LF	ICS650R-21L	Tubes	20-pin SSOP	0 to +70° C
650R-21LFT	ICS650R-21L	Tape and Reel	20-pin SSOP	0 to +70° C
650R-21ILF	650R-21ILF	Tubes	20-pin SSOP	-40 to 85° C
650R-21ILFT	650R-21ILF	Tape and Reel	20-pin SSOP	-40 to 85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
G	P. Griffith	02/15/06	Added “Power-up Time” spec in AC chars.
H		11/04/09	Added EOL note for non-green parts.
J		05/13/10	Removed EOL note and non-green parts.

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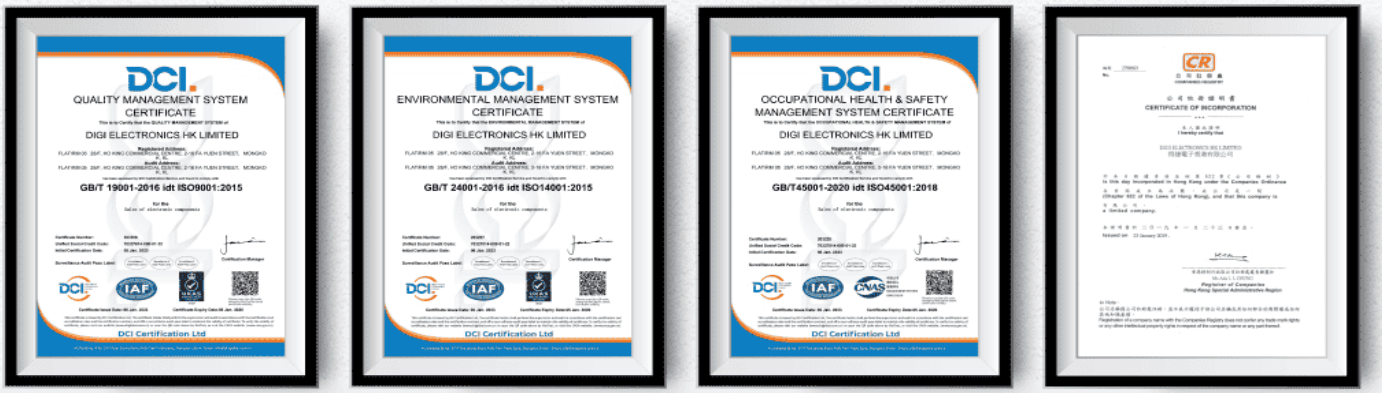

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