

8P34S1106NLGI8 Datasheet



| | |
|------------------------------|--|
| DiGi Electronics Part Number | 8P34S1106NLGI8-DG |
| Manufacturer | Renesas Electronics Corporation |
| Manufacturer Product Number | 8P34S1106NLGI8 |
| Description | IC CLK BUF 1:6 1.2GHZ 20VFQFPN |
| Detailed Description | Clock Fanout Buffer (Distribution) IC 1:6 1.2 GHz 20-VFQFN Exposed Pad |

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Purchase and inquiry

Manufacturer Product Number:

8P34S1106NLG18

Series:

-

Type:

Fanout Buffer (Distribution)

Ratio - Input:Output:

1:6

Input:

CML, LVDS

Frequency - Max:

1.2 GHz

Operating Temperature:

-40°C ~ 85°C

Package / Case:

20-VFQFN Exposed Pad

Base Product Number:

8P34S1106

Manufacturer:

Renesas Electronics Corporation

Product Status:

Active

Number of Circuits:

1

Differential - Input:Output:

Yes/Yes

Output:

LVDS

Voltage - Supply:

1.71V ~ 1.89V

Mounting Type:

Surface Mount

Supplier Device Package:

20-VFQFPN (4x4)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

Description

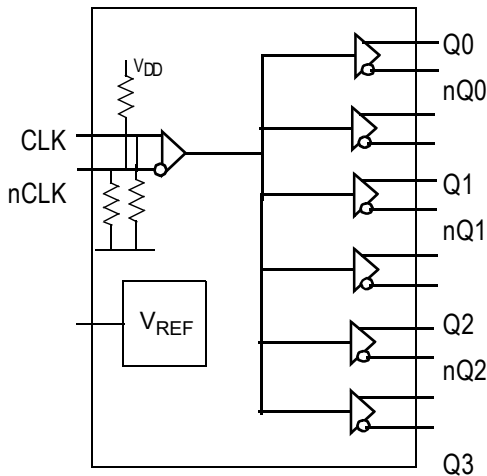
The 8P34S1106I is a high-performance differential LVDS fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The 8P34S1106I is characterized to operate from a 1.8V power supply.

Guaranteed output-to-output and part-to-part skew characteristics make the 8P34S1106I ideal for those clock distribution applications demanding well-defined performance and repeatability. One differential input and six low skew outputs are available. The integrated bias voltage reference enables easy interfacing of single-ended signals to the differential device input. The device is optimized for low power consumption and low additive phase jitter.

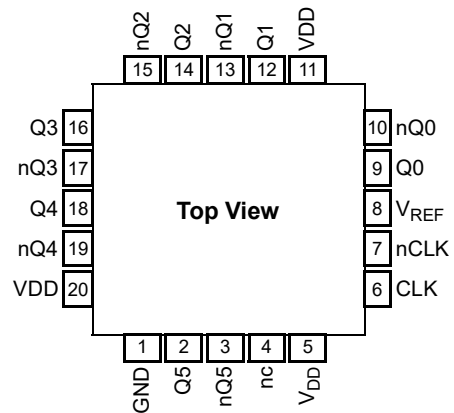
Features

- Six low skew, low additive jitter LVDS output pairs
- One differential clock input pair
- Differential CLK, nCLK pair can accept the following differential input levels: LVDS, CML
- Maximum input clock frequency: 1.2GHz (maximum)
- Output skew: 20ps (typical)
- Propagation delay: 290ps (typical)
- Low additive phase jitter, RMS; $f_{REF} = 156.25\text{MHz}$, $V_{PP} = 1\text{V}$, 12kHz–20MHz: 39fs (typical)
- Full 1.8V supply voltage
- Lead-free (RoHS 6), 20-Lead VFQFN packaging
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment


8P34S1106I
20-VFQFPN
4 x 4 x 0.9 mm package body
2.1 x 2.1 mm ePad Size
NLG Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions^[a]

| Number | Name | Type | | Description |
|-----------|------------------|--------|---------------------|---|
| 1 | GND | Power | | Power supply ground. |
| 2, 3 | Q5, nQ5 | Output | | Differential output pair 5. LVDS interface levels. |
| 4 | NC | Unused | | Do not connect. |
| 5, 11, 20 | V _{DD} | Power | | Power supply pins. |
| 6 | CLK | Input | Pulldown | Non-inverting differential clock/data input. |
| 7 | nCLK | Input | Pulldown/ Pullup | Inverting differential clock/data input. |
| 8 | V _{REF} | | | Bias voltage reference. Provides an input bias voltage for the CLK, nCLK input pair in AC-coupled applications. Refer to <i>Figures 2B and 2C</i> for applicable AC-coupled input interfaces. |
| 9, 10 | Q0, nQ0 | Output | | Differential output pair 0. LVDS interface levels. |
| 12, 13 | Q1, nQ1 | Output | | Differential output pair 1. LVDS interface levels. |
| 14, 15 | Q2, nQ2 | Output | | Differential output pair 2. LVDS interface levels. |
| 16, 17 | Q3, nQ3 | Output | | Differential output pair 3. LVDS interface levels. |
| 18, 19 | Q4, nQ4 | Output | | Differential output pair 4. LVDS interface levels. |

[a] *Pulldown* and *Pullup* refers to an internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 2 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied.

| Item | Rating |
|---|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O Continuous Current Surge Current | 10mA 15mA |
| Input Sink/Source, I_{REF} | $\pm 2mA$ |
| Maximum Junction Temperature, $T_{J,MAX}$ | 150°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |
| ESD - Human Body Model ^[a] | 2000V |
| ESD - Charged Device Model ^{Note 1} | 1500V |

[a] According to JEDEC JS-001-2012/JESD22-C101E.

Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|--------|-------------------------|---------|---------|---------|-------|
| T_A | Ambient air temperature | -40 | | 85 | °C |
| T_J | Junction temperature | | | 125 | °C |

NOTE 1: It is the user's responsibility to ensure that device junction temperature remains below the maximum allowed.

NOTE 2: All conditions in the table must be met to guarantee device functionality.

NOTE 3: The device is verified to the maximum operating junction temperature through simulation.

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|--|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| I_{DD} | Power Supply Current | Q0 to Q5 terminated 100Ω between nQx, Qx | | 100 | 114 | mA |

Table 3B. Differential Input Characteristics, $V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---|--|---------|---------|-----------------------|---------------|
| I_{IH} | Input High Current | CLK, nCLK $V_{IN} = V_{DD} = 1.89V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLK $V_{IN} = 0V, V_{DD} = 1.89V$ | -10 | | | μA |
| | | nCLK $V_{IN} = 0V, V_{DD} = 1.89V$ | -150 | | | μA |
| V_{REF} | Reference Voltage for Input Bias ^[a] | $I_{REF} = +100\mu\text{A}, V_{DD} = 1.8V$ | 0.9 | | 1.30 | V |
| V_{PP} | Peak-to-Peak Voltage <small>Note3.</small> | $V_{DD} = 1.89V$ | 0.2 | | 1.0 | V |
| V_{CMR} | Common Mode Input Voltage ^[b] [c] | | 0.9 | | $V_{DD} - (V_{PP}/2)$ | V |

[a] V_{REF} specification is applicable to the AC-coupled input interfaces shown in *Figures 2B and 2C*.

[b] Common mode input voltage is defined as crosspoint voltage.

[c] V_{IL} should not be less than $-0.3V$ and V_{IH} should not be higher than V_{DD} .

Table 3C. LVDS DC Characteristics, $V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|---------------------------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | Outputs Loaded with 100Ω | 247 | 350 | 454 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1.0 | 1.23 | 1.4 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

AC Electrical Characteristics

Table 4. AC Electrical Characteristics, $V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$ ^[a]

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|---|-----------|--|---------|---------|---------|-------|
| f_{REF} | Input Frequency | CLK, nCLK | | | | 1.2 | GHz |
| $\Delta V/\Delta t$ | Input Edge Rate | CLK, nCLK | | 1.5 | | | V/ns |
| t_{PD} | Propagation Delay ^[b] | | CLK, nCLK to any Qx, nQx for $V_{PP} = 0.4V$ | 190 | 290 | 400 | ps |
| $t_{sk(o)}$ | Output Skew ^[c] [d] | | | | 20 | 40 | ps |
| $t_{sk(p)}$ | Pulse Skew | | $f_{REF} = 100MHz$ | | 4 | 20 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew ^[e] | | | | | 250 | ps |
| t_{JIT} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | | $f_{REF} = 122.88MHz$ Square Wave, $V_{PP} = 1V$, Integration Range: 1kHz – 40MHz | | 117 | 221 | fs |
| | | | $f_{REF} = 122.88MHz$ Square Wave, $V_{PP} = 1V$, Integration Range: 10kHz – 20MHz | | 89 | 110 | fs |
| | | | $f_{REF} = 122.88MHz$ Square Wave, $V_{PP} = 1V$, Integration Range: 12kHz – 20MHz | | 85 | 110 | fs |
| | | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 1V$, Integration Range: 1kHz – 40MHz | | 52 | 107 | fs |
| | | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 1V$, Integration Range: 10kHz – 20MHz | | 40 | 78 | fs |
| | | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 1V$, Integration Range: 12kHz – 20MHz | | 39 | 78 | fs |
| | | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 1kHz – 40MHz | | 51 | 112 | fs |
| | | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 10kHz – 20MHz | | 37 | 85 | fs |
| | | | $f_{REF} = 156.25MHz$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 12kHz – 20MHz | | 36 | 85 | fs |
| t_R / t_F | Output Rise/ Fall Time | | 10% to 90% outputs loaded with 100 Ω | | 270 | 400 | ps |
| | | | 20% to 80% outputs loaded with 100 Ω | | 162 | 260 | ps |

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Measured from the differential input crossing point to the differential output crossing point

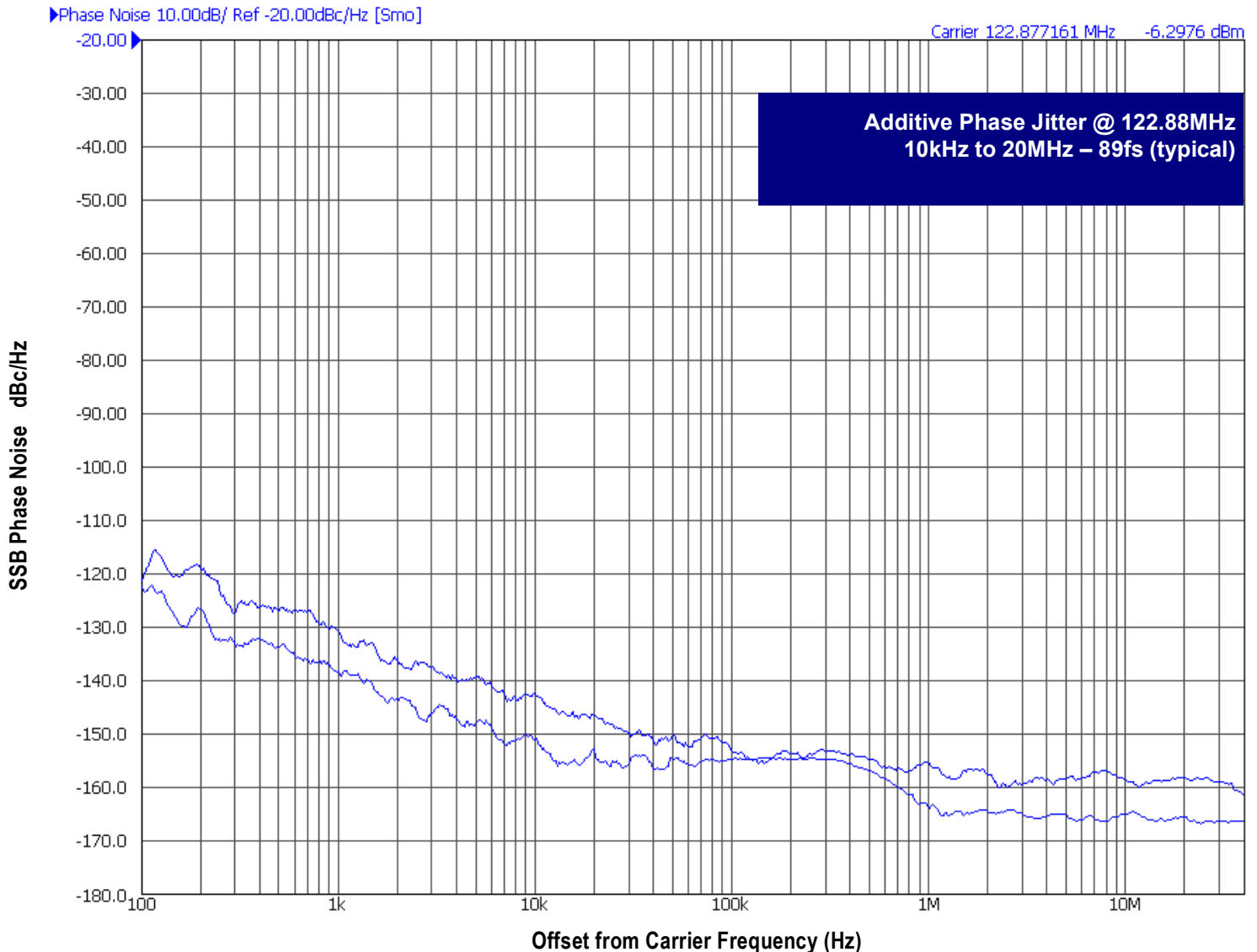
[c] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

[d] This parameter is defined in accordance with JEDEC Standard 65.

[e] Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the outputs are measured at the differential cross points.

Additive Phase Jitter

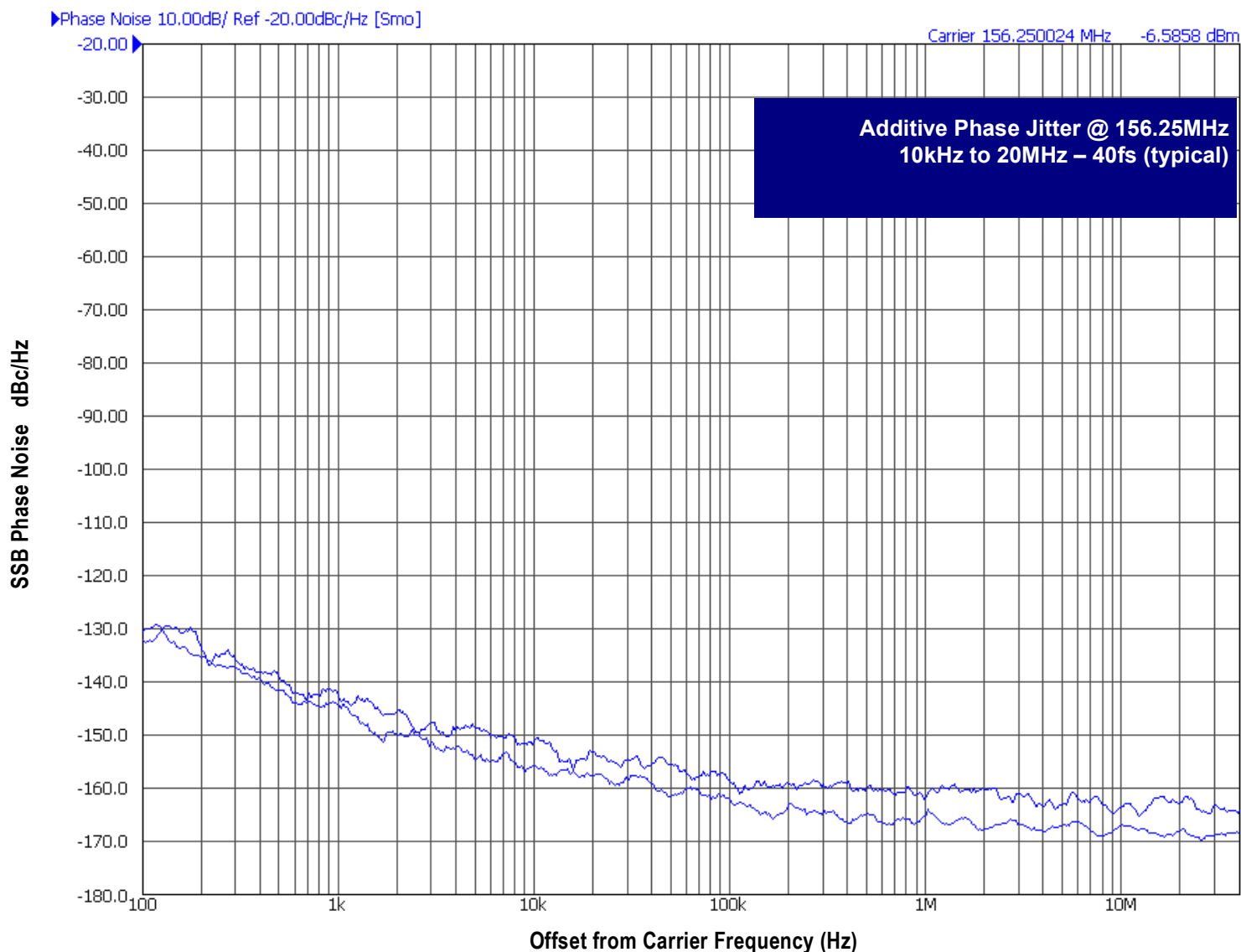
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment. Measured using a Rohde & Schwarz SMA 100 A Signal Generator as the input source.

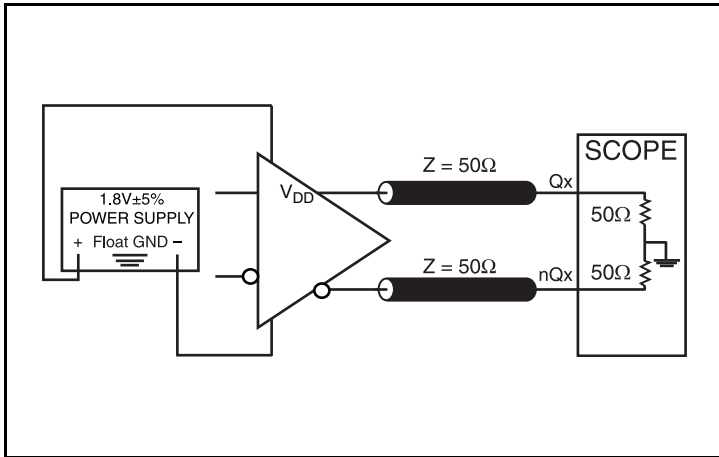
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the dBc Phase Noise. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a dBc value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

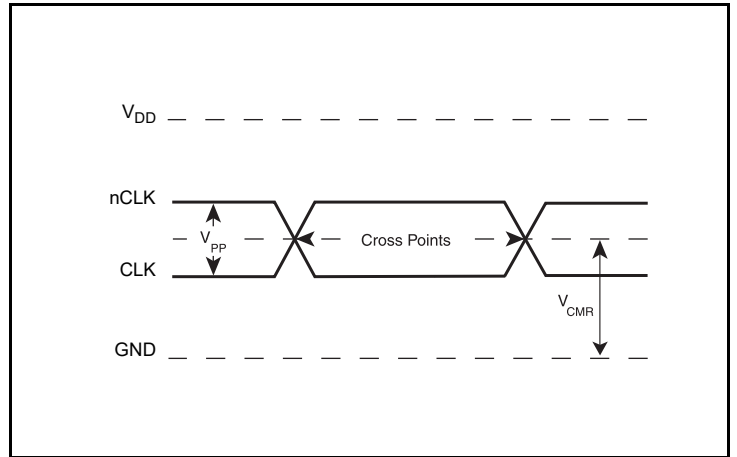


As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment. Measured using a Wenzel 156.25MHz Oscillator as the input source.

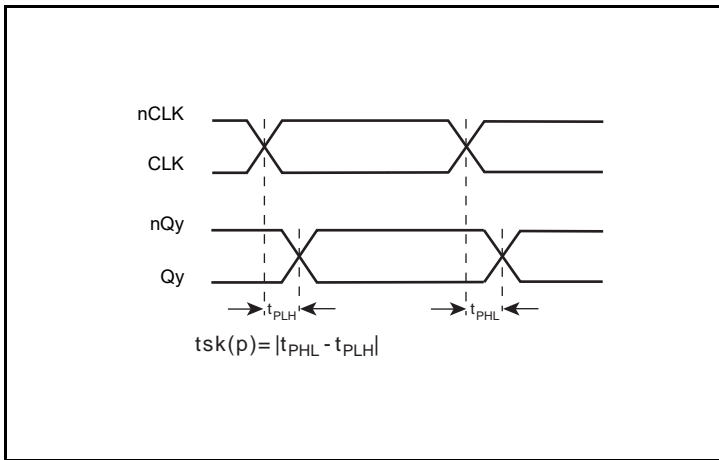
Parameter Measurement Information



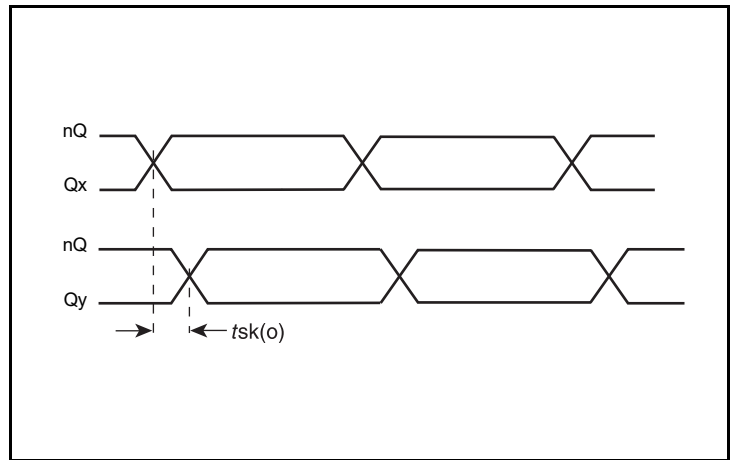
1.8V LVDS Output Load Test Circuit



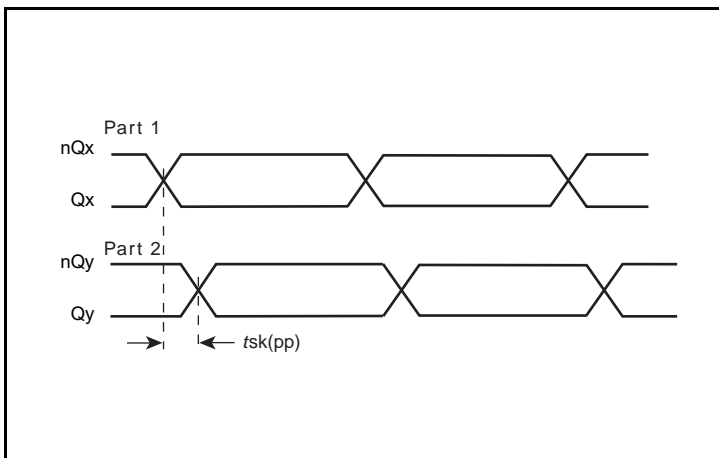
Differential Input Level



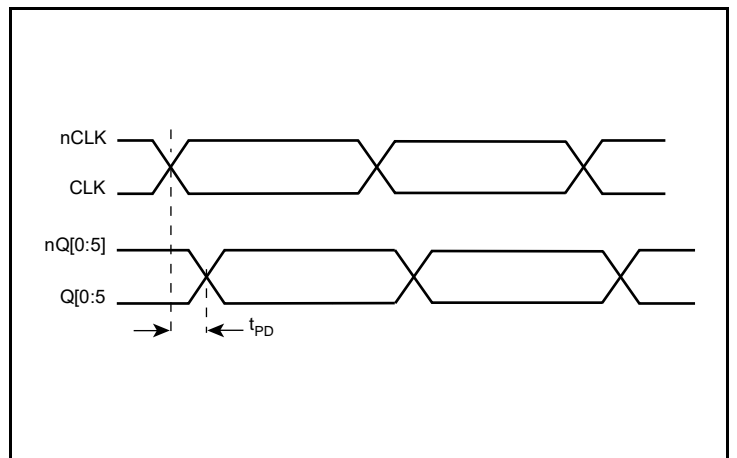
Pulse Skew



Output Skew

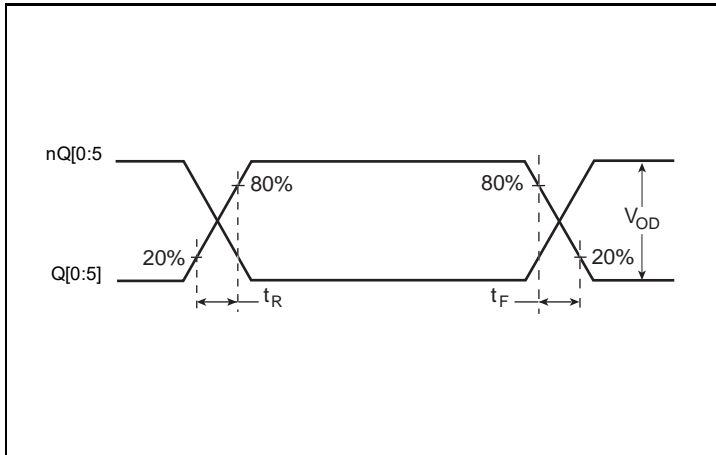


Part-to-Part Skew

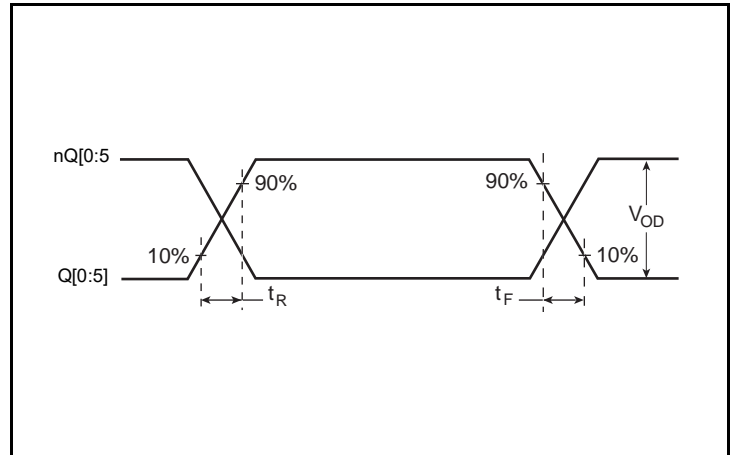


Propagation Delay

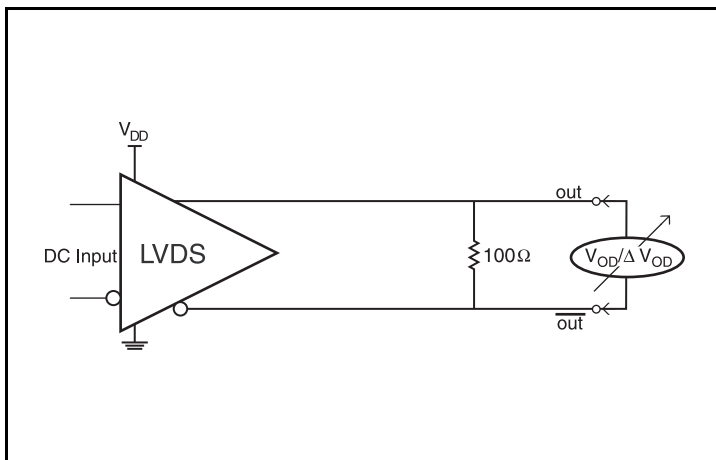
Parameter Measurement Information, continued



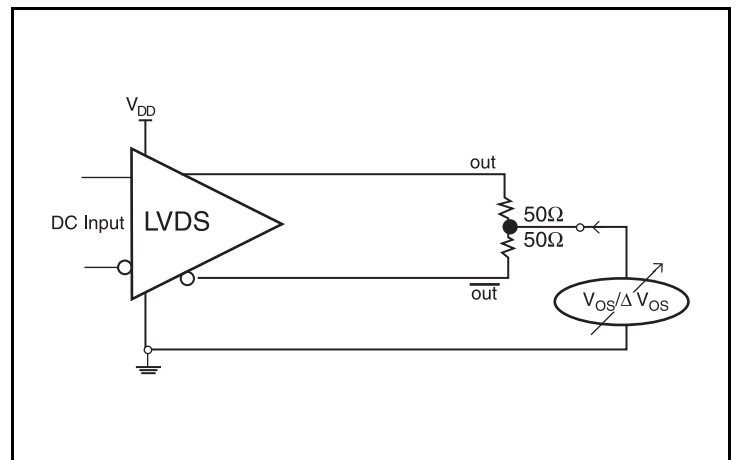
Output Rise/Fall Time, 20% - 80%



Output Rise/Fall Time, 10% - 90%



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1A and Figure 1B show examples of how a differential input can be wired to accept single-ended levels. The values below are for when both the single ended swing and VDD are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_3 and R_4 in parallel should equal the transmission line impedance and the signal DC offset after AC coupling should be equal to V_1 . For most $Z_o = 50\Omega$ applications, $R_3 = 100\Omega$ and R_4 can be 100Ω .

By keeping the same R_3/R_4 ratio, the values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the input can handle larger amplitude signaling, it is recommended that the amplitude be reduced. For single-ended applications, the swing can be larger. Make sure the single-ended logic high and logic low signal operates within specification limit. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

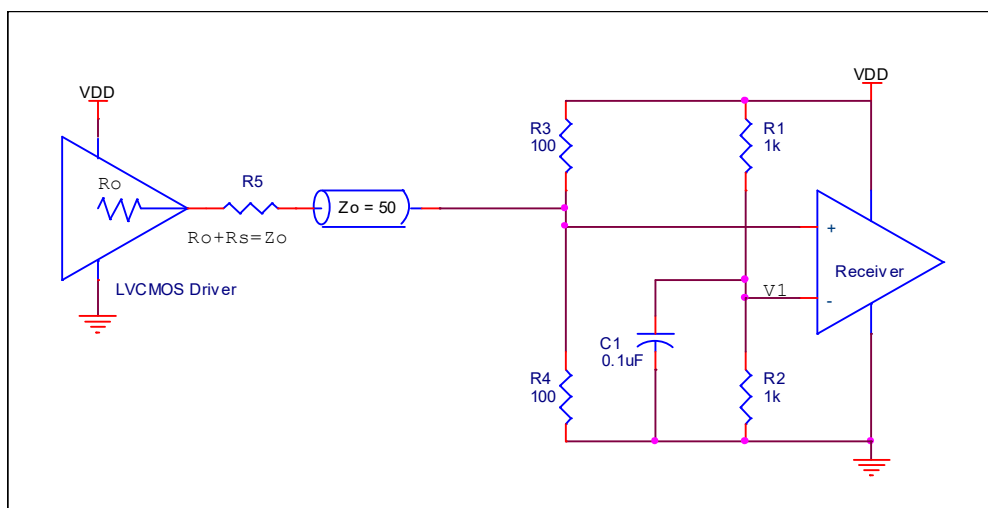


Figure 1A. DC Coupling Example for Wiring a Differential Input to Accept Single-ended Levels

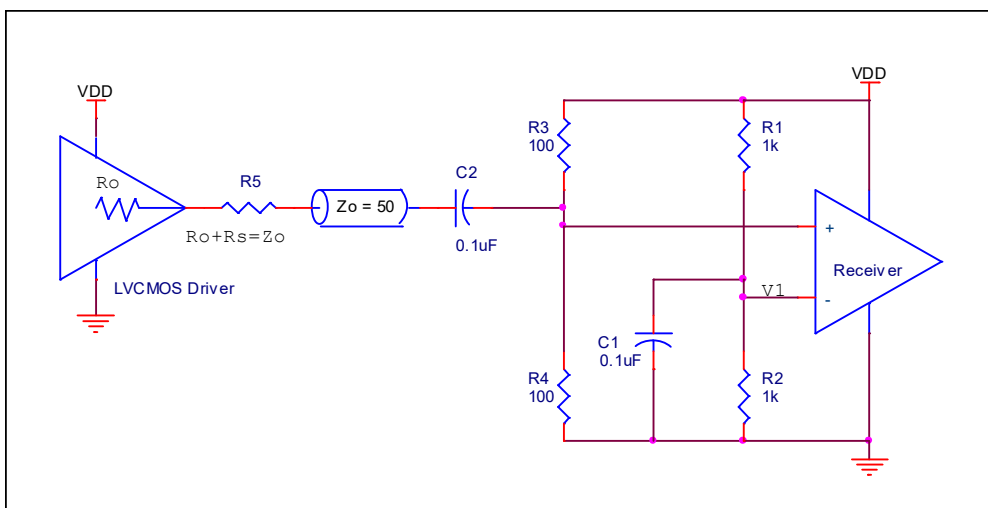


Figure 1B. AC Coupling Example for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Output Pins

Outputs

LVDS Outputs

Unused LVDS outputs must either have a 100Ω differential termination or have a 100Ω pull-up resistor to V_{DD} in order to ensure proper device operation.

1.8V Differential Clock Input Interface

The CLK /nCLK accepts LVDS and other differential signals. The differential input signal must meet both the V_{PP} and V_{CMR} input requirements. Figures 2A to 2D show interface examples for the CLK /nCLK input driven by the most common driver types. The input

interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

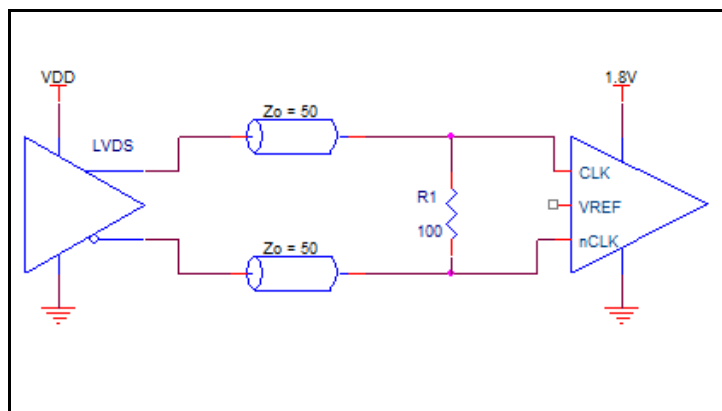


Figure 2A. Differential Input Driven by an LVDS Driver - DC Coupling

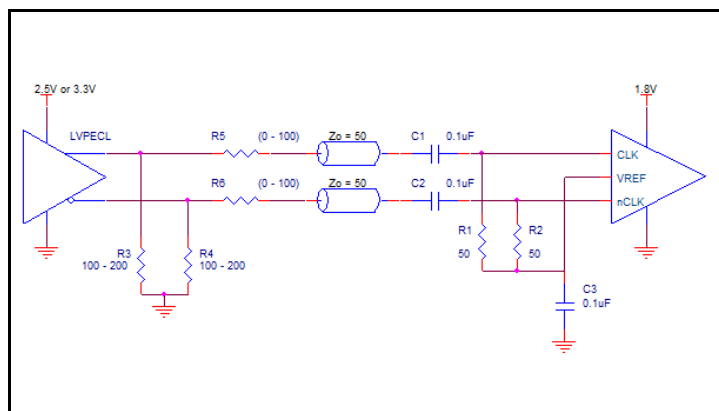


Figure 2B. Differential Input Driven by an LVPECL Driver - AC Coupling

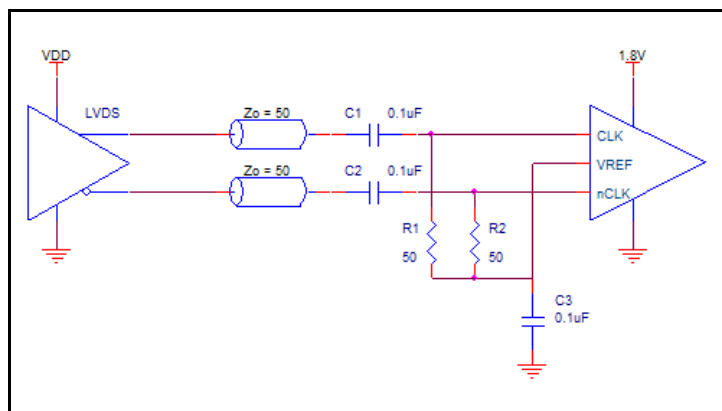


Figure 2C. Differential Input Driven by an LVDS Driver - AC Coupling

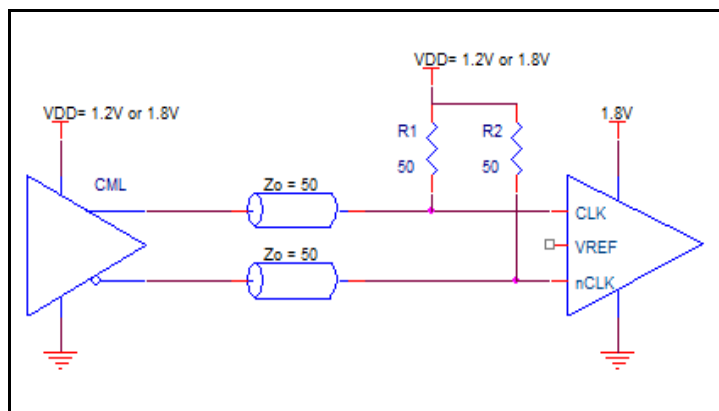
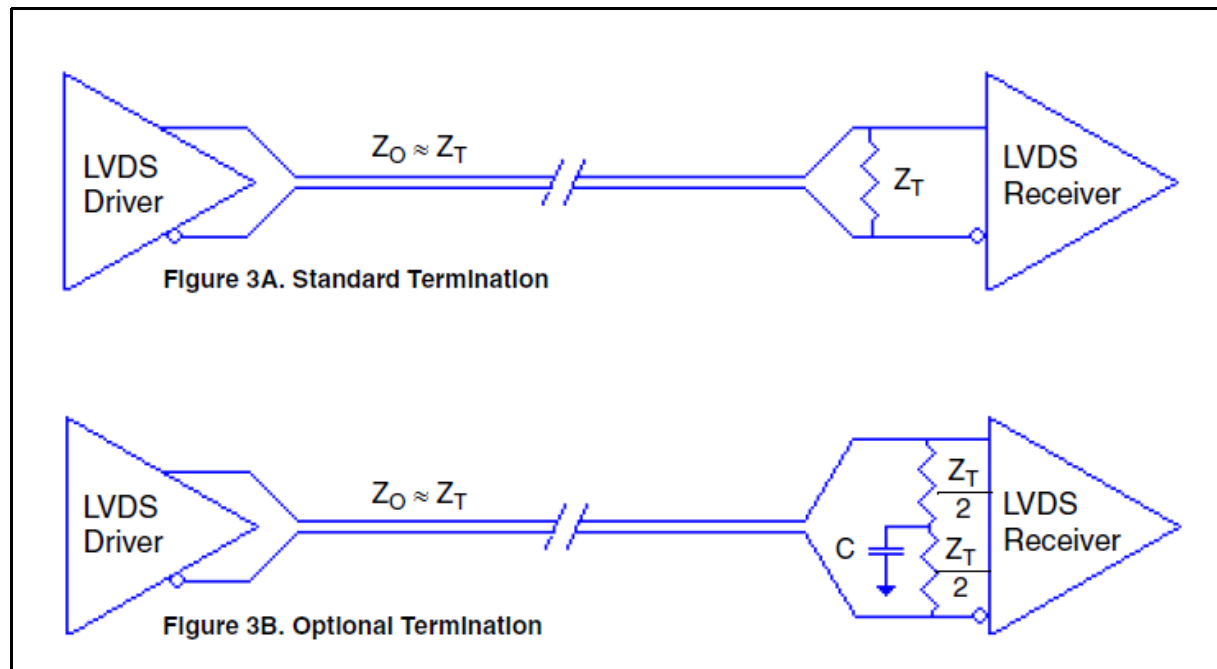


Figure 2D. Differential Input Driven by a CML Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage

source. The standard termination schematic as shown in Figure 3A can be used with either type of output structure. Figure 3B, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 4. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements.

Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

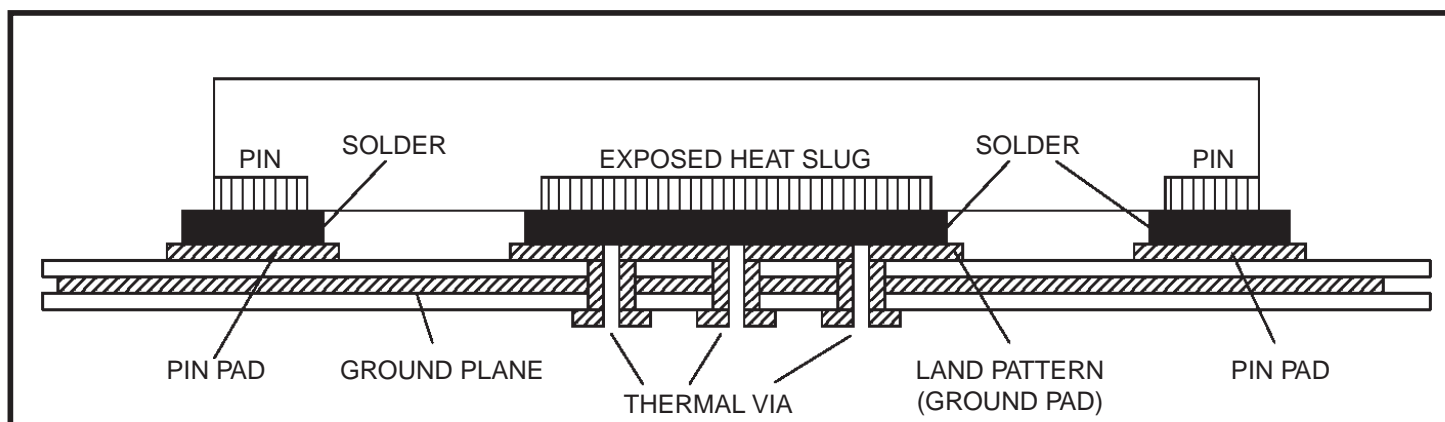


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8P34S1106I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8P34S1106I is the sum of the core power plus the output power dissipation due to the load. The following is the power dissipation for $V_{DD} = 1.8V + 5\% = 1.89V$, which gives worst case results.

The maximum current at 85°C is as follows:

$$I_{DD_MAX} = 107\text{mA}$$

- $\text{Power}_{(core)MAX} = V_{DD_MAX} * I_{DD_MAX} = 1.89V * 107\text{mA} = \mathbf{202.23mW}$

$$\mathbf{\text{Total Power}_{MAX} = 202.23mW}$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 62.2°C/W per Table 5 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.203\text{W} * 62.2^\circ\text{C/W} = 97.6^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 20 Lead VFQFN

| Meters per Second | θ_{JA} at 0 Air Flow | | |
|---|-----------------------------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 62.2°C/W | 54.4°C/W | 48.8°C/W |

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 20-lead VFQFN

| θ_{JA} vs. Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 62.2°C/W | 54.4°C/W | 48.8°C/W |

Transistor Count

The transistor count for the 8P34S1106I is: 976

Package Outline Drawings

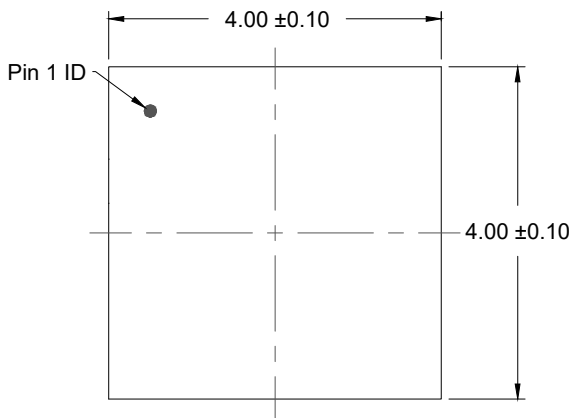
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

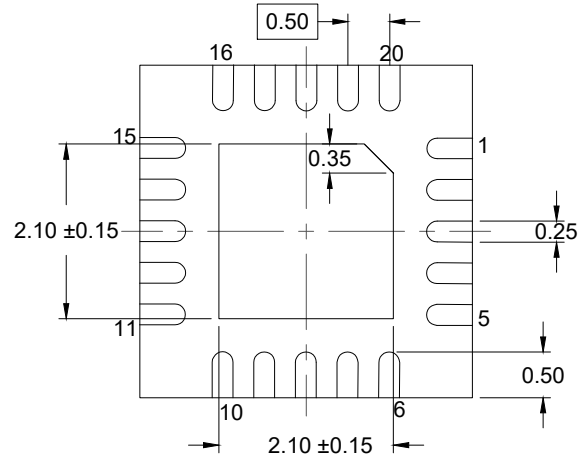
| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------------|--|--------------------|---------------|
| 8P34S1106NLGI | 8P34S1106NLGI | 4.0 × 4.0 × 0.9 mm 20-VFQFPN | Tray | -40°C to 85°C |
| 8P34S1106NLGI8 | 8P34S1106NLGI | 4.0 × 4.0 × 0.9 mm 20-VFQFPN | Tape & Reel | -40°C to 85°C |

Revision History

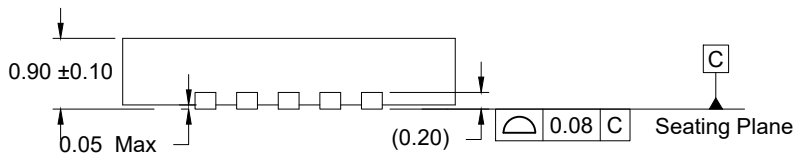
| Revision Date | Description of Change |
|-------------------|---|
| February 6, 2023 | Updated POD link in Ordering Information . |
| May 10, 2021 | <ul style="list-style-type: none"> ▪ Updated Ordering Information; changed Shipping Packaging from “Tube” to “Tray”; added link to POD in Package column. ▪ Updated Package Outline Drawings section. |
| September 8, 2020 | Updated the section “Wiring the Differential Input to Accept Single-Ended Levels”. |
| October 18, 2019 | <ul style="list-style-type: none"> ▪ Corrected the “shipping packaging” information for 8P34S1106NLGI in Ordering Information ▪ Completed other minor changes |
| November 29, 2018 | Updated the description of Absolute Maximum Ratings Added Recommended Operating Conditions Updated the Package Outline Drawings ; however, no technical changes |
| December 17, 2015 | Initial release. |



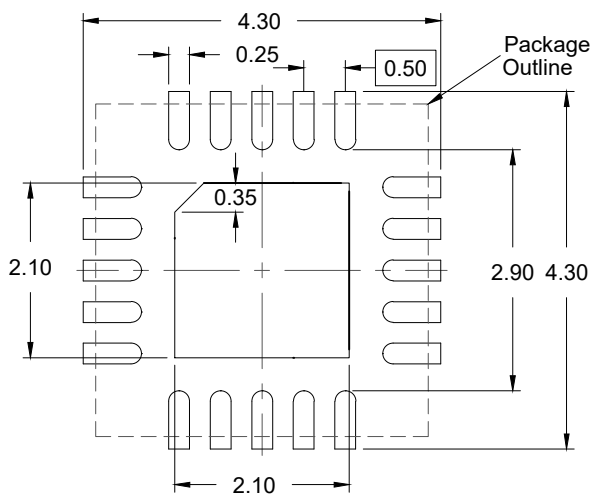
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

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