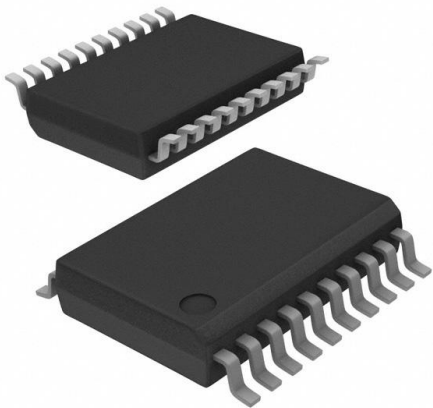


# IDT74FCT807BTPY Datasheet

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DiGi Electronics Part Number	IDT74FCT807BTPY-DG
Manufacturer	<a href="#">Renesas Electronics Corporation</a>
Manufacturer Product Number	IDT74FCT807BTPY
Description	IC CLK BUFFER 1:10 100MHZ 20SSOP
Detailed Description	Clock Fanout Buffer (Distribution) IC 1:10 100 MHz 20-SSOP (0.209", 5.30mm Width)



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

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## Purchase and inquiry

Manufacturer Product Number:

IDT74FCT807BTPY

Series:

74FCT

Type:

Fanout Buffer (Distribution)

Ratio - Input:Output:

1:10

Input:

TTL

Frequency - Max:

100 MHz

Operating Temperature:

0°C ~ 70°C

Grade:

-

Package / Case:

20-SSOP (0.209", 5.30mm Width)

Base Product Number:

IDT74FCT807

Manufacturer:

Renesas Electronics Corporation

Product Status:

Obsolete

Number of Circuits:

1

Differential - Input:Output:

No/No

Output:

TTL

Voltage - Supply:

4.75V ~ 5.25V

Mounting Type:

Surface Mount

Qualification:

-

Supplier Device Package:

20-SSOP

## Environmental & Export classification

RoHS Status:

RoHS non-compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



## FAST CMOS 1-TO-10 CLOCK DRIVER

### IDT74FCT807BT/CT

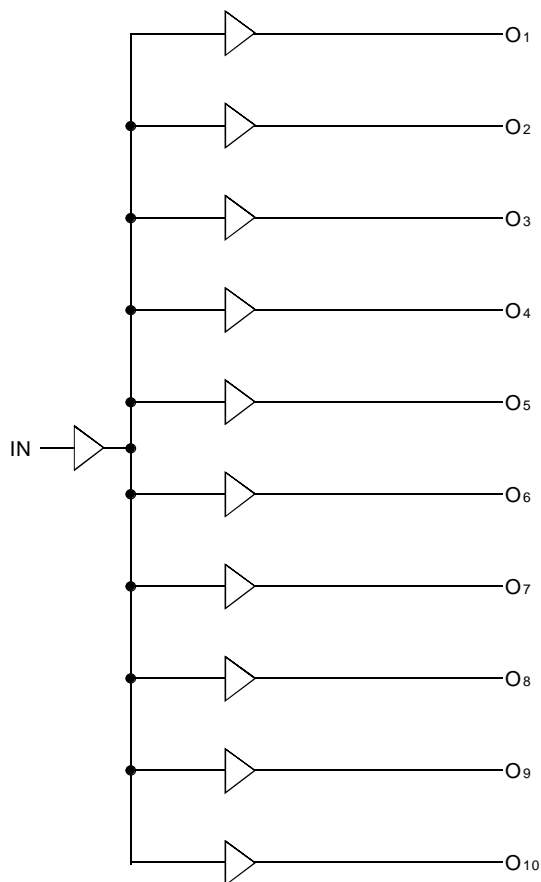
#### FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 250ps (max.)
- Very low duty cycle distortion < 350ps (max.)
- High speed: propagation delay < 2.5ns (max.)
- 100MHz operation
- TTL compatible inputs and outputs
- TTL level output voltage swings
- 1:10 fanout
- Output rise and fall time < 1.5ns (max)
- Low input capacitance: 4.5pF typical
- High drive: -32mA  $I_{OH}$ , +48mA  $I_{OL}$
- Available in QSOP, SSOP, and SOIC packages

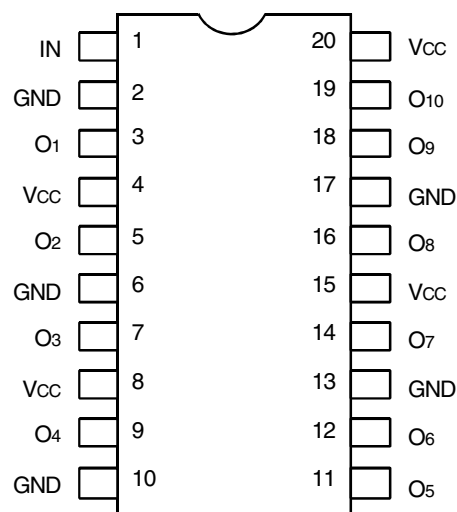
#### DESCRIPTION:

The FCT807T clock driver is built using advanced dual metal CMOS technology. This low skew clock driver features 1:10 fanout, providing minimal loading on the preceding drivers. The FCT807T offers low capacitance inputs with hysteresis for improved noise margins. TTL level outputs and multiple power and grounds reduce noise. The device also features -32/48mA drive capability for driving low impedance traces.

#### FUNCTIONAL BLOCK DIAGRAM



#### PIN CONFIGURATION



QSOP/ SOIC/ SSOP  
TOP VIEW

**IDT74FCT807BT/CT**  
**FAST CMOS 1-TO-10 CLOCK DRIVER**
**COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES**
**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Description	Max	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

**NOTE:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8	pF

**NOTE:**

- This parameter is measured at characterization but not tested.

**PIN DESCRIPTION**

Pin Names	Description
IN	Inputs
Ox	Outputs

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:

 Commercial: T<sub>A</sub> = 0°C to +70°C, Industrial: T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5V ± 5%

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
V <sub>IH</sub>	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2	—	—	V	
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I <sub>IH</sub>	Input HIGH Current (Input pins)	V <sub>CC</sub> = Max., V <sub>I</sub> = 2.7V	—	—	±1	μA	
I <sub>IL</sub>	Input LOW Current (Input pins)	V <sub>CC</sub> = Max., V <sub>I</sub> = 0.5V	—	—	±1	μA	
I <sub>OZH</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = Max., V <sub>O</sub> = 2.7V	—	—	±1	μA	
I <sub>OZL</sub>			—	—	±1		
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>I</sub> = V <sub>CC</sub> (Max.)	—	—	±1	μA	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V	
I <sub>OS</sub>	Short Circuit Current <sup>(4)</sup>	V <sub>CC</sub> = Max., V <sub>O</sub> = GND <sup>(3)</sup>	-60	-120	-225	mA	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -15mA	2.4	3.3	—	V
			I <sub>OH</sub> = -32mA	2	3	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	—	0.3	0.55	V	
I <sub>OFF</sub>	Input/Output Power Off Leakage	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> ≤ 4.5V	—	—	±1	μA	
V <sub>H</sub>	Input Hysteresis for all inputs	—	—	150	—	mV	
I <sub>CCL</sub> I <sub>CCH</sub> I <sub>CCZ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub>	—	5	500	μA	

**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5V, +25°C ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition should not exceed one second.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V		—	0.5	2	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(3)</sup>	V <sub>CC</sub> = Max. Input Toggling 50% Duty Cycle Outputs Open	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	0.4	0.6	mA/MHz
I <sub>C</sub>	Total Power Supply Current <sup>(5)</sup>	V <sub>CC</sub> = Max. Input Toggling 50% Duty Cycle Outputs Open f <sub>i</sub> = 50MHz	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	20	30.5 <sup>(4)</sup>	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	20.3	31.3 <sup>(4)</sup>	

## NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>C</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$   
I<sub>CC</sub> = Quiescent Current (I<sub>CC1</sub>, I<sub>CC2</sub> and I<sub>CC3</sub>)  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
D<sub>H</sub> = Duty Cycle for TTL Inputs High  
N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
f<sub>o</sub> = Output Frequency  
N<sub>o</sub> = Number of Outputs at f<sub>o</sub>  
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL<sup>(3,4)</sup>

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT807BT		FCT807CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	50Ω to V <sub>CC</sub> /2, C <sub>L</sub> = 10pF (See figure 1) or 50Ω ac termination, C <sub>L</sub> = 10pF (See figure 2) f ≤ 100MHz Outputs connected in groups of two	1.3	2.7	1.3	2.5	ns
t <sub>R</sub>	Output Rise Time		—	1.5	—	1.5	ns
t <sub>F</sub>	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.25	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		—	0.5	—	0.35	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	0.9	—	0.65	ns	

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT807BT		FCT807CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	C <sub>L</sub> = 30pF f ≤ 67MHz (See figure 3)	1.5	3.8	1.5	3.5	ns
t <sub>R</sub>	Output Rise Time		—	1.5	—	1.5	ns
t <sub>F</sub>	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.25	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		—	0.5	—	0.35	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	0.9	—	0.75	ns	

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT807BT		FCT807CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	C <sub>L</sub> = 30pF f ≤ 40MHz (See figure 4)	1.5	3.8	1.5	3.5	ns
t <sub>R</sub>	Output Rise Time		—	1.5	—	1.5	ns
t <sub>F</sub>	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		—	0.6	—	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	1	—	0.75	ns	

## NOTES:

- See test circuits and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- t<sub>PLH</sub>, t<sub>PHL</sub>, tsk(t) are production tested. All other parameters guaranteed but not production tested.
- Propagation delay range indicated by Min. and Max. limit is due to V<sub>CC</sub>, operating temperature and process parameters. These propagation delay limits do not imply skew.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL<sup>(3,4)</sup>

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT807BT		FCT807CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	50Ω to V <sub>CC</sub> /2, C <sub>L</sub> = 10pF (See figure 1) or 50Ω ac termination, C <sub>L</sub> = 10pF (See figure 2) f ≤ 100MHz Outputs connected in groups of two	1.3	2.9	1.3	2.7	ns
t <sub>R</sub>	Output Rise Time		—	1.5	—	1.5	ns
t <sub>F</sub>	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		—	0.6	—	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	0.9	—	0.65	ns	

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT807BT		FCT807CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	C <sub>L</sub> = 30pF f ≤ 67MHz (See figure 3)	1.5	4	1.5	3.7	ns
t <sub>R</sub>	Output Rise Time		—	1.5	—	1.5	ns
t <sub>F</sub>	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		—	0.6	—	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	0.9	—	0.75	ns	

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT807BT		FCT807CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	C <sub>L</sub> = 30pF f ≤ 40MHz (See figure 4)	1.5	4	1.5	3.7	ns
t <sub>R</sub>	Output Rise Time		—	1.5	—	1.5	ns
t <sub>F</sub>	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.45	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		—	0.7	—	0.55	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	1	—	0.75	ns	

## NOTES:

- See test circuits and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- t<sub>PLH</sub>, t<sub>PHL</sub>, tsk(t) are production tested. All other parameters guaranteed but not production tested.
- Propagation delay range indicated by Min. and Max. limit is due to V<sub>CC</sub>, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS

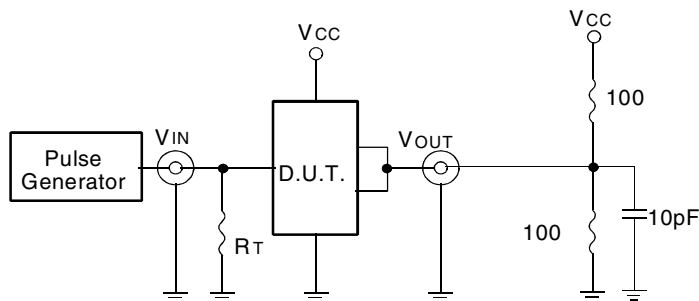


Fig. 1: 50Ω to Vcc/2, CL = 10pF

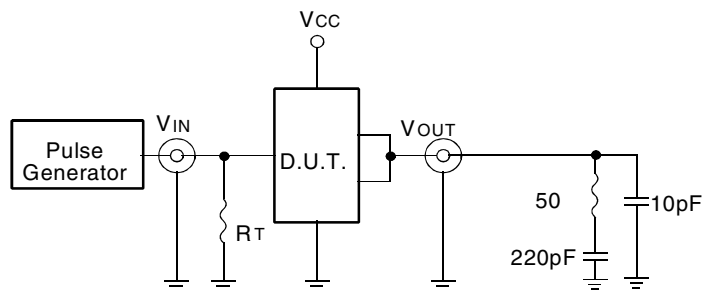


Fig. 2: 50Ω AC Termination, CL = 10pF

The capacitor value for AC termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

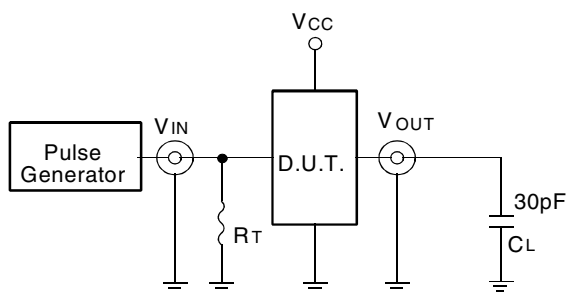


Fig. 3: CL = 30pF Circuit

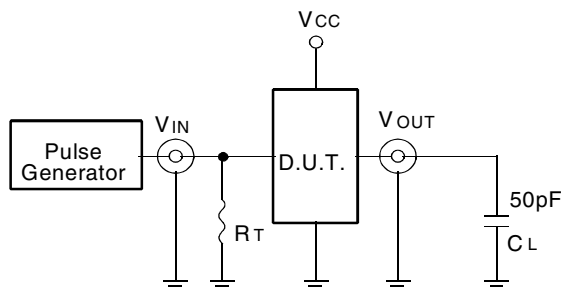


Fig. 4: CL = 50pF Circuit

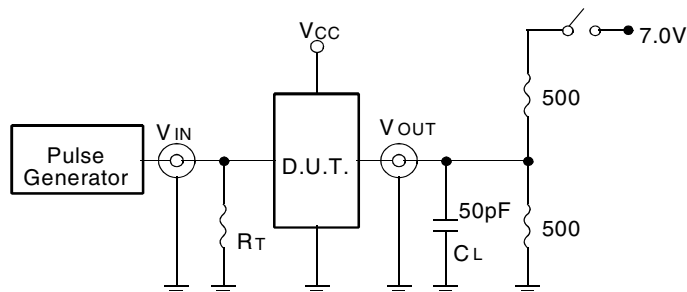


Fig. 5: Enable and Disable Time Circuit

SWITCH POSITION

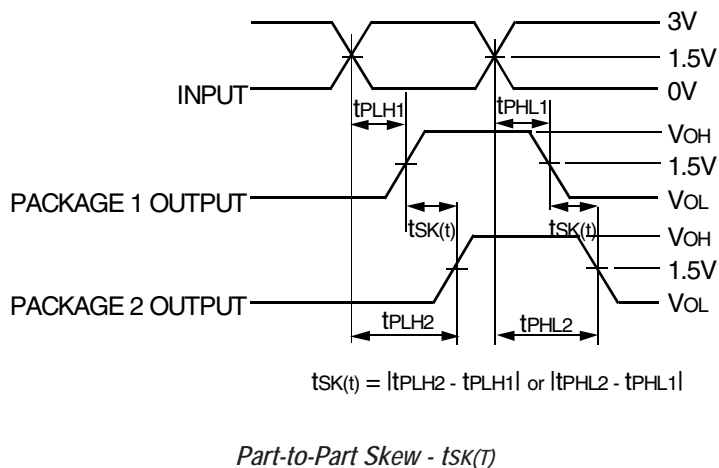
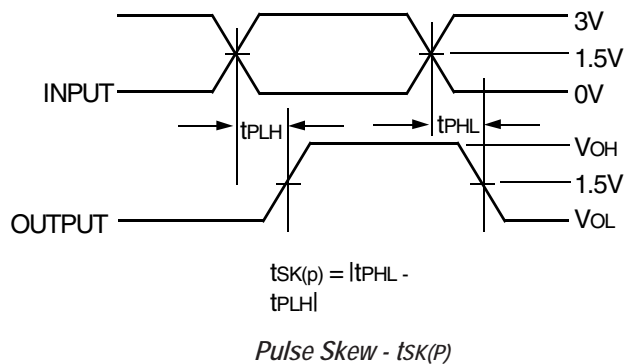
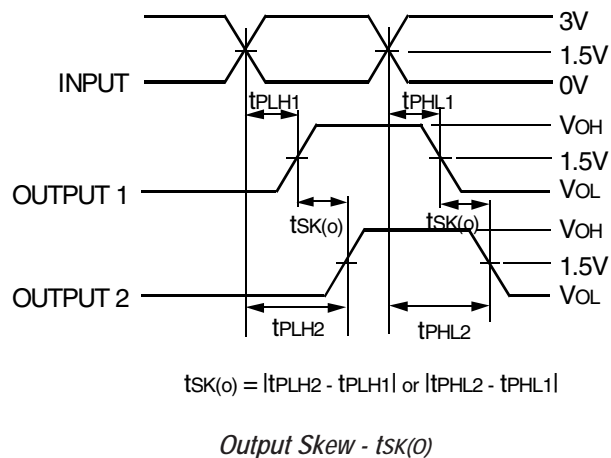
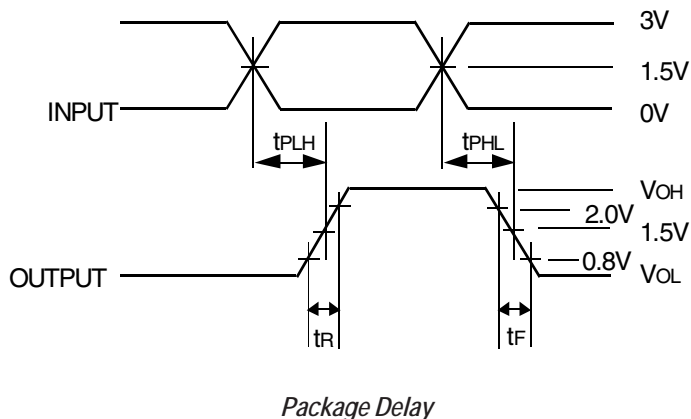
Test	Switch
Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to Zout of the Pulse Generator.

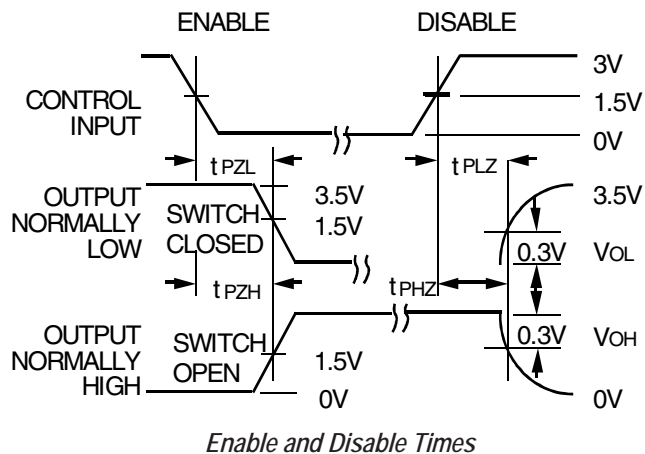


TEST WAVEFORMS



NOTE:

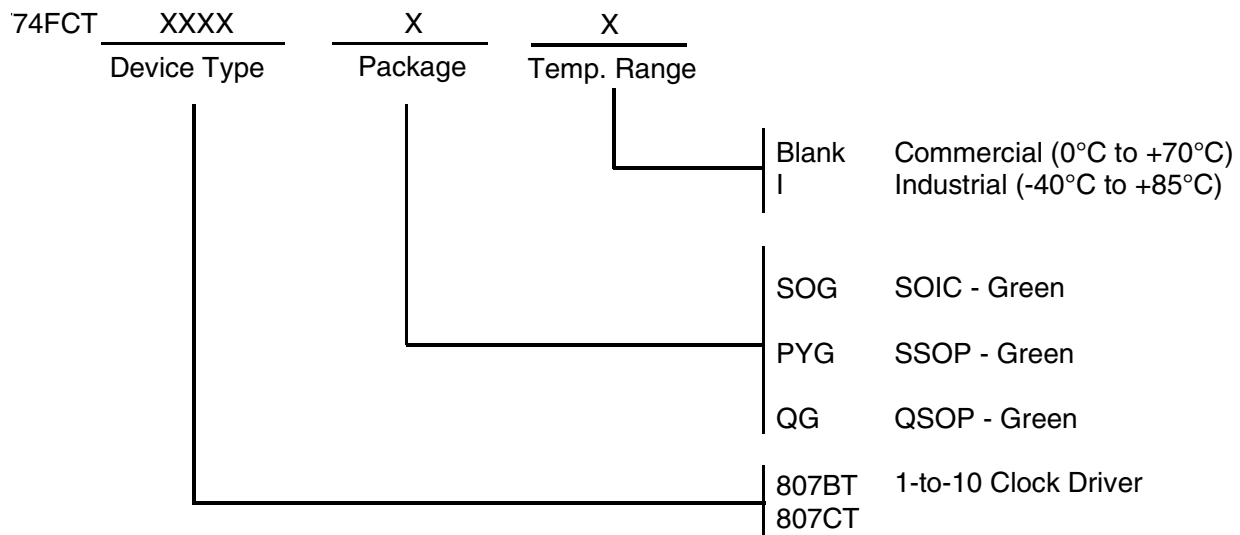
1. Package 1 and Package 2 are same device type and speed grade.



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$

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TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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