25LC320AT-H/SN16KVAO Datasheet

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DiGi Electronics Part Number	25LC320AT-H/SN16KVAO-DG
Manufacturer	Microchip Technology
Manufacturer Product Number	25LC320AT-H/SN16KVAO
Description	IC EEPROM 32KBIT SPI 10MHZ 8SOIC
Detailed Description	EEPROM Memory IC 32Kbit SPI 10 MHz 8-SOIC

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
25LC320AT-H/SN16KVAO	Microchip Technology
Series:	Product Status:
-	Active
DiGi-Electronics Programmable:	Memory Type:
Not Verified	Non-Volatile
Memory Format:	Technology:
EEPROM	EEPROM
Memory Size:	Memory Organization:
32Kbit	4K x 8
Memory Interface:	Clock Frequency:
SPI	10 MHz
Write Cycle Time - Word, Page:	Voltage - Supply:
5ms	2.5V ~ 5.5V
Operating Temperature:	Grade:
-40°C ~ 150°C (TA)	Automotive
Qualification:	Mounting Type:
AEC-Q100	Surface Mount
Package / Case:	Supplier Device Package:
8-SOIC (0.154", 3.90mm Width)	8-SOIC
Base Product Number:	
25LC320	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	3 (168 Hours)
REACH Status:	ECCN:
REACH Unaffected	3A001A2A
HTSUS:	
8542.32.0051	

25LC080C/25LC080D/25LC160C/ 25LC160D/25LC320A/25LC640A/ 25LC128/25LC256

8K-256K SPI Serial EEPROM High Temp Family Data Sheet

Features

- Maximum Clock: 5 MHz
- Low-Power CMOS Technology:
  - Write current: 5 mA at 5.5V (maximum)
  - Read current: 5 mA at 5.5V, 5 MHz
  - Standby current: 10 µA at 5.5V
- 1,024 x 8 through 32,768 x 8-bit Organization
- Byte and Page-Level Write Operations
- Self-Timed Erase and Write Cycles (6 ms maximum)
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Sequential Read
- High Reliability:
  - Endurance: >1,000,000 erase/write cycles
  - Data retention: >200 years
  - ESD protection: >4000V
- Temperature Range Supported:
  - Extended (H): -40°C to +150°C
- RoHS Compliant
- Automotive AECQ-100 Qualified

Description

Microchip Technology Inc. 25LCXXX(1) devices are Mid-density 8- through 256-Kbit Serial Electrically Erasable PROMs (EEPROM). The devices are organized in blocks of x8-bit memory and support the Serial Peripheral Interface (SPI) compatible serial bus architecture. Byte-level and page-level functions are supported. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{\text{CS}}$) input.

Communication to the device can be paused via the hold pin ($\overline{\text{HOLD}}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

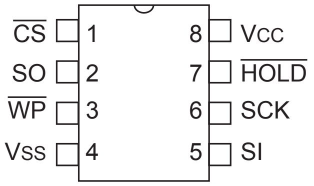
Note 1: 25LCXXX is used in this document as a generic part number for the 25LC080C/ 25LC080D/25LC160C/25LC160D/ 25LC320A/25LC640A/25LC128/ 25LC256 devices.

Packages

- 8-Lead SOIC

Package Types (not to scale)

8-Lead SOIC
(Top View)



Pin Function Table

Name	Function
$\overline{\text{CS}}$	Chip Select Input
SO	Serial Data Output
$\overline{\text{WP}}$	Write-Protect
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{\text{HOLD}}$	Hold Input
Vcc	Supply Voltage

DEVICE SELECTION TABLE

Part Number	Density (bits)	Organization	VCC Range	Max. Speed (MHz)	Page Size (Bytes)	Temp. Range	Package
25LC080C	8K	1,024 x 8	2.5V-5.5V	5	16	H	SN
25LC080D	8K	1,024 x 8	2.5V-5.5V	5	32	H	SN
25LC160C	16K	2,048 x 8	2.5V-5.5V	5	16	H	SN
25LC160D	16K	2,048 x 8	2.5V-5.5V	5	32	H	SN
25LC320A	32K	4,096 x 8	2.5V-5.5V	5	32	H	SN
25LC640A	64K	8,192 x 8	2.5V-5.5V	5	32	H	SN
25LC128	128K	16,384 x 8	2.5V-5.5V	5	64	H	SN
25LC256	256K	32,768 x 8	2.5V-5.5V	5	64	H	SN

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC....................6.5V
All inputs and outputs w.r.t. VSS .... -0.6V to VCC +1.0V
Storage temperature ....-65°C to +155°C
Ambient temperature under bias .... -40°C to +150°C(1)
ESD protection on all pins....................4 kV

Note 1: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time between +125°C and +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Extended (H): TA = -40°C to +150°C VCC = 2.5V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	VIH1	High-Level Input Voltage	0.7 VCC	VCC + 1	V	
D002	VIL1	Low-Level Input Voltage	-0.3	0.3VCC	V	VCC ≥ 2.7V
D003	VIL2		-0.3	0.2VCC	V	VCC < 2.7V
D004	VOL1	Low-Level Output Voltage	—	0.4	V	IOL = 2.1 mA
D005	VOL2		—	0.2	V	IOL = 1.0 mA
D006	VOH	High-Level Output Voltage	VCC – 0.5	—	V	IOH = -400 µA
D007	ILI	Input Leakage Current	—	±2	µA	$\overline{CS}$ = VCC, VIN = VSS OR VCC
D008	ILO	Output Leakage Current	—	±2	µA	$\overline{CS}$ = VCC, VOUT = VSS OR VCC
D009	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V (**Note 1**)
D010	ICC Read	Operating Current	—	5	mA	VCC = 5.5V; FCLK = 5.0 MHz; SO = Open
			—	2.5	mA	VCC = 2.5V; FCLK = 3.0 MHz; SO = Open
D011	ICC Write	Operating Current	—	5	mA	VCC = 5.5V
			—	3	mA	VCC = 2.5V
D012	ICCS	Standby Current	—	10	µA	$\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS, +150°C

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Extended (H): TA = -40°C to +150°C VCC = 2.5V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	—	5	MHz	4.5V ≤ Vcc ≤ 5.5V
			—	3	MHz	2.5V ≤ Vcc < 4.5V
2	TCSS	$\overline{\text{CS}}$ Setup Time	100	—	ns	4.5V ≤ Vcc ≤ 5.5V
			150	—	ns	2.5V ≤ Vcc < 4.5V
3	TCSH	$\overline{\text{CS}}$ Hold Time	200	—	ns	4.5V ≤ Vcc ≤ 5.5V
			250	—	ns	2.5V ≤ Vcc < 4.5V
4	TCSD	$\overline{\text{CS}}$ Disable Time	50	—	ns	—
5	Tsu	Data Setup Time	20	—	ns	4.5V ≤ Vcc ≤ 5.5V
			30	—	ns	2.5V ≤ Vcc < 4.5V
6	THD	Data Hold Time	40	—	ns	4.5V ≤ Vcc ≤ 5.5V
			50	—	ns	2.5V ≤ Vcc < 4.5V
7	TR	CLK Rise Time	—	2	µs	**Note 1**
8	TF	CLK Fall Time	—	2	µs	**Note 1**
9	THI	Clock High Time	100	—	ns	4.5V ≤ Vcc ≤ 5.5V
			150	—	ns	2.5V ≤ Vcc < 4.5V
10	TLO	Clock Low Time	100	—	ns	4.5V ≤ Vcc ≤ 5.5V
			150	—	ns	2.5V ≤ Vcc < 4.5V
11	TCLD	Clock Delay Time	50	—	ns	
12	TCLE	Clock Enable Time	50	—	ns	
13	TV	Output Valid from Clock Low	—	100	ns	4.5V ≤ Vcc ≤ 5.5V
			—	160	ns	2.5V ≤ Vcc < 4.5V
14	THO	Output Hold Time	0	—	ns	**Note 1**
15	TDIS	Output Disable Time	—	80	ns	4.5V ≤ Vcc ≤ 5.5V (**Note 1**)
			—	160	ns	2.5V ≤ Vcc < 4.5V (**Note 1**)
16	THS	$\overline{\text{HOLD}}$ Setup Time	40	—	ns	4.5V ≤ Vcc ≤ 5.5V
			80	—	ns	2.5V ≤ Vcc < 4.5V
17	THH	$\overline{\text{HOLD}}$ Hold Time	40	—	ns	4.5V ≤ Vcc ≤ 5.5V
			80	—	ns	2.5V ≤ Vcc < 4.5V
18	THZ	$\overline{\text{HOLD}}$ Low to Output High Z	—	60	ns	4.5V ≤ Vcc ≤ 5.5V (**Note 1**)
			—	160	ns	2.5V ≤ Vcc < 4.5V (**Note 1**)
19	THV	$\overline{\text{HOLD}}$ High to Output Valid	—	60	ns	4.5V ≤ Vcc ≤ 5.5V
			—	160	ns	2.5V ≤ Vcc < 4.5V
20	TWC	Internal Write Cycle Time	—	6	ms	**Note 2**
21		Endurance	1,000,000	—	E/W Cycles	Page mode, 25°C, VCC = 5.5V (**Note 3**)

Note 1: This parameter is periodically sampled and not 100% tested.

2: TWC begins on the rising edge of $\overline{\text{CS}}$ after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our website: www.microchip.com.

TABLE 1-3:

AC Waveform	
V_{LO} = 0.2V	
V_{HI} = V_{CC} – 0.2V	**Note 1**
V_{HI} = 4.0V	**Note 2**
C_L = 50 pF	
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For V_{CC} ≤ 4.0V

2: For V_{CC} > 4.0V

FIGURE 1-1: HOLD TIMING

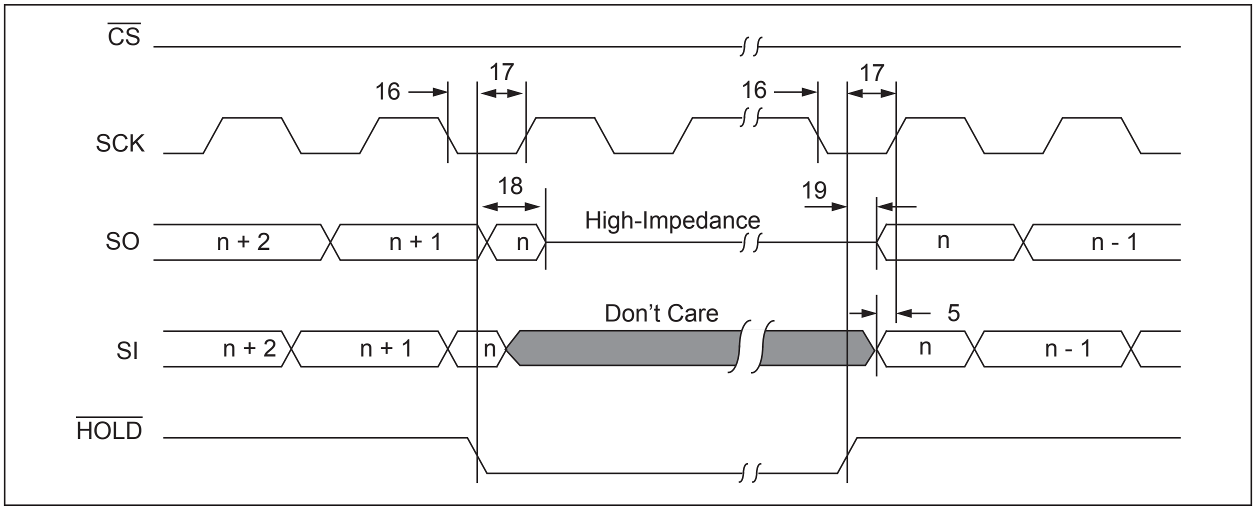


FIGURE 1-2: SERIAL INPUT TIMING

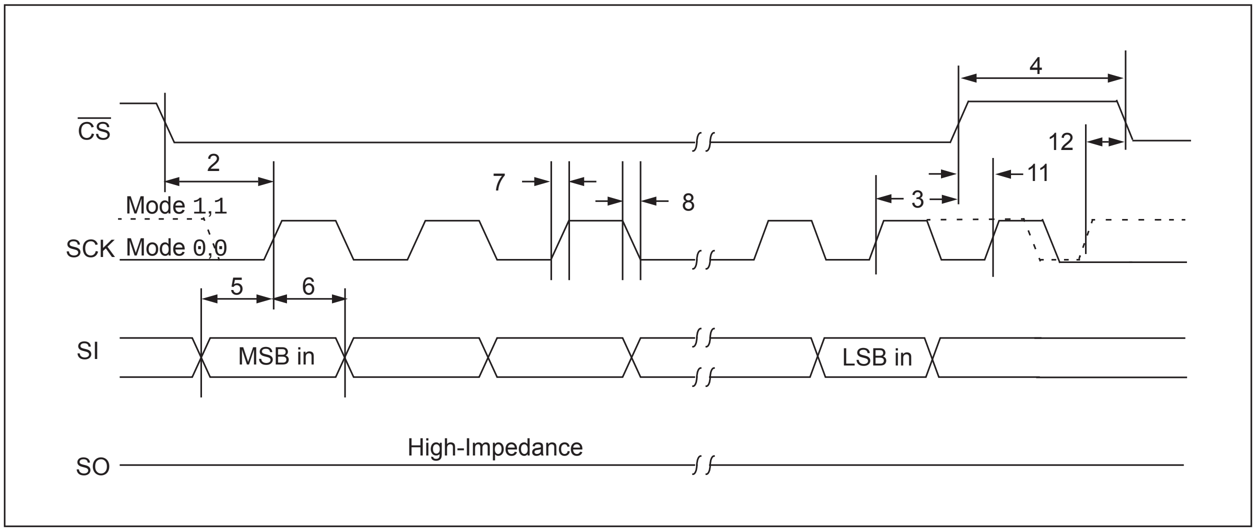
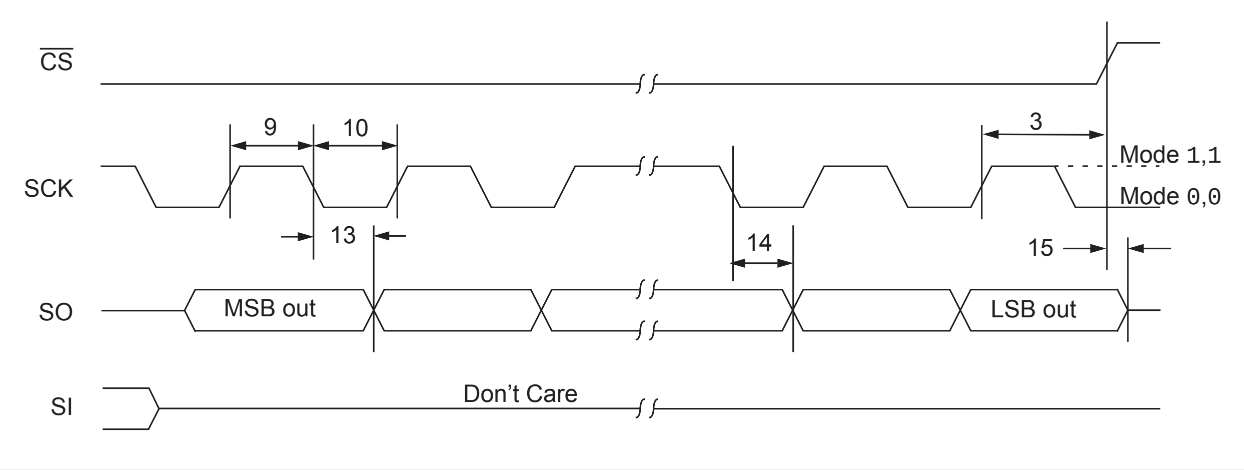


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	Pin Number	Function
$\overline{\text{CS}}$	1	Chip Select Input
SO	2	Serial Data Output
$\overline{\text{WP}}$	3	Write-Protect Pin
V_{SS}	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
$\overline{\text{HOLD}}$	7	Hold Input
V_{CC}	8	Supply Voltage

2.1 Chip Select ($\overline{\text{CS}}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{\text{CS}}$ input signal. If $\overline{\text{CS}}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{\text{CS}}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25LCXXX. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Write-Protect ($\overline{\text{WP}}$)

This pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When $\overline{\text{WP}}$ is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When $\overline{\text{WP}}$ is high, all functions, including writes to the nonvolatile bits in the STATUS register operate normally. If the WPEN bit is set, $\overline{\text{WP}}$ low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, $\overline{\text{WP}}$ going low will have no effect on the write.

The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the 25LCXXX in a system with $\overline{\text{WP}}$ pin grounded and still be able to write to the STATUS register. The $\overline{\text{WP}}$ pin functions will be enabled when the WPEN bit is set high.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25LCXXX. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.6 Hold ($\overline{\text{HOLD}}$)

The $\overline{\text{HOLD}}$ pin is used to suspend transmission to the 25LCXXX while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{\text{HOLD}}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{\text{HOLD}}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25LCXXX must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{\text{HOLD}}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 Principles of Operation

The 25LCXXX are Mid-Density Serial EEPROMs designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25LCXXX contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred Most Significant bit (MSb) first, Least Significant bit (LSb) last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25LCXXX in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

Block Diagram

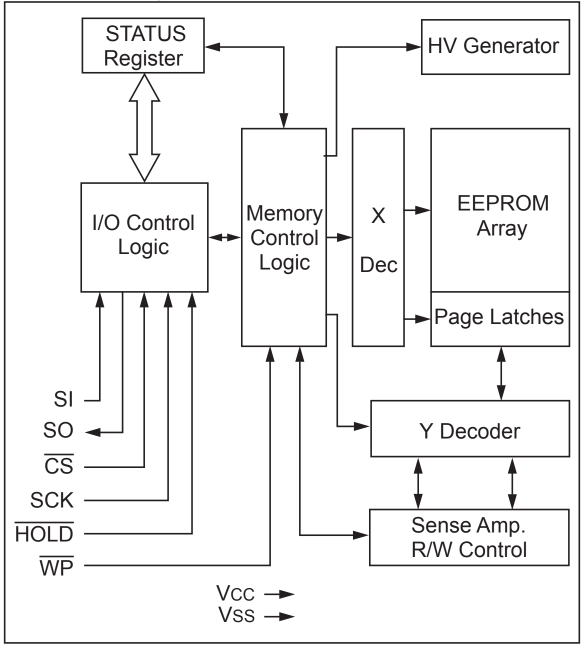


TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
`READ`	`0000 0011`	Read data from memory array beginning at selected address
`WRITE`	`0000 0010`	Write data to memory array beginning at selected address
`WRDI`	`0000 0100`	Reset the write enable latch (disable write operations)
`WREN`	`0000 0110`	Set the write enable latch (enable write operations)
`RDSR`	`0000 0101`	Read STATUS register
`WRSR`	`0000 0001`	Write STATUS register

3.2 Read Sequence

The device is selected by pulling CS low. The 8-bit `READ` instruction is transmitted to the 25LCXXX followed by the 16-bit address. After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the CS pin (Figure 3-1).

3.3 Write Sequence

Prior to any attempt to write data to the 25LCXXX, the write enable latch must be set by issuing the `WREN` instruction (Figure 3-4). This is done by setting CS low and then clocking out the proper instruction into the 25LCXXX. After all eight bits of the instruction are transmitted, the CS must be brought high to set the write enable latch. If the write operation is initiated immediately after the `WREN` instruction without CS being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the CS low, issuing a `WRITE` instruction, followed by the 16-bit address, and then the data to be written. Depending upon the density, a page of data that ranges from 16 bytes to 64 bytes can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and, end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the CS must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If CS is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

FIGURE 3-1: READ SEQUENCE

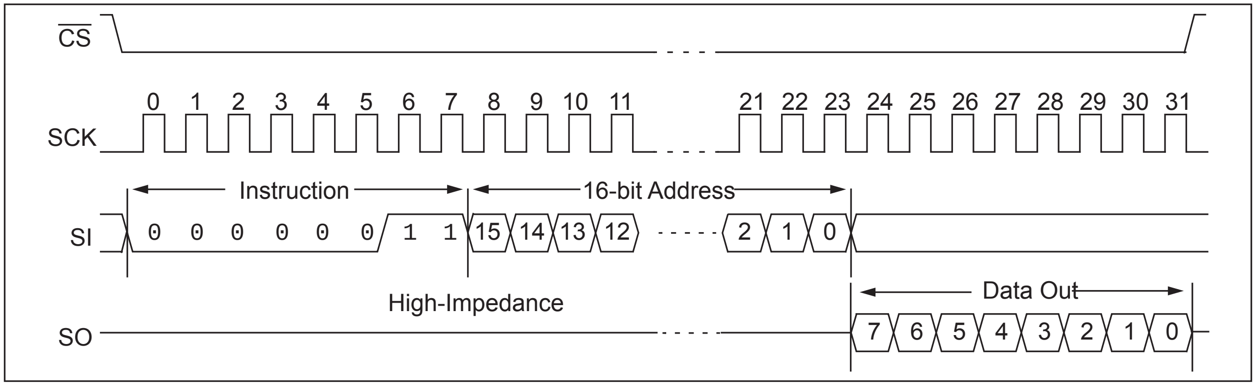


FIGURE 3-2: BYTE WRITE SEQUENCE

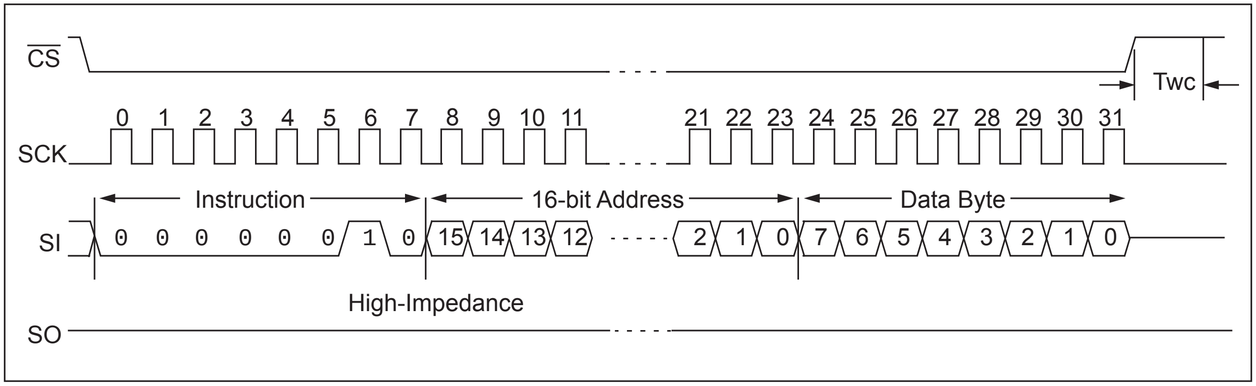
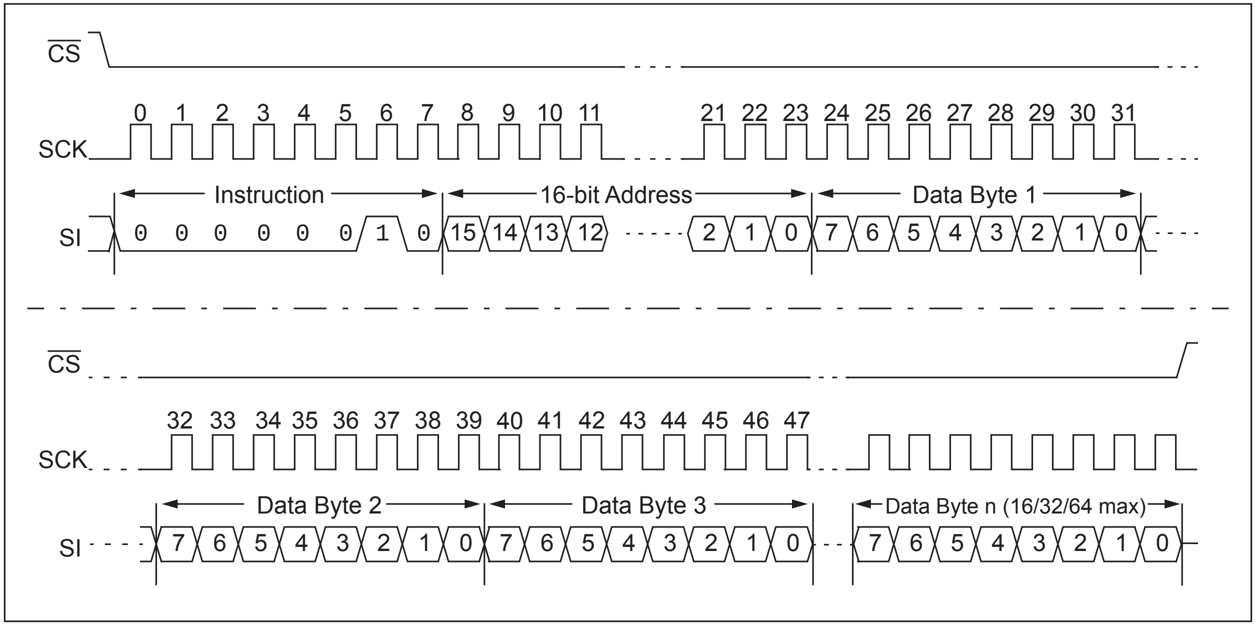


FIGURE 3-3: PAGE WRITE SEQUENCE



3.4 Write Enable (`WREN`) and Write Disable (`WRDI`)

The 25LCXXX contains a write enable latch. See Table 5-1 for the write-protect functionality matrix. This latch must be set before any write operation will be completed internally. The `WREN` instruction will set the latch, and the `WRDI` will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- `WRDI` instruction successfully executed
- `WRSR` instruction successfully executed
- `WRITE` instruction successfully executed

FIGURE 3-4: WRITE ENABLE SEQUENCE (`WREN`)

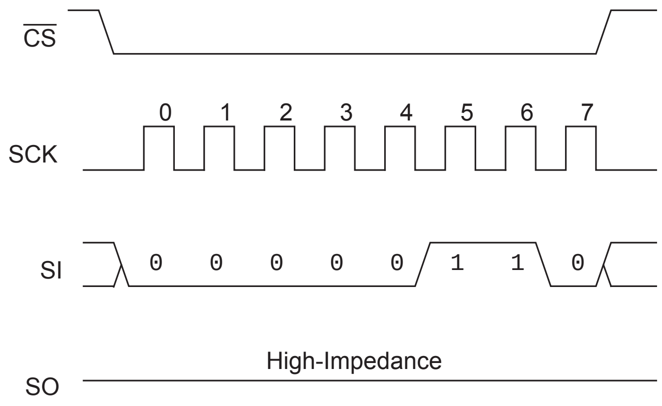
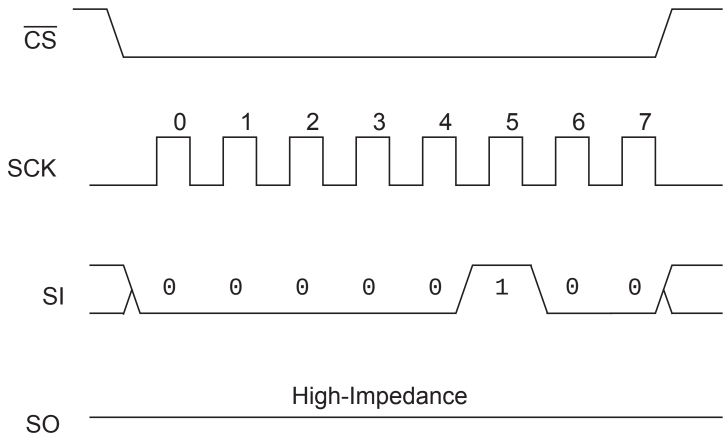


FIGURE 3-5: WRITE DISABLE SEQUENCE (`WRDI`)



3.5 Read STATUS Register Instruction (`RDSR`)

The Read STATUS Register instruction (`RDSR`) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as seen in Table 3-2.

TABLE 3-2: STATUS REGISTER

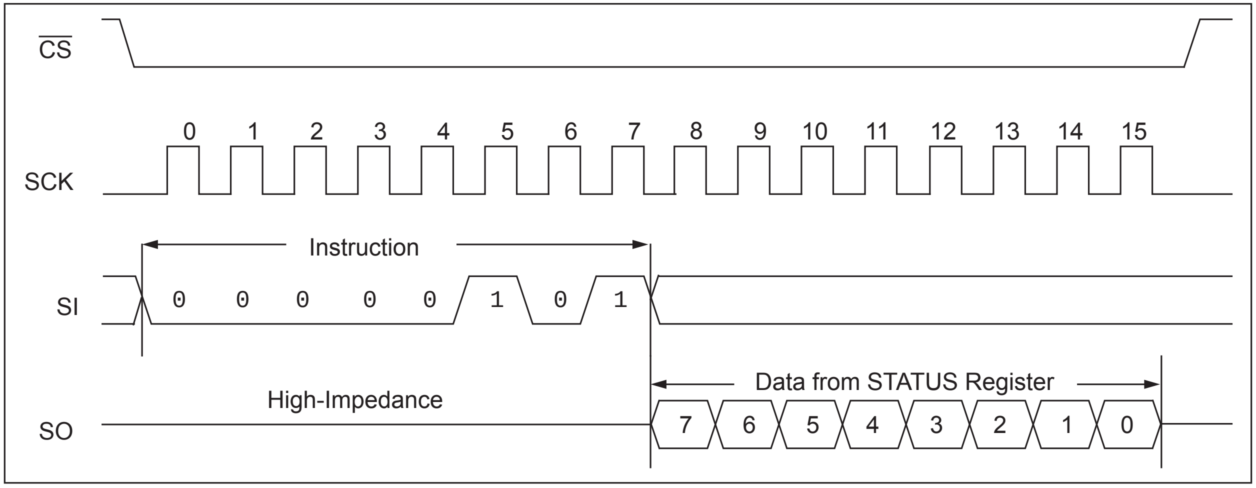
7	6	5	4	3	2	1	0
W/R	—	—	—	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

The **Write-In-Process (WIP)** bit indicates whether the 25LCXXX is busy with a write operation. When set to a ‘`1`’, a write is in progress, when set to a ‘`0`’, no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a ‘`1`’, the latch allows writes to the array, when set to a ‘`0`’, the latch prohibits writes to the array. The state of this bit can always be updated via the `WREN` or `WRDI` commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 3-4 and Figure 3-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the `WRSR` instruction. These bits are nonvolatile, and are shown in Table 3-3. See Figure 3-6 for the `RDSR` timing sequence.

FIGURE 3-6: READ STATUS REGISTER TIMING SEQUENCE (`RDSR`)



3.6 Write Status Register Instruction (`WRSR`)

The Write STATUS Register instruction (`WRSR`) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 3-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two or all four of the segments of the array. The partitioning is controlled as shown in Table 3-3.

The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{\text{WP}}$ pin. The Write-Protect ($\overline{\text{WP}}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{\text{WP}}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{\text{WP}}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 5-1 for a matrix of functionality on the WPEN bit. See Figure 3-7 for the `WRSR` timing sequence.

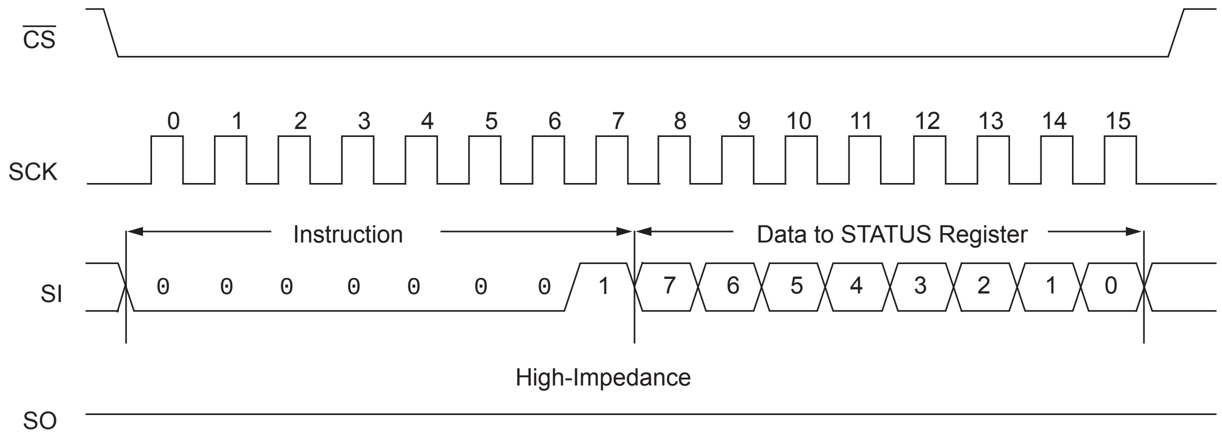
TABLE 3-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected	Array Addresses Unprotected
0	0	None	All
0	1	Upper 1/4	Lower 3/4
1	0	Upper 1/2	Lower 1/2
1	1	All	None

TABLE 3-4: ARRAY PROTECTED ADDRESS LOCATIONS

Density	Upper 1/4	Upper 1/2	All
8K	300h-3FFh	200h-3FFh	000h-3FFh
16K	600h-7FFh	400h-7FFh	000h-7FFh
32K	C00h-FFFh	800h-FFFh	000h-FFFh
64K	1800h-1FFFh	1000h-1FFFh	0000h-1FFFh
128K	3000h-3FFFh	2000h-3FFFh	0000h-3FFFh
256K	6000h-7FFFh	4000h-7FFFh	0000h-7FFFh

FIGURE 3-7: WRITE STATUS REGISTER TIMING SEQUENCE (`WRSR`)



Note: An internal write cycle (T_{WC}) is initiated on the rising edge of $\overline{\text{CS}}$ after a valid write STATUS register sequence.

4.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{\text{CS}}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

5.0 POWER-ON STATE

The 25LCXXX powers on in the following state:

- The device is in low-power Standby mode ($\overline{\text{CS}} = 1$)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{\text{CS}}$ is required to enter active state

TABLE 5-1: WRITE-PROTECT FUNCTIONALITY MATRIX

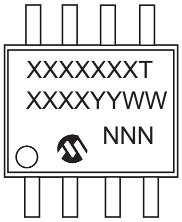
WEL (SR bit 1)	WPEN (SR bit 7)	$\overline{\text{WP}}$ (pin 3)	Protected Blocks	Unprotected Blocks	STATUS Register
`0`	`x`	`x`	Protected	Protected	Protected
`1`	`0`	`x`	Protected	Writable	Writable
`1`	`1`	`0` (low)	Protected	Writable	Protected
`1`	`1`	`1` (high)	Protected	Writable	Writable

`x` = don’t care

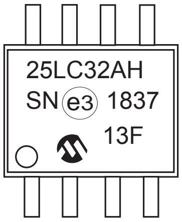
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

8-Lead SOIC



Example



Part Number	1st Line Marking Codes
	SOIC
25LC080C	25LC08CT
25LC080D	25LC08DT
25LC160C	25LC16CT
25LC160D	25LC16DT
25LC320A	25LC32AT
25LC640A	25L640AT
25LC128	25LC128T
25LC256	25LC256T

Note: T = Temperature Grade (H).

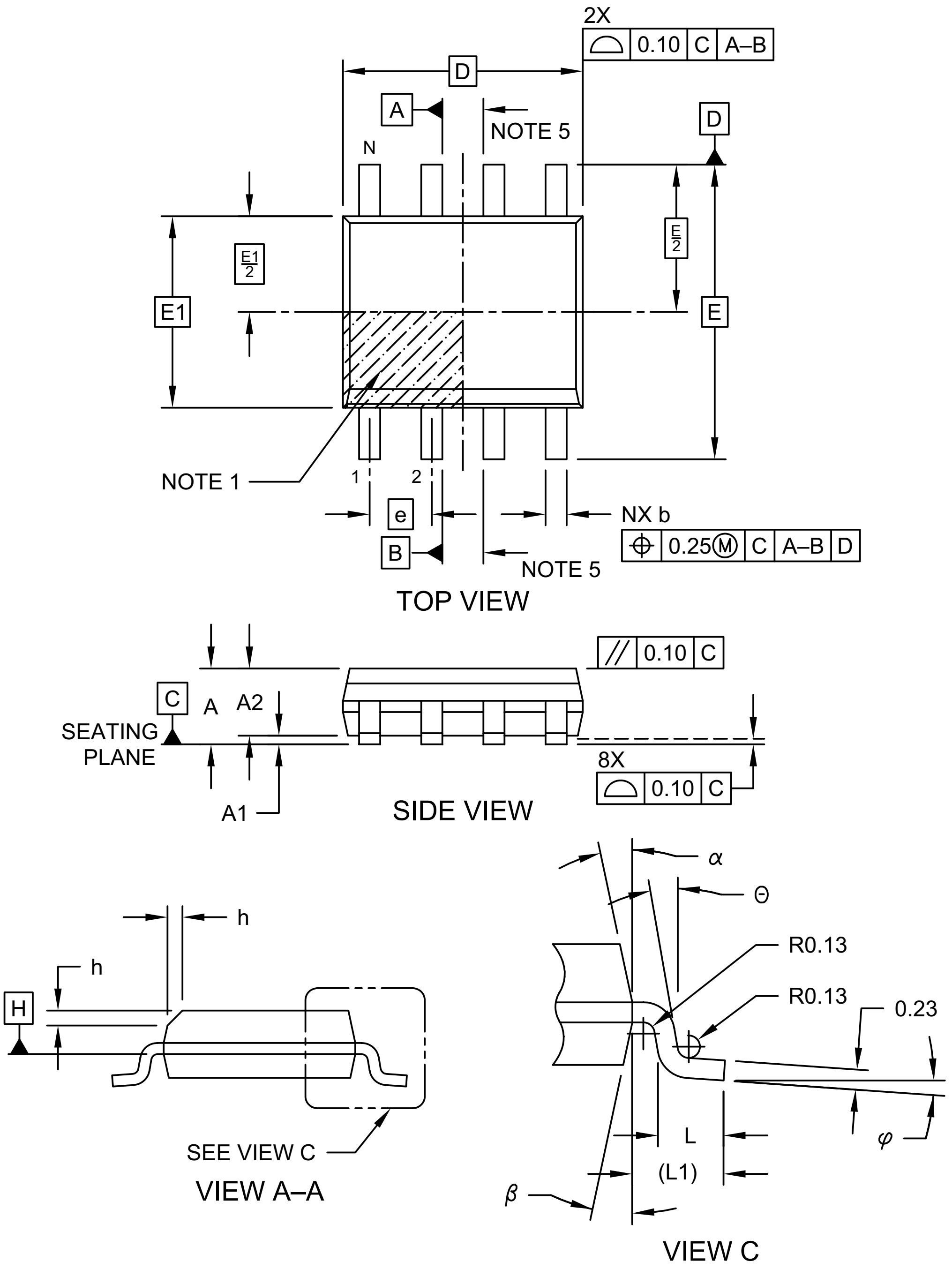
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	JEDEC designator for Matte Tin (Sn)
	*****	This package is RoHS compliant. The JEDEC designator (e3) can be found on the outer packaging for this package.

***** Custom marking available.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

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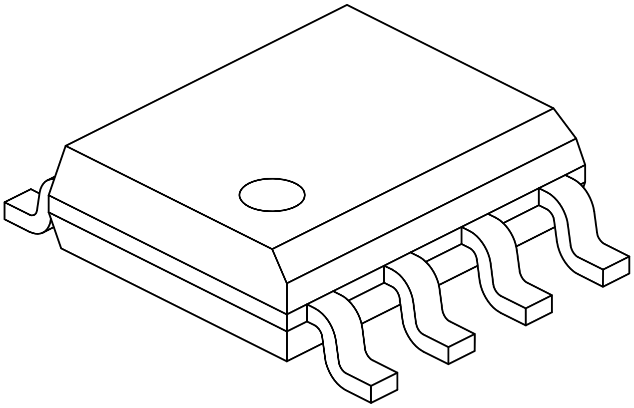


	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

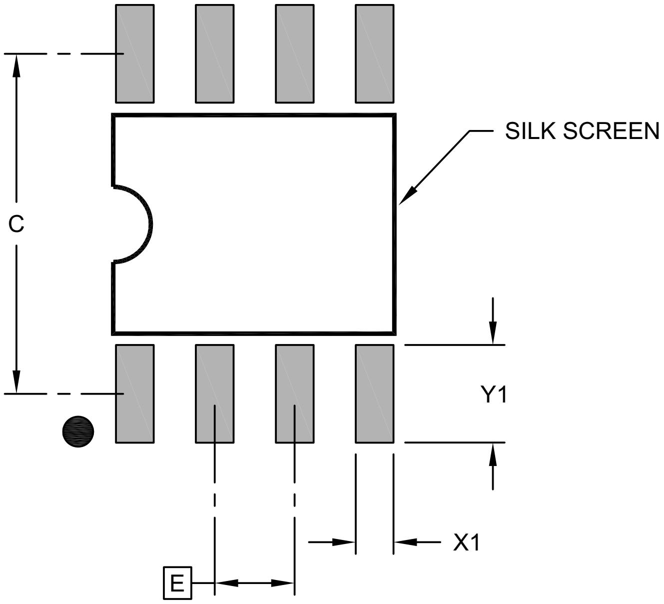
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

REVISION HISTORY

Revision A (01/2009)

Initial release of this document.

Revision B (04/2009)

Revised part number from 25XX to 25LCXXX; Added Note 1 to Electrical Characteristics.

Revision C (06/2009)

Revised Features: Endurance and Package; Revised Table 1-2, Para. 21.

Revision D (09/2018)

Removed Preliminary status; Minor typographical corrections.

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PART NO.	**[X]**(1)	**-X**	**/XX**
Device	**Tape and Reel Option**	**Temperature Range**	**Package**

Device:
25LC080C = 8-Kbit SPI Serial EEPROM
25LC080D = 8-Kbit SPI Serial EEPROM
25LC160C = 16-Kbit SPI Serial EEPROM
25LC160D = 16-Kbit SPI Serial EEPROM
25LC320A = 32-Kbit SPI Serial EEPROM
25LC640A = 64-Kbit SPI Serial EEPROM
25LC128 = 128-Kbit SPI Serial EEPROM
25LC256 = 256-Kbit SPI Serial EEPROM

Tape and Reel Option:
Blank = Standard packaging (tube or tray)
T = Tape and Reel(1)

Temperature Range:
H = -40°C to +150°C (Extended)

Package:
SN = 8-Lead Plastic Small Outline – Narrow, 3.90 mm Body SOIC

Examples:

a) 25LC080CT-H/SN = Tape and Reel, Extended Temp., 16-Byte Page, 2.5V-5.5V, SOIC package.
b) 25LC080D-H/SN = Extended Temp., 32-Byte Page, 2.5V-5.5V, SOIC package.
c) 25LC160CT-H/SN = Tape and Reel, Extended Temp. 16-Byte Page, 2.5V-5.5V, SOIC Package.
d) 25LC160D-H/SN = Extended Temp., 32-Byte Page, 2.5V-5.5V, SOIC Package.
e) 25LC320AT-H/SN = Tape and Reel, Extended Temp. 32-Byte Page, 2.5V-5.5V, SOIC Package.
f) 25LC640A-H/SN = Extended Temp. 32-Byte Page, 2.5V-5.5V, SOIC Package.
g) 25LC128T-H/SN = Tape and Reel, Extended Temp. 64-Byte Page, 2.5V-5.5V, SOIC Package.
h) 25LC256-H/SN = Extended Temp. 64-Byte Page, 2.5V-5.5V, SOIC Package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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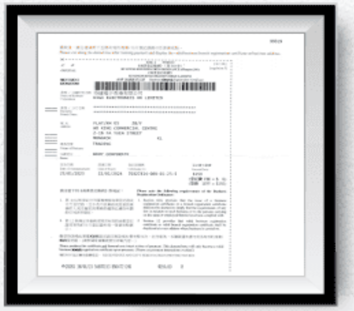

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