

A54SX32-1TQG144M Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|---|
| DiGi Electronics Part Number | A54SX32-1TQG144M-DG |
| Manufacturer | Microchip Technology |
| Manufacturer Product Number | A54SX32-1TQG144M |
| Description | IC FPGA 113 I/O 144TQFP |
| Detailed Description | SX Field Programmable Gate Array (FPGA) IC 113 144-LQFP |

This model A54SX32-1TQG144M is available at DiGi Electronics.

DiGi Electronics offers a global database of semiconductor and electronic component datasheets.

We welcome your inquiries regarding pricing, lead time, or other product-related questions.

 [Request a Quote](#)

 [Datasheet Search](#)



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

A54SX32-1TQG144M

Series:

SX

DiGi-Electronics Programmable:

Not Verified

Number of I/O:

113

Voltage - Supply:

3V ~ 3.6V, 4.75V ~ 5.25V

Operating Temperature:

-55°C ~ 125°C (TC)

Supplier Device Package:

144-TQFP (20x20)

Manufacturer:

Microchip Technology

Product Status:

Active

Number of LABs/CLBs:

2880

Number of Gates:

48000

Mounting Type:

Surface Mount

Package / Case:

144-LQFP

Base Product Number:

A54SX32

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A001A2C



SX-A Family FPGAs



Leading-Edge Performance

- 250 MHz System Performance
- 350 MHz Internal Performance

Specifications

- 12,000 to 108,000 Available System Gates
- Up to 360 User-Programmable I/O Pins
- Up to 2,012 Dedicated Flip-Flops
- 0.22 μ / 0.25 μ CMOS Process Technology

Features

- Hot-Swap Compliant I/Os
- Power-Up/Down Friendly (No Sequencing Required for Supply Voltages)
- 66 MHz PCI Compliant
- Nonvolatile, Single-Chip Solution

- Configurable I/O Support for 3.3 V / 5 V PCI, 5 V TTL, 3.3 V LVTTL, 2.5 V LVCMOS2
- 2.5 V, 3.3 V, and 5 V Mixed-Voltage Operation with 5 V Input Tolerance and 5 V Drive Strength
- Devices Support Multiple Temperature Grades
- Configurable Weak-Resistor Pull-Up or Pull-Down for I/O at Power-Up
- Individual Output Slew Rate Control
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary-Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft

Table 1 • SX-A Product Profile

| Device | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|---------------------------|------------------|---------------------|---------------------|---------------------|
| Capacity | | | | |
| Typical Gates | 8,000 | 16,000 | 32,000 | 72,000 |
| System Gates | 12,000 | 24,000 | 48,000 | 108,000 |
| Logic Modules | 768 | 1,452 | 2,880 | 6,036 |
| Combinatorial Cells | 512 | 924 | 1,800 | 4,024 |
| Dedicated Flip-Flops | 256 | 528 | 1,080 | 2,012 |
| Maximum Flip-Flops | 512 ¹ | 990 | 1,980 | 4,024 |
| Maximum User I/Os | 130 | 180 | 249 | 360 |
| Global Clocks | 3 | 3 | 3 | 3 |
| Quadrant Clocks | 0 | 0 | 0 | 4 |
| Boundary Scan Testing | Yes | Yes | Yes | Yes |
| 3.3 V / 5 V PCI | Yes | Yes | Yes | Yes |
| Input Set-Up (External) | 0 ns | 0 ns | 0 ns | 0 ns |
| Speed Grades ² | -F, Std, -1, -2 | -F, Std, -1, -2, -3 | -F, Std, -1, -2, -3 | -F, Std, -1, -2, -3 |
| Temperature Grades | C, I, A, M | C, I, A, M | C, I, A, M | C, I, A, M |
| Package (by pin count) | | | | |
| PQFP | 208 | 208 | 208 | 208 |
| TQFP | 100, 144 | 100, 144 | 100, 144, 176 | - |
| PBGA | - | - | 329 | - |
| FBGA | 144 | 144, 256 | 144, 256, 484 | 256, 484 |
| CQFP | - | - | 208, 256 | 208, 256 |

Notes:

1. A maximum of 512 registers is possible if all 512 C cells are used to build an additional 256 registers.
2. All -3 speed grades have been discontinued.

Ordering Information



Notes:

- For more information about the CQFP package options, refer to the [HiRel SX-A datasheet](#).
- All -3 speed grades have been discontinued.

Device Resources

| Device | User I/Os (Including Clock Buffers) | | | | | | | |
|----------|-------------------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| | 208-Pin PQFP | 100-Pin TQFP | 144-Pin TQFP | 176-Pin TQFP | 329-Pin PBGA | 144-Pin FBGA | 256-Pin FBGA | 484-Pin FBGA |
| A54SX08A | 130 | 81 | 113 | – | – | 111 | – | – |
| A54SX16A | 175 | 81 | 113 | – | – | 111 | 180 | – |
| A54SX32A | 174 | 81 | 113 | 147 | 249 | 111 | 203 | 249 |
| A54SX72A | 171 | – | – | – | – | – | 203 | 360 |

Notes: Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

Temperature Grade Offering

| Package | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|---------|----------|----------|----------|----------|
| PQ208 | C,I,A,M | C,I,A,M | C,I,A,M | C,I,A,M |
| TQ100 | C,I,A,M | C,I,A,M | C,I,A,M | |
| TQ144 | C,I,A,M | C,I,A,M | C,I,A,M | |
| TQ176 | | | C,I,M | |
| BG329 | | | C,I,M | |
| FG144 | C,I,A,M | C,I,A,M | C,I,A,M | |
| FG256 | | C,I,A,M | C,I,A,M | C,I,A,M |
| FG484 | | | C,I,M | C,I,A,M |
| CQ208 | | | C,M,B | C,M,B |
| CQ256 | | | C,M,B | C,M,B |

Notes:

1. C = Commercial
2. I = Industrial
3. A = Automotive
4. M = Military
5. B = MIL-STD-883 Class B
6. For more information regarding automotive products, refer to the [SX-A Automotive Family FPGAs datasheet](#).
7. For more information regarding Mil-Temp and ceramic packages, refer to the [HiRel SX-A Family FPGAs datasheet](#).

Speed Grade and Temperature Grade Matrix

| | F | Std | -1 | -2 | -3 |
|--------------|---|-----|----|----|--------------|
| Commercial | ✓ | ✓ | ✓ | ✓ | Discontinued |
| Industrial | | ✓ | ✓ | ✓ | Discontinued |
| Automotive | | ✓ | | | |
| Military | | ✓ | ✓ | | |
| MIL-STD-883B | | ✓ | ✓ | | |

Notes:

1. For more information regarding automotive products, refer to the [SX-A Automotive Family FPGAs datasheet](#).
2. For more information regarding Mil-Temp and ceramic packages, refer to the [HiRel SX-A Family FPGAs datasheet](#).

Contact your Actel Sales representative for more information on availability.

Table of Contents

General Description

| | |
|------------------------------------|------|
| Introduction | 1-1 |
| SX-A Family Architecture | 1-1 |
| Other Architectural Features | 1-7 |
| Programming | 1-13 |
| Related Documents | 1-14 |
| Pin Description | 1-15 |

Detailed Specifications

| | |
|--|------|
| Operating Conditions | 2-1 |
| Typical SX-A Standby Current | 2-1 |
| Electrical Specifications | 2-2 |
| PCI Compliance for the SX-A Family | 2-3 |
| Thermal Characteristics | 2-11 |
| SX-A Timing Model | 2-14 |
| Sample Path Calculations | 2-14 |
| Output Buffer Delays | 2-15 |
| AC Test Loads | 2-15 |
| Input Buffer Delays | 2-16 |
| C-Cell Delays | 2-16 |
| Cell Timing Characteristics | 2-16 |
| Timing Characteristics | 2-17 |
| Temperature and Voltage Derating Factors | 2-17 |
| Timing Characteristics | 2-18 |

Package Pin Assignments

| | |
|--------------------|------|
| 208-Pin PQFP | 3-1 |
| 100-Pin TQFP | 3-5 |
| 144-Pin TQFP | 3-8 |
| 176-Pin TQFP | 3-11 |
| 329-Pin PBGA | 3-14 |
| 144-Pin FBGA | 3-18 |
| 256-Pin FBGA | 3-21 |
| 484-Pin FBGA | 3-26 |

Datasheet Information

| | |
|--|-----|
| List of Changes | 4-1 |
| Datasheet Categories | 4-3 |
| International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR) | 4-3 |

General Description

Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements

SX-A Family FPGAs

Logic Module Design

The SX-A family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000

different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.



Figure 1-2 • R-Cell

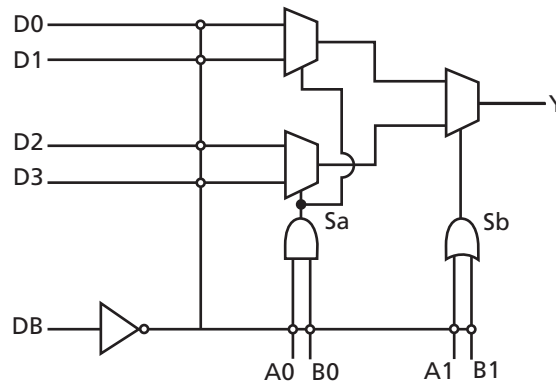


Figure 1-3 • C-Cell

Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable

interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.



Figure 1-4 • Cluster Organization

SX-A Family FPGAs



Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters



Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinatorial logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA

and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Devices* and *Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

Table 1-1 • SX-A Clock Resources

| | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|--|----------|----------|----------|----------|
| Routed Clocks (CLKA, CLKB) | 2 | 2 | 2 | 2 |
| Hardwired Clocks (HCLK) | 1 | 1 | 1 | 1 |
| Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD) | 0 | 0 | 0 | 4 |

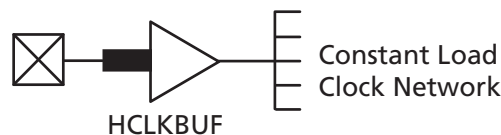


Figure 1-7 • SX-A HCLK Clock Buffer

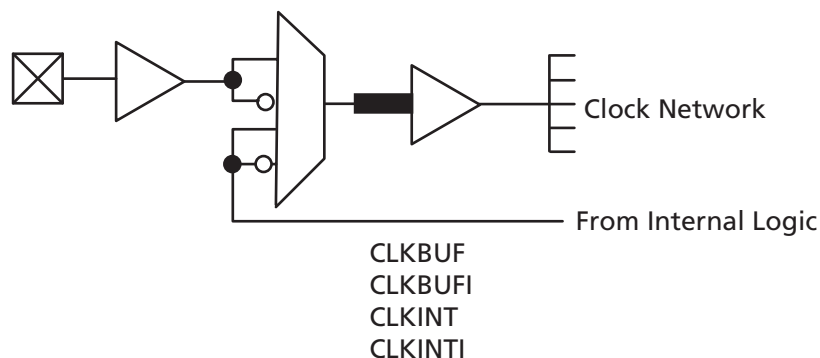


Figure 1-8 • SX-A Routed Clock Buffer

SX-A Family FPGAs



Figure 1-9 • SX-A QCLK Architecture



Figure 1-10 • A54SX72A Routed Clock and QCLK Buffer

Other Architectural Features

Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using 0.22 μ / 0.25 μ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).



Figure 1-11 • FuseLock

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than V_{CC1} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and V_{CC1} is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 k Ω that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before V_{CCA} reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

SX-A Family FPGAs

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions

are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, [Actel SX-A and RT54SX-5 Devices in Hot-Swap and Cold-Sparing Applications](#).

Table 1-2 • I/O Features

| Function | Description |
|-----------------------------------|--|
| Input Buffer Threshold Selections | <ul style="list-style-type: none"> 5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only) |
| Flexible Output Driver | <ul style="list-style-type: none"> 5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only) |
| Output Buffer | <p>"Hot-Swap" Capability (3.3 V PCI is not hot swappable)</p> <ul style="list-style-type: none"> I/O on an unpowered device does not sink current Can be used for "cold-sparing" <p>Selectable on an individual I/O basis</p> <p>Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.</p> |
| Power-Up | <p>Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate)</p> <p>Enables deterministic power-up of device</p> <p>V_{CCA} and V_{CCI} can be powered in any order</p> |

Table 1-3 • I/O Characteristics for All I/O Configurations

| | Hot Swappable | Slew Rate Control | Power-Up Resistor |
|----------------------|---------------|--|----------------------|
| TTL, LVTTTL, LVCMOS2 | Yes | Yes. Only affects falling edges of outputs | Pull-up or pull-down |
| 3.3 V PCI | No | No. High slew rate only | Pull-up or pull-down |
| 5 V PCI | Yes | No. High slew rate only | Pull-up or pull-down |

Table 1-4 • Power-Up Time at which I/Os Become Active

| Supply Ramp Rate | 0.25 V/ μ s | 0.025 V/ μ s | 5 V/ms | 2.5 V/ms | 0.5 V/ms | 0.25 V/ms | 0.1 V/ms | 0.025 V/ms |
|------------------|-----------------|------------------|--------|----------|----------|-----------|----------|------------|
| Units | μ s | μ s | ms | ms | ms | ms | ms | ms |
| A54SX08A | 10 | 96 | 0.34 | 0.65 | 2.7 | 5.4 | 12.9 | 50.8 |
| A54SX16A | 10 | 100 | 0.36 | 0.62 | 2.5 | 4.7 | 11.0 | 41.6 |
| A54SX32A | 10 | 100 | 0.46 | 0.74 | 2.8 | 5.2 | 12.1 | 47.2 |
| A54SX72A | 10 | 100 | 0.41 | 0.67 | 2.6 | 5.0 | 12.1 | 47.2 |

Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.



Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

| Pin | Function |
|-------------------------|--|
| Reserve JTAG | Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS) |
| Reserve JTAG Test Reset | Regular I/O or JTAG reset with an internal pull-up |
| Reserve Probe | Keeps pins from being used or regular I/O |

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CC} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • Boundary-Scan Pin Configurations and Functions

| Mode | Designer "Reserve JTAG" Selection | TAP Controller State |
|---------------------|-----------------------------------|-----------------------------|
| Dedicated (JTAG) | Checked | Any |
| Flexible (User I/O) | Unchecked | Test-Logic-Reset |
| Flexible (JTAG) | Unchecked | Any EXCEPT Test-Logic-Reset |

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

SX-A Family FPGAs**JTAG Instructions**

Table 1-7 lists the supported instructions with the corresponding IR codes for SX-A devices.

Table 1-8 lists the codes returned after executing the IDCODE instruction for SX-A devices. Note that bit 0 is always '1'. Bits 11-1 are always '02F', which is the Actel manufacturer code.

Table 1-7 • JTAG Instruction Code

| Instructions (IR4:IR0) | Binary Code |
|------------------------|-------------|
| EXTEST | 00000 |
| SAMPLE/PRELOAD | 00001 |
| INTEST | 00010 |
| USERCODE | 00011 |
| IDCODE | 00100 |
| HighZ | 01110 |
| CLAMP | 01111 |
| Diagnostic | 10000 |
| BYPASS | 11111 |
| Reserved | All others |

Table 1-8 • JTAG Instruction Code

| Device | Process | Revision | Bits 31-28 | Bits 27-12 |
|----------|-------------|----------|------------|------------|
| A54SX08A | 0.22 μ | 0 | 8, 9 | 40B4, 42B4 |
| | | 1 | A, B | 40B4, 42B4 |
| A54SX16A | 0.22 μ | 0 | 9 | 40B8, 42B8 |
| | | 1 | B | 40B8, 42B8 |
| | 0.25 μ | 1 | B | 22B8 |
| A54SX32A | 0.2 2 μ | 0 | 9 | 40BD, 42BD |
| | | 1 | B | 40BD, 42BD |
| | 0.25 μ | 1 | B | 22BD |
| A54SX72A | 0.22 μ | 0 | 9 | 40B2, 42B2 |
| | | 1 | B | 40B2, 42B2 |
| | 0.25 μ | 1 | B | 22B2 |

Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

When selecting the **Reserve Probe Pin** box as shown in [Figure 1-12 on page 1-9](#), direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. [Table 1-9](#) summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved)

| JTAG Mode | TRST ¹ | Security Fuse Programmed | PRA, PRB ² | TDI, TCK, TDO ² |
|-----------|-------------------|--------------------------|-----------------------|----------------------------|
| Dedicated | Low | No | User I/O ³ | JTAG Disabled |
| | High | No | Probe Circuit Outputs | JTAG I/O |
| Flexible | Low | No | User I/O ³ | User I/O ³ |
| | | Yes | Probe Circuit Secured | Probe Circuit Secured |
| | High | No | Probe Circuit Outputs | JTAG I/O |

Notes:

1. If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.
2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.

SX-A Family FPGAs

SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the

PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70 Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.



Figure 1-13 • Probe Setup

Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, ModelSim® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User's Guide*.

Related Documents

Application Notes

Global Clock Networks in Actel's Antifuse Devices

http://www.actel.com/documents/GlobalClk_AN.pdf

Using A54SX72A and RT54SX72S Quadrant Clocks

http://www.actel.com/documents/QCLK_AN.pdf

Implementation of Security in Actel Antifuse FPGAs

http://www.actel.com/documents/Antifuse_Security_AN.pdf

Actel eX, SX-A, and RTSX-S I/Os

http://www.actel.com/documents/AntifuseIO_AN.pdf

Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications

http://www.actel.com/documents/HotSwapColdSparing_AN.pdf

Programming Antifuse Devices

http://www.actel.com/documents/AntifuseProgram_AN.pdf

Datasheets

HiRel SX-A Family FPGAs

http://www.actel.com/documents/HRSXA_DS.pdf

SX-A Automotive Family FPGAs

http://www.actel.com/documents/SXA_Auto_DS.pdf

User's Guides

Silicon Sculptor User's Guide

http://www.actel.com/documents/SiliSculptII_Sculpt3_ug.pdf

Pin Description

CLKA/B, I/O Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND Ground

Low supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC No Connection

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to [Table 1-6 on page 1-9](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to [Table 1-6 on page 1-9](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to [Table 1-6 on page 1-9](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user I/O when checksum is complete.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to [Table 1-6 on page 1-9](#)). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See [Table 2-2 on page 2-1](#). All V_{CCI} power pins in the device should be connected.

V_{CCA} Supply Voltage

Supply voltage for array. See [Table 2-2 on page 2-1](#). All V_{CCA} power pins in the device should be connected.

Detailed Specifications

Operating Conditions

Table 2-1 • Absolute Maximum Ratings

| Symbol | Parameter | Limits | Units |
|-----------|------------------------------|---------------------------|-------|
| V_{CCI} | DC Supply Voltage for I/Os | -0.3 to +6.0 | V |
| V_{CCA} | DC Supply Voltage for Arrays | -0.3 to +3.0 | V |
| V_I | Input Voltage | -0.5 to +5.75 | V |
| V_O | Output Voltage | -0.5 to + V_{CCI} + 0.5 | V |
| T_{STG} | Storage Temperature | -65 to +150 | °C |

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".

Table 2-2 • Recommended Operating Conditions

| Parameter | Commercial | Industrial | Units |
|--|--------------|--------------|-------|
| Temperature Range | 0 to +70 | -40 to +85 | °C |
| 2.5 V Power Supply Range (V_{CCA} and V_{CCI}) | 2.25 to 2.75 | 2.25 to 2.75 | V |
| 3.3 V Power Supply Range (V_{CCI}) | 3.0 to 3.6 | 3.0 to 3.6 | V |
| 5 V Power Supply Range (V_{CCI}) | 4.75 to 5.25 | 4.75 to 5.25 | V |

Typical SX-A Standby Current

Table 2-3 • Typical Standby Current for SX-A at 25°C with $V_{CCA} = 2.5$ V

| Product | $V_{CCI} = 2.5$ V | $V_{CCI} = 3.3$ V | $V_{CCI} = 5$ V |
|----------|-------------------|-------------------|-----------------|
| A54SX08A | 0.8 mA | 1.0 mA | 2.9 mA |
| A54SX16A | 0.8 mA | 1.0 mA | 2.9 mA |
| A54SX32A | 0.9 mA | 1.0 mA | 3.0 mA |
| A54SX72A | 3.6 mA | 3.8 mA | 4.5 mA |

Table 2-4 • Supply Voltages

| V_{CCA} | V_{CCI} * | Maximum Input Tolerance | Maximum Output Drive |
|-----------|-------------|-------------------------|----------------------|
| 2.5 V | 2.5 V | 5.75 V | 2.7 V |
| 2.5 V | 3.3 V | 5.75 V | 3.6 V |
| 2.5 V | 5 V | 5.75 V | 5.25 V |

Note: *3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.

SX-A Family FPGAs

Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

| Symbol | Parameter | | Commercial | | Industrial | | Units |
|----------------------------------|---|---------------------------|----------------------|------|----------------------|------|-------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | V _{CC1} = Minimum V _I = V _{IH} or V _{IL} | (I _{OH} = -1 mA) | 0.9 V _{CC1} | | 0.9 V _{CC1} | | V |
| | V _{CC1} = Minimum V _I = V _{IH} or V _{IL} | (I _{OH} = -8 mA) | 2.4 | | 2.4 | | V |
| V _{OL} | V _{CC1} = Minimum V _I = V _{IH} or V _{IL} | (I _{OL} = 1 mA) | 0.4 | | 0.4 | | V |
| | V _{CC1} = Minimum V _I = V _{IH} or V _{IL} | (I _{OL} = 12 mA) | 0.4 | | 0.4 | | V |
| V _{IL} | Input Low Voltage | | 0.8 | | 0.8 | | V |
| V _{IH} | Input High Voltage | | 2.0 | 5.75 | 2.0 | 5.75 | V |
| I _{IL} /I _{IH} | Input Leakage Current, V _{IN} = V _{CC1} or GND | | -10 | 10 | -10 | 10 | μA |
| I _{OZ} | Tristate Output Leakage Current | | -10 | 10 | -10 | 10 | μA |
| t _R , t _F | Input Transition Time t _R , t _F | | 10 | | 10 | | ns |
| C _{IO} | I/O Capacitance | | 10 | | 10 | | pF |
| I _{CC} | Standby Current | | 10 | | 20 | | mA |
| IV Curve* | Can be derived from the IBIS model on the web. | | | | | | |

Note: *The IBIS model can be found at <http://www.actel.com/download/ibis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

| Symbol | Parameter | | Commercial | | Industrial | | Units |
|----------------------------------|---|-----------------------------|------------|------|------------|------|-------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | V _{DD} = MIN, V _I = V _{IH} or V _{IL} | (I _{OH} = -100 μA) | 2.1 | | 2.1 | | V |
| | V _{DD} = MIN, V _I = V _{IH} or V _{IL} | (I _{OH} = -1 mA) | 2.0 | | 2.0 | | V |
| | V _{DD} = MIN, V _I = V _{IH} or V _{IL} | (I _{OH} = -2 mA) | 1.7 | | 1.7 | | V |
| V _{OL} | V _{DD} = MIN, V _I = V _{IH} or V _{IL} | (I _{OL} = 100 μA) | 0.2 | | 0.2 | | V |
| | V _{DD} = MIN, V _I = V _{IH} or V _{IL} | (I _{OL} = 1 mA) | 0.4 | | 0.4 | | V |
| | V _{DD} = MIN, V _I = V _{IH} or V _{IL} | (I _{OL} = 2 mA) | 0.7 | | 0.7 | | V |
| V _{IL} | Input Low Voltage, V _{OUT} ≤ V _{VOL(max)} | | -0.3 | 0.7 | -0.3 | 0.7 | V |
| V _{IH} | Input High Voltage, V _{OUT} ≥ V _{VOH(min)} | | 1.7 | 5.75 | 1.7 | 5.75 | V |
| I _{IL} /I _{IH} | Input Leakage Current, V _{IN} = V _{CC1} or GND | | -10 | 10 | -10 | 10 | μA |
| I _{OZ} | Tristate Output Leakage Current, V _{OUT} = V _{CC1} or GND | | -10 | 10 | -10 | 10 | μA |
| t _R , t _F | Input Transition Time t _R , t _F | | 10 | | 10 | | ns |
| C _{IO} | I/O Capacitance | | 10 | | 10 | | pF |
| I _{CC} | Standby Current | | 10 | | 20 | | mA |
| IV Curve* | Can be derived from the IBIS model on the web. | | | | | | |

Note: *The IBIS model can be found at <http://www.actel.com/download/ibis/default.aspx>.

PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

| Symbol | Parameter | Condition | Min. | Max. | Units |
|------------------|---|-------------------------------|------|------|-------|
| V _{CCA} | Supply Voltage for Array | | 2.25 | 2.75 | V |
| V _{CCI} | Supply Voltage for I/Os | | 4.75 | 5.25 | V |
| V _{IH} | Input High Voltage | | 2.0 | 5.75 | V |
| V _{IL} | Input Low Voltage | | -0.5 | 0.8 | V |
| I _{IH} | Input High Leakage Current ¹ | V _{IN} = 2.7 | - | 70 | μA |
| I _{IL} | Input Low Leakage Current ¹ | V _{IN} = 0.5 | - | -70 | μA |
| V _{OH} | Output High Voltage | I _{OUT} = -2 mA | 2.4 | - | V |
| V _{OL} | Output Low Voltage ² | I _{OUT} = 3 mA, 6 mA | - | 0.55 | V |
| C _{IN} | Input Pin Capacitance ³ | | - | 10 | pF |
| C _{CLK} | CLK Pin Capacitance | | 5 | 12 | pF |

Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

SX-A Family FPGAs

Table 2-8 • AC Specifications (5 V PCI Operation)

| Symbol | Parameter | Condition | Min. | Max. | Units |
|--------------|------------------------|--|---------------------------------|--------------------|-------|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 1.4$ ¹ | -44 | - | mA |
| | | $1.4 \leq V_{OUT} < 2.4$ ^{1,2} | $(-44 + (V_{OUT} - 1.4)/0.024)$ | - | mA |
| | | $3.1 < V_{OUT} < V_{CCI}$ ^{1,3} | - | EQ 2-1 on page 2-5 | - |
| | (Test Point) | $V_{OUT} = 3.1$ ³ | - | -142 | mA |
| $I_{OL(AC)}$ | Switching Current Low | $V_{OUT} \geq 2.2$ ¹ | 95 | - | mA |
| | | $2.2 > V_{OUT} > 0.55$ ¹ | $(V_{OUT}/0.023)$ | - | mA |
| | | $0.71 > V_{OUT} > 0$ ^{1,3} | - | EQ 2-2 on page 2-5 | - |
| | (Test Point) | $V_{OUT} = 0.71$ ³ | - | 206 | mA |
| I_{CL} | Low Clamp Current | $-5 < V_{IN} \leq -1$ | $-25 + (V_{IN} + 1)/0.015$ | - | mA |
| $slew_R$ | Output Rise Slew Rate | 0.4 V to 2.4 V load ⁴ | 1 | 5 | V/ns |
| $slew_F$ | Output Fall Slew Rate | 2.4 V to 0.4 V load ⁴ | 1 | 5 | V/ns |

Notes:

1. Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

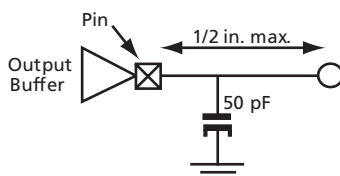


Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

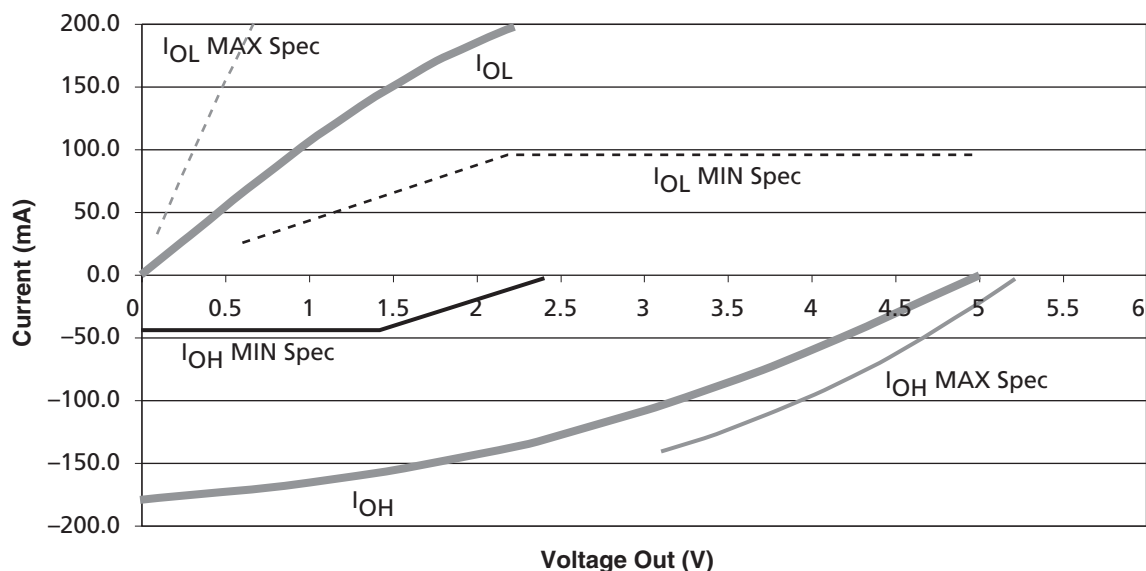


Figure 2-1 • 5 V PCI V/I Curve for SX-A Family

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for $V_{CCI} > V_{OUT} > 3.1V$

EQ 2-1

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for $0V < V_{OUT} < 0.71V$

EQ 2-2

Table 2-9 • DC Specifications (3.3 V PCI Operation)

| Symbol | Parameter | Condition | Min. | Max. | Units |
|-----------|------------------------------------|-------------------------|--------------|-----------------|---------|
| V_{CCA} | Supply Voltage for Array | | 2.25 | 2.75 | V |
| V_{CCI} | Supply Voltage for I/Os | | 3.0 | 3.6 | V |
| V_{IH} | Input High Voltage | | $0.5V_{CCI}$ | $V_{CCI} + 0.5$ | V |
| V_{IL} | Input Low Voltage | | -0.5 | $0.3V_{CCI}$ | V |
| I_{IPU} | Input Pull-up Voltage ¹ | | $0.7V_{CCI}$ | - | V |
| I_{IL} | Input Leakage Current ² | $0 < V_{IN} < V_{CCI}$ | -10 | +10 | μA |
| V_{OH} | Output High Voltage | $I_{OUT} = -500 \mu A$ | $0.9V_{CCI}$ | - | V |
| V_{OL} | Output Low Voltage | $I_{OUT} = 1,500 \mu A$ | - | $0.1V_{CCI}$ | V |
| C_{IN} | Input Pin Capacitance ³ | | - | 10 | pF |
| C_{CLK} | CLK Pin Capacitance | | 5 | 12 | pF |

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

SX-A Family FPGAs

Table 2-10 • AC Specifications (3.3 V PCI Operation)

| Symbol | Parameter | Condition | Min. | Max. | Units |
|--------------|------------------------|---|-------------------------------------|--------------------|-------|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 0.3V_{CCI}^1$ | $-12V_{CCI}$ | – | mA |
| | | $0.3V_{CCI} \leq V_{OUT} < 0.9V_{CCI}^1$ | $(-17.1(V_{CCI} - V_{OUT}))$ | – | mA |
| | | $0.7V_{CCI} < V_{OUT} < V_{CCI}^{1,2}$ | – | EQ 2-3 on page 2-7 | – |
| | (Test Point) | $V_{OUT} = 0.7V_{CC}^2$ | – | $-32V_{CCI}$ | mA |
| $I_{OL(AC)}$ | Switching Current Low | $V_{CCI} > V_{OUT} \geq 0.6V_{CCI}^1$ | $16V_{CCI}$ | – | mA |
| | | $0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}^1$ | $(26.7V_{OUT})$ | – | mA |
| | | $0.18V_{CCI} > V_{OUT} > 0^{1,2}$ | – | EQ 2-4 on page 2-7 | – |
| | (Test Point) | $V_{OUT} = 0.18V_{CC}^2$ | – | $38V_{CCI}$ | mA |
| I_{CL} | Low Clamp Current | $-3 < V_{IN} \leq -1$ | $-25 + (V_{IN} + 1)/0.015$ | – | mA |
| I_{CH} | High Clamp Current | $V_{CCI} + 4 > V_{IN} \geq V_{CCI} + 1$ | $25 + (V_{IN} - V_{CCI} - 1)/0.015$ | – | mA |
| $slew_R$ | Output Rise Slew Rate | $0.2V_{CCI} - 0.6V_{CCI}$ load ³ | 1 | 4 | V/ns |
| $slew_F$ | Output Fall Slew Rate | $0.6V_{CCI} - 0.2V_{CCI}$ load ³ | 1 | 4 | V/ns |

Notes:

1. Refer to the V/I curves in Figure 2-2 on page 2-7. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 2-2 on page 2-7. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.



Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.



Figure 2-2 • 3.3 V PCI V/I Curve for SX-A Family

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

for $0.7 V_{CCI} < V_{OUT} < V_{CCI}$

EQ 2-3

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

for $0V < V_{OUT} < 0.18 V_{CCI}$

EQ 2-4

Power Dissipation

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

A complete power evaluation should be performed early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Dissipation

The total power dissipation for the SX-A family is the sum of the DC power dissipation and the AC power dissipation:

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 2-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. An estimation of DC power dissipation under typical conditions is given by:

$$P_{\text{DC}} = I_{\text{standby}} * V_{\text{CCA}}$$

EQ 2-6

Note: For other combinations of temperature and voltage settings, refer to the [eX, SX-A and RT54SX-5 Power Calculator](#).

AC Power Dissipation

The power dissipation of the SX-A family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined as follows:

$$P_{\text{AC}} = P_{\text{C-cells}} + P_{\text{R-cells}} + P_{\text{CLKA}} + P_{\text{CLKB}} + P_{\text{HCLK}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 2-7

or:

$$P_{\text{AC}} = V_{\text{CCA}}^2 * [(m * C_{\text{EQCM}} * f_m)_{\text{C-cells}} + (m * C_{\text{EQSM}} * f_m)_{\text{R-cells}} + (n * C_{\text{EQI}} * f_n)_{\text{Input Buffer}} + (p * (C_{\text{EQO}} + C_L) * f_p)_{\text{Output Buffer}} + (0.5 * (q_1 * C_{\text{EQCR}} * f_{q1}) + (r_1 * f_{q1}))_{\text{CLKA}} + (0.5 * (q_2 * C_{\text{EQCR}} * f_{q2}) + (r_2 * f_{q2}))_{\text{CLKB}} + (0.5 * (s_1 * C_{\text{EQHV}} * f_{s1}) + (C_{\text{EQHF}} * f_{s1}))_{\text{HCLK}]$$

EQ 2-8

Where:

- C_{EQCM} = Equivalent capacitance of combinatorial modules (C-cells) in pF
 C_{EQSM} = Equivalent capacitance of sequential modules (R-Cells) in pF
 C_{EQI} = Equivalent capacitance of input buffers in pF
 C_{EQO} = Equivalent capacitance of output buffers in pF
 C_{EQCR} = Equivalent capacitance of CLKA/B in pF
 C_{EQHV} = Variable capacitance of HCLK in pF
 C_{EQHF} = Fixed capacitance of HCLK in pF
 C_L = Output lead capacitance in pF
 f_m = Average logic module switching rate in MHz
 f_n = Average input buffer switching rate in MHz
 f_p = Average output buffer switching rate in MHz
 f_{q1} = Average CLKA rate in MHz
 f_{q2} = Average CLKB rate in MHz
 f_{s1} = Average HCLK rate in MHz
 m = Number of logic modules switching at f_m
 n = Number of input buffers switching at f_n
 p = Number of output buffers switching at f_p
 q_1 = Number of clock loads on CLKA
 q_2 = Number of clock loads on CLKB
 r_1 = Fixed capacitance due to CLKA
 r_2 = Fixed capacitance due to CLKB
 s_1 = Number of clock loads on HCLK
 x = Number of I/Os at logic low
 y = Number of I/Os at logic high

Table 2-11 • CEQ Values for SX-A Devices

| | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|--|-----------------|-----------------|-----------------|-----------------|
| Combinatorial modules (C_{EQCM}) | 1.70 pF | 2.00 pF | 2.00 pF | 1.80 pF |
| Sequential modules (C_{EQSM}) | 1.50 pF | 1.50 pF | 1.30 pF | 1.50 pF |
| Input buffers (C_{EQI}) | 1.30 pF | 1.30 pF | 1.30 pF | 1.30 pF |
| Output buffers (C_{EQO}) | 7.40 pF | 7.40 pF | 7.40 pF | 7.40 pF |
| Routed array clocks (C_{EQCR}) | 1.05 pF | 1.05 pF | 1.05 pF | 1.05 pF |
| Dedicated array clocks – variable (C_{EQHV}) | 0.85 pF | 0.85 pF | 0.85 pF | 0.85 pF |
| Dedicated array clocks – fixed (C_{EQHF}) | 30.00 pF | 55.00 pF | 110.00 pF | 240.00 pF |
| Routed array clock A (r_1) | 35.00 pF | 50.00 pF | 90.00 pF | 310.00 pF |

Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules

Inputs Switching (n) = Number inputs/4

Outputs Switching (p) = Number of outputs/4

CLKA Loads (q1) = 20% of R-cells

CLKB Loads (q2) = 20% of R-cells

Load Capacitance (CL) = 35 pF

Average Logic Module Switching Rate (fm) = f/10

Average Input Switching Rate (fn) = f/5

Average Output Switching Rate (fp) = f/10

Average CLKA Rate (fq1) = f/2

Average CLKB Rate (fq2) = f/2

Average HCLK Rate (fs1) = f

HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the [eX, SX-A and RT54SX-S Power Calculator](#) worksheet.

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 2-9

$$\theta_{JA} = \frac{T_C - T_A}{P}$$

EQ 2-10

Where:

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_C = Ambient temperature
- P = total power dissipated by the device

Table 2-12 • Package Thermal Characteristics

| Package Type | Pin Count | θ_{JC} | θ_{JA} | | | Units |
|---|-----------|---------------|---------------|-------------------------|-------------------------|-------|
| | | | Still Air | 1.0 m/s 200 ft./min. | 2.5 m/s 500 ft./min. | |
| Thin Quad Flat Pack (TQFP) | 100 | 14 | 33.5 | 27.4 | 25 | °C/W |
| Thin Quad Flat Pack (TQFP) | 144 | 11 | 33.5 | 28 | 25.7 | °C/W |
| Thin Quad Flat Pack (TQFP) | 176 | 11 | 24.7 | 19.9 | 18 | °C/W |
| Plastic Quad Flat Pack (PQFP) ¹ | 208 | 8 | 26.1 | 22.5 | 20.8 | °C/W |
| Plastic Quad Flat Pack (PQFP) with Heat Spreader ² | 208 | 3.8 | 16.2 | 13.3 | 11.9 | °C/W |
| Plastic Ball Grid Array (PBGA) | 329 | 3 | 17.1 | 13.8 | 12.8 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 144 | 3.8 | 26.9 | 22.9 | 21.5 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 256 | 3.8 | 26.6 | 22.8 | 21.5 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 484 | 3.2 | 18 | 14.7 | 13.6 | °C/W |

Notes:

- The A54SX08A PQ208 has no heat spreader.
- The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$$\theta_{JA} = 17.1^{\circ}\text{C/W} \text{ is taken from Table 2-12 on page 2-11}$$

$$T_A = 125^{\circ}\text{C} \text{ is the maximum limit of ambient (from the datasheet)}$$

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{17.1^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

$$T_J = 110^{\circ}\text{C}$$

$$T_A = 70^{\circ}\text{C}$$

From the datasheet:

$$\theta_{JA} = 18.0^{\circ}\text{C/W}$$

$$\theta_{JC} = 3.2^{\circ}\text{C/W}$$

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{18.0^{\circ}\text{C/W}} = 2.22 \text{ W}$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{3.00 \text{ W}} = 13.33^{\circ}\text{C/W}$$

EQ 2-13

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 2-14

where:

$$\theta_{CS} = 0.37^{\circ}C/W$$

= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$$\theta_{SA} = \text{thermal resistance of the heat sink in } ^{\circ}C/W$$

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33^{\circ}C/W - 3.20^{\circ}C/W - 0.37^{\circ}C/W$$

$$\theta_{SA} = 9.76^{\circ}C/W$$

A heat sink with a thermal resistance of $9.76^{\circ}C/W$ or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

SX-A Timing Model



Note: *Values shown for A54SX72A, -2, worst-case commercial conditions at 5 V PCI with standard place-and-route.

Figure 2-3 • SX-A Timing Model

Sample Path Calculations

Hardwired Clock

$$\begin{aligned} \text{External Setup} &= (t_{IN\text{YH}} + t_{RD1} + t_{SUD}) - t_{HCKH} \\ &= 0.6 + 0.3 + 0.8 - 1.8 = -0.1 \text{ ns} \\ \text{Clock-to-Out (Pad-to-Pad)} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.8 + 0.8 + 0.3 + 3.9 = 6.8 \text{ ns} \end{aligned}$$

Routed Clock

$$\begin{aligned} \text{External Setup} &= (t_{IN\text{YH}} + t_{RD1} + t_{SUD}) - t_{RCKH} \\ &= 0.6 + 0.3 + 0.8 - 3.0 = -1.3 \text{ ns} \\ \text{Clock-to-Out (Pad-to-Pad)} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 3.0 + 0.8 + 0.3 + 3.9 = 8.0 \text{ ns} \end{aligned}$$

Output Buffer Delays

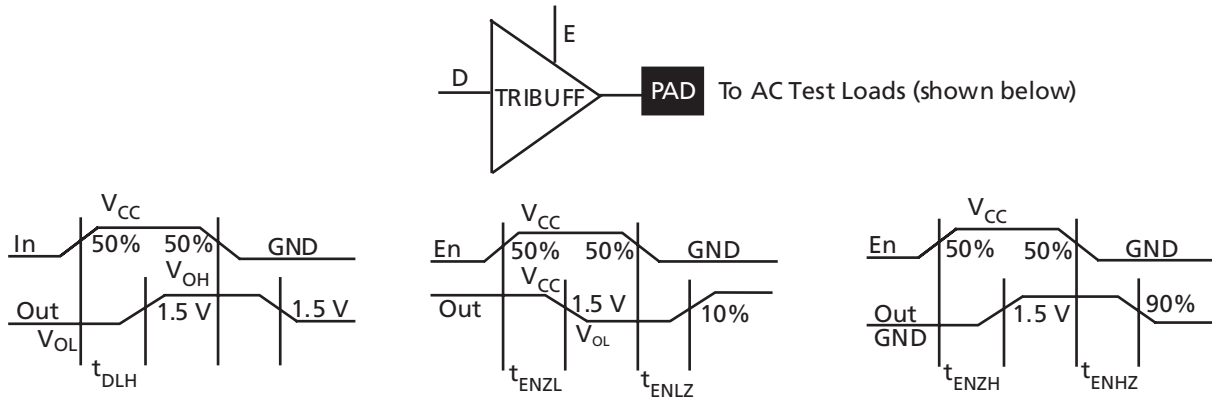


Figure 2-4 • Output Buffer Delays

AC Test Loads

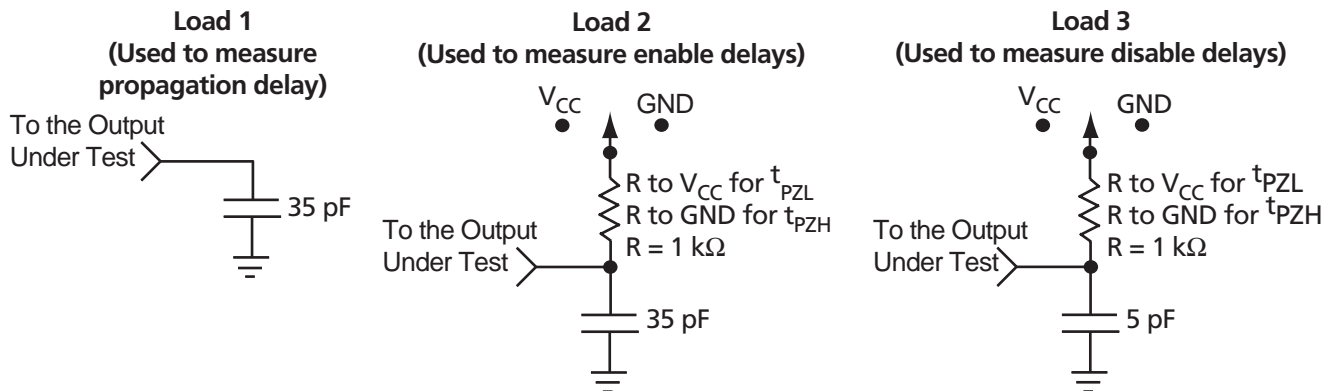


Figure 2-5 • AC Test Loads

Input Buffer Delays



Figure 2-6 • Input Buffer Delays

C-Cell Delays



Figure 2-7 • C-Cell Delays

Cell Timing Characteristics



Figure 2-8 • Flip-Flops

Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 2-13 • Temperature and Voltage Derating Factors
(Normalized to Worst-Case Commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 2.25\text{ V}$)

| V_{CCA} | Junction Temperature (T_J) | | | | | | |
|-----------|--------------------------------|---------------------|-------------------|--------------------|--------------------|--------------------|---------------------|
| | -55°C | -40°C | 0°C | 25°C | 70°C | 85°C | 125°C |
| 2.250 V | 0.79 | 0.80 | 0.87 | 0.89 | 1.00 | 1.04 | 1.14 |
| 2.500 V | 0.74 | 0.75 | 0.82 | 0.83 | 0.94 | 0.97 | 1.07 |
| 2.750 V | 0.68 | 0.69 | 0.75 | 0.77 | 0.87 | 0.90 | 0.99 |

SX-A Family FPGAs

Timing Characteristics

Table 2-14 • A54SX08A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|---------------------------------------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| C-Cell Propagation Delays¹ | | | | | | | | | | |
| t_{PD} | Internal Array Module | | 0.9 | | 1.1 | | 1.2 | | 1.7 | ns |
| Predicted Routing Delays² | | | | | | | | | | |
| t_{DC} | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| t_{FC} | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| t_{RD1} | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| t_{RD2} | FO = 2 Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| t_{RD3} | FO = 3 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| t_{RD4} | FO = 4 Routing Delay | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| t_{RD8} | FO = 8 Routing Delay | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| t_{RD12} | FO = 12 Routing Delay | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| R-Cell Timing | | | | | | | | | | |
| t_{RCO} | Sequential Clock-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| t_{CLR} | Asynchronous Clear-to-Q | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| t_{PRESET} | Asynchronous Preset-to-Q | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| t_{SUD} | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| t_{HD} | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t_{WASYN} | Asynchronous Pulse Width | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| $t_{RECA SYN}$ | Asynchronous Recovery Time | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| t_{HASYN} | Asynchronous Hold Time | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| t_{MPW} | Clock Pulse Width | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| Input Module Propagation Delays | | | | | | | | | | |
| t_{INYH} | Input Data Pad to Y High 2.5 V LVCMOS | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| t_{INYL} | Input Data Pad to Y Low 2.5 V LVCMOS | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| t_{INYH} | Input Data Pad to Y High 3.3 V PCI | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| t_{INYL} | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| t_{INYH} | Input Data Pad to Y High 3.3 V LVTTTL | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| t_{INYL} | Input Data Pad to Y Low 3.3 V LVTTTL | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-14 • A54SX08A Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|----------------------------------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{INYH} | Input Data Pad to Y High 5 V PCI | | 0.5 | | 0.6 | | 0.7 | | 0.9 | ns |
| t_{INYL} | Input Data Pad to Y Low 5 V PCI | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| t_{INYH} | Input Data Pad to Y High 5 V TTL | | 0.5 | | 0.6 | | 0.7 | | 0.9 | ns |
| t_{INYL} | Input Data Pad to Y Low 5 V TTL | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| Input Module Predicted Routing Delays² | | | | | | | | | | |
| t_{IRD1} | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| t_{IRD2} | FO = 2 Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| t_{IRD3} | FO = 3 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| t_{IRD4} | FO = 4 Routing Delay | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| t_{IRD8} | FO = 8 Routing Delay | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| t_{IRD12} | FO = 12 Routing Delay | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

SX-A Family FPGAs

Table 2-15 • **A54SX08A Timing Characteristics**
 (Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.4 | | 1.6 | | 1.8 | | 2.6 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| t_{HP} | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| f_{HMAX} | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| Routed Array Clock Networks | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |

Table 2-16 • A54SX08A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.6 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 2.2 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.4 | | 0.5 | | 0.5 | | 0.8 | ns |
| t_{HP} | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| f_{HMAX} | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| Routed Array Clock Networks | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |

SX-A Family FPGAs

Table 2-17 • **A54SX08A Timing Characteristics**
 (Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.3 | | 1.5 | | 2.3 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.4 | | 2.0 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.4 | | 0.4 | | 0.5 | | 0.8 | ns |
| t_{HP} | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| f_{HMAX} | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| Routed Array Clock Networks | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 0.8 | | 1.0 | | 1.1 | | 1.5 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |

Table 2-18 • A54SX08A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|----------------------------------|----------|-------|----------|-------|------------|-------|----------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 2.5 V LVCMOS Output Module Timing^{1,2} | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 3.9 | | 4.4 | | 5.2 | | 7.2 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 3.0 | | 3.4 | | 3.9 | | 5.5 | ns |
| t_{DHLS} | Data-to-Pad High to Low—low slew | | 13.3 | | 15.1 | | 17.7 | | 24.8 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| t_{ENZLS} | Data-to-Pad, Z to L—low slew | | 13.7 | | 15.5 | | 18.2 | | 25.5 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 3.9 | | 4.4 | | 5.2 | | 7.2 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.3 | | 4.7 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 3.0 | | 3.4 | | 3.9 | | 5.5 | ns |
| d_{TLH}^3 | Delta Low to High | | 0.037 | | 0.043 | | 0.051 | | 0.071 | ns/pF |
| d_{THL}^3 | Delta High to Low | | 0.017 | | 0.023 | | 0.023 | | 0.037 | ns/pF |
| d_{THLS}^3 | Delta High to Low—low slew | | 0.06 | | 0.071 | | 0.086 | | 0.117 | ns/pF |

Note:

- Delays based on 35 pF loading.
- The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$

where C_{load} is the load capacitance driven by the I/O in pF

$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

SX-A Family FPGAs

Table 2-19 • A54SX08A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|----------|-------|----------|-------|------------|-------|----------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 3.3 V PCI Output Module Timing¹ | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 2.2 | | 2.4 | | 2.9 | | 4.0 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.2 | | 2.4 | | 2.9 | | 4.0 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| d_{TLH}^2 | Delta Low to High | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| d_{THL}^2 | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| 3.3 V LVTTL Output Module Timing³ | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| t_{DHLS} | Data-to-Pad High to Low—low slew | | 10.4 | | 11.8 | | 13.8 | | 19.3 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| t_{ENZLS} | Enable-to-Pad, Z to L—low slew | | 18.9 | | 21.3 | | 25.4 | | 34.9 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 3 | | 3.4 | | 4 | | 5.6 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 3 | | 3.3 | | 3.9 | | 5.5 | ns |
| d_{TLH}^2 | Delta Low to High | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| d_{THL}^2 | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| d_{THLS}^2 | Delta High to Low—low slew | | 0.053 | | 0.067 | | 0.073 | | 0.107 | ns/pF |

Notes:

- Delays based on 10 pF loading and 25 Ω resistance.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

Table 2-20 • A54SX08A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|----------|-------|----------|-------|------------|-------|----------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 5 V PCI Output Module Timing¹ | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| d_{TLH}^2 | Delta Low to High | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| d_{THL}^2 | Delta High to Low | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| 5 V TTL Output Module Timing³ | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| t_{DHLS} | Data-to-Pad High to Low—low slew | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| t_{ENZLS} | Enable-to-Pad, Z to L—low slew | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| d_{TLH} | Delta Low to High | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| d_{THL} | Delta High to Low | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| d_{THLS} | Delta High to Low—low slew | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

Notes:

- Delays based on 50 pF loading.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

SX-A Family FPGAs

Table 2-21 • A54SX16A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|---------------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| C-Cell Propagation Delays² | | | | | | | | | | | | |
| t_{PD} | Internal Array Module | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | | ns |
| Predicted Routing Delays³ | | | | | | | | | | | | |
| t_{DC} | FO = 1 Routing Delay, Direct Connect | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | ns |
| t_{FC} | FO = 1 Routing Delay, Fast Connect | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| t_{RD1} | FO = 1 Routing Delay | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | | ns |
| t_{RD2} | FO = 2 Routing Delay | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | | ns |
| t_{RD3} | FO = 3 Routing Delay | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | | ns |
| t_{RD4} | FO = 4 Routing Delay | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | | ns |
| t_{RD8} | FO = 8 Routing Delay | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| t_{RD12} | FO = 12 Routing Delay | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | | ns |
| R-Cell Timing | | | | | | | | | | | | |
| t_{RCO} | Sequential Clock-to-Q | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| t_{CLR} | Asynchronous Clear-to-Q | 0.5 | | 0.6 | | 0.6 | | 0.8 | | 1.0 | | ns |
| t_{PRESET} | Asynchronous Preset-to-Q | 0.7 | | 0.8 | | 0.8 | | 1.0 | | 1.4 | | ns |
| t_{SUD} | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| t_{HD} | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t_{WASYN} | Asynchronous Pulse Width | 1.3 | | 1.5 | | 1.6 | | 1.9 | | 2.7 | | ns |
| t_{REASYN} | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| t_{HASYN} | Asynchronous Removal Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| t_{MPW} | Clock Minimum Pulse Width | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| Input Module Propagation Delays | | | | | | | | | | | | |
| t_{INYH} | Input Data Pad to Y High 2.5 V LVCMOS | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | | ns |
| t_{INYL} | Input Data Pad to Y Low 2.5 V LVCMOS | 0.8 | | 0.9 | | 1.0 | | 1.1 | | 1.6 | | ns |
| t_{INYH} | Input Data Pad to Y High 3.3 V PCI | 0.5 | | 0.6 | | 0.6 | | 0.7 | | 1.0 | | ns |
| t_{INYL} | Input Data Pad to Y Low 3.3 V PCI | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| t_{INYH} | Input Data Pad to Y High 3.3 V LVTTTL | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| t_{INYL} | Input Data Pad to Y Low 3.3 V LVTTTL | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | | ns |

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-21 • A54SX16A Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|----------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{INYH} | Input Data Pad to Y High 5 V PCI | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | ns |
| t_{INYL} | Input Data Pad to Y Low 5 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| t_{INYH} | Input Data Pad to Y High 5 V TTL | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | ns |
| t_{INYL} | Input Data Pad to Y Low 5 V TTL | | 0.7 | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| Input Module Predicted Routing Delays² | | | | | | | | | | | | |
| t_{IRD1} | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| t_{IRD2} | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| t_{IRD3} | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| t_{IRD4} | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| t_{IRD8} | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 0.8 | | 2.5 | ns |
| t_{IRD12} | FO = 12 Routing Delay | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 3.6 | ns |

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

SX-A Family FPGAs

Table 2-22 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.8 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.2 | | 1.5 | | 2.2 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.7 | ns |
| t_{HP} | Minimum Period | 2.8 | | 3.4 | | 3.8 | | 4.4 | | 6.0 | | ns |
| f_{HMAX} | Maximum Frequency | | 357 | | 294 | | 263 | | 227 | | 167 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

Note: *All -3 speed grades have been discontinued.

Table 2-23 • A54SX16A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.8 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.2 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.6 | ns |
| t_{HP} | Minimum Period | 2.8 | | 3.4 | | 3.8 | | 4.4 | | 6.0 | | ns |
| f_{HMAX} | Maximum Frequency | | 357 | | 294 | | 263 | | 227 | | 167 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.1 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.4 | | 1.7 | | 2.3 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

Note: *All -3 speed grades have been discontinued.

SX-A Family FPGAs

Table 2-24 • A54SX16A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.8 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.2 | | 1.5 | | 2.2 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.7 | ns |
| t_{HP} | Minimum Period | 2.8 | | 3.4 | | 3.8 | | 4.4 | | 6.0 | | ns |
| f_{HMAX} | Maximum Frequency | | 357 | | 294 | | 263 | | 227 | | 167 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

Note: *All -3 speed grades have been discontinued.

Table 2-25 • A54SX16A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 2.5 V LVCMOS Output Module Timing^{2, 3} | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | 3.4 | | 3.9 | | 4.5 | | 5.2 | | 7.3 | | ns |
| t_{DHL} | Data-to-Pad High to Low | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | | ns |
| t_{DHLS} | Data-to-Pad High to Low—low slew | 11.6 | | 13.4 | | 15.2 | | 17.9 | | 25.0 | | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | | ns |
| t_{ENZLS} | Data-to-Pad, Z to L—low slew | 11.8 | | 13.7 | | 15.5 | | 18.2 | | 25.5 | | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | 3.4 | | 3.9 | | 4.5 | | 5.2 | | 7.3 | | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.7 | | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | | ns |
| d_{TLH}^4 | Delta Low to High | 0.031 | | 0.037 | | 0.043 | | 0.051 | | 0.071 | | ns/pF |
| d_{THL}^4 | Delta High to Low | 0.017 | | 0.017 | | 0.023 | | 0.023 | | 0.037 | | ns/pF |
| d_{THLS}^4 | Delta High to Low—low slew | 0.057 | | 0.06 | | 0.071 | | 0.086 | | 0.117 | | ns/pF |

Note:

1. All -3 speed grades have been discontinued.
2. Delays based on 35 pF loading.
3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$

where C_{load} is the load capacitance driven by the I/O in pF

$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

SX-A Family FPGAs

Table 2-26 • A54SX16A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|-----------------------|-------|----------|-------|----------|-------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 3.3 V PCI Output Module Timing² | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | 2.0 | 2.3 | 2.6 | 3.1 | 4.3 | ns | | | | | |
| t_{DHL} | Data-to-Pad High to Low | 2.2 | 2.5 | 2.8 | 3.3 | 4.6 | ns | | | | | |
| t_{ENZL} | Enable-to-Pad, Z to L | 1.4 | 1.7 | 1.9 | 2.2 | 3.1 | ns | | | | | |
| t_{ENZH} | Enable-to-Pad, Z to H | 2.0 | 2.3 | 2.6 | 3.1 | 4.3 | ns | | | | | |
| t_{ENLZ} | Enable-to-Pad, L to Z | 2.5 | 2.8 | 3.2 | 3.8 | 5.3 | ns | | | | | |
| t_{ENHZ} | Enable-to-Pad, H to Z | 2.2 | 2.5 | 2.8 | 3.3 | 4.6 | ns | | | | | |
| d_{TLH}^3 | Delta Low to High | 0.025 | 0.03 | 0.03 | 0.04 | 0.045 | ns/pF | | | | | |
| d_{THL}^3 | Delta High to Low | 0.015 | 0.015 | 0.015 | 0.015 | 0.025 | ns/pF | | | | | |
| 3.3 V LVTTL Output Module Timing⁴ | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | 2.8 | 3.2 | 3.6 | 4.3 | 6.0 | ns | | | | | |
| t_{DHL} | Data-to-Pad High to Low | 2.7 | 3.1 | 3.5 | 4.1 | 5.7 | ns | | | | | |
| t_{DHLS} | Data-to-Pad High to Low—low slew | 9.5 | 10.9 | 12.4 | 14.6 | 20.4 | ns | | | | | |
| t_{ENZL} | Enable-to-Pad, Z to L | 2.2 | 2.6 | 2.9 | 3.4 | 4.8 | ns | | | | | |
| t_{ENZLS} | Enable-to-Pad, Z to L—low slew | 15.8 | 18.9 | 21.3 | 25.4 | 34.9 | ns | | | | | |
| t_{ENZH} | Enable-to-Pad, Z to H | 2.8 | 3.2 | 3.6 | 4.3 | 6.0 | ns | | | | | |
| t_{ENLZ} | Enable-to-Pad, L to Z | 2.9 | 3.3 | 3.7 | 4.4 | 6.2 | ns | | | | | |
| t_{ENHZ} | Enable-to-Pad, H to Z | 2.7 | 3.1 | 3.5 | 4.1 | 5.7 | ns | | | | | |
| d_{TLH}^3 | Delta Low to High | 0.025 | 0.03 | 0.03 | 0.04 | 0.045 | ns/pF | | | | | |
| d_{THL}^3 | Delta High to Low | 0.015 | 0.015 | 0.015 | 0.015 | 0.025 | ns/pF | | | | | |
| d_{THLS}^3 | Delta High to Low—low slew | 0.053 | 0.053 | 0.067 | 0.073 | 0.107 | ns/pF | | | | | |

Notes:

- All -3 speed grades have been discontinued.
- Delays based on 10 pF loading and 25 Ω resistance.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

Table 2-27 • A54SX16A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|-----------------------|-------|----------|-------|----------|-------|------------|-------|----------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 5 V PCI Output Module Timing² | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 3.0 | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| d_{TLH}^3 | Delta Low to High | | 0.016 | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| d_{THL}^3 | Delta High to Low | | 0.026 | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| 5 V TTL Output Module Timing⁴ | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| t_{DHLS} | Data-to-Pad High to Low—low slew | | 6.7 | | 7.7 | | 8.7 | | 10.2 | | 14.3 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| t_{ENZLS} | Enable-to-Pad, Z to L—low slew | | 7.4 | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 1.9 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 3.6 | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 2.5 | | 2.9 | | 3.3 | | 3.9 | | 5.4 | ns |
| d_{TLH}^3 | Delta Low to High | | 0.014 | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| d_{THL}^3 | Delta High to Low | | 0.023 | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| d_{THLS}^3 | Delta High to Low—low slew | | 0.043 | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

Notes:

1. All -3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

SX-A Family FPGAs

Table 2-28 • A54SX32A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|---------------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| C-Cell Propagation Delays² | | | | | | | | | | | | |
| t_{PD} | Internal Array Module | 0.8 | | 0.9 | | 1.1 | | 1.2 | | 1.7 | | ns |
| Predicted Routing Delays³ | | | | | | | | | | | | |
| t_{DC} | FO = 1 Routing Delay, Direct Connect | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | ns |
| t_{FC} | FO = 1 Routing Delay, Fast Connect | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| t_{RD1} | FO = 1 Routing Delay | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | | ns |
| t_{RD2} | FO = 2 Routing Delay | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | | ns |
| t_{RD3} | FO = 3 Routing Delay | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | | ns |
| t_{RD4} | FO = 4 Routing Delay | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| t_{RD8} | FO = 8 Routing Delay | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| t_{RD12} | FO = 12 Routing Delay | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 3.6 | | ns |
| R-Cell Timing | | | | | | | | | | | | |
| t_{RCO} | Sequential Clock-to-Q | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| t_{CLR} | Asynchronous Clear-to-Q | 0.5 | | 0.6 | | 0.6 | | 0.8 | | 1.0 | | ns |
| t_{PRESET} | Asynchronous Preset-to-Q | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | | ns |
| t_{SUD} | Flip-Flop Data Input Set-Up | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| t_{HD} | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t_{WASYN} | Asynchronous Pulse Width | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| t_{REASYN} | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| t_{HASYN} | Asynchronous Removal Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| t_{MPW} | Clock Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| Input Module Propagation Delays | | | | | | | | | | | | |
| t_{INYH} | Input Data Pad to Y High 2.5 V LVCMOS | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| t_{INYL} | Input Data Pad to Y Low 2.5 V LVCMOS | 1.2 | | 1.3 | | 1.5 | | 1.8 | | 2.5 | | ns |
| t_{INYH} | Input Data Pad to Y High 3.3 V PCI | 0.5 | | 0.6 | | 0.6 | | 0.7 | | 1.0 | | ns |
| t_{INYL} | Input Data Pad to Y Low 3.3 V PCI | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| t_{INYH} | Input Data Pad to Y High 3.3 V LVTTTL | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.6 | | ns |
| t_{INYL} | Input Data Pad to Y Low 3.3 V LVTTTL | 1.4 | | 1.6 | | 1.8 | | 2.2 | | 3.0 | | ns |

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-28 • A54SX32A Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|----------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{INYH} | Input Data Pad to Y High 5 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| t_{INYL} | Input Data Pad to Y Low 5 V PCI | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| t_{INYH} | Input Data Pad to Y High 5 V TTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| t_{INYL} | Input Data Pad to Y Low 5 V TTL | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| Input Module Predicted Routing Delays³ | | | | | | | | | | | | |
| t_{IRD1} | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| t_{IRD2} | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| t_{IRD3} | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| t_{IRD4} | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| t_{IRD8} | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| t_{IRD12} | FO = 12 Routing Delay | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

SX-A Family FPGAs

Table 2-29 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.3 | ns |
| t_{HP} | Minimum Period | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| f_{HMAX} | Maximum Frequency | | 357 | | 313 | | 278 | | 238 | | 172 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.9 | | 3.4 | | 4.7 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.4 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.0 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |

Note: *All -3 speed grades have been discontinued.

Table 2-30 • A54SX32A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.3 | ns |
| t_{HP} | Minimum Period | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| f_{HMAX} | Maximum Frequency | | 357 | | 313 | | 278 | | 238 | | 172 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.3 | | 2.7 | | 3.1 | | 3.6 | | 5 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.9 | | 3.4 | | 4.7 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.1 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |

Note: *All -3 speed grades have been discontinued.

SX-A Family FPGAs

Table 2-31 • A54SX32A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.7 | | 1.9 | | 2.2 | | 2.6 | | 4.0 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.3 | ns |
| t_{HP} | Minimum Period | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| f_{HMAX} | Maximum Frequency | | 357 | | 313 | | 278 | | 238 | | 172 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.7 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.5 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.7 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.2 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

Note: *All -3 speed grades have been discontinued.

Table 2-32 • A54SX32A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|----------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 2.5 V LVCMOS Output Module Timing^{2,3} | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | 3.3 | | 3.8 | | 4.2 | | 5.0 | | 7.0 | | ns |
| t_{DHL} | Data-to-Pad High to Low | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | | ns |
| t_{DHLS} | Data-to-Pad High to Low—low slew | 11.1 | | 12.8 | | 14.5 | | 17.0 | | 23.8 | | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | | ns |
| t_{ENZLS} | Data-to-Pad, Z to L—low slew | 11.8 | | 13.7 | | 15.5 | | 18.2 | | 25.5 | | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | 3.3 | | 3.8 | | 4.2 | | 5.0 | | 7.0 | | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.7 | | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | | ns |
| d_{TLH}^4 | Delta Low to High | 0.031 | | 0.037 | | 0.043 | | 0.051 | | 0.071 | | ns/pF |
| d_{THL}^4 | Delta High to Low | 0.017 | | 0.017 | | 0.023 | | 0.023 | | 0.037 | | ns/pF |
| d_{THLS}^4 | Delta High to Low—low slew | 0.057 | | 0.06 | | 0.071 | | 0.086 | | 0.117 | | ns/pF |

Note:

1. All -3 speed grades have been discontinued.
2. Delays based on 35 pF loading.
3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$

where C_{load} is the load capacitance driven by the I/O in pF

$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

SX-A Family FPGAs

Table 2-33 • A54SX32A Timing Characteristics
 (Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|-----------------------|-------|----------|-------|----------|-------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 3.3 V PCI Output Module Timing² | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | 1.9 | 2.2 | 2.4 | 2.9 | 4.0 | ns | | | | | |
| t_{DHL} | Data-to-Pad High to Low | 2.0 | 2.3 | 2.6 | 3.1 | 4.3 | ns | | | | | |
| t_{ENZL} | Enable-to-Pad, Z to L | 1.4 | 1.7 | 1.9 | 2.2 | 3.1 | ns | | | | | |
| t_{ENZH} | Enable-to-Pad, Z to H | 1.9 | 2.2 | 2.4 | 2.9 | 4.0 | ns | | | | | |
| t_{ENLZ} | Enable-to-Pad, L to Z | 2.5 | 2.8 | 3.2 | 3.8 | 5.3 | ns | | | | | |
| t_{ENHZ} | Enable-to-Pad, H to Z | 2.0 | 2.3 | 2.6 | 3.1 | 4.3 | ns | | | | | |
| d_{TLH}^3 | Delta Low to High | 0.025 | 0.03 | 0.03 | 0.04 | 0.045 | ns/pF | | | | | |
| d_{THL}^3 | Delta High to Low | 0.015 | 0.015 | 0.015 | 0.015 | 0.025 | ns/pF | | | | | |
| 3.3 V LVTTL Output Module Timing⁴ | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | 2.6 | 3.0 | 3.4 | 4.0 | 5.6 | ns | | | | | |
| t_{DHL} | Data-to-Pad High to Low | 2.6 | 3.0 | 3.3 | 3.9 | 5.5 | ns | | | | | |
| t_{DHLs} | Data-to-Pad High to Low—low slew | 9.0 | 10.4 | 11.8 | 13.8 | 19.3 | ns | | | | | |
| t_{ENZL} | Enable-to-Pad, Z to L | 2.2 | 2.6 | 2.9 | 3.4 | 4.8 | ns | | | | | |
| t_{ENZLS} | Enable-to-Pad, Z to L—low slew | 15.8 | 18.9 | 21.3 | 25.4 | 34.9 | ns | | | | | |
| t_{ENZH} | Enable-to-Pad, Z to H | 2.6 | 3.0 | 3.4 | 4.0 | 5.6 | ns | | | | | |
| t_{ENLZ} | Enable-to-Pad, L to Z | 2.9 | 3.3 | 3.7 | 4.4 | 6.2 | ns | | | | | |
| t_{ENHZ} | Enable-to-Pad, H to Z | 2.6 | 3.0 | 3.3 | 3.9 | 5.5 | ns | | | | | |
| d_{TLH}^3 | Delta Low to High | 0.025 | 0.03 | 0.03 | 0.04 | 0.045 | ns/pF | | | | | |
| d_{THL}^3 | Delta High to Low | 0.015 | 0.015 | 0.015 | 0.015 | 0.025 | ns/pF | | | | | |
| d_{THLS}^3 | Delta High to Low—low slew | 0.053 | 0.053 | 0.067 | 0.073 | 0.107 | ns/pF | | | | | |

Notes:

- All -3 speed grades have been discontinued.
- Delays based on 10 pF loading and 25 Ω resistance.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

Table 2-34 • A54SX32A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|-----------------------|-------|----------|-------|----------|-------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 5 V PCI Output Module Timing² | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | 2.1 | 2.4 | 2.8 | 3.2 | 3.6 | 4.2 | 4.5 | 5.9 | ns | | |
| t_{DHL} | Data-to-Pad High to Low | 2.8 | 3.2 | 3.6 | 4.2 | 4.5 | 5.9 | ns | | | | |
| t_{ENZL} | Enable-to-Pad, Z to L | 1.3 | 1.5 | 1.7 | 2.0 | 2.8 | 3.2 | 4.5 | ns | | | |
| t_{ENZH} | Enable-to-Pad, Z to H | 2.1 | 2.4 | 2.8 | 3.2 | 3.6 | 4.2 | 4.5 | 5.9 | ns | | |
| t_{ENLZ} | Enable-to-Pad, L to Z | 3.0 | 3.5 | 3.9 | 4.6 | 5.9 | 6.4 | ns | | | | |
| t_{ENHZ} | Enable-to-Pad, H to Z | 2.8 | 3.2 | 3.6 | 4.2 | 4.5 | 5.9 | ns | | | | |
| d_{TLH}^3 | Delta Low to High | 0.016 | 0.016 | 0.02 | 0.022 | 0.032 | 0.032 | ns/pF | | | | |
| d_{THL}^3 | Delta High to Low | 0.026 | 0.03 | 0.032 | 0.04 | 0.052 | ns/pF | | | | | |
| 5 V TTL Output Module Timing⁴ | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | 1.9 | 2.2 | 2.5 | 2.9 | 3.3 | 3.9 | 4.1 | 5.4 | ns | | |
| t_{DHL} | Data-to-Pad High to Low | 2.5 | 2.9 | 3.3 | 3.9 | 4.1 | 5.4 | ns | | | | |
| t_{DHLS} | Data-to-Pad High to Low—low slew | 6.6 | 7.6 | 8.6 | 10.1 | 14.2 | ns | | | | | |
| t_{ENZL} | Enable-to-Pad, Z to L | 2.1 | 2.4 | 2.7 | 3.2 | 4.5 | ns | | | | | |
| t_{ENZLS} | Enable-to-Pad, Z to L—low slew | 7.4 | 8.4 | 9.5 | 11.0 | 15.4 | ns | | | | | |
| t_{ENZH} | Enable-to-Pad, Z to H | 1.9 | 2.2 | 2.5 | 2.9 | 4.1 | ns | | | | | |
| t_{ENLZ} | Enable-to-Pad, L to Z | 3.6 | 4.2 | 4.7 | 5.6 | 7.8 | ns | | | | | |
| t_{ENHZ} | Enable-to-Pad, H to Z | 2.5 | 2.9 | 3.3 | 3.9 | 5.4 | ns | | | | | |
| d_{TLH}^3 | Delta Low to High | 0.014 | 0.017 | 0.017 | 0.023 | 0.031 | ns/pF | | | | | |
| d_{THL}^3 | Delta High to Low | 0.023 | 0.029 | 0.031 | 0.037 | 0.051 | ns/pF | | | | | |
| d_{THLS}^3 | Delta High to Low—low slew | 0.043 | 0.046 | 0.057 | 0.066 | 0.089 | ns/pF | | | | | |

Notes:

1. All -3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

SX-A Family FPGAs

Table 2-35 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|---------------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| C-Cell Propagation Delays² | | | | | | | | | | | | |
| t_{PD} | Internal Array Module | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.0 | | ns |
| Predicted Routing Delays³ | | | | | | | | | | | | |
| t_{DC} | FO = 1 Routing Delay, Direct Connect | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | ns |
| t_{FC} | FO = 1 Routing Delay, Fast Connect | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| t_{RD1} | FO = 1 Routing Delay | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | | ns |
| t_{RD2} | FO = 2 Routing Delay | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 1 | | ns |
| t_{RD3} | FO = 3 Routing Delay | 0.5 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| t_{RD4} | FO = 4 Routing Delay | 0.7 | | 0.9 | | 1 | | 1.1 | | 1.5 | | ns |
| t_{RD8} | FO = 8 Routing Delay | 1.2 | | 1.5 | | 1.7 | | 2.1 | | 2.9 | | ns |
| t_{RD12} | FO = 12 Routing Delay | 1.7 | | 2.2 | | 2.5 | | 3 | | 4.2 | | ns |
| R-Cell Timing | | | | | | | | | | | | |
| t_{RCO} | Sequential Clock-to-Q | 0.7 | | 0.8 | | 0.9 | | 1.1 | | 1.5 | | ns |
| t_{CLR} | Asynchronous Clear-to-Q | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | | ns |
| t_{PRESET} | Asynchronous Preset-to-Q | 0.7 | | 0.8 | | 0.8 | | 1.0 | | 1.4 | | ns |
| t_{SUD} | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| t_{HD} | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t_{WASYN} | Asynchronous Pulse Width | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | | ns |
| t_{REASYN} | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| t_{HASYN} | Asynchronous Hold Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| t_{MPW} | Clock Minimum Pulse Width | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| Input Module Propagation Delays | | | | | | | | | | | | |
| t_{INYH} | Input Data Pad to Y High 2.5 V LVCMOS | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| t_{INYL} | Input Data Pad to Y Low 2.5 V LVCMOS | 0.8 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | | ns |
| t_{INYH} | Input Data Pad to Y High 3.3 V PCI | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | | ns |
| t_{INYL} | Input Data Pad to Y Low 3.3 V PCI | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| t_{INYH} | Input Data Pad to Y High 3.3 V LVTTTL | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| t_{INYL} | Input Data Pad to Y Low 3.3 V LVTTTL | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.1 | | ns |

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-35 • A54SX72A Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|--|----------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{INYH} | Input Data Pad to Y High 5 V PCI | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| t_{INYL} | Input Data Pad to Y Low 5 V PCI | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.6 | ns |
| t_{INYH} | Input Data Pad to Y High 5 V TTL | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| t_{INYL} | Input Data Pad to Y Low 5 V TTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| Input Module Predicted Routing Delays³ | | | | | | | | | | | | |
| t_{IRD1} | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | ns |
| t_{IRD2} | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 1 | ns |
| t_{IRD3} | FO = 3 Routing Delay | | 0.5 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| t_{IRD4} | FO = 4 Routing Delay | | 0.7 | | 0.9 | | 1 | | 1.1 | | 1.5 | ns |
| t_{IRD8} | FO = 8 Routing Delay | | 1.2 | | 1.5 | | 1.7 | | 2.1 | | 2.9 | ns |
| t_{IRD12} | FO = 12 Routing Delay | | 1.7 | | 2.2 | | 2.5 | | 3 | | 4.2 | ns |

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

SX-A Family FPGAs

Table 2-36 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{HCKSW} | Maximum Skew | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.3 | ns |
| t_{HP} | Minimum Period | 3.0 | | 3.4 | | 4.0 | | 4.6 | | 6.4 | | ns |
| f_{HMAX} | Maximum Frequency | | 333 | | 294 | | 250 | | 217 | | 156 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.3 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.7 | | 4.3 | | 6.0 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.9 | | 3.3 | | 3.8 | | 4.5 | | 6.2 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 3.1 | | 3.6 | | 4.0 | | 4.7 | | 6.6 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| Quadrant Array Clock Networks | | | | | | | | | | | | |
| t_{QCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| t_{QCHL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| t_{QCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| t_{QCHL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |

Note: *All -3 speed grades have been discontinued.

Table 2-36 • A54SX72A Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|-------------|--|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{QCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 3.0 | | 3.4 | | 3.9 | | 4.6 | | 6.4 | ns |
| t_{QCHKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 2.9 | | 3.4 | | 3.8 | | 4.5 | | 6.3 | ns |
| t_{QPWH} | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{QPWL} | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{QCKSW} | Maximum Skew (Light Load) | | 0.2 | | 0.3 | | 0.3 | | 0.3 | | 0.5 | ns |
| t_{QCKSW} | Maximum Skew (50% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |
| t_{QCKSW} | Maximum Skew (100% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |

Note: *All -3 speed grades have been discontinued.

SX-A Family FPGAs

Table 2-37 • **A54SX72A Timing Characteristics**
 (Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.7 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{HCKSW} | Maximum Skew | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.3 | ns |
| t_{HP} | Minimum Period | 3.0 | | 3.4 | | 4.0 | | 4.6 | | 6.4 | | ns |
| f_{HMAX} | Maximum Frequency | | 333 | | 294 | | 250 | | 217 | | 156 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.8 | | 3.3 | | 3.7 | | 4.3 | | 6.0 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.9 | | 3.4 | | 3.8 | | 4.5 | | 6.2 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 3.1 | | 3.6 | | 4.1 | | 4.8 | | 6.7 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 1.9 | | 2.2 | | 2.5 | | 3 | | 4.1 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 1.9 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 1.9 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| Quadrant Array Clock Networks | | | | | | | | | | | | |
| t_{QCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 1.9 | | 2.7 | ns |
| t_{QCHL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2 | | 2.8 | ns |
| t_{QCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| t_{QCHL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.5 | | 1.8 | | 2 | | 2.3 | | 3.2 | ns |

Note: *All -3 speed grades have been discontinued.

Table 2-37 • A54SX72A Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|-------------|--|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{QCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.5 | ns |
| t_{QCHKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| t_{QPWH} | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{QPWL} | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{QCKSW} | Maximum Skew (Light Load) | | 0.2 | | 0.3 | | 0.3 | | 0.3 | | 0.5 | ns |
| t_{QCKSW} | Maximum Skew (50% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |
| t_{QCKSW} | Maximum Skew (100% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |

Note: *All -3 speed grades have been discontinued.

SX-A Family FPGAs

Table 2-38 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|---|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Networks | | | | | | | | | | | | |
| t_{HCKH} | Input Low to High (Pad to R-cell Input) | | 1.6 | | 1.8 | | 2.1 | | 2.4 | | 3.8 | ns |
| t_{HCKL} | Input High to Low (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| t_{HPWH} | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{HCKSW} | Maximum Skew | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.3 | ns |
| t_{HP} | Minimum Period | 3.0 | | 3.4 | | 4.0 | | 4.6 | | 6.4 | | ns |
| f_{HMAX} | Maximum Frequency | | 333 | | 294 | | 250 | | 217 | | 156 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t_{RCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.3 | | 2.6 | | 3.0 | | 3.5 | | 4.9 | ns |
| t_{RCKL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| t_{RCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| t_{RCKL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 3.0 | | 3.4 | | 3.9 | | 4.6 | | 6.4 | ns |
| t_{RCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 3.9 | | 5.5 | ns |
| t_{RCKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 3.2 | | 3.6 | | 4.1 | | 4.8 | | 6.8 | ns |
| t_{RPWH} | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{RPWL} | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{RCKSW} | Maximum Skew (Light Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| t_{RCKSW} | Maximum Skew (50% Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| t_{RCKSW} | Maximum Skew (100% Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| Quadrant Array Clock Networks | | | | | | | | | | | | |
| t_{QCKH} | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.6 | ns |
| t_{QCHL} | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| t_{QCKH} | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.0 | ns |
| t_{QCHL} | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |

Note: *All -3 speed grades have been discontinued.

Table 2-38 • A54SX72A Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed* | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|-------------|--|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{QCKH} | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.6 | | 1.8 | | 2.1 | | 2.4 | | 3.4 | ns |
| t_{QCHKL} | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.5 | ns |
| t_{QPWH} | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{QPWL} | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| t_{QCKSW} | Maximum Skew (Light Load) | | 0.2 | | 0.3 | | 0.3 | | 0.3 | | 0.5 | ns |
| t_{QCKSW} | Maximum Skew (50% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |
| t_{QCKSW} | Maximum Skew (100% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |

Note: *All -3 speed grades have been discontinued.

SX-A Family FPGAs

Table 2-39 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|-----------------------|-------|----------|-------|----------|-------|------------|------|----------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 2.5 V LVCMOS Output Module Timing^{2, 3} | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | 3.9 | 4.5 | 5.1 | 6.0 | 8.4 | ns | | | | | |
| t_{DHL} | Data-to-Pad High to Low | 3.1 | 3.6 | 4.1 | 4.8 | 6.7 | ns | | | | | |
| t_{DHLS} | Data-to-Pad High to Low—low slew | 12.7 | 14.6 | 16.5 | 19.4 | 27.2 | ns | | | | | |
| t_{ENZL} | Enable-to-Pad, Z to L | 2.4 | 2.8 | 3.2 | 3.7 | 5.2 | ns | | | | | |
| t_{ENZLS} | Data-to-Pad, Z to L—low slew | 11.8 | 13.7 | 15.5 | 18.2 | 25.5 | ns | | | | | |
| t_{ENZH} | Enable-to-Pad, Z to H | 3.9 | 4.5 | 5.1 | 6.0 | 8.4 | ns | | | | | |
| t_{ENLZ} | Enable-to-Pad, L to Z | 2.1 | 2.5 | 2.8 | 3.3 | 4.7 | ns | | | | | |
| t_{ENHZ} | Enable-to-Pad, H to Z | 3.1 | 3.6 | 4.1 | 4.8 | 6.7 | ns | | | | | |
| d_{TLH}^4 | Delta Low to High | 0.031 | 0.037 | 0.043 | 0.051 | 0.071 | ns/pF | | | | | |
| d_{THL}^4 | Delta High to Low | 0.017 | 0.017 | 0.023 | 0.023 | 0.037 | ns/pF | | | | | |
| d_{THLS}^4 | Delta High to Low—low slew | 0.057 | 0.06 | 0.071 | 0.086 | 0.117 | ns/pF | | | | | |

Note:

- All -3 speed grades have been discontinued.
- Delays based on 35 pF loading.
- The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-40 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|-----------------------|-------|----------|-------|----------|-------|------------|-------|----------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 3.3 V PCI Output Module Timing² | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 2.3 | | 2.7 | | 3.0 | | 3.6 | | 5.0 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.3 | | 2.7 | | 3.0 | | 3.6 | | 5.0 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| d_{TLH}^3 | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| d_{THL}^3 | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| 3.3 V LVTTL Output Module Timing⁴ | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 3.2 | | 3.7 | | 4.2 | | 5.0 | | 6.9 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 3.2 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| t_{DHLS} | Data-to-Pad High to Low—low slew | | 10.3 | | 11.9 | | 13.5 | | 15.8 | | 22.2 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| t_{ENZLS} | Enable-to-Pad, Z to L—low slew | | 15.8 | | 18.9 | | 21.3 | | 25.4 | | 34.9 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 3.2 | | 3.7 | | 4.2 | | 5.0 | | 6.9 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 3.2 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| d_{TLH}^3 | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| d_{THL}^3 | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| d_{THLS}^3 | Delta High to Low—low slew | | 0.053 | | 0.053 | | 0.067 | | 0.073 | | 0.107 | ns/pF |

Notes:

- All -3 speed grades have been discontinued.
- Delays based on 10 pF loading and 25 Ω resistance.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

SX-A Family FPGAs

Table 2-41 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | -3 Speed ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | -F Speed | | Units |
|---|----------------------------------|-----------------------|-------|----------|-------|----------|-------|------------|-------|----------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 5 V PCI Output Module Timing² | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 3.4 | | 3.9 | | 4.4 | | 5.1 | | 7.2 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 3.0 | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 3.4 | | 3.9 | | 4.4 | | 5.1 | | 7.2 | ns |
| d_{TLH}^3 | Delta Low to High | | 0.016 | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| d_{THL}^3 | Delta High to Low | | 0.026 | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| 5 V TTL Output Module Timing⁴ | | | | | | | | | | | | |
| t_{DLH} | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.1 | ns |
| t_{DHL} | Data-to-Pad High to Low | | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | ns |
| t_{DHLs} | Data-to-Pad High to Low—low slew | | 7.4 | | 8.5 | | 9.7 | | 11.4 | | 15.9 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| t_{ENZLS} | Enable-to-Pad, Z to L—low slew | | 7.4 | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.1 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 3.6 | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | ns |
| d_{TLH}^3 | Delta Low to High | | 0.014 | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| d_{THL}^3 | Delta High to Low | | 0.023 | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| d_{THLS}^3 | Delta High to Low—low slew | | 0.043 | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

Notes:

1. All -3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Package Pin Assignments

208-Pin PQFP

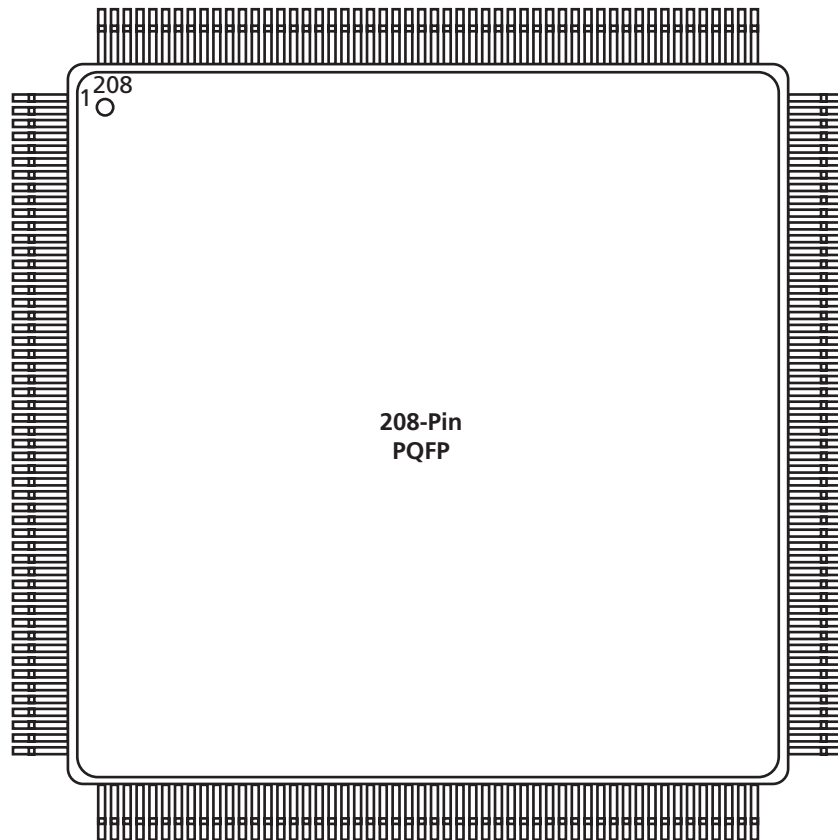


Figure 3-1 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

SX-A Family FPGAs

| 208-Pin PQFP | | | | |
|--------------|-------------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| 1 | GND | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O | I/O |
| 4 | NC | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O | I/O |
| 6 | NC | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O | I/O |
| 9 | I/O | I/O | I/O | I/O |
| 10 | I/O | I/O | I/O | I/O |
| 11 | TMS | TMS | TMS | TMS |
| 12 | V _{CCI} | V _{CCI} | V _{CCI} | V _{CCI} |
| 13 | I/O | I/O | I/O | I/O |
| 14 | NC | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O | I/O |
| 17 | NC | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O | GND |
| 19 | I/O | I/O | I/O | V _{CCA} |
| 20 | NC | I/O | I/O | I/O |
| 21 | I/O | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O | I/O |
| 23 | NC | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O | I/O |
| 25 | NC | NC | NC | I/O |
| 26 | GND | GND | GND | GND |
| 27 | V _{CCA} | V _{CCA} | V _{CCA} | V _{CCA} |
| 28 | GND | GND | GND | GND |
| 29 | I/O | I/O | I/O | I/O |
| 30 | TRST, I/O | TRST, I/O | TRST, I/O | TRST, I/O |
| 31 | NC | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O | I/O |
| 35 | NC | I/O | I/O | I/O |

| 208-Pin PQFP | | | | |
|--------------|-------------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| 36 | I/O | I/O | I/O | I/O |
| 37 | I/O | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O | I/O |
| 39 | NC | I/O | I/O | I/O |
| 40 | V _{CCI} | V _{CCI} | V _{CCI} | V _{CCI} |
| 41 | V _{CCA} | V _{CCA} | V _{CCA} | V _{CCA} |
| 42 | I/O | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O | I/O |
| 44 | I/O | I/O | I/O | I/O |
| 45 | I/O | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O | I/O |
| 48 | NC | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O | I/O |
| 50 | NC | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O | I/O |
| 52 | GND | GND | GND | GND |
| 53 | I/O | I/O | I/O | I/O |
| 54 | I/O | I/O | I/O | I/O |
| 55 | I/O | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O | I/O |
| 57 | I/O | I/O | I/O | I/O |
| 58 | I/O | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O | I/O |
| 60 | V _{CCI} | V _{CCI} | V _{CCI} | V _{CCI} |
| 61 | NC | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O | I/O |
| 64 | NC | I/O | I/O | I/O |
| 65 | I/O | I/O | NC | I/O |
| 66 | I/O | I/O | I/O | I/O |
| 67 | NC | I/O | I/O | I/O |
| 68 | I/O | I/O | I/O | I/O |
| 69 | I/O | I/O | I/O | I/O |
| 70 | NC | I/O | I/O | I/O |

| 208-Pin PQFP | | | | |
|--------------|-------------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| 71 | I/O | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O | I/O |
| 73 | NC | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O | QCLKA |
| 75 | NC | I/O | I/O | I/O |
| 76 | PRB, I/O | PRB, I/O | PRB, I/O | PRB, I/O |
| 77 | GND | GND | GND | GND |
| 78 | V _{CCA} | V _{CCA} | V _{CCA} | V _{CCA} |
| 79 | GND | GND | GND | GND |
| 80 | NC | NC | NC | NC |
| 81 | I/O | I/O | I/O | I/O |
| 82 | HCLK | HCLK | HCLK | HCLK |
| 83 | I/O | I/O | I/O | V _{CCI} |
| 84 | I/O | I/O | I/O | QCLKB |
| 85 | NC | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O | I/O |
| 88 | NC | I/O | I/O | I/O |
| 89 | I/O | I/O | I/O | I/O |
| 90 | I/O | I/O | I/O | I/O |
| 91 | NC | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O | I/O |
| 94 | NC | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O | I/O |
| 97 | NC | I/O | I/O | I/O |
| 98 | V _{CCI} | V _{CCI} | V _{CCI} | V _{CCI} |
| 99 | I/O | I/O | I/O | I/O |
| 100 | I/O | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O | I/O |
| 103 | TDO, I/O | TDO, I/O | TDO, I/O | TDO, I/O |
| 104 | I/O | I/O | I/O | I/O |
| 105 | GND | GND | GND | GND |

| 208-Pin PQFP | | | | |
|--------------|-------------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| 106 | NC | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O | I/O |
| 108 | NC | I/O | I/O | I/O |
| 109 | I/O | I/O | I/O | I/O |
| 110 | I/O | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O | I/O |
| 114 | V _{CCA} | V _{CCA} | V _{CCA} | V _{CCA} |
| 115 | V _{CCI} | V _{CCI} | V _{CCI} | V _{CCI} |
| 116 | NC | I/O | I/O | GND |
| 117 | I/O | I/O | I/O | V _{CCA} |
| 118 | I/O | I/O | I/O | I/O |
| 119 | NC | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O | I/O |
| 122 | NC | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O | I/O |
| 125 | NC | I/O | I/O | I/O |
| 126 | I/O | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O | I/O |
| 129 | GND | GND | GND | GND |
| 130 | V _{CCA} | V _{CCA} | V _{CCA} | V _{CCA} |
| 131 | GND | GND | GND | GND |
| 132 | NC | NC | NC | I/O |
| 133 | I/O | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O | I/O |
| 135 | NC | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O | I/O |
| 138 | NC | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O | I/O |
| 140 | I/O | I/O | I/O | I/O |

SX-A Family FPGAs

| 208-Pin PQFP | | | | |
|--------------|-------------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| 141 | NC | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O | I/O |
| 143 | NC | I/O | I/O | I/O |
| 144 | I/O | I/O | I/O | I/O |
| 145 | V _{CCA} | V _{CCA} | V _{CCA} | V _{CCA} |
| 146 | GND | GND | GND | GND |
| 147 | I/O | I/O | I/O | I/O |
| 148 | V _{CCI} | V _{CCI} | V _{CCI} | V _{CCI} |
| 149 | I/O | I/O | I/O | I/O |
| 150 | I/O | I/O | I/O | I/O |
| 151 | I/O | I/O | I/O | I/O |
| 152 | I/O | I/O | I/O | I/O |
| 153 | I/O | I/O | I/O | I/O |
| 154 | I/O | I/O | I/O | I/O |
| 155 | NC | I/O | I/O | I/O |
| 156 | NC | I/O | I/O | I/O |
| 157 | GND | GND | GND | GND |
| 158 | I/O | I/O | I/O | I/O |
| 159 | I/O | I/O | I/O | I/O |
| 160 | I/O | I/O | I/O | I/O |
| 161 | I/O | I/O | I/O | I/O |
| 162 | I/O | I/O | I/O | I/O |
| 163 | I/O | I/O | I/O | I/O |
| 164 | V _{CCI} | V _{CCI} | V _{CCI} | V _{CCI} |
| 165 | I/O | I/O | I/O | I/O |
| 166 | I/O | I/O | I/O | I/O |
| 167 | NC | I/O | I/O | I/O |
| 168 | I/O | I/O | I/O | I/O |
| 169 | I/O | I/O | I/O | I/O |
| 170 | NC | I/O | I/O | I/O |
| 171 | I/O | I/O | I/O | I/O |
| 172 | I/O | I/O | I/O | I/O |
| 173 | NC | I/O | I/O | I/O |
| 174 | I/O | I/O | I/O | I/O |
| 175 | I/O | I/O | I/O | I/O |

| 208-Pin PQFP | | | | |
|--------------|-------------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| 176 | NC | I/O | I/O | I/O |
| 177 | I/O | I/O | I/O | I/O |
| 178 | I/O | I/O | I/O | QCLKD |
| 179 | I/O | I/O | I/O | I/O |
| 180 | CLKA | CLKA | CLKA | CLKA |
| 181 | CLKB | CLKB | CLKB | CLKB |
| 182 | NC | NC | NC | NC |
| 183 | GND | GND | GND | GND |
| 184 | V _{CCA} | V _{CCA} | V _{CCA} | V _{CCA} |
| 185 | GND | GND | GND | GND |
| 186 | PRA, I/O | PRA, I/O | PRA, I/O | PRA, I/O |
| 187 | I/O | I/O | I/O | V _{CCI} |
| 188 | I/O | I/O | I/O | I/O |
| 189 | NC | I/O | I/O | I/O |
| 190 | I/O | I/O | I/O | QCLKC |
| 191 | I/O | I/O | I/O | I/O |
| 192 | NC | I/O | I/O | I/O |
| 193 | I/O | I/O | I/O | I/O |
| 194 | I/O | I/O | I/O | I/O |
| 195 | NC | I/O | I/O | I/O |
| 196 | I/O | I/O | I/O | I/O |
| 197 | I/O | I/O | I/O | I/O |
| 198 | NC | I/O | I/O | I/O |
| 199 | I/O | I/O | I/O | I/O |
| 200 | I/O | I/O | I/O | I/O |
| 201 | V _{CCI} | V _{CCI} | V _{CCI} | V _{CCI} |
| 202 | NC | I/O | I/O | I/O |
| 203 | NC | I/O | I/O | I/O |
| 204 | I/O | I/O | I/O | I/O |
| 205 | NC | I/O | I/O | I/O |
| 206 | I/O | I/O | I/O | I/O |
| 207 | I/O | I/O | I/O | I/O |
| 208 | TCK, I/O | TCK, I/O | TCK, I/O | TCK, I/O |

100-Pin TQFP

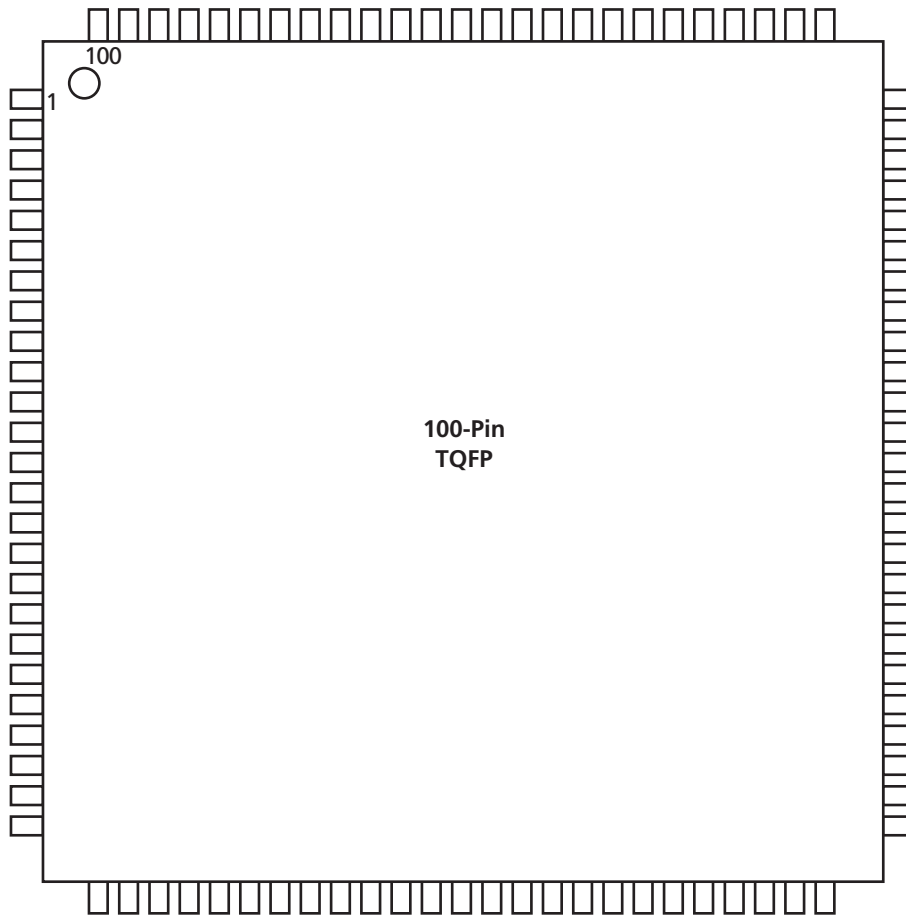


Figure 3-2 • 100-Pin TQFP

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

SX-A Family FPGAs

| 100-TQFP | | | |
|------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | TMS | TMS | TMS |
| 8 | V _{CCI} | V _{CCI} | V _{CCI} |
| 9 | GND | GND | GND |
| 10 | I/O | I/O | I/O |
| 11 | I/O | I/O | I/O |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | TRST, I/O | TRST, I/O | TRST, I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | I/O | I/O | I/O |
| 20 | V _{CCI} | V _{CCI} | V _{CCI} |
| 21 | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | I/O | I/O | I/O |
| 29 | I/O | I/O | I/O |
| 30 | I/O | I/O | I/O |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | PRB, I/O | PRB, I/O | PRB, I/O |
| 35 | V _{CCA} | V _{CCA} | V _{CCA} |

| 100-TQFP | | | |
|------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 36 | GND | GND | GND |
| 37 | NC | NC | NC |
| 38 | I/O | I/O | I/O |
| 39 | HCLK | HCLK | HCLK |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | V _{CCI} | V _{CCI} | V _{CCI} |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | TDO, I/O | TDO, I/O | TDO, I/O |
| 50 | I/O | I/O | I/O |
| 51 | GND | GND | GND |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | I/O | I/O | I/O |
| 55 | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O |
| 57 | V _{CCA} | V _{CCA} | V _{CCA} |
| 58 | V _{CCI} | V _{CCI} | V _{CCI} |
| 59 | I/O | I/O | I/O |
| 60 | I/O | I/O | I/O |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | V _{CCA} | V _{CCA} | V _{CCA} |
| 68 | GND | GND | GND |
| 69 | GND | GND | GND |
| 70 | I/O | I/O | I/O |

| 100-TQFP | | | |
|-------------------|------------------------------|------------------------------|------------------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | I/O | I/O | I/O |
| 80 | I/O | I/O | I/O |
| 81 | I/O | I/O | I/O |
| 82 | V _{CCI} | V _{CCI} | V _{CCI} |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | CLKA | CLKA | CLKA |
| 88 | CLKB | CLKB | CLKB |
| 89 | NC | NC | NC |
| 90 | V _{CCA} | V _{CCA} | V _{CCA} |
| 91 | GND | GND | GND |
| 92 | PRA, I/O | PRA, I/O | PRA, I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | I/O | I/O | I/O |
| 99 | I/O | I/O | I/O |
| 100 | TCK, I/O | TCK, I/O | TCK, I/O |

144-Pin TQFP

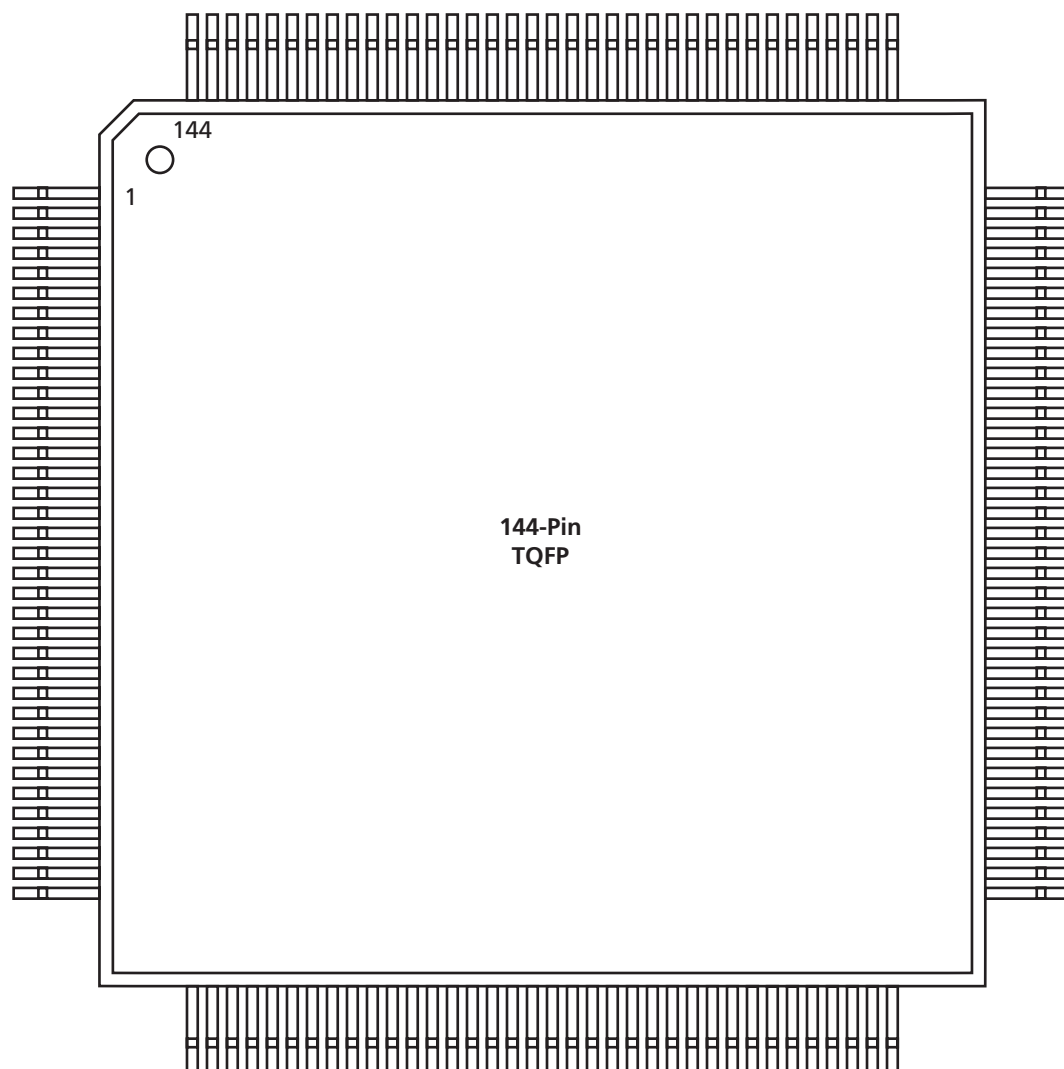


Figure 3-3 • 144-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 144-Pin TQFP | | | |
|--------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | TMS | TMS | TMS |
| 10 | V _{CCI} | V _{CCI} | V _{CCI} |
| 11 | GND | GND | GND |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | NC | NC | NC |
| 20 | V _{CCA} | V _{CCA} | V _{CCA} |
| 21 | I/O | I/O | I/O |
| 22 | TRST, I/O | TRST, I/O | TRST, I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | GND | GND | GND |
| 29 | V _{CCI} | V _{CCI} | V _{CCI} |
| 30 | V _{CCA} | V _{CCA} | V _{CCA} |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | GND | GND | GND |
| 37 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|--------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | V _{CCI} | V _{CCI} | V _{CCI} |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | PRB, I/O | PRB, I/O | PRB, I/O |
| 55 | I/O | I/O | I/O |
| 56 | V _{CCA} | V _{CCA} | V _{CCA} |
| 57 | GND | GND | GND |
| 58 | NC | NC | NC |
| 59 | I/O | I/O | I/O |
| 60 | HCLK | HCLK | HCLK |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | V _{CCI} | V _{CCI} | V _{CCI} |
| 69 | I/O | I/O | I/O |
| 70 | I/O | I/O | I/O |
| 71 | TDO, I/O | TDO, I/O | TDO, I/O |
| 72 | I/O | I/O | I/O |
| 73 | GND | GND | GND |
| 74 | I/O | I/O | I/O |

SX-A Family FPGAs

| 144-Pin TQFP | | | |
|--------------|----------------------|----------------------|----------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | V _{CCA} | V _{CCA} | V _{CCA} |
| 80 | V _{CCI} | V _{CCI} | V _{CCI} |
| 81 | GND | GND | GND |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | V _{CCA} | V _{CCA} | V _{CCA} |
| 90 | NC | NC | NC |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | V _{CCA} | V _{CCA} | V _{CCA} |
| 99 | GND | GND | GND |
| 100 | I/O | I/O | I/O |
| 101 | GND | GND | GND |
| 102 | V _{CCI} | V _{CCI} | V _{CCI} |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |
| 109 | GND | GND | GND |
| 110 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|--------------|----------------------|----------------------|----------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | V _{CCI} | V _{CCI} | V _{CCI} |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | CLKA | CLKA | CLKA |
| 126 | CLKB | CLKB | CLKB |
| 127 | NC | NC | NC |
| 128 | GND | GND | GND |
| 129 | V _{CCA} | V _{CCA} | V _{CCA} |
| 130 | I/O | I/O | I/O |
| 131 | PRA, I/O | PRA, I/O | PRA, I/O |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | V _{CCI} | V _{CCI} | V _{CCI} |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | TCK, I/O | TCK, I/O | TCK, I/O |

176-Pin TQFP

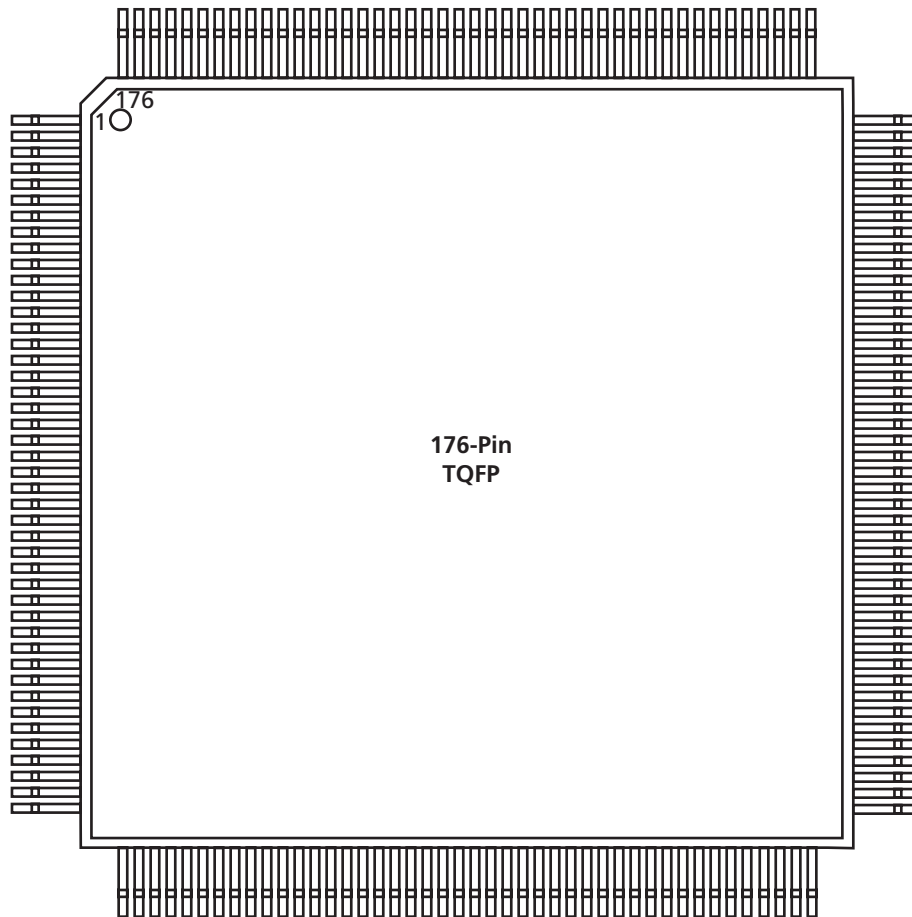


Figure 3-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

SX-A Family FPGAs

| 176-Pin TQFP | | 176-Pin TQFP | | 176-Pin TQFP | | 176-Pin TQFP | |
|--------------|-------------------|--------------|-------------------|--------------|-------------------|--------------|-------------------|
| Pin Number | A54SX32A Function | Pin Number | A54SX32A Function | Pin Number | A54SX32A Function | Pin Number | A54SX32A Function |
| 1 | GND | 37 | I/O | 73 | I/O | 109 | V _{CCA} |
| 2 | TDI, I/O | 38 | I/O | 74 | I/O | 110 | GND |
| 3 | I/O | 39 | I/O | 75 | I/O | 111 | I/O |
| 4 | I/O | 40 | I/O | 76 | I/O | 112 | I/O |
| 5 | I/O | 41 | I/O | 77 | I/O | 113 | I/O |
| 6 | I/O | 42 | I/O | 78 | I/O | 114 | I/O |
| 7 | I/O | 43 | I/O | 79 | I/O | 115 | I/O |
| 8 | I/O | 44 | GND | 80 | I/O | 116 | I/O |
| 9 | I/O | 45 | I/O | 81 | I/O | 117 | I/O |
| 10 | TMS | 46 | I/O | 82 | V _{CCI} | 118 | I/O |
| 11 | V _{CCI} | 47 | I/O | 83 | I/O | 119 | I/O |
| 12 | I/O | 48 | I/O | 84 | I/O | 120 | I/O |
| 13 | I/O | 49 | I/O | 85 | I/O | 121 | I/O |
| 14 | I/O | 50 | I/O | 86 | I/O | 122 | V _{CCA} |
| 15 | I/O | 51 | I/O | 87 | TDO, I/O | 123 | GND |
| 16 | I/O | 52 | V _{CCI} | 88 | I/O | 124 | V _{CCI} |
| 17 | I/O | 53 | I/O | 89 | GND | 125 | I/O |
| 18 | I/O | 54 | I/O | 90 | I/O | 126 | I/O |
| 19 | I/O | 55 | I/O | 91 | I/O | 127 | I/O |
| 20 | I/O | 56 | I/O | 92 | I/O | 128 | I/O |
| 21 | GND | 57 | I/O | 93 | I/O | 129 | I/O |
| 22 | V _{CCA} | 58 | I/O | 94 | I/O | 130 | I/O |
| 23 | GND | 59 | I/O | 95 | I/O | 131 | I/O |
| 24 | I/O | 60 | I/O | 96 | I/O | 132 | I/O |
| 25 | TRST, I/O | 61 | I/O | 97 | I/O | 133 | GND |
| 26 | I/O | 62 | I/O | 98 | V _{CCA} | 134 | I/O |
| 27 | I/O | 63 | I/O | 99 | V _{CCI} | 135 | I/O |
| 28 | I/O | 64 | PRB, I/O | 100 | I/O | 136 | I/O |
| 29 | I/O | 65 | GND | 101 | I/O | 137 | I/O |
| 30 | I/O | 66 | V _{CCA} | 102 | I/O | 138 | I/O |
| 31 | I/O | 67 | NC | 103 | I/O | 139 | I/O |
| 32 | V _{CCI} | 68 | I/O | 104 | I/O | 140 | V _{CCI} |
| 33 | V _{CCA} | 69 | HCLK | 105 | I/O | 141 | I/O |
| 34 | I/O | 70 | I/O | 106 | I/O | 142 | I/O |
| 35 | I/O | 71 | I/O | 107 | I/O | 143 | I/O |
| 36 | I/O | 72 | I/O | 108 | GND | 144 | I/O |

| 176-Pin TQFP | |
|--------------|-------------------|
| Pin Number | A54SX32A Function |
| 145 | I/O |
| 146 | I/O |
| 147 | I/O |
| 148 | I/O |
| 149 | I/O |
| 150 | I/O |
| 151 | I/O |
| 152 | CLKA |
| 153 | CLKB |
| 154 | NC |
| 155 | GND |
| 156 | V _{CCA} |
| 157 | PRA, I/O |
| 158 | I/O |
| 159 | I/O |
| 160 | I/O |
| 161 | I/O |
| 162 | I/O |
| 163 | I/O |
| 164 | I/O |
| 165 | I/O |
| 166 | I/O |
| 167 | I/O |
| 168 | I/O |
| 169 | V _{CCI} |
| 170 | I/O |
| 171 | I/O |
| 172 | I/O |
| 173 | I/O |
| 174 | I/O |
| 175 | I/O |
| 176 | TCK, I/O |

329-Pin PBGA



Figure 3-5 • 329-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 329-Pin PBGA | | 329-Pin PBGA | | 329-Pin PBGA | | 329-Pin PBGA | |
|--------------|-------------------|--------------|-------------------|--------------|-------------------|--------------|-------------------|
| Pin Number | A54SX32A Function | Pin Number | A54SX32A Function | Pin Number | A54SX32A Function | Pin Number | A54SX32A Function |
| A1 | GND | AA15 | I/O | AC6 | I/O | B20 | I/O |
| A2 | GND | AA16 | I/O | AC7 | I/O | B21 | I/O |
| A3 | V _{CCI} | AA17 | I/O | AC8 | I/O | B22 | GND |
| A4 | NC | AA18 | I/O | AC9 | V _{CCI} | B23 | V _{CCI} |
| A5 | I/O | AA19 | I/O | AC10 | I/O | C1 | NC |
| A6 | I/O | AA20 | TDO, I/O | AC11 | I/O | C2 | TDI, I/O |
| A7 | V _{CCI} | AA21 | V _{CCI} | AC12 | I/O | C3 | GND |
| A8 | NC | AA22 | I/O | AC13 | I/O | C4 | I/O |
| A9 | I/O | AA23 | V _{CCI} | AC14 | I/O | C5 | I/O |
| A10 | I/O | AB1 | I/O | AC15 | NC | C6 | I/O |
| A11 | I/O | AB2 | GND | AC16 | I/O | C7 | I/O |
| A12 | I/O | AB3 | I/O | AC17 | I/O | C8 | I/O |
| A13 | CLKB | AB4 | I/O | AC18 | I/O | C9 | I/O |
| A14 | I/O | AB5 | I/O | AC19 | I/O | C10 | I/O |
| A15 | I/O | AB6 | I/O | AC20 | I/O | C11 | I/O |
| A16 | I/O | AB7 | I/O | AC21 | NC | C12 | I/O |
| A17 | I/O | AB8 | I/O | AC22 | V _{CCI} | C13 | I/O |
| A18 | I/O | AB9 | I/O | AC23 | GND | C14 | I/O |
| A19 | I/O | AB10 | I/O | B1 | V _{CCI} | C15 | I/O |
| A20 | I/O | AB11 | PRB, I/O | B2 | GND | C16 | I/O |
| A21 | NC | AB12 | I/O | B3 | I/O | C17 | I/O |
| A22 | V _{CCI} | AB13 | HCLK | B4 | I/O | C18 | I/O |
| A23 | GND | AB14 | I/O | B5 | I/O | C19 | I/O |
| AA1 | V _{CCI} | AB15 | I/O | B6 | I/O | C20 | I/O |
| AA2 | I/O | AB16 | I/O | B7 | I/O | C21 | V _{CCI} |
| AA3 | GND | AB17 | I/O | B8 | I/O | C22 | GND |
| AA4 | I/O | AB18 | I/O | B9 | I/O | C23 | NC |
| AA5 | I/O | AB19 | I/O | B10 | I/O | D1 | I/O |
| AA6 | I/O | AB20 | I/O | B11 | I/O | D2 | I/O |
| AA7 | I/O | AB21 | I/O | B12 | PRA, I/O | D3 | I/O |
| AA8 | I/O | AB22 | GND | B13 | CLKA | D4 | TCK, I/O |
| AA9 | I/O | AB23 | I/O | B14 | I/O | D5 | I/O |
| AA10 | I/O | AC1 | GND | B15 | I/O | D6 | I/O |
| AA11 | I/O | AC2 | V _{CCI} | B16 | I/O | D7 | I/O |
| AA12 | I/O | AC3 | NC | B17 | I/O | D8 | I/O |
| AA13 | I/O | AC4 | I/O | B18 | I/O | D9 | I/O |
| AA14 | I/O | AC5 | I/O | B19 | I/O | D10 | I/O |

SX-A Family FPGAs

| 329-Pin PBGA | | 329-Pin PBGA | | 329-Pin PBGA | | 329-Pin PBGA | |
|--------------|-------------------|--------------|-------------------|--------------|-------------------|--------------|-------------------|
| Pin Number | A54SX32A Function | Pin Number | A54SX32A Function | Pin Number | A54SX32A Function | Pin Number | A54SX32A Function |
| D11 | V _{CCA} | H1 | I/O | L14 | GND | P12 | GND |
| D12 | NC | H2 | I/O | L20 | NC | P13 | GND |
| D13 | I/O | H3 | I/O | L21 | I/O | P14 | GND |
| D14 | I/O | H4 | I/O | L22 | I/O | P20 | I/O |
| D15 | I/O | H20 | V _{CCA} | L23 | NC | P21 | I/O |
| D16 | I/O | H21 | I/O | M1 | I/O | P22 | I/O |
| D17 | I/O | H22 | I/O | M2 | I/O | P23 | I/O |
| D18 | I/O | H23 | I/O | M3 | I/O | R1 | I/O |
| D19 | I/O | J1 | NC | M4 | V _{CCA} | R2 | I/O |
| D20 | I/O | J2 | I/O | M10 | GND | R3 | I/O |
| D21 | I/O | J3 | I/O | M11 | GND | R4 | I/O |
| D22 | I/O | J4 | I/O | M12 | GND | R20 | I/O |
| D23 | I/O | J20 | I/O | M13 | GND | R21 | I/O |
| E1 | V _{CCI} | J21 | I/O | M14 | GND | R22 | I/O |
| E2 | I/O | J22 | I/O | M20 | V _{CCA} | R23 | I/O |
| E3 | I/O | J23 | I/O | M21 | I/O | T1 | I/O |
| E4 | I/O | K1 | I/O | M22 | I/O | T2 | I/O |
| E20 | I/O | K2 | I/O | M23 | V _{CCI} | T3 | I/O |
| E21 | I/O | K3 | I/O | N1 | I/O | T4 | I/O |
| E22 | I/O | K4 | I/O | N2 | TRST, I/O | T20 | I/O |
| E23 | I/O | K10 | GND | N3 | I/O | T21 | I/O |
| F1 | I/O | K11 | GND | N4 | I/O | T22 | I/O |
| F2 | TMS | K12 | GND | N10 | GND | T23 | I/O |
| F3 | I/O | K13 | GND | N11 | GND | U1 | I/O |
| F4 | I/O | K14 | GND | N12 | GND | U2 | I/O |
| F20 | I/O | K20 | I/O | N13 | GND | U3 | V _{CCA} |
| F21 | I/O | K21 | I/O | N14 | GND | U4 | I/O |
| F22 | I/O | K22 | I/O | N20 | NC | U20 | I/O |
| F23 | I/O | K23 | I/O | N21 | I/O | U21 | V _{CCA} |
| G1 | I/O | L1 | I/O | N22 | I/O | U22 | I/O |
| G2 | I/O | L2 | I/O | N23 | I/O | U23 | I/O |
| G3 | I/O | L3 | I/O | P1 | I/O | V1 | V _{CCI} |
| G4 | I/O | L4 | NC | P2 | I/O | V2 | I/O |
| G20 | I/O | L10 | GND | P3 | I/O | V3 | I/O |
| G21 | I/O | L11 | GND | P4 | I/O | V4 | I/O |
| G22 | I/O | L12 | GND | P10 | GND | V20 | I/O |
| G23 | GND | L13 | GND | P11 | GND | V21 | I/O |

| 329-Pin PBGA | |
|--------------|-------------------|
| Pin Number | A54SX32A Function |
| V22 | I/O |
| V23 | I/O |
| W1 | I/O |
| W2 | I/O |
| W3 | I/O |
| W4 | I/O |
| W20 | I/O |
| W21 | I/O |
| W22 | I/O |
| W23 | NC |
| Y1 | NC |
| Y2 | I/O |
| Y3 | I/O |
| Y4 | GND |
| Y5 | I/O |
| Y6 | I/O |
| Y7 | I/O |
| Y8 | I/O |
| Y9 | I/O |
| Y10 | I/O |
| Y11 | I/O |
| Y12 | V _{CCA} |
| Y13 | NC |
| Y14 | I/O |
| Y15 | I/O |
| Y16 | I/O |
| Y17 | I/O |
| Y18 | I/O |
| Y19 | I/O |
| Y20 | GND |
| Y21 | I/O |
| Y22 | I/O |
| Y23 | I/O |

144-Pin FBGA

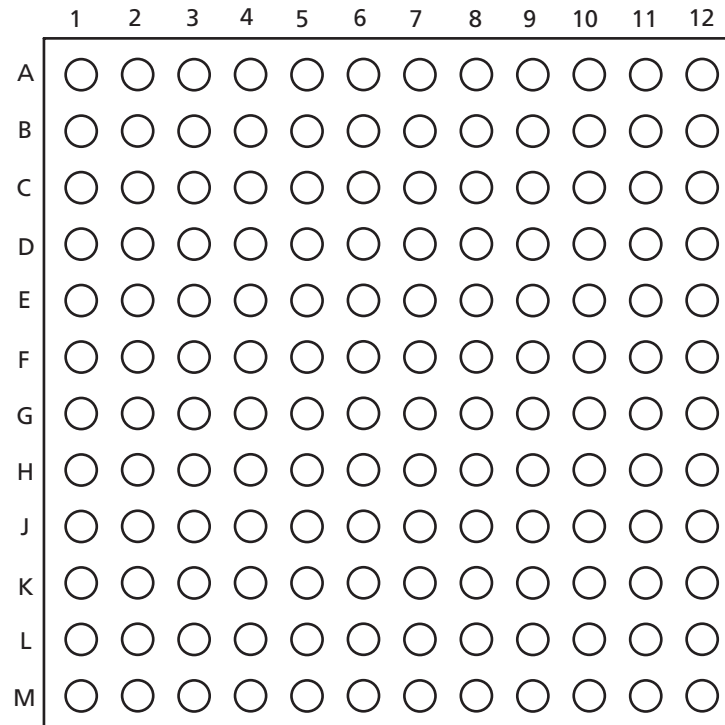


Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 144-Pin FBGA | | | |
|--------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| A1 | I/O | I/O | I/O |
| A2 | I/O | I/O | I/O |
| A3 | I/O | I/O | I/O |
| A4 | I/O | I/O | I/O |
| A5 | V _{CCA} | V _{CCA} | V _{CCA} |
| A6 | GND | GND | GND |
| A7 | CLKA | CLKA | CLKA |
| A8 | I/O | I/O | I/O |
| A9 | I/O | I/O | I/O |
| A10 | I/O | I/O | I/O |
| A11 | I/O | I/O | I/O |
| A12 | I/O | I/O | I/O |
| B1 | I/O | I/O | I/O |
| B2 | GND | GND | GND |
| B3 | I/O | I/O | I/O |
| B4 | I/O | I/O | I/O |
| B5 | I/O | I/O | I/O |
| B6 | I/O | I/O | I/O |
| B7 | CLKB | CLKB | CLKB |
| B8 | I/O | I/O | I/O |
| B9 | I/O | I/O | I/O |
| B10 | I/O | I/O | I/O |
| B11 | GND | GND | GND |
| B12 | I/O | I/O | I/O |
| C1 | I/O | I/O | I/O |
| C2 | I/O | I/O | I/O |
| C3 | TCK, I/O | TCK, I/O | TCK, I/O |
| C4 | I/O | I/O | I/O |
| C5 | I/O | I/O | I/O |
| C6 | PRA, I/O | PRA, I/O | PRA, I/O |
| C7 | I/O | I/O | I/O |
| C8 | I/O | I/O | I/O |
| C9 | I/O | I/O | I/O |
| C10 | I/O | I/O | I/O |
| C11 | I/O | I/O | I/O |
| C12 | I/O | I/O | I/O |

| 144-Pin FBGA | | | |
|--------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| D1 | I/O | I/O | I/O |
| D2 | V _{CCI} | V _{CCI} | V _{CCI} |
| D3 | TDI, I/O | TDI, I/O | TDI, I/O |
| D4 | I/O | I/O | I/O |
| D5 | I/O | I/O | I/O |
| D6 | I/O | I/O | I/O |
| D7 | I/O | I/O | I/O |
| D8 | I/O | I/O | I/O |
| D9 | I/O | I/O | I/O |
| D10 | I/O | I/O | I/O |
| D11 | I/O | I/O | I/O |
| D12 | I/O | I/O | I/O |
| E1 | I/O | I/O | I/O |
| E2 | I/O | I/O | I/O |
| E3 | I/O | I/O | I/O |
| E4 | I/O | I/O | I/O |
| E5 | TMS | TMS | TMS |
| E6 | V _{CCI} | V _{CCI} | V _{CCI} |
| E7 | V _{CCI} | V _{CCI} | V _{CCI} |
| E8 | V _{CCI} | V _{CCI} | V _{CCI} |
| E9 | V _{CCA} | V _{CCA} | V _{CCA} |
| E10 | I/O | I/O | I/O |
| E11 | GND | GND | GND |
| E12 | I/O | I/O | I/O |
| F1 | I/O | I/O | I/O |
| F2 | I/O | I/O | I/O |
| F3 | NC | NC | NC |
| F4 | I/O | I/O | I/O |
| F5 | GND | GND | GND |
| F6 | GND | GND | GND |
| F7 | GND | GND | GND |
| F8 | V _{CCI} | V _{CCI} | V _{CCI} |
| F9 | I/O | I/O | I/O |
| F10 | GND | GND | GND |
| F11 | I/O | I/O | I/O |
| F12 | I/O | I/O | I/O |

SX-A Family FPGAs

| 144-Pin FBGA | | | |
|--------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| G1 | I/O | I/O | I/O |
| G2 | GND | GND | GND |
| G3 | I/O | I/O | I/O |
| G4 | I/O | I/O | I/O |
| G5 | GND | GND | GND |
| G6 | GND | GND | GND |
| G7 | GND | GND | GND |
| G8 | V _{CCI} | V _{CCI} | V _{CCI} |
| G9 | I/O | I/O | I/O |
| G10 | I/O | I/O | I/O |
| G11 | I/O | I/O | I/O |
| G12 | I/O | I/O | I/O |
| H1 | TRST, I/O | TRST, I/O | TRST, I/O |
| H2 | I/O | I/O | I/O |
| H3 | I/O | I/O | I/O |
| H4 | I/O | I/O | I/O |
| H5 | V _{CCA} | V _{CCA} | V _{CCA} |
| H6 | V _{CCA} | V _{CCA} | V _{CCA} |
| H7 | V _{CCI} | V _{CCI} | V _{CCI} |
| H8 | V _{CCI} | V _{CCI} | V _{CCI} |
| H9 | V _{CCA} | V _{CCA} | V _{CCA} |
| H10 | I/O | I/O | I/O |
| H11 | I/O | I/O | I/O |
| H12 | NC | NC | NC |
| J1 | I/O | I/O | I/O |
| J2 | I/O | I/O | I/O |
| J3 | I/O | I/O | I/O |
| J4 | I/O | I/O | I/O |
| J5 | I/O | I/O | I/O |
| J6 | PRB, I/O | PRB, I/O | PRB, I/O |
| J7 | I/O | I/O | I/O |
| J8 | I/O | I/O | I/O |
| J9 | I/O | I/O | I/O |
| J10 | I/O | I/O | I/O |
| J11 | I/O | I/O | I/O |
| J12 | V _{CCA} | V _{CCA} | V _{CCA} |

| 144-Pin FBGA | | | |
|--------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| K1 | I/O | I/O | I/O |
| K2 | I/O | I/O | I/O |
| K3 | I/O | I/O | I/O |
| K4 | I/O | I/O | I/O |
| K5 | I/O | I/O | I/O |
| K6 | I/O | I/O | I/O |
| K7 | GND | GND | GND |
| K8 | I/O | I/O | I/O |
| K9 | I/O | I/O | I/O |
| K10 | GND | GND | GND |
| K11 | I/O | I/O | I/O |
| K12 | I/O | I/O | I/O |
| L1 | GND | GND | GND |
| L2 | I/O | I/O | I/O |
| L3 | I/O | I/O | I/O |
| L4 | I/O | I/O | I/O |
| L5 | I/O | I/O | I/O |
| L6 | I/O | I/O | I/O |
| L7 | HCLK | HCLK | HCLK |
| L8 | I/O | I/O | I/O |
| L9 | I/O | I/O | I/O |
| L10 | I/O | I/O | I/O |
| L11 | I/O | I/O | I/O |
| L12 | I/O | I/O | I/O |
| M1 | I/O | I/O | I/O |
| M2 | I/O | I/O | I/O |
| M3 | I/O | I/O | I/O |
| M4 | I/O | I/O | I/O |
| M5 | I/O | I/O | I/O |
| M6 | I/O | I/O | I/O |
| M7 | V _{CCA} | V _{CCA} | V _{CCA} |
| M8 | I/O | I/O | I/O |
| M9 | I/O | I/O | I/O |
| M10 | I/O | I/O | I/O |
| M11 | TDO, I/O | TDO, I/O | TDO, I/O |
| M12 | I/O | I/O | I/O |

256-Pin FBGA

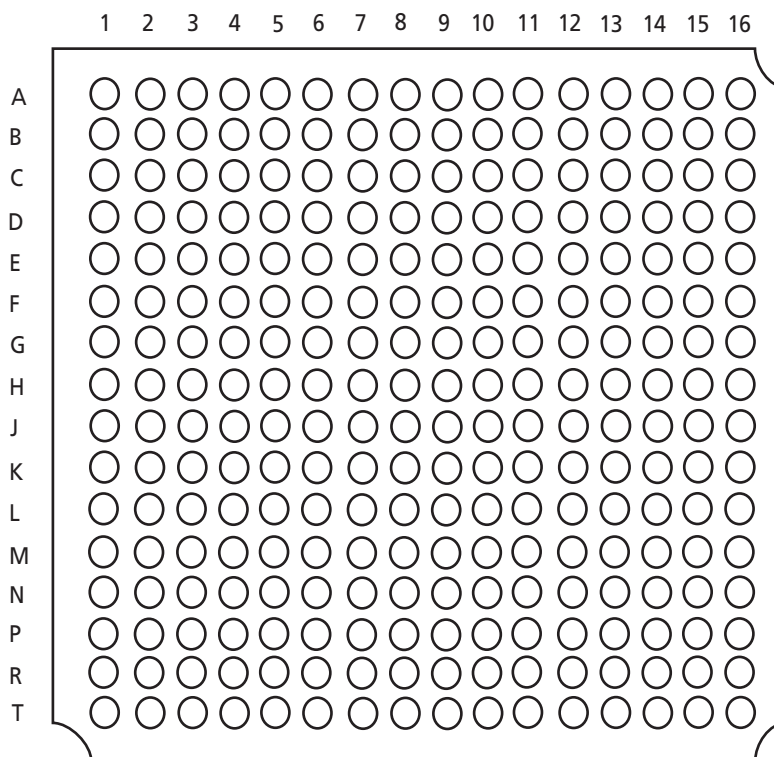


Figure 3-7 • 256-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

SX-A Family FPGAs

| 256-Pin FBGA | | | |
|--------------|----------------------|----------------------|----------------------|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| A1 | GND | GND | GND |
| A2 | TCK, I/O | TCK, I/O | TCK, I/O |
| A3 | I/O | I/O | I/O |
| A4 | I/O | I/O | I/O |
| A5 | I/O | I/O | I/O |
| A6 | I/O | I/O | I/O |
| A7 | I/O | I/O | I/O |
| A8 | I/O | I/O | I/O |
| A9 | CLKB | CLKB | CLKB |
| A10 | I/O | I/O | I/O |
| A11 | I/O | I/O | I/O |
| A12 | NC | I/O | I/O |
| A13 | I/O | I/O | I/O |
| A14 | I/O | I/O | I/O |
| A15 | GND | GND | GND |
| A16 | GND | GND | GND |
| B1 | I/O | I/O | I/O |
| B2 | GND | GND | GND |
| B3 | I/O | I/O | I/O |
| B4 | I/O | I/O | I/O |
| B5 | I/O | I/O | I/O |
| B6 | NC | I/O | I/O |
| B7 | I/O | I/O | I/O |
| B8 | V _{CCA} | V _{CCA} | V _{CCA} |
| B9 | I/O | I/O | I/O |
| B10 | I/O | I/O | I/O |
| B11 | NC | I/O | I/O |
| B12 | I/O | I/O | I/O |
| B13 | I/O | I/O | I/O |
| B14 | I/O | I/O | I/O |
| B15 | GND | GND | GND |
| B16 | I/O | I/O | I/O |
| C1 | I/O | I/O | I/O |
| C2 | TDI, I/O | TDI, I/O | TDI, I/O |
| C3 | GND | GND | GND |
| C4 | I/O | I/O | I/O |
| C5 | NC | I/O | I/O |

| 256-Pin FBGA | | | |
|--------------|----------------------|----------------------|----------------------|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| C6 | I/O | I/O | I/O |
| C7 | I/O | I/O | I/O |
| C8 | I/O | I/O | I/O |
| C9 | CLKA | CLKA | CLKA |
| C10 | I/O | I/O | I/O |
| C11 | I/O | I/O | I/O |
| C12 | I/O | I/O | I/O |
| C13 | I/O | I/O | I/O |
| C14 | I/O | I/O | I/O |
| C15 | I/O | I/O | I/O |
| C16 | I/O | I/O | I/O |
| D1 | I/O | I/O | I/O |
| D2 | I/O | I/O | I/O |
| D3 | I/O | I/O | I/O |
| D4 | I/O | I/O | I/O |
| D5 | I/O | I/O | I/O |
| D6 | I/O | I/O | I/O |
| D7 | I/O | I/O | I/O |
| D8 | PRA, I/O | PRA, I/O | PRA, I/O |
| D9 | I/O | I/O | QCLKD |
| D10 | I/O | I/O | I/O |
| D11 | NC | I/O | I/O |
| D12 | I/O | I/O | I/O |
| D13 | I/O | I/O | I/O |
| D14 | I/O | I/O | I/O |
| D15 | I/O | I/O | I/O |
| D16 | I/O | I/O | I/O |
| E1 | I/O | I/O | I/O |
| E2 | I/O | I/O | I/O |
| E3 | I/O | I/O | I/O |
| E4 | I/O | I/O | I/O |
| E5 | I/O | I/O | I/O |
| E6 | I/O | I/O | I/O |
| E7 | I/O | I/O | QCLKC |
| E8 | I/O | I/O | I/O |
| E9 | I/O | I/O | I/O |
| E10 | I/O | I/O | I/O |

| 256-Pin FBGA | | | |
|--------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| E11 | I/O | I/O | I/O |
| E12 | I/O | I/O | I/O |
| E13 | NC | I/O | I/O |
| E14 | I/O | I/O | I/O |
| E15 | I/O | I/O | I/O |
| E16 | I/O | I/O | I/O |
| F1 | I/O | I/O | I/O |
| F2 | I/O | I/O | I/O |
| F3 | I/O | I/O | I/O |
| F4 | TMS | TMS | TMS |
| F5 | I/O | I/O | I/O |
| F6 | I/O | I/O | I/O |
| F7 | V _{CCI} | V _{CCI} | V _{CCI} |
| F8 | V _{CCI} | V _{CCI} | V _{CCI} |
| F9 | V _{CCI} | V _{CCI} | V _{CCI} |
| F10 | V _{CCI} | V _{CCI} | V _{CCI} |
| F11 | I/O | I/O | I/O |
| F12 | V _{CCA} | V _{CCA} | V _{CCA} |
| F13 | I/O | I/O | I/O |
| F14 | I/O | I/O | I/O |
| F15 | I/O | I/O | I/O |
| F16 | I/O | I/O | I/O |
| G1 | NC | I/O | I/O |
| G2 | I/O | I/O | I/O |
| G3 | NC | I/O | I/O |
| G4 | I/O | I/O | I/O |
| G5 | I/O | I/O | I/O |
| G6 | V _{CCI} | V _{CCI} | V _{CCI} |
| G7 | GND | GND | GND |
| G8 | GND | GND | GND |
| G9 | GND | GND | GND |
| G10 | GND | GND | GND |
| G11 | V _{CCI} | V _{CCI} | V _{CCI} |
| G12 | I/O | I/O | I/O |
| G13 | GND | GND | GND |
| G14 | NC | I/O | I/O |
| G15 | V _{CCA} | V _{CCA} | V _{CCA} |

| 256-Pin FBGA | | | |
|--------------|-------------------|-------------------|-------------------|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| G16 | I/O | I/O | I/O |
| H1 | I/O | I/O | I/O |
| H2 | I/O | I/O | I/O |
| H3 | V _{CCA} | V _{CCA} | V _{CCA} |
| H4 | TRST, I/O | TRST, I/O | TRST, I/O |
| H5 | I/O | I/O | I/O |
| H6 | V _{CCI} | V _{CCI} | V _{CCI} |
| H7 | GND | GND | GND |
| H8 | GND | GND | GND |
| H9 | GND | GND | GND |
| H10 | GND | GND | GND |
| H11 | V _{CCI} | V _{CCI} | V _{CCI} |
| H12 | I/O | I/O | I/O |
| H13 | I/O | I/O | I/O |
| H14 | I/O | I/O | I/O |
| H15 | I/O | I/O | I/O |
| H16 | NC | I/O | I/O |
| J1 | NC | I/O | I/O |
| J2 | NC | I/O | I/O |
| J3 | NC | I/O | I/O |
| J4 | I/O | I/O | I/O |
| J5 | I/O | I/O | I/O |
| J6 | V _{CCI} | V _{CCI} | V _{CCI} |
| J7 | GND | GND | GND |
| J8 | GND | GND | GND |
| J9 | GND | GND | GND |
| J10 | GND | GND | GND |
| J11 | V _{CCI} | V _{CCI} | V _{CCI} |
| J12 | I/O | I/O | I/O |
| J13 | I/O | I/O | I/O |
| J14 | I/O | I/O | I/O |
| J15 | I/O | I/O | I/O |
| J16 | I/O | I/O | I/O |
| K1 | I/O | I/O | I/O |
| K2 | I/O | I/O | I/O |
| K3 | NC | I/O | I/O |
| K4 | V _{CCA} | V _{CCA} | V _{CCA} |

SX-A Family FPGAs

| 256-Pin FBGA | | | |
|--------------|----------------------|----------------------|----------------------|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| K5 | I/O | I/O | I/O |
| K6 | V _{CCI} | V _{CCI} | V _{CCI} |
| K7 | GND | GND | GND |
| K8 | GND | GND | GND |
| K9 | GND | GND | GND |
| K10 | GND | GND | GND |
| K11 | V _{CCI} | V _{CCI} | V _{CCI} |
| K12 | I/O | I/O | I/O |
| K13 | I/O | I/O | I/O |
| K14 | I/O | I/O | I/O |
| K15 | NC | I/O | I/O |
| K16 | I/O | I/O | I/O |
| L1 | I/O | I/O | I/O |
| L2 | I/O | I/O | I/O |
| L3 | I/O | I/O | I/O |
| L4 | I/O | I/O | I/O |
| L5 | I/O | I/O | I/O |
| L6 | I/O | I/O | I/O |
| L7 | V _{CCI} | V _{CCI} | V _{CCI} |
| L8 | V _{CCI} | V _{CCI} | V _{CCI} |
| L9 | V _{CCI} | V _{CCI} | V _{CCI} |
| L10 | V _{CCI} | V _{CCI} | V _{CCI} |
| L11 | I/O | I/O | I/O |
| L12 | I/O | I/O | I/O |
| L13 | I/O | I/O | I/O |
| L14 | I/O | I/O | I/O |
| L15 | I/O | I/O | I/O |
| L16 | NC | I/O | I/O |
| M1 | I/O | I/O | I/O |
| M2 | I/O | I/O | I/O |
| M3 | I/O | I/O | I/O |
| M4 | I/O | I/O | I/O |
| M5 | I/O | I/O | I/O |
| M6 | I/O | I/O | I/O |
| M7 | I/O | I/O | QCLKA |
| M8 | PRB, I/O | PRB, I/O | PRB, I/O |
| M9 | I/O | I/O | I/O |

| 256-Pin FBGA | | | |
|--------------|----------------------|----------------------|----------------------|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| M10 | I/O | I/O | I/O |
| M11 | I/O | I/O | I/O |
| M12 | NC | I/O | I/O |
| M13 | I/O | I/O | I/O |
| M14 | NC | I/O | I/O |
| M15 | I/O | I/O | I/O |
| M16 | I/O | I/O | I/O |
| N1 | I/O | I/O | I/O |
| N2 | I/O | I/O | I/O |
| N3 | I/O | I/O | I/O |
| N4 | I/O | I/O | I/O |
| N5 | I/O | I/O | I/O |
| N6 | I/O | I/O | I/O |
| N7 | I/O | I/O | I/O |
| N8 | I/O | I/O | I/O |
| N9 | I/O | I/O | I/O |
| N10 | I/O | I/O | I/O |
| N11 | I/O | I/O | I/O |
| N12 | I/O | I/O | I/O |
| N13 | I/O | I/O | I/O |
| N14 | I/O | I/O | I/O |
| N15 | I/O | I/O | I/O |
| N16 | I/O | I/O | I/O |
| P1 | I/O | I/O | I/O |
| P2 | GND | GND | GND |
| P3 | I/O | I/O | I/O |
| P4 | I/O | I/O | I/O |
| P5 | NC | I/O | I/O |
| P6 | I/O | I/O | I/O |
| P7 | I/O | I/O | I/O |
| P8 | I/O | I/O | I/O |
| P9 | I/O | I/O | I/O |
| P10 | NC | I/O | I/O |
| P11 | I/O | I/O | I/O |
| P12 | I/O | I/O | I/O |
| P13 | V _{CCA} | V _{CCA} | V _{CCA} |
| P14 | I/O | I/O | I/O |

| 256-Pin FBGA | | | |
|--------------|----------------------|----------------------|----------------------|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| P15 | I/O | I/O | I/O |
| P16 | I/O | I/O | I/O |
| R1 | I/O | I/O | I/O |
| R2 | GND | GND | GND |
| R3 | I/O | I/O | I/O |
| R4 | NC | I/O | I/O |
| R5 | I/O | I/O | I/O |
| R6 | I/O | I/O | I/O |
| R7 | I/O | I/O | I/O |
| R8 | I/O | I/O | I/O |
| R9 | HCLK | HCLK | HCLK |
| R10 | I/O | I/O | QCLKB |
| R11 | I/O | I/O | I/O |
| R12 | I/O | I/O | I/O |
| R13 | I/O | I/O | I/O |
| R14 | I/O | I/O | I/O |
| R15 | GND | GND | GND |
| R16 | GND | GND | GND |
| T1 | GND | GND | GND |
| T2 | I/O | I/O | I/O |
| T3 | I/O | I/O | I/O |
| T4 | NC | I/O | I/O |
| T5 | I/O | I/O | I/O |
| T6 | I/O | I/O | I/O |
| T7 | I/O | I/O | I/O |
| T8 | I/O | I/O | I/O |
| T9 | V _{CCA} | V _{CCA} | V _{CCA} |
| T10 | I/O | I/O | I/O |
| T11 | I/O | I/O | I/O |
| T12 | NC | I/O | I/O |
| T13 | I/O | I/O | I/O |
| T14 | I/O | I/O | I/O |
| T15 | TDO, I/O | TDO, I/O | TDO, I/O |
| T16 | GND | GND | GND |

484-Pin FBGA



Figure 3-8 • 484-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| A1 | NC* | NC |
| A2 | NC* | NC |
| A3 | NC* | I/O |
| A4 | NC* | I/O |
| A5 | NC* | I/O |
| A6 | I/O | I/O |
| A7 | I/O | I/O |
| A8 | I/O | I/O |
| A9 | I/O | I/O |
| A10 | I/O | I/O |
| A11 | NC* | I/O |
| A12 | NC* | I/O |
| A13 | I/O | I/O |
| A14 | NC* | NC |
| A15 | NC* | I/O |
| A16 | NC* | I/O |
| A17 | I/O | I/O |
| A18 | I/O | I/O |
| A19 | I/O | I/O |
| A20 | I/O | I/O |
| A21 | NC* | I/O |
| A22 | NC* | I/O |
| A23 | NC* | I/O |
| A24 | NC* | I/O |
| A25 | NC* | NC |
| A26 | NC* | NC |
| AA1 | NC* | I/O |
| AA2 | NC* | I/O |
| AA3 | V _{CCA} | V _{CCA} |
| AA4 | I/O | I/O |
| AA5 | I/O | I/O |
| AA22 | I/O | I/O |
| AA23 | I/O | I/O |
| AA24 | I/O | I/O |
| AA25 | NC* | I/O |

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| AA26 | NC* | I/O |
| AB1 | NC* | NC |
| AB2 | V _{CCI} | V _{CCI} |
| AB3 | I/O | I/O |
| AB4 | I/O | I/O |
| AB5 | NC* | I/O |
| AB6 | I/O | I/O |
| AB7 | I/O | I/O |
| AB8 | I/O | I/O |
| AB9 | I/O | I/O |
| AB10 | I/O | I/O |
| AB11 | I/O | I/O |
| AB12 | PRB, I/O | PRB, I/O |
| AB13 | V _{CCA} | V _{CCA} |
| AB14 | I/O | I/O |
| AB15 | I/O | I/O |
| AB16 | I/O | I/O |
| AB17 | I/O | I/O |
| AB18 | I/O | I/O |
| AB19 | I/O | I/O |
| AB20 | TDO, I/O | TDO, I/O |
| AB21 | GND | GND |
| AB22 | NC* | I/O |
| AB23 | I/O | I/O |
| AB24 | I/O | I/O |
| AB25 | NC* | I/O |
| AB26 | NC* | I/O |
| AC1 | I/O | I/O |
| AC2 | I/O | I/O |
| AC3 | I/O | I/O |
| AC4 | NC* | I/O |
| AC5 | V _{CCI} | V _{CCI} |
| AC6 | I/O | I/O |
| AC7 | V _{CCI} | V _{CCI} |
| AC8 | I/O | I/O |

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| AC9 | I/O | I/O |
| AC10 | I/O | I/O |
| AC11 | I/O | I/O |
| AC12 | I/O | QCLKA |
| AC13 | I/O | I/O |
| AC14 | I/O | I/O |
| AC15 | I/O | I/O |
| AC16 | I/O | I/O |
| AC17 | I/O | I/O |
| AC18 | I/O | I/O |
| AC19 | I/O | I/O |
| AC20 | V _{CCI} | V _{CCI} |
| AC21 | I/O | I/O |
| AC22 | I/O | I/O |
| AC23 | NC* | I/O |
| AC24 | I/O | I/O |
| AC25 | NC* | I/O |
| AC26 | NC* | I/O |
| AD1 | I/O | I/O |
| AD2 | I/O | I/O |
| AD3 | GND | GND |
| AD4 | I/O | I/O |
| AD5 | I/O | I/O |
| AD6 | I/O | I/O |
| AD7 | I/O | I/O |
| AD8 | I/O | I/O |
| AD9 | V _{CCI} | V _{CCI} |
| AD10 | I/O | I/O |
| AD11 | I/O | I/O |
| AD12 | I/O | I/O |
| AD13 | V _{CCI} | V _{CCI} |
| AD14 | I/O | I/O |
| AD15 | I/O | I/O |
| AD16 | I/O | I/O |
| AD17 | V _{CCI} | V _{CCI} |

Note: *These pins must be left floating on the A54SX32A device.

SX-A Family FPGAs

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| AD18 | I/O | I/O |
| AD19 | I/O | I/O |
| AD20 | I/O | I/O |
| AD21 | I/O | I/O |
| AD22 | I/O | I/O |
| AD23 | V _{CCI} | V _{CCI} |
| AD24 | NC* | I/O |
| AD25 | NC* | I/O |
| AD26 | NC* | I/O |
| AE1 | NC* | NC |
| AE2 | I/O | I/O |
| AE3 | NC* | I/O |
| AE4 | NC* | I/O |
| AE5 | NC* | I/O |
| AE6 | NC* | I/O |
| AE7 | I/O | I/O |
| AE8 | I/O | I/O |
| AE9 | I/O | I/O |
| AE10 | I/O | I/O |
| AE11 | NC* | I/O |
| AE12 | I/O | I/O |
| AE13 | I/O | I/O |
| AE14 | I/O | I/O |
| AE15 | NC* | I/O |
| AE16 | NC* | I/O |
| AE17 | I/O | I/O |
| AE18 | I/O | I/O |
| AE19 | I/O | I/O |
| AE20 | I/O | I/O |
| AE21 | NC* | I/O |
| AE22 | NC* | I/O |
| AE23 | NC* | I/O |
| AE24 | NC* | I/O |
| AE25 | NC* | NC |
| AE26 | NC* | NC |

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| AF1 | NC* | NC |
| AF2 | NC* | NC |
| AF3 | NC | I/O |
| AF4 | NC* | I/O |
| AF5 | NC* | I/O |
| AF6 | NC* | I/O |
| AF7 | I/O | I/O |
| AF8 | I/O | I/O |
| AF9 | I/O | I/O |
| AF10 | I/O | I/O |
| AF11 | NC* | I/O |
| AF12 | NC* | NC |
| AF13 | HCLK | HCLK |
| AF14 | I/O | QCLKB |
| AF15 | NC* | I/O |
| AF16 | NC* | I/O |
| AF17 | I/O | I/O |
| AF18 | I/O | I/O |
| AF19 | I/O | I/O |
| AF20 | NC* | I/O |
| AF21 | NC* | I/O |
| AF22 | NC* | I/O |
| AF23 | NC* | I/O |
| AF24 | NC* | I/O |
| AF25 | NC* | NC |
| AF26 | NC* | NC |
| B1 | NC* | NC |
| B2 | NC* | NC |
| B3 | NC* | I/O |
| B4 | NC* | I/O |
| B5 | NC* | I/O |
| B6 | I/O | I/O |
| B7 | I/O | I/O |
| B8 | I/O | I/O |
| B9 | I/O | I/O |

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| B10 | I/O | I/O |
| B11 | NC* | I/O |
| B12 | NC* | I/O |
| B13 | V _{CCI} | V _{CCI} |
| B14 | CLKA | CLKA |
| B15 | NC* | I/O |
| B16 | NC* | I/O |
| B17 | I/O | I/O |
| B18 | V _{CCI} | V _{CCI} |
| B19 | I/O | I/O |
| B20 | I/O | I/O |
| B21 | NC* | I/O |
| B22 | NC* | I/O |
| B23 | NC* | I/O |
| B24 | NC* | I/O |
| B25 | I/O | I/O |
| B26 | NC* | NC |
| C1 | NC* | I/O |
| C2 | NC* | I/O |
| C3 | NC* | I/O |
| C4 | NC* | I/O |
| C5 | I/O | I/O |
| C6 | V _{CCI} | V _{CCI} |
| C7 | I/O | I/O |
| C8 | I/O | I/O |
| C9 | V _{CCI} | V _{CCI} |
| C10 | I/O | I/O |
| C11 | I/O | I/O |
| C12 | I/O | I/O |
| C13 | PRA, I/O | PRA, I/O |
| C14 | I/O | I/O |
| C15 | I/O | QCLKD |
| C16 | I/O | I/O |
| C17 | I/O | I/O |
| C18 | I/O | I/O |

Note: *These pins must be left floating on the A54SX32A device.

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| C19 | I/O | I/O |
| C20 | V _{CCI} | V _{CCI} |
| C21 | I/O | I/O |
| C22 | I/O | I/O |
| C23 | I/O | I/O |
| C24 | I/O | I/O |
| C25 | NC* | I/O |
| C26 | NC* | I/O |
| D1 | NC* | I/O |
| D2 | TMS | TMS |
| D3 | I/O | I/O |
| D4 | V _{CCI} | V _{CCI} |
| D5 | NC* | I/O |
| D6 | TCK, I/O | TCK, I/O |
| D7 | I/O | I/O |
| D8 | I/O | I/O |
| D9 | I/O | I/O |
| D10 | I/O | I/O |
| D11 | I/O | I/O |
| D12 | I/O | QCLKC |
| D13 | I/O | I/O |
| D14 | I/O | I/O |
| D15 | I/O | I/O |
| D16 | I/O | I/O |
| D17 | I/O | I/O |
| D18 | I/O | I/O |
| D19 | I/O | I/O |
| D20 | I/O | I/O |
| D21 | V _{CCI} | V _{CCI} |
| D22 | GND | GND |
| D23 | I/O | I/O |
| D24 | I/O | I/O |
| D25 | NC* | I/O |
| D26 | NC* | I/O |
| E1 | NC* | I/O |

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| E2 | NC* | I/O |
| E3 | I/O | I/O |
| E4 | I/O | I/O |
| E5 | GND | GND |
| E6 | TDI, IO | TDI, IO |
| E7 | I/O | I/O |
| E8 | I/O | I/O |
| E9 | I/O | I/O |
| E10 | I/O | I/O |
| E11 | I/O | I/O |
| E12 | I/O | I/O |
| E13 | V _{CCA} | V _{CCA} |
| E14 | CLKB | CLKB |
| E15 | I/O | I/O |
| E16 | I/O | I/O |
| E17 | I/O | I/O |
| E18 | I/O | I/O |
| E19 | I/O | I/O |
| E20 | I/O | I/O |
| E21 | I/O | I/O |
| E22 | I/O | I/O |
| E23 | I/O | I/O |
| E24 | I/O | I/O |
| E25 | V _{CCI} | V _{CCI} |
| E26 | GND | GND |
| F1 | V _{CCI} | V _{CCI} |
| F2 | NC* | I/O |
| F3 | NC* | I/O |
| F4 | I/O | I/O |
| F5 | I/O | I/O |
| F22 | I/O | I/O |
| F23 | I/O | I/O |
| F24 | I/O | I/O |
| F25 | I/O | I/O |
| F26 | NC* | I/O |

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| G1 | NC* | I/O |
| G2 | NC* | I/O |
| G3 | NC* | I/O |
| G4 | I/O | I/O |
| G5 | I/O | I/O |
| G22 | I/O | I/O |
| G23 | V _{CCA} | V _{CCA} |
| G24 | I/O | I/O |
| G25 | NC* | I/O |
| G26 | NC* | I/O |
| H1 | NC* | I/O |
| H2 | NC* | I/O |
| H3 | I/O | I/O |
| H4 | I/O | I/O |
| H5 | I/O | I/O |
| H22 | I/O | I/O |
| H23 | I/O | I/O |
| H24 | I/O | I/O |
| H25 | NC* | I/O |
| H26 | NC* | I/O |
| J1 | NC* | I/O |
| J2 | NC* | I/O |
| J3 | I/O | I/O |
| J4 | I/O | I/O |
| J5 | I/O | I/O |
| J22 | I/O | I/O |
| J23 | I/O | I/O |
| J24 | I/O | I/O |
| J25 | V _{CCI} | V _{CCI} |
| J26 | NC* | I/O |
| K1 | I/O | I/O |
| K2 | V _{CCI} | V _{CCI} |
| K3 | I/O | I/O |
| K4 | I/O | I/O |
| K5 | V _{CCA} | V _{CCA} |

Note: *These pins must be left floating on the A54SX32A device.

SX-A Family FPGAs

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| K10 | GND | GND |
| K11 | GND | GND |
| K12 | GND | GND |
| K13 | GND | GND |
| K14 | GND | GND |
| K15 | GND | GND |
| K16 | GND | GND |
| K17 | GND | GND |
| K22 | I/O | I/O |
| K23 | I/O | I/O |
| K24 | NC* | NC |
| K25 | NC* | I/O |
| K26 | NC* | I/O |
| L1 | NC* | I/O |
| L2 | NC* | I/O |
| L3 | I/O | I/O |
| L4 | I/O | I/O |
| L5 | I/O | I/O |
| L10 | GND | GND |
| L11 | GND | GND |
| L12 | GND | GND |
| L13 | GND | GND |
| L14 | GND | GND |
| L15 | GND | GND |
| L16 | GND | GND |
| L17 | GND | GND |
| L22 | I/O | I/O |
| L23 | I/O | I/O |
| L24 | I/O | I/O |
| L25 | I/O | I/O |
| L26 | I/O | I/O |
| M1 | NC* | NC |
| M2 | I/O | I/O |
| M3 | I/O | I/O |
| M4 | I/O | I/O |

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| M5 | I/O | I/O |
| M10 | GND | GND |
| M11 | GND | GND |
| M12 | GND | GND |
| M13 | GND | GND |
| M14 | GND | GND |
| M15 | GND | GND |
| M16 | GND | GND |
| M17 | GND | GND |
| M22 | I/O | I/O |
| M23 | I/O | I/O |
| M24 | I/O | I/O |
| M25 | NC* | I/O |
| M26 | NC* | I/O |
| N1 | I/O | I/O |
| N2 | V _{CCI} | V _{CCI} |
| N3 | I/O | I/O |
| N4 | I/O | I/O |
| N5 | I/O | I/O |
| N10 | GND | GND |
| N11 | GND | GND |
| N12 | GND | GND |
| N13 | GND | GND |
| N14 | GND | GND |
| N15 | GND | GND |
| N16 | GND | GND |
| N17 | GND | GND |
| N22 | V _{CCA} | V _{CCA} |
| N23 | I/O | I/O |
| N24 | I/O | I/O |
| N25 | I/O | I/O |
| N26 | NC* | NC |
| P1 | NC* | I/O |
| P2 | NC* | I/O |
| P3 | I/O | I/O |

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| P4 | I/O | I/O |
| P5 | V _{CCA} | V _{CCA} |
| P10 | GND | GND |
| P11 | GND | GND |
| P12 | GND | GND |
| P13 | GND | GND |
| P14 | GND | GND |
| P15 | GND | GND |
| P16 | GND | GND |
| P17 | GND | GND |
| P22 | I/O | I/O |
| P23 | I/O | I/O |
| P24 | V _{CCI} | V _{CCI} |
| P25 | I/O | I/O |
| P26 | I/O | I/O |
| R1 | NC* | I/O |
| R2 | NC* | I/O |
| R3 | I/O | I/O |
| R4 | I/O | I/O |
| R5 | TRST, I/O | TRST, I/O |
| R10 | GND | GND |
| R11 | GND | GND |
| R12 | GND | GND |
| R13 | GND | GND |
| R14 | GND | GND |
| R15 | GND | GND |
| R16 | GND | GND |
| R17 | GND | GND |
| R22 | I/O | I/O |
| R23 | I/O | I/O |
| R24 | I/O | I/O |
| R25 | NC* | I/O |
| R26 | NC* | I/O |
| T1 | NC* | I/O |
| T2 | NC* | I/O |

Note: *These pins must be left floating on the A54SX32A device.

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| T3 | I/O | I/O |
| T4 | I/O | I/O |
| T5 | I/O | I/O |
| T10 | GND | GND |
| T11 | GND | GND |
| T12 | GND | GND |
| T13 | GND | GND |
| T14 | GND | GND |
| T15 | GND | GND |
| T16 | GND | GND |
| T17 | GND | GND |
| T22 | I/O | I/O |
| T23 | I/O | I/O |
| T24 | I/O | I/O |
| T25 | NC* | I/O |
| T26 | NC* | I/O |
| U1 | I/O | I/O |
| U2 | V _{CCI} | V _{CCI} |
| U3 | I/O | I/O |
| U4 | I/O | I/O |
| U5 | I/O | I/O |
| U10 | GND | GND |
| U11 | GND | GND |
| U12 | GND | GND |
| U13 | GND | GND |
| U14 | GND | GND |
| U15 | GND | GND |
| U16 | GND | GND |
| U17 | GND | GND |
| U22 | I/O | I/O |
| U23 | I/O | I/O |
| U24 | I/O | I/O |
| U25 | V _{CCI} | V _{CCI} |
| U26 | I/O | I/O |
| V1 | NC* | I/O |

| 484-Pin FBGA | | |
|--------------|-------------------|-------------------|
| Pin Number | A54SX32A Function | A54SX72A Function |
| V2 | NC* | I/O |
| V3 | I/O | I/O |
| V4 | I/O | I/O |
| V5 | I/O | I/O |
| V22 | V _{CCA} | V _{CCA} |
| V23 | I/O | I/O |
| V24 | I/O | I/O |
| V25 | NC* | I/O |
| V26 | NC* | I/O |
| W1 | I/O | I/O |
| W2 | I/O | I/O |
| W3 | I/O | I/O |
| W4 | I/O | I/O |
| W5 | I/O | I/O |
| W22 | I/O | I/O |
| W23 | V _{CCA} | V _{CCA} |
| W24 | I/O | I/O |
| W25 | NC* | I/O |
| W26 | NC* | I/O |
| Y1 | NC* | I/O |
| Y2 | NC* | I/O |
| Y3 | I/O | I/O |
| Y4 | I/O | I/O |
| Y5 | NC* | I/O |
| Y22 | I/O | I/O |
| Y23 | I/O | I/O |
| Y24 | V _{CCI} | V _{CCI} |
| Y25 | I/O | I/O |
| Y26 | I/O | I/O |

Note: *These pins must be left floating on the A54SX32A device.

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v5.3) | Page |
|-------------------------|---|-------|
| v5.2 (June 2006) | –3 speed grades have been discontinued. | N/A |
| | The "SX-A Timing Model" was updated with –2 data. | 2-14 |
| v5.1 February 2005 | RoHS information was added to the "Ordering Information". | ii |
| | The "Programming" section was updated. | 1-13 |
| v5.0 | Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device. | i |
| | The "Thermal Characteristics" section was updated. | 2-11 |
| | The "176-Pin TQFP" was updated to add pins 81 to 90. | 3-11 |
| | The "484-Pin FBGA" was updated to add pins R4 to Y26 | 3-26 |
| v4.0 | The "Temperature Grade Offering" is new. | 1-iii |
| | The "Speed Grade and Temperature Grade Matrix" is new. | 1-iii |
| | "SX-A Family Architecture" was updated. | 1-1 |
| | "Clock Resources" was updated. | 1-5 |
| | "User Security" was updated. | 1-7 |
| | "Power-Up/Down and Hot Swapping" was updated. | 1-7 |
| | "Dedicated Mode" is new | 1-9 |
| | Table 1-5 is new. | 1-9 |
| | "JTAG Instructions" is new | 1-10 |
| | "Design Considerations" was updated. | 1-12 |
| | The "Programming" section is new. | 1-13 |
| | "Design Environment" was updated. | 1-13 |
| | "Pin Description" was updated. | 1-15 |
| | Table 2-1 was updated. | 2-1 |
| | Table 2-2 was updated. | 2-1 |
| | Table 2-3 is new. | 2-1 |
| | Table 2-4 is new. | 2-1 |
| | Table 2-5 was updated. | 2-2 |
| | Table 2-6 was updated. | 2-2 |
| | "Power Dissipation" is new. | 2-8 |
| Table 2-11 was updated. | 2-9 | |

SX-A Family FPGAs

| Previous Version | Changes in Current Version (v5.3) | Page |
|--|---|--------------|
| v4.0 (continued) | Table 2-12 was updated. | 2-11 |
| | The was updated. | 2-14 |
| | The "Sample Path Calculations" were updated. | 2-14 |
| | Table 2-13 was updated. | 2-17 |
| | Table 2-13 was updated. | 2-17 |
| | All timing tables were updated. | 2-18 to 2-52 |
| v3.0 | The "Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft" section was updated. | 1-i |
| | The "Ordering Information" section was updated. | 1-ii |
| | The "Temperature Grade Offering" section was updated. | 1-iii |
| | The Figure 1-1 • SX-A Family Interconnect Elements was updated. | 1-1 |
| | The "Clock Resources" section was updated | 1-5 |
| | The Table 1-1 • SX-A Clock Resources is new. | 1-5 |
| | The "User Security" section is new. | 1-7 |
| | The "I/O Modules" section was updated. | 1-7 |
| | The Table 1-2 • I/O Features was updated. | 1-8 |
| | The Table 1-3 • I/O Characteristics for All I/O Configurations is new. | 1-8 |
| | The Table 1-4 • Power-Up Time at which I/Os Become Active is new | 1-8 |
| | The Figure 1-12 • Device Selection Wizard is new. | 1-9 |
| | The "Boundary-Scan Pin Configurations and Functions" section is new. | 1-9 |
| | The Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved) is new. | 1-11 |
| | The "SX-A Probe Circuit Control Pins" section was updated. | 1-12 |
| | The "Design Considerations" section was updated. | 1-12 |
| | The Figure 1-13 • Probe Setup was updated. | 1-12 |
| | The Design Environment was updated. | 1-13 |
| | The Figure 1-13 • Design Flow is new. | 1-11 |
| | The "Absolute Maximum Ratings*" section was updated. | 1-12 |
| | The "Recommended Operating Conditions" section was updated. | 1-12 |
| | The "Electrical Specifications" section was updated. | 1-12 |
| | The "2.5V LVCMOS2 Electrical Specifications" section was updated. | 1-13 |
| | The "SX-A Timing Model" and "Sample Path Calculations" equations were updated. | 1-23 |
| The "Pin Description" section was updated. | 1-15 | |
| v2.0.1 | The "Design Environment" section has been updated. | 1-13 |
| | The "I/O Modules" section, and Table 1-2 • I/O Features have been updated. | 1-8 |
| | The "SX-A Timing Model" section and the "Timing Characteristics" section have new timing numbers. | 1-23 |

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

The products described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR) or the Export Administration Regulations (EAR). They may require an approved export license prior to their export. An export can include a release or disclosure to a foreign national inside or outside the United States.

Actel and the Actel logo are registered trademarks of Actel Corporation.
All other trademarks are the property of their owners.



www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA

Phone 650.318.4200

Fax 650.318.4600

Actel Europe Ltd.

River Court, Meadows Business Park
Station Approach, Blackwater
Camberley, Surrey GU17 9AB
United Kingdom

Phone +44 (0) 1276 609 300

Fax +44 (0) 1276 607 540

Actel Japan

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan

Phone +81.03.3445.7671

Fax +81.03.3445.7668

www.jp.actel.com

Actel Hong Kong

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong

Phone +852 2185 6460

Fax +852 2185 6488

www.actel.com.cn

OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we stricly control the quality of products and services. Welcome your RFQ to

Email: Info@DiGi-Electronics.com



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.