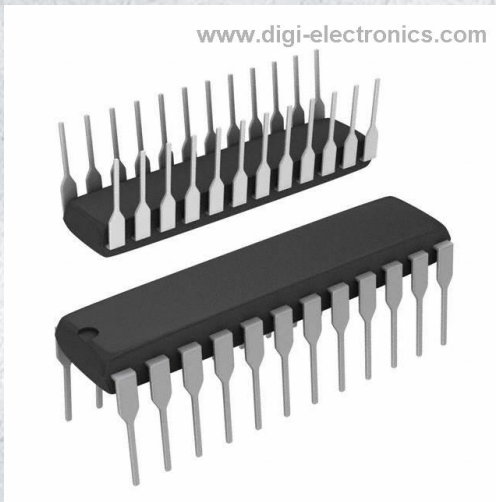


ATF22LV10C-10PI Datasheet



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|--|
| DiGi Electronics Part Number | ATF22LV10C-10PI-DG |
| Manufacturer | Microchip Technology |
| Manufacturer Product Number | ATF22LV10C-10PI |
| Description | IC PLD 10MC 10NS 24DIP |
| Detailed Description | 22V10 Programmable Logic Device (PLD) IC 10 Mac rocells 24-PDIP |

This model ATF22LV10C-10PI is available at DiGi Electronics.

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Purchase and inquiry

Manufacturer Product Number:

ATF22LV10C-10PI

Series:

22V10

DiGi-Electronics Programmable:

Not Verified

Number of Macrocells:

10

Speed:

10 ns

Package / Case:

24-DIP (0.300", 7.62mm)

Base Product Number:

ATF22LV10C

Manufacturer:

Microchip Technology

Product Status:

Obsolete

Programmable Type:

EE PLD

Voltage - Input:

3.3V

Mounting Type:

Through Hole

Supplier Device Package:

24-PDIP

Environmental & Export classification

RoHS Status:

RoHS non-compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

Features

- 3.0V to 5.5V Operating Range
- Advanced Low-voltage Electrically-erasable Programmable Logic Device
- User-controlled Power-down Pin Option
- Pin-controlled Standby Power (10 μ A Typical)
- Well-suited for Battery Powered Systems
- 10ns Maximum Propagation Delay
- CMOS and TTL Compatible Inputs and Outputs
- Latch Feature Hold Inputs to Previous Logic States
- Advanced Electrically-erasable Technology
 - Reprogrammable
 - 100% Tested
- High-reliability CMOS Process
 - 20 year Data Retention
 - 100 Erase/Write Cycles
 - 2,000V ESD Protection
 - 200mA Latchup Immunity
- Industrial Temperature Ranges
- Dual-in-line and Surface Mount Packages in Standard Pinouts
- Inputs are 5V Tolerant
- Green Package Options (Pb/Halide-free/RoHS Compliant) Available
- Applications include Glue logic for 3.3V systems, DMA Control, State Machine Control, Graphics processing

1. Description

The Atmel[®] ATF22LV10C is a high-performance CMOS (electrically erasable) programmable logic device (PLD) that utilizes the Atmel proven electrically erasable Flash memory technology. Speeds down to 10ns and power dissipation as low as 10mA are offered. All speed ranges are specified over the 3.0V to 5.5V range for industrial and commercial temperature ranges.

The ATF22LV10C provides a low-voltage and user controlled “zero” power CMOS PLD solution. A user-controlled power-down feature offers “zero” (10 μ A typical) standby power. This feature allows the user to manage total system power to meet specific application requirements and enhance reliability, all without sacrificing speed. (The Atmel ATF22LV10CQZ provides edge-sensing “zero” standby power (3 μ A typical), as well as low voltage operation. See the ATF22LV10CQZ datasheet.)

The ATF22LV10C is capable of operating at supply voltages down to 3.0V. When the power-down pin is active, the device is placed into a zero standby power-down mode. When the power-down pin is not used or active, the device operates in a full power low voltage mode. Pin “keeper” circuits on input and output pins hold pins to their previous logic levels when idle, which eliminate static power consumed by pull-up resistors.

The ATF22LV10C macrocell incorporates a variable product term architecture. Each output is allocated from 8 to 16 product terms which allows highly-complex logic functions to be realized. Two additional product terms are included to provide synchronous reset and asynchronous reset. These additional product terms are common to all ten registers and are automatically cleared upon power-up. Register preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.



High-performance Electrically Erasable Programmable Logic Device

Atmel ATF22LV10C

See separate datasheet for Atmel
ATF22LV10C(Q)Z option



Figure 1-1. Block Diagram

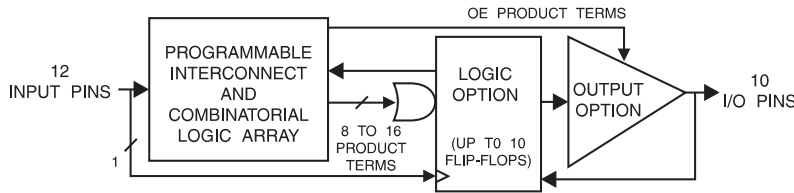


Figure 1-2. Pin Configurations

Pin Configurations (All Pinouts Top View)

| Pin Name | Function |
|----------|-------------------------|
| CLK | Clock |
| IN | Logic Inputs |
| I/O | Bi-directional Buffers |
| VCC | (3V to 5.5V) Supply |
| PD | Programmable Power-down |

Figure 1-3. TSSOP

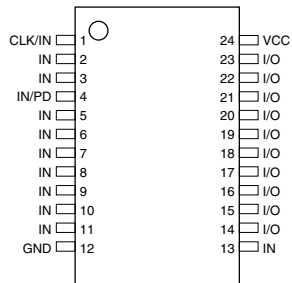


Figure 1-4. DIP/SOIC

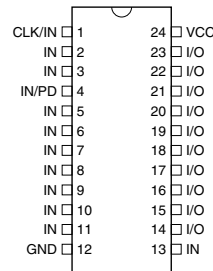
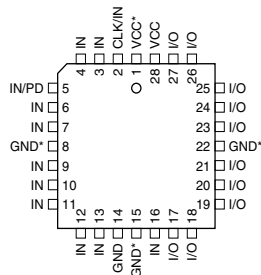


Figure 1-5. PLCC



Note: For PLCC, pins 1, 8, 15, and 22 can be left unconnected. For superior performance, connect VCC to pin 1 and GND to 8, 15, and 22

2. Absolute Maximum Ratings*

| | |
|--|--------------------------------|
| Temperature Under Bias | -40°C to +85°C |
| Storage Temperature..... | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground..... | -2.0V to +7.0V ⁽¹⁾ |
| Voltage on Input Pins with Respect to Ground During Programming..... | -2.0V to +14.0V ⁽¹⁾ |
| Programming Voltage with Respect to Ground..... | -2.0V to +14.0V ⁽¹⁾ |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC, which may overshoot to 7.0V for pulses of less than 20ns.

3. DC and AC Operating Conditions

| | Commercial | Industrial |
|---------------------------------|-------------|--------------|
| Operating Temperature (Ambient) | 0°C - 70°C | -40°C - 85°C |
| V_{CC} Power Supply | 3.0V - 5.5V | 3.0V - 5.5V |

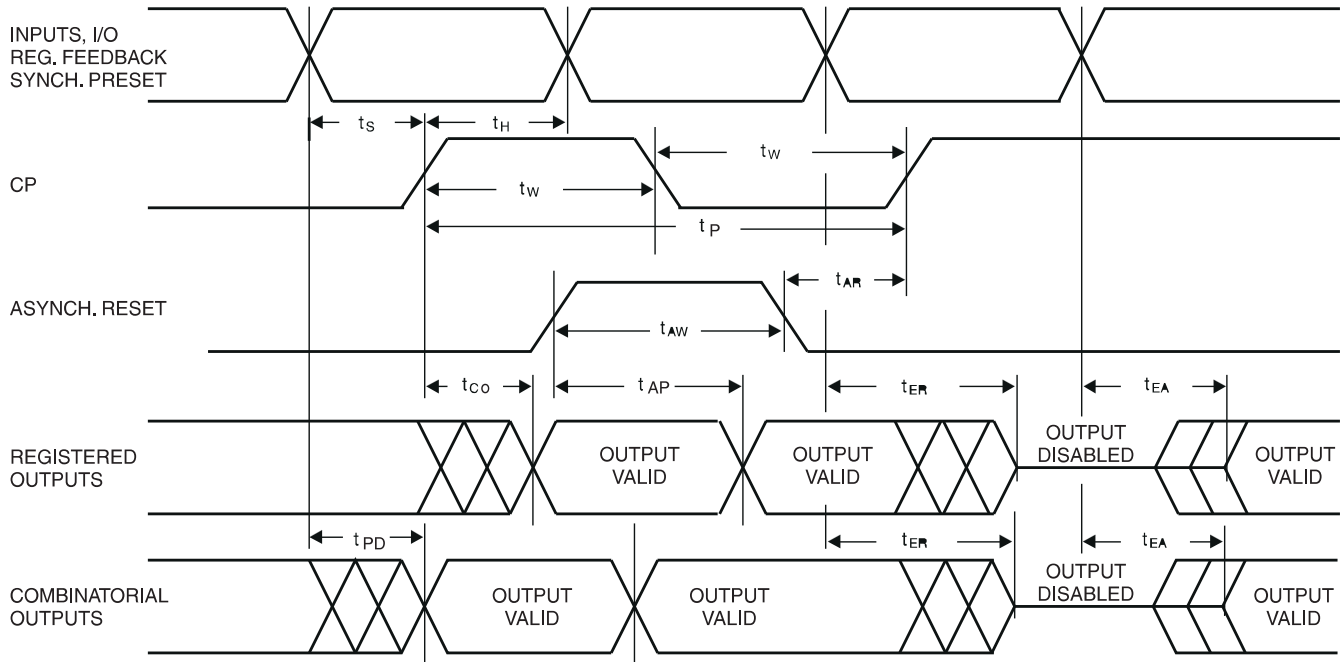
3.1 DC Characteristics

| Symbol | Parameter | Condition ⁽²⁾ | Min | Typ | Max | Units |
|----------------|--|---|-----------------|-----|-----------------|---------------|
| I_{IL} | Input or I/O Low Leakage Current | $0 \leq V_{IN} \leq V_{IL}(\text{Max})$ | | | -10 | μA |
| I_{IH} | Input or I/O High Leakage Current | $(V_{CC} - 0.2)V \leq V_{IN} \leq V_{CC}$ | | | 10 | μA |
| I_{CC} | Power Supply Current | $V_{CC} = \text{Max}, V_{IN} = \text{Max}$ Outputs Open | Com. | 55 | 85 | mA |
| | | | Ind. | 60 | 90 | mA |
| I_{CC2} | Clocked Power Supply Current | $V_{CC} = \text{Max}$ Outputs Open, $f = 15\text{MHz}$ | Com. | | 100 | mA |
| | | | Ind. | | 105 | mA |
| I_{PD} | Power Supply Current, Power-down Mode | $V_{CC} = 3.6V, \text{Max}$ $V_{IN} = 0, \text{Outputs Open}$ | Com. | 10 | 100 | μA |
| | | | Ind. | 10 | 120 | μA |
| $I_{OS}^{(1)}$ | Output Short Circuit Current | $V_{OUT} = 0.5V$ | | | -130 | mA |
| V_{IL} | Input Low Voltage | | -0.5 | | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | | $V_{CC} + 0.75$ | V |
| V_{OL} | Output Low Voltage | $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min}$ $I_{OL} = 16\text{mA}$ | | | 0.5 | V |
| V_{OH} | Output High Voltage | $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min}$ $I_{OH} = -2.0\text{mA}$ | 2.4 | | | V |
| V_{OH} | Output High Voltage | $I_{OH} = -100\mu\text{A}$ | $V_{CC} - 0.2V$ | | | V |

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec
2. For DC characteristics, the test condition of $V_{CC} = \text{Max}$ corresponds to 3.6V



3.2 AC Waveforms



3.3 AC Characteristics(1)

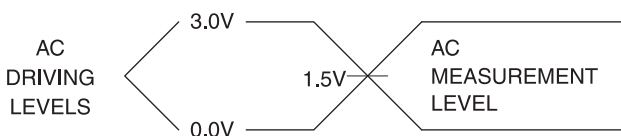
| Symbol | Parameter | -10 | | -15 | | Units |
|-----------|--|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | |
| t_{PD} | Input or Feedback to Non-Registered Output | 3 | 10 | 3 | 15 | ns |
| t_{CF} | Clock to Feedback | | 5 | | 8 | ns |
| t_{CO} | Clock to Output | 2 | 6.5 | 2 | 10 | ns |
| t_S | Input or Feedback Setup Time | 7.5 | | 12 | | ns |
| t_H | Input Hold Time | 0 | | 0 | | ns |
| t_P | Clock Period | 12 | | 16 | | ns |
| t_W | Clock Width | 6 | | 8 | | ns |
| f_{MAX} | External Feedback $1/(t_S + t_{CO})$ | | 71.4 | | 45.5 | MHz |
| | Internal Feedback $1/(t_S + t_{CF})$ | | 80 | | 50 | MHz |
| | No Feedback $1/(t_P)$ | | 83.3 | | 62.5 | MHz |
| t_{EA} | Input to Output Enable | 3 | 12 | 3 | 15 | ns |
| t_{ER} | Input to Output Disable | 2 | 12 | 2 | 15 | ns |
| t_{AP} | Input or I/O to Asynchronous Reset of Register | 3 | 13 | 3 | 15 | ns |
| t_{SP} | Setup Time, Synchronous Preset | 10 | | 10 | | ns |
| t_{AW} | Asynchronous Reset Width | 8 | | 8 | | ns |
| t_{AR} | Asynchronous Reset Recovery Time | 6 | | 6 | | ns |
| t_{SPR} | Synchronous Preset to Clock Recovery Time | 10 | | 10 | | ns |

Note: 1. See ordering information for valid part numbers

3.4 Power-down AC Characteristics

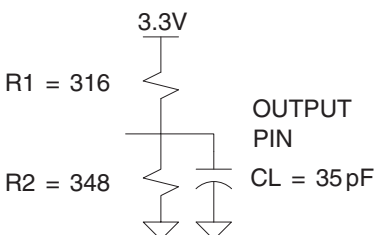
| Symbol | Parameter | -10 | | -15 | | Units |
|------------|--|-----|-----|-----|-----|-------|
| | | Min | Max | Min | Max | |
| t_{IVDH} | Valid Input before PD High | 10 | | 15 | | ns |
| t_{GVDH} | Valid \overline{OE} before PD High | 0 | | 0 | | ns |
| t_{CVDH} | Valid Clock before PD High | 0 | | 0 | | ns |
| t_{DHIX} | Input Don't Care after PD High | | 10 | | 15 | ns |
| t_{DHGX} | \overline{OE} Don't Care after PD High | | 10 | | 15 | ns |
| t_{DHCX} | Clock Don't Care after PD High | | 10 | | 15 | ns |
| t_{DLIV} | PD Low to Valid Input | | 10 | | 15 | ns |
| t_{DLGV} | PD Low to Valid \overline{OE} | | 25 | | 30 | ns |
| t_{DLCV} | PD Low to Valid Clock | | 25 | | 30 | ns |
| t_{DLOV} | PD Low to Valid Output | | 30 | | 35 | ns |

3.5 Input Test Waveforms and Measurement Levels



$$t_R, t_F < 1.5\text{ns}$$

3.6 Output Test Loads



Note: Similar competitor devices are specified with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel® devices are tested with sufficient margins to meet compatible device specification conditions.

Table 3-1. Pin Capacitance (f = 1MHz, T = 25°C⁽¹⁾)

| | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 5 | 8 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 6 | 8 | pF | $V_{OUT} = 0V$ |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested



3.7 Power-up Reset

The registers in the Atmel® ATF22LV10C are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be reset to the low state. The output state will depend on the polarity of the buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic and start below 0.7V
2. The clock must remain stable during T_{PR}
3. After T_{PR} , all input and feedback setup times must be met before driving the clock pin high

3.8 Preload of Register Outputs

The ATF22LV10C registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

4. Electronic Signature Word

There are 64-bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

5. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22LV10C fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

6. Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See CMOS PLD Programming Hardware & Software Support for information on software/programming.

Table 6-1. Programming/Erasing

| Parameter | Description | Typ | Max | Units |
|-----------|------------------------|-----|-------|-------|
| T_{PR} | Power-up Reset Time | 600 | 1,000 | ns |
| V_{RST} | Power-up Reset Voltage | 2.5 | 3.0 | V |

7. Input and I/O Pin-keeper

All ATF22LV10C family members have internal input and I/O pin-keeper circuits. Therefore, whenever inputs or I/Os are not being driven externally, they will maintain their last driven state. This ensures that all logic array inputs and device outputs are at known states. These are relatively weak active circuits that can be easily overridden by TTL-compatible drivers (see Input and I/O diagrams on [page 7](#)).

8. Power-down Mode

The Atmel® ATF22LV10C includes an optional pin controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin (Pin 4 on the DIP/SOIC packages and Pin 5 on the PLCC package). When the PD pin is high, the device supply current is reduced to less than 100mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs which were in an undetermined state at the onset of power-down will remain at the same state. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to insure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using the power-down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

PD pin configuration is controlled by the design file, and appears as a separate fuse bit in the JEDEC file. When the power-down feature is not specified in the design file, the IN/PD pin will be configured as a regular logic input.

Note: Some programmers list the 22V10 JEDEC-compatible 22V10C (no PD used) separately from the non-22V10 JEDEC-compatible 22V10CEX (with PD used).

Figure 8-1. Input Diagram

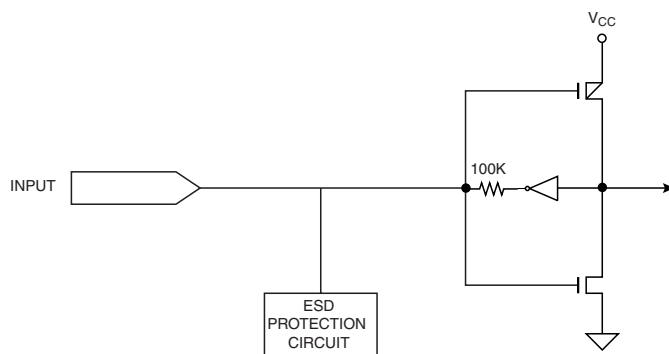
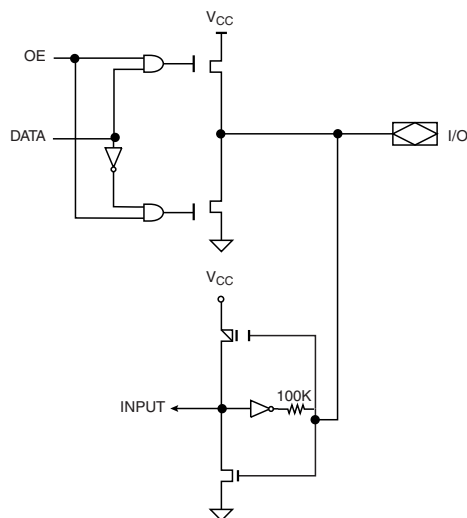


Figure 8-2. I/O Diagram





9. Compiler Mode Selection

Table 9-1. Compiler Mode Selection

| | PAL Mode (5828 Fuses) | GAL Mode (5892 Fuses) | Power-down Mode⁽¹⁾ (5893 Fuses) |
|---------|---|---|---|
| Synario | Atmel ATF22C10C (DIP) Atmel ATF22V10C (PLCC) | Atmel ATF22C10C DIO (UES) Atmel ATF22V10C PLCC (UES) | Atmel ATF22C10C DIP (PWD) Atmel ATF22C10V PLCC (PWD) |
| WINCUPL | P22V10 P22V10LCC | G22V10 G22V10LCC | G22V10CP G22V10CPLCC |

Note: 1. These device types will create a JEDEC file which when programmed in an Atmel ATF22V10C device will enable the power-down mode feature. All other devices have this feature disabled.

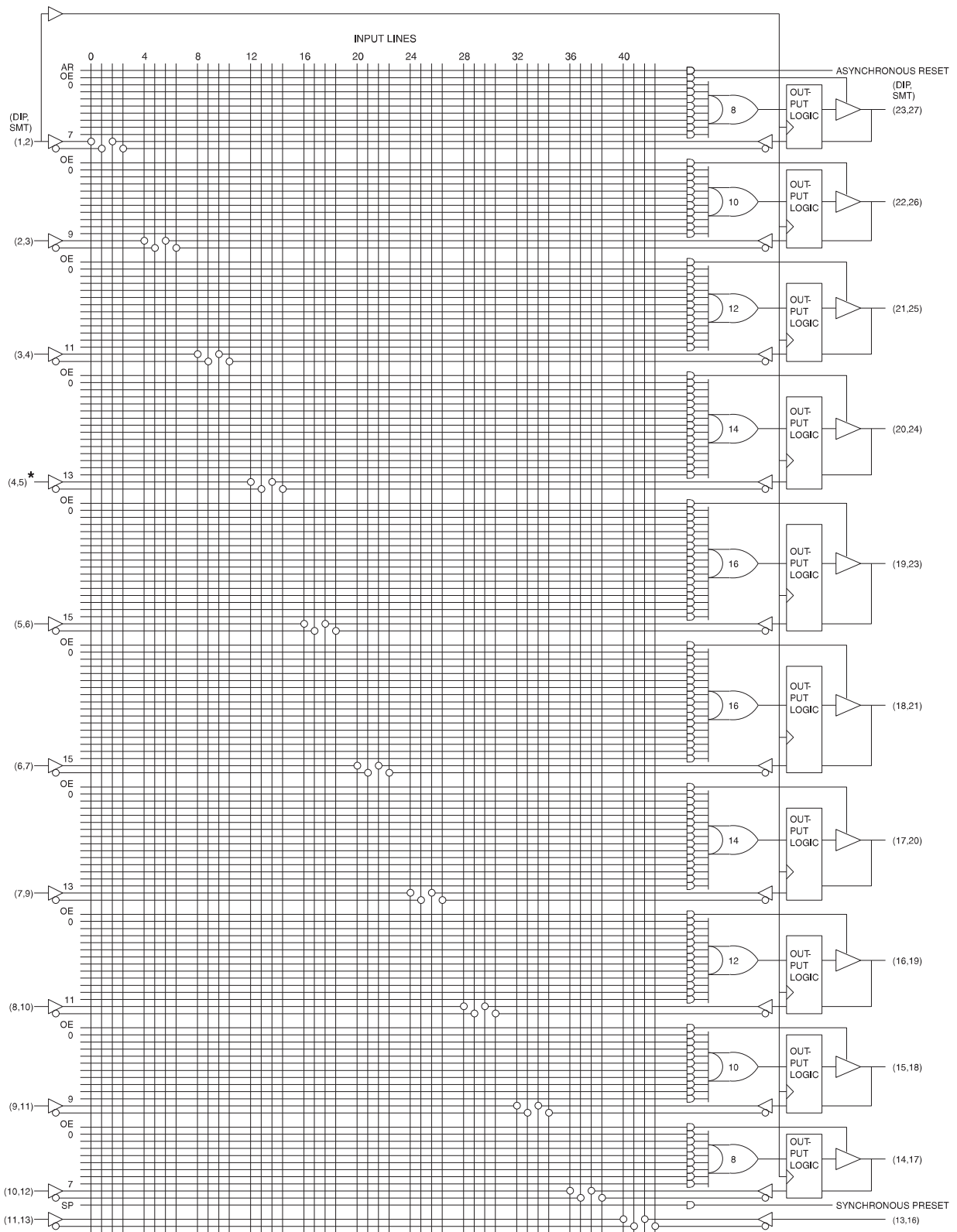
10. Functional Logic Diagram Description

The functional logic diagram describes the Atmel[®] ATF22LV10C architecture.

The ATF22LV10C has twelve inputs and ten I/O macrocells. Each macrocell can be configured into one of four output configurations: active high/low, registered/combinatorial output. The universal architecture of the ATF22LV10C can be programmed to emulate most 24-pin PAL devices.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF22LV10C. Eight bytes (64-fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

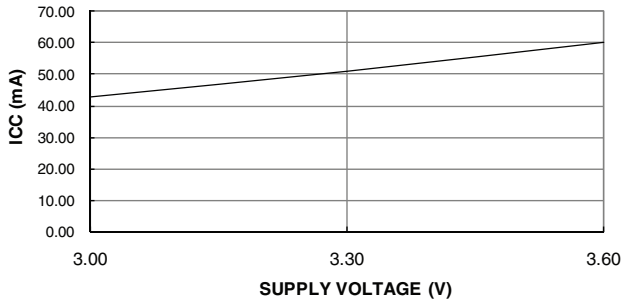
Figure 10-1. Functional Logic Diagram Atmel ATF22LV10C



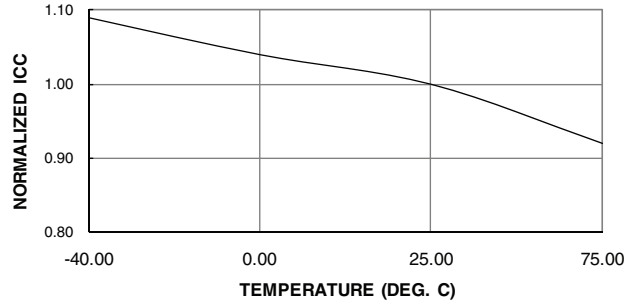
Note: 1. *Input not available if the power-down (PD) option is utilized



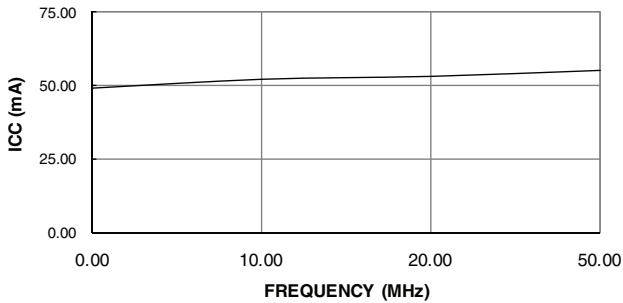
**ATMEL ATF22LV10C
SUPPLY CURRENT VS. SUPPLY VOLTAGE ($T_A = 25^\circ\text{C}$)**



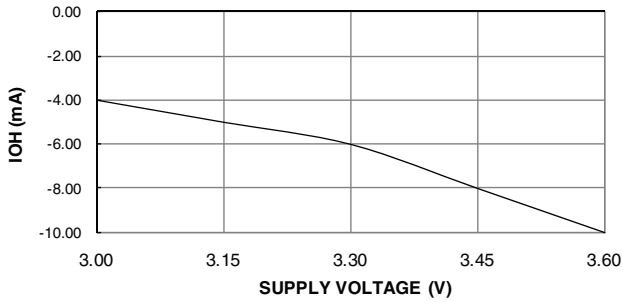
**ATMEL ATF22LV10C
NORMALIZED I_{CC} VS. TEMP.**



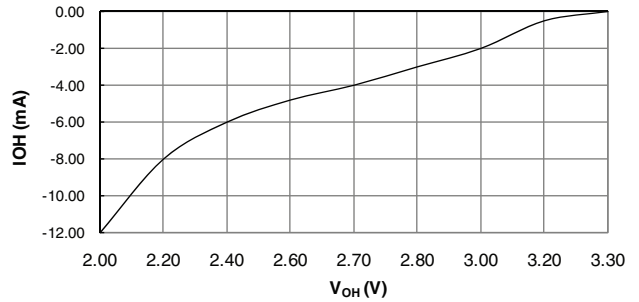
**ATMEL ATF22LV10C SUPPLY CURRENT VS.
INPUT FREQUENCY ($V_{CC} = 3.3\text{V}, T_A = 25^\circ\text{C}$)**



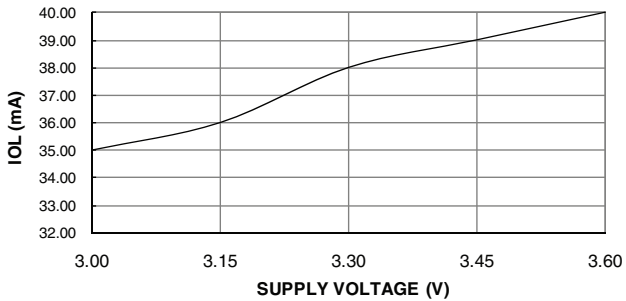
**ATMEL ATF22LV10C OUTPUT SOURCE
CURRENT VS. SUPPLY VOLTAGE ($V_{OH} = 2.4\text{V}$)**



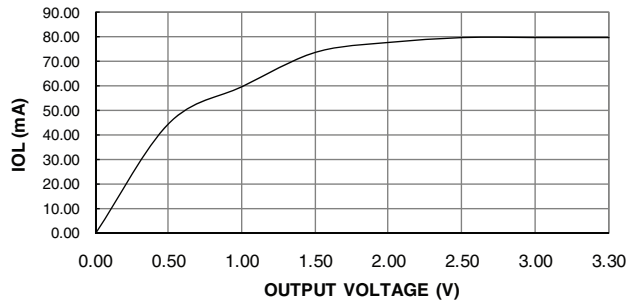
**ATMEL ATF22LV10C OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE ($V_{CC} = 3.3\text{V}, T_A = 25^\circ\text{C}$)**



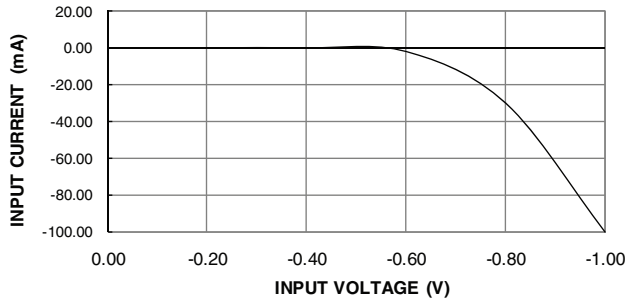
**ATMEL ATF22LV10C
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE ($V_{OL} = 0.5\text{V}$)**



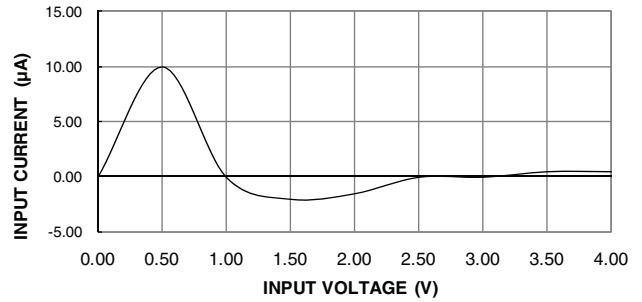
**ATMEL ATF22LV10C OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE ($V_{CC} = 3.3\text{V}, T_A = 25^\circ\text{C}$)**



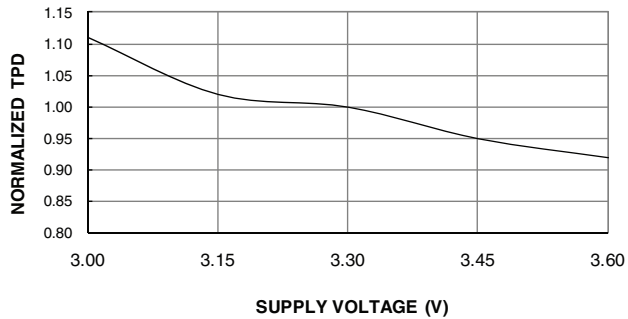
ATMEL ATF22LV10C INPUT CLAMP CURRENT VS. INPUT VOLTAGE ($V_{CC} = 3.3V, T_A = 25^\circ C$)



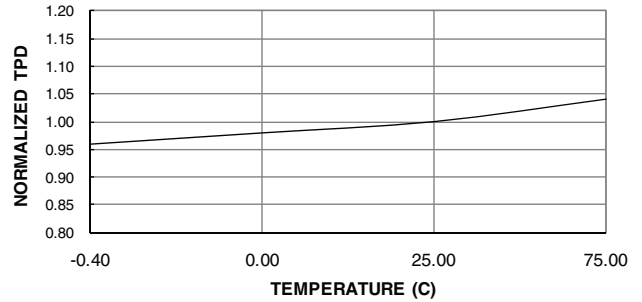
ATMEL ATF22LV10C INPUT CURRENT VS. INPUT VOLTAGE ($V_{CC} = 3.3V, T_A = 25^\circ C$)



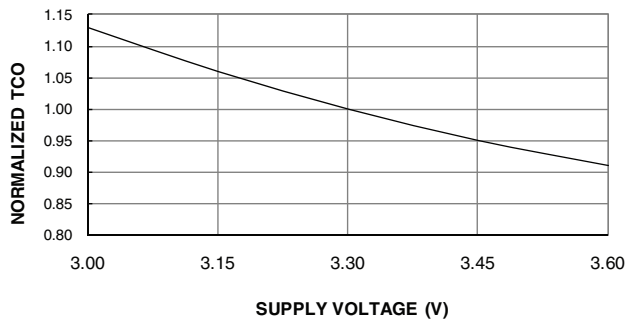
NORMALIZED T_{PD} VS. V_{CC}



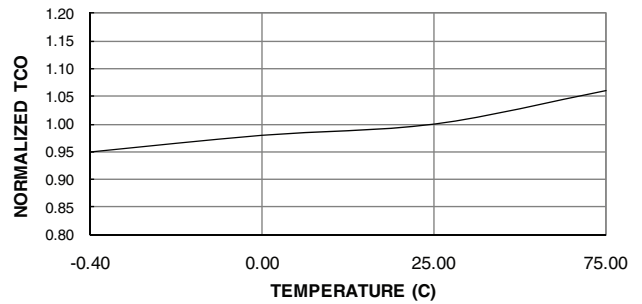
NORMALIZED T_{PD} VS. TEMP



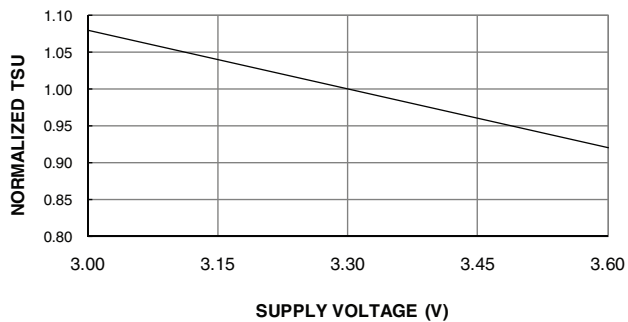
NORMALIZED T_{CO} VS. V_{CC}



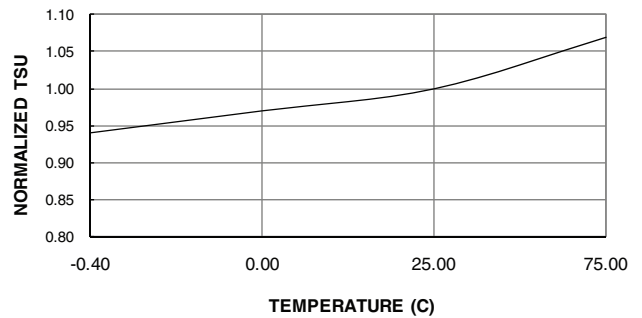
NORMALIZED T_{CO} VS. TEMP



NORMALIZED T_{SU} VS. V_{CC}

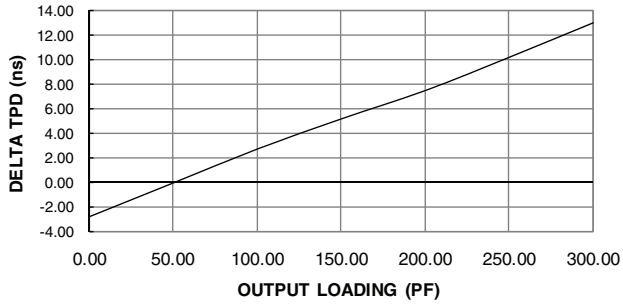


NORMALIZED T_{SU} VS. TEMP

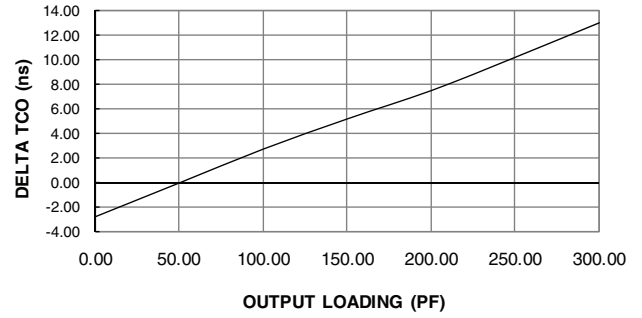




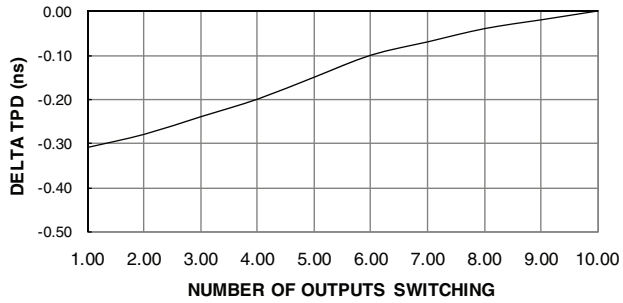
**ATMEL ATF22LV10C
DELTA T_{PD} VS. OUTPUT LOADING**



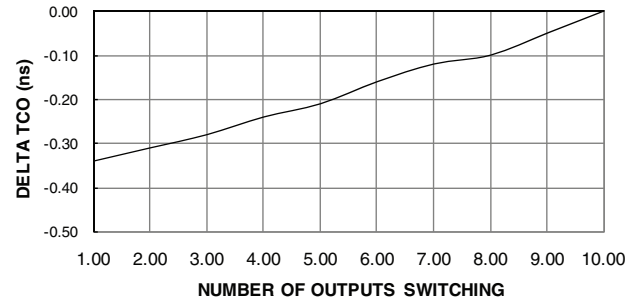
**ATMEL ATF22LV10C
DELTA T_{CO} VS. OUTPUT LOADING**



**ATMEL ATF22LV10C DELTA T_{PD} VS.
NUMBER OF OUTPUT SWITCHING**



**ATMEL ATF22LV10C DELTA T_{CO} VS.
NUMBER OF OUTPUT SWITCHING**



11. Ordering Information

11.1 Ordering Code Detail

| t_{PD} (ns) | t_S (ns) | t_{CO} (ns) | Ordering Code | Package | Operation Range |
|------------------|---------------|------------------|-----------------|---------|--------------------------------|
| 10 | 7.5 | 7.5 | ATF22LV10C-10JC | 28J | Commercial (0°C to 70°C) |
| | | | ATF22LV10C-10PC | 24P3 | |
| | | | ATF22LV10C-10SC | 24S | |
| | | | ATF22LV10C-10XC | 24X | |
| 10 | 7.5 | 7.5 | ATF22LV10C-10JI | 28J | Industrial (0°C to 85°C) |
| | | | ATF22LV10C-10PI | 24P3 | |
| | | | ATF22LV10C-10SI | 24S | |
| | | | ATF22LV10C-10XI | 24X | |
| 15 | 12 | 10 | ATF22LV10C-15JC | 28J | Commercial (0°C to 70°C) |
| | | | ATF22LV10C-15PC | 24P3 | |
| | | | ATF22LV10C-15SC | 24S | |
| | | | ATF22LV10C-15XC | 24X | |
| | 12 | 10 | ATF22LV10C-15JI | 28J | Industrial (-40°C to +85°C) |
| | | | ATF22LV10C-15PI | 24P3 | |
| | | | ATF22LV10C-15SI | 24S | |
| | | | ATF22LV10C-15XI | 24X | |

Note: Lead based packages will become obsolete, and are not recommended for new designs

11.2 Green Package Options (Pb/Halide-free/RoHS Compliant)

| t_{PD} (ns) | t_S (ns) | t_{CO} (ns) | Ordering Code | Package | Operation Range |
|------------------|---------------|------------------|-----------------|---------|------------------------------|
| 10 | 7.5 | 7.5 | ATF22LV10C-10JU | 28J | Industrial (0°C to +85°C) |
| | | | ATF22LV10C-10PU | 24P3 | |
| | | | ATF22LV10C-10SU | 24S | |
| | | | ATF22LV10C-10XU | 24X | |

11.3 Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, simply de-rate I_{CC} by 15% on the “C” device. No speed de-rating is necessary.

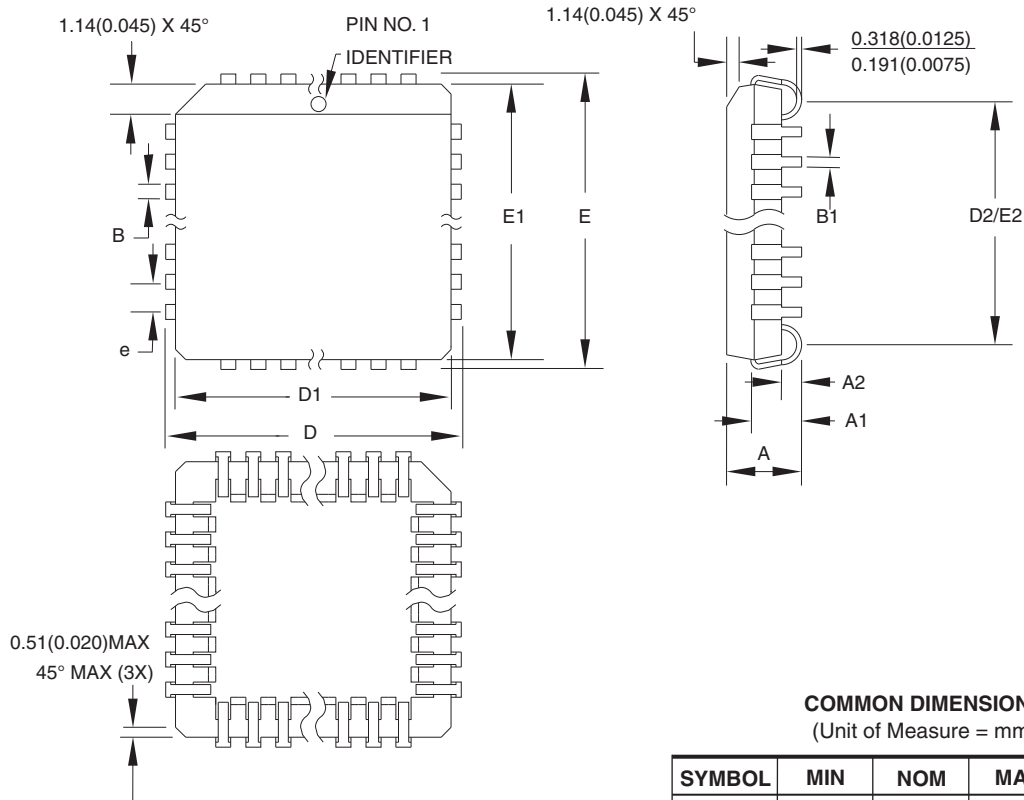
| Package Type | |
|--------------|--|
| 28J | 28-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 24P3 | 24-lead, 0.300" Wide, Plastic Dual In-line Package (PDIP) |
| 24S | 24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |
| 24X | 24-lead, 4.4mm Wide, Plastic Thin Shrink Small Outline (TSSOP) |





12. Package Information

12.1 28J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | 4.191 | – | 4.572 | |
| A1 | 2.286 | – | 3.048 | |
| A2 | 0.508 | – | – | |
| D | 12.319 | – | 12.573 | |
| D1 | 11.430 | – | 11.582 | Note 2 |
| E | 12.319 | – | 12.573 | |
| E1 | 11.430 | – | 11.582 | Note 2 |
| D2/E2 | 9.906 | – | 10.922 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102mm) maximum.

10/04/01



Package Drawing Contact:
packagedrawings@atmel.com

TITLE

28J, 28-lead, Plastic J-leded Chip Carrier (PLCC)

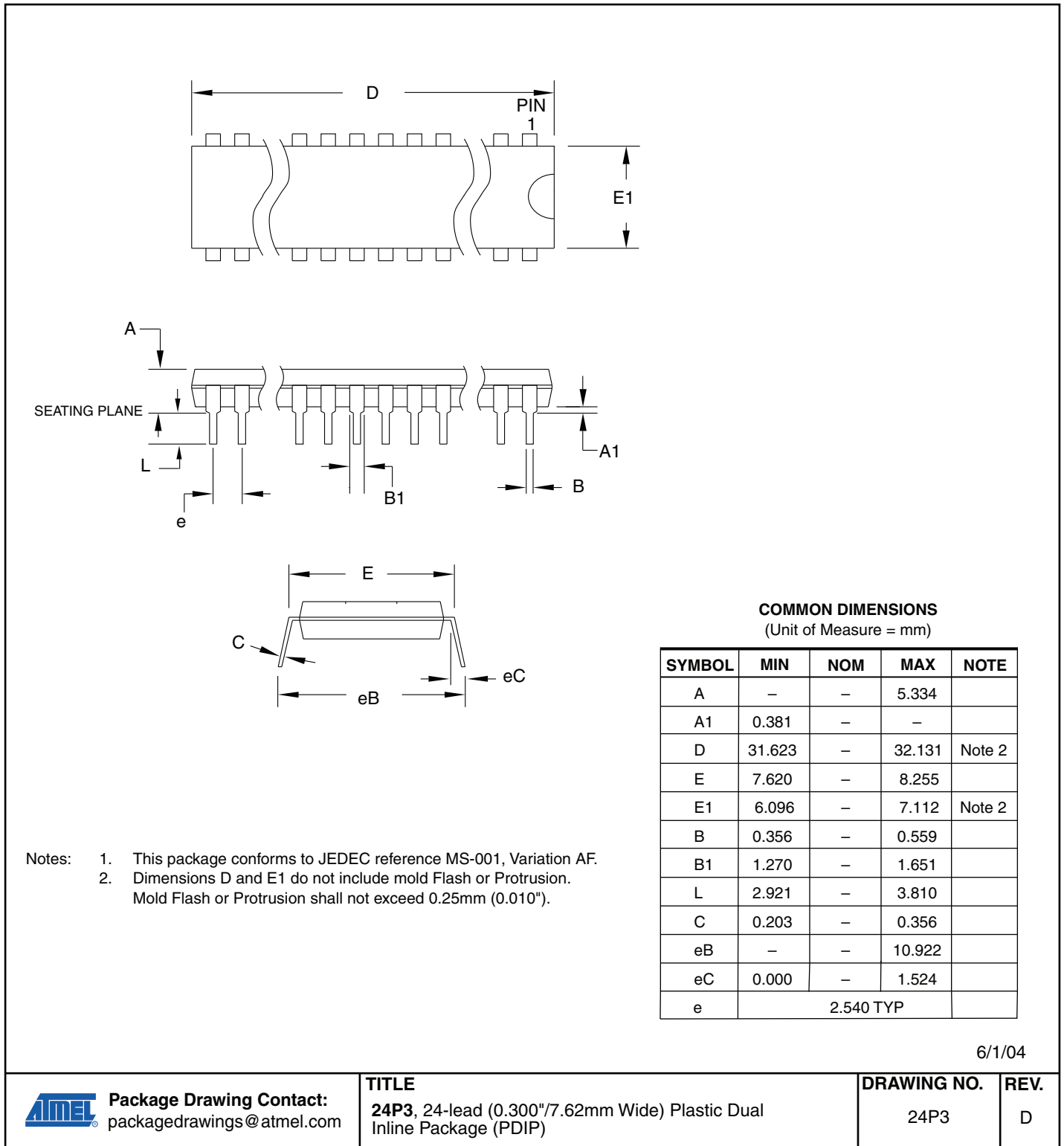
DRAWING NO.

28J

REV.

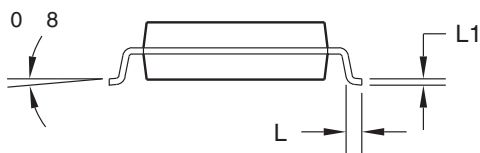
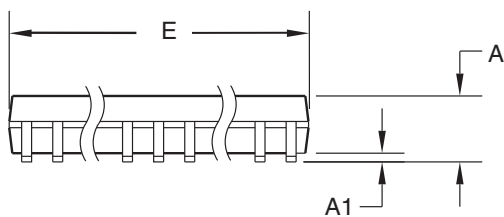
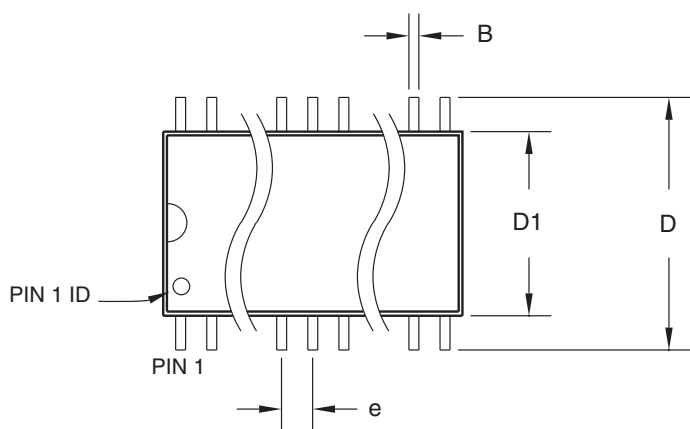
B

12.2 24P3 – PDIP





12.3 24S – SOIC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-----|-------|------|
| A | – | – | 2.65 | |
| A1 | 0.10 | – | 0.30 | |
| D | 10.00 | – | 10.65 | |
| D1 | 7.40 | – | 7.60 | |
| E | 15.20 | – | 15.60 | |
| B | 0.33 | – | 0.51 | |
| L | 0.40 | – | 1.27 | |
| L1 | 0.23 | – | 0.32 | |
| e | 1.27 BSC | | | |

06/17/2002



Package Drawing Contact:
packagedrawings@atmel.com

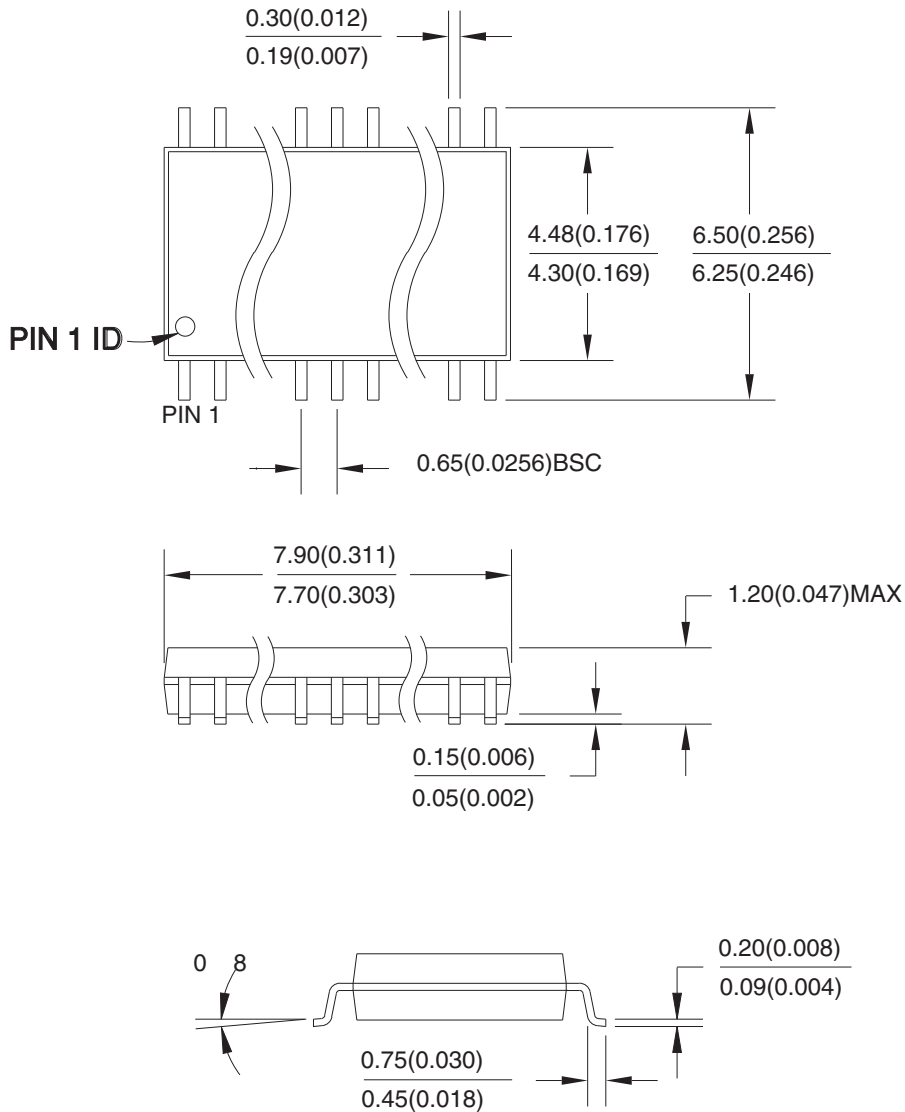
TITLE
24S, 24-lead (0.300" body) Plastic Gull Wing Small
Outline (SOIC)

DRAWING NO.
24S

REV.
B

12.4 24X – TSSOP

Dimensions in Millimeter and (Inches)*
 JEDEC STANDARD MO-153 AD
 Controlling dimension: millimeters



04/11/2001

| | | | | |
|--|---|---|--|---|
| | <p>Package Drawing Contact: packagedrawings@atmel.com</p> | <p>TITLE 24X, 24-lead (4.4mm body width) Plastic Thin Shrink Small Outline Package (TSSOP)</p> | <p>DRAWING NO. 24X</p> | <p>REV. A</p> |
|--|---|---|--|---|



13. Revision History

| Doc. Rev. | Date | Comments |
|-----------|---------|---|
| 0780M | 07/2010 | Update the standby current parameters for Powerdown mode from 100 μ A to 120 μ A. Shade Ordering Package Option table and add note, "Lead based packages will become obsolete and are not recommended for new designs." |
| 0780L | 12/2005 | Add Green Package options |



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