# M2S010-VF400 Datasheet

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| DiGi Electronics Part Number | M2S010-VF400-DG |
| Manufacturer | Microchip Technology |
| Manufacturer Product Number | M2S010-VF400 |
| Description | IC SOC CORTEX-M3 166MHZ 400VFBGA |
| Detailed Description | ARM® Cortex®-M3 System On Chip (SOC) IC SmartFusion®2 FPGA - 10K Logic Modules 166MHz 400-VFBGA (17x17) |

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## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| M2S010-VF400 | Microchip Technology |
| Series: | Product Status: |
| SmartFusion®2 | Active |
| Architecture: | Core Processor: |
| MCU, FPGA | ARM® Cortex®-M3 |
| Flash Size: | RAM Size: |
| 256KB | 64KB |
| Peripherals: | Connectivity: |
| DDR, PCIe, SERDES | CANbus, Ethernet, I2C, SPI, UART/USART, USB |
| Speed: | Primary Attributes: |
| 166MHz | FPGA - 10K Logic Modules |
| Operating Temperature: | Package / Case: |
| 0°C ~ 85°C (TJ) | 400-LFBGA |
| Supplier Device Package: | Number of I/O: |
| 400-VFBGA (17x17) | 195 |
| Base Product Number: | |
| M2S010 | |

## Environmental & Export classification

| RoHS Status: | Moisture Sensitivity Level (MSL): |
| --- | --- |
| RoHS non-compliant | 3 (168 Hours) |
| REACH Status: | ECCN: |
| REACH Unaffected | 3A991D |
| HTSUS: | |
| 8542.39.0001 | |

M2S010-VF400 Microchip Technology IC SOC CORTEX-M3 166MHZ 400VFBGA

# DS0128
# Datasheet
# IGLOO2 FPGA and SmartFusion2 SoC FPGA

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# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated Table 24, page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added Non-Deterministic Random Bit Generator (NRBG) Characteristics, page 106 (SAR 73114 and 79517).
- Added 060 device in Table 282, page 110 (SAR 79860).
- Added DEVRST_N to Functional Times, page 116 (SAR 73114).
- Added Cryptographic Block Characteristics, page 106 (SAR 73114 and 79516).
- Update Table 296, page 121 with VTX-AMP details (SAR 81756).
- Update note in Table 297, page 122 (SAR 74570 and 80677).
- Update Table 298, page 122 with generic EPCS details (SAR 75307).
- Added Table 308, page 129 (SAR 50424).

## 1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note*. (SAR 76865 and 76623).
- Added 060 device in Table 4, page 6 (SAR 76383).
- Updated Table 24, page 22 for ramp time input (SAR 72103).
- Added 060 device details in Table 284, page 112 (SAR 74927).
- Updated Table 290, page 116 for name change (SAR 74925).
- Updated Table 283, page 111 for 060 FG676 Package details (SAR 78849).
- Updated Table 305, page 126 for SmartFusion2 and Table 310, page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated Table 293, page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
- Updated Table 297, page 122 for RX-CID information (SAR 78271).
- Added Table 8, page 8 and Figure 1, page 9 (SAR 78932).
- Updated Table 223, page 76 for timing characteristics and Table 224, page 77(SAR 75998).
- Added SRAM PUF, page 105 (SAR 64406).
- Added a footnote on digest cycle in Table 5, page 7 (SAR 79812).

## 1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in Table 5, page 7 (SAR 71506).
- Added a note in Table 6, page 8 (SAR 74616).
- Added a note in Figure 3, page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in Table 11, page 12 and Table 12, page 13 (SAR 74483).
- Updated programming currents for 060 in Table 13, page 13, Table 14, page 13, and Table 15, page 14.
- Added DEVRST_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in Table 18, page 19 and Table 21, page 20 (SAR 69829).
- Updated Table 24, page 22 (SAR 69418).
- Updated Table 25, page 22, Table 26, page 23, Table 27, page 23 (SAR 74570).
- Updated all AC/DC table to link to the Input Capacitance, Leakage Current, and Ramp Time, page 22 for reference (SAR 69418).

- Added Table 244, page 94 and Table 256, page 99 (SAR 73971).
- Updated the SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 71171).
- Added the DEVRST_N Characteristics, page 116 (SAR 64100, 72103).
- Added Table 298, page 122 (SAR 71897).
- Updated Table 25, page 22, Table 26, page 23, and Table 27, page 23 (SAR 74570).
- Added 060 devices in Table 277, page 107, Table 278, page 108, and Table 279, page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in Table 280, page 109 and Table 281, page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in Table 282, page 110 (SAR 68281).
- Updated Table 293, page 119 for 060 devices (SAR 57828).
- Updated Table 297, page 122 for CID value (SAR 70878).

## 1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated Table 11, page 12 (SAR 69218).
- Updated Table 12, page 13 (SAR 69218).
- Updated Table 283, page 111 (SAR 69000).

## 1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Table 1, page 4(SAR 68620).

## 1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated Table 5, page 7 (SAR 65949).
- Updated Table 9, page 10 (SAR 62995).
- Updated Table 123, page 47 and Table 133, page 49 (SAR 67210).
- Added Embedded NVM (eNVM) Characteristics, page 104 (SAR 52509).
- Updated Table 277, page 107 (SAR 64855).
- Updated Table 282, page 110 (SAR 65958 and SAR 56666).
- Added DDR Memory Interface Characteristics, page 120 (SAR 66223).
- Added SFP Transceiver Characteristics, page 120 (SAR 63105).
- Updated Table 302, page 123 and Table 309, page 129 (SAR 66314).

## 1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated Table 1, page 4.
- Updated Table 4, page 6 for $T_J$ symbol information.
- Updated Table 5, page 7 (SAR 63109).
- Updated Table 9, page 10.
- Updated Table 282, page 110 (SAR 62012).
- Added Table 290, page 116 (SAR 64100).
- Added Table 306, page 128, Table 307, page 128 (SAR 50424).

## 1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated Table 1, page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated Figure 10, page 70. Removed inverter bubble from DDR_IN latch (SAR 61418).
- Updated SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 62836).

## 1.9 Revision 3.0

In revision 3.0 of this document, the Theta B/C columns and FCS325 package was updated. For more information, see Table 9, page 10 (SAR 62002).

## 1.10 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Table 1, page 4 was updated (SAR 59056).
- Table 7, page 8 temperature and data retention information was updated SAR (61363).
- Storage Operating Table was updated and split into three tables – Table 5, page 7, Table 7, page 8 (SAR 58725).
- Updated Theta B/C columns and FCS325 package in Table 9, page 10 (SAR 62002).
- Added 090-FCS325 thermal resistance to Table 9, page 10 (SAR 59384).
- TQ144 package was added to Table 9, page 10 (SAR 57708).
- Added PLL jitter data for the VF400 package (SAR 53162).
- Added Additional Worst Case IDD to Table 11, page 12 and Table 12, page 13 (SAR 59077).
- Table 13, page 13, Table 14, page 13, and Table 15, page 14 were added to verify Inrush currents (SAR 56348).
- Table 18, page 19 and Table 21, page 20 – I/O speeds were replaced.
- Max speed was changed in Table 41, page 26 (SAR 57221) and in Table 52, page 29 (SAR 57113).
- Minimum and Maximum DC/AC Input and Output Levels Specification, page 29 and Table 49, page 29–Table 57, page 31 were added.
- Added Cload to Table 89, page 39 (SAR 56238).
- Removed "Rs" information in DDR Timing Measurement Table 123, page 47, Table 133, page 49, and Table 144, page 52.
- Updated drive programming for M/B-LVDS outputs (SAR 58154).
- Added an inverter bubble to DDR_IN latch in Figure 10, page 70 (SAR 61418).
- QF waveform in Figure 11, page 71 was updated (SAR 59816).
- uSRAM Write Clock minimum values were updated in Table 237, page 86–Table 243, page 93 (SAR 55236).
- Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).
- The "On-Chip Oscillator" section was split, and the Embedded NVM (eNVM) Characteristics, page 104 was added. Table 277, page 107–Table 281, page 109 were revised.(SARs 57898 and 59669).
- PLL VCP Frequency and conditions were added to Table 282, page 110 (SAR 57416).
- Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).
- Updated FCCC information in Table 282, page 110 and Table 283, page 111 (SAR 60799).
- Device 025 specifications were added to Table 283, page 111 (SAR 51625).
- JTAG Table 284, page 112 was replaced (SAR 51188).
- Flash*Freeze Table 293, page 119 was replaced (SAR 57828).
- Added support for HCSL I/O Standard for SERDES reference clocks in Table 300, page 123 and Table 301, page 123 (SAR 50748).
- Tir and Tif parameters were added to Table 303, page 124 (SAR 52203).
- Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).
- Added jitter attenuation information (SAR 59405).

## 1.11 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.

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# 2 IGLOO2 FPGA and SmartFusion2 SoC FPGA

Microsemi's mainstream SmartFusion®2 SoC and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks, multiple embedded memory blocks, and high-performance SerDes communication interfaces on a single chip. Both families benefit from low-power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MBs of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low-power, real-time microcontroller subsystem (MSS) with a rich set of industry-standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

## 2.1 Device Status

The following table shows the design security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

***Table 1 •*** **IGLOO2 and SmartFusion2 Design Security Densities**

| Design Security Device Densities | Status |
|---|---|
| 005 | Production |
| 010, 010T | Production |
| 025, 025T | Production |
| 050, 050T | Production |
| 060, 060T | Production |
| 090, 090T | Production |
| 150, 150T | Production |

The following table shows the data security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

***Table 2 •*** **IGLOO2 and SmartFusion2 Data Security Densities**

| Data Security Device Densities | Status |
|---|---|
| 005S | Production |
| 010TS | Production |
| 025TS | Production |
| 050TS | Production |
| 060TS | Production |
| 090TS | Production |
| 150TS | Production |

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## 2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:
http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga
http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview

## 2.3 Electrical Specifications

### 2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

***Table 3 •*** **Absolute Maximum Ratings**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC core supply voltage. Must always power this pin. | $V_{DD}$ | –0.3 | 1.32 | V |
| Power supply for charge pumps (for normal operation and programming). Must always power this pin. | $V_{PP}$ | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | MSS_MDDR_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | HPMS_MDDR_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power pad for FDDR PLL | FDDR_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | PLL0_PLL1_MSS_MDDR_VDDA | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | PLL0_PLL1_HPMS_MDDR_VDDA | –0.3 | 3.63 | V |
| Analog power pad for PLL0–5 | CCC_XX[01]_PLL_VDDA | –0.3 | 3.63 | V |
| High supply voltage for PLL SerDes[01] | SERDES_[01]_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply. | SERDES_[01]_L[0123]_VDDAPLL | –0.3 | 2.75 | V |
| TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply. | SERDES_[01]_L[0123]_VDDAIO | –0.3 | 1.32 | V |
| PCIe/PCS power supply | SERDES_[01]_VDD | –0.3 | 1.32 | V |
| DC FPGA I/O buffer supply voltage for MSIO I/O bank | $V_{DDIx}$ | –0.3 | 3.63 | V |
| DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks | $V_{DDIx}$ | –0.3 | 2.75 | V |
| I/O Input voltage for MSIO I/O bank | $V_I$ | –0.3 | 3.63 | V |
| I/O Input voltage for MSIOD/DDRIO I/O bank | $V_I$ | –0.3 | 2.75 | V |
| Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$. | $V_{PPNVM}$ | –0.3 | 3.63 | V |
| Storage temperature[1] | $T_{STG}$ | –65 | 150 | °C |
| Junction temperature | $T_J$ | –55 | 135 | °C |

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1. For flash programming and retention maximum limits, see Table 5, page 7. For recommended operating conditions, see Table 4, page 6.

***Table 4 •*** **Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Operating junction temperature | $T_J$ | 0 | 25 | 85 | °C | Commercial |
| | | –40 | 25 | 100 | °C | Industrial |
| Programming junction temperatures[1] | $T_J$ | 0 | 25 | 85 | °C | Commercial |
| | | –40 | 25 | 100 | °C | Industrial |
| DC core supply voltage. Must always power this pin. | $V_{DD}$ | 1.14 | 1.2 | 1.26 | V | |
| Power supply for charge pumps (for normal operation and programming) for the 005, 010, 025, 050, 060 devices | $V_{PP}$ | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Power supply for charge pumps (for normal operation and programming) for the 090 and 150 devices | $V_{PP}$ | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | MSS_MDDR_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | HPMS_MDDR_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for FDDR PLL | FDDR_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | PLL0_PLL1_MSS_MDDR_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | PLL0_PLL1_HPMS_MDDR_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for PLL0 to PLL5 | CCC_XX[01]_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| High supply voltage for PLL SerDes[01] | SERDES_[01]_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power for SerDes[01] PLL Lane 0 to Lane 3. This is a 2.5 V SerDes internal PLL supply. | SERDES_[01]_L[0123]_VDDAPLL | 2.375 | 2.5 | 2.625 | V | |
| TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply. | SERDES_[01]_L[0123]_VDDAIO | 1.14 | 1.2 | 1.26 | V | |
| PCIe/PCS power supply | SERDES_[01]_VDD | 1.14 | 1.2 | 1.26 | V | |
| 1.2 V DC supply voltage | $V_{DDIx}$ | 1.14 | 1.2 | 1.26 | V | |
| 1.5 V DC supply voltage | $V_{DDIx}$ | 1.425 | 1.5 | 1.575 | V | |
| 1.8 V DC supply voltage | $V_{DDIx}$ | 1.71 | 1.8 | 1.89 | V | |
| 2.5 V DC supply voltage | $V_{DDIx}$ | 2.375 | 2.5 | 2.625 | V | |

***Table 4 •*** **Recommended Operating Conditions *(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| 3.3 V DC supply voltage | $V_{DDIx}$ | 3.15 | 3.3 | 3.45 | V | |
| LVDS differential I/O | $V_{DDIx}$ | 2.375 | 2.5 | 3.45 | V | |
| B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O | $V_{DDIx}$ | 2.375 | 2.5 | 2.625 | V | |
| LVPECL differential I/O | $V_{DDIx}$ | 3.15 | 3.3 | 3.45 | V | |
| Reference voltage supply for FDDR (Bank0) and MDDR (Bank5) | $V_{REFx}$ | 0.49 × $V_{DDIx}$ | 0.5 × $V_{DDIx}$ | 0.51 × $V_{DDIx}$ | V | |
| Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$. | $V_{PPNVM}$ | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |

1. Programming at Industrial temperature range is available only with $V_{PP}$ = 3.3 V.

**Note:** Power supply ramps must all be strictly monotonic, without plateaus.

***Table 5 •*** **FPGA Operating Limits**

| Product Grade | Element | Programming Temperature | Operating Temperature | Programming Cycles | Digest Temperature | Digest Cycles | Retention (Biased/ Unbiased) |
|---|---|---|---|---|---|---|---|
| Commercial | FPGA | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | 500 | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | 2000 | 20 years |
| Industrial[1] | FPGA | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | 500 | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | 2000 | 20 years |

1. Programming at Industrial temperature range is available only with VPP = 3.3 V.

**Note:** The retention specification is defined as the total number of programing and digest cycles. For example, 20 years of retention after 500 programming cycles.

**Note:** The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

**Note:** If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

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The following table lists the embedded operating flash limits.

***Table 6 •*** **Embedded Operating Flash Limits**

| Product Grade | Element | Programming Temperature | Maximum Operating Temperature | Programming Cycles | Retention (Biased/Unbiased) |
|---|---|---|---|---|---|
| Commercial | Embedded flash | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | < 1000 cycles per page, up to two million cycles per eNVM array | 20 years |
| | | | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | < 10000 cycles per page, up to 20 million cycles per eNVM array | 10 years |
| Industrial | Embedded flash | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | < 1000 cycles per page, up to two million cycles per eNVM array | 20 years |
| | | | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | < 10000 cycles per page, up to 20 million cycles per eNVM array | 10 years |

**Note:** If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

***Table 7 •*** **Device Storage Temperature and Retention**

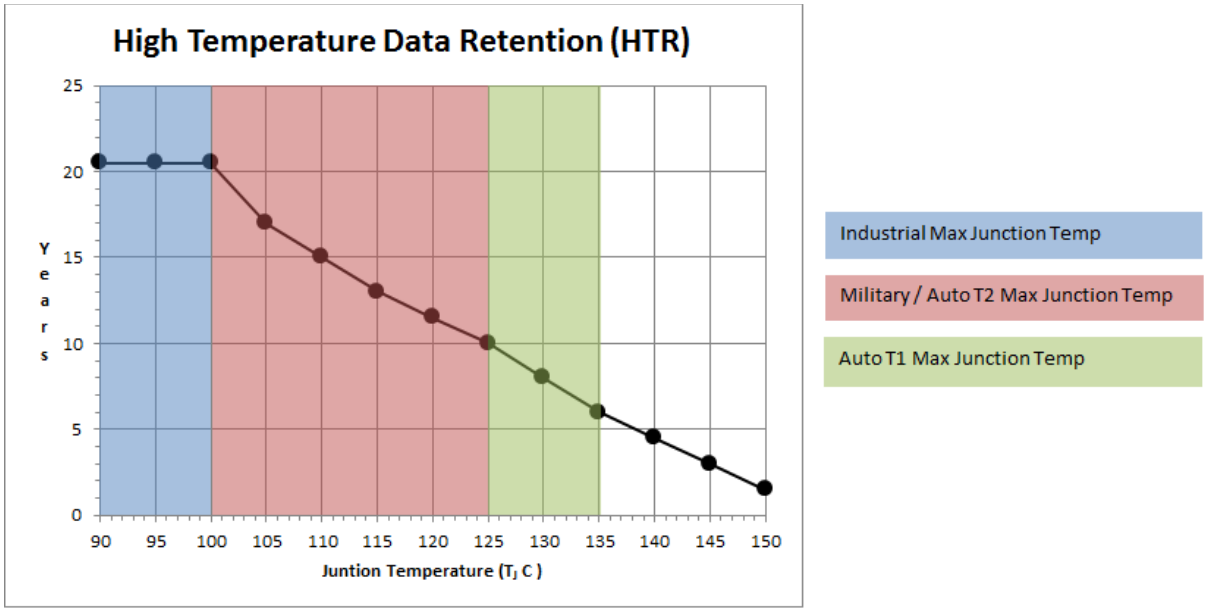
| Product Grade | Storage Temperature (Tstg) | Retention |
|---|---|---|
| Commercial | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | 20 years |
| Industrial | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | 20 years |

***Table 8 •*** **High Temperature Data Retention (HTR) Lifetime**

| $T_J$ (C) | HTR Lifetime[1] (yrs) |
|---|---|
| 90 | 20.5 |
| 95 | 20.5 |
| 100 | 20.5 |
| 105 | 17.0 |
| 110 | 15.0 |
| 115 | 13.0 |
| 120 | 11.5 |
| 125 | 10.0 |
| 130 | 8.0 |
| 135 | 6.0 |
| 140 | 4.5 |
| 145 | 3.0 |
| 150 | 1.5 |

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

***Figure 1 •*** **High Temperature Data Retention (HTR)**




### 2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to –1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to $V_{CCI}$ + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

**Note:** The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

### 2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

*EQ 1*

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

*EQ 2*

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

*EQ 3*

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where

$\theta_{JA}$ = Junction-to-air thermal resistance

$\theta_{JB}$ = Junction-to-board thermal resistance

$\theta_{JC}$ = Junction-to-case thermal resistance

$T_J$ = Junction temperature

$T_A$ = Ambient temperature

$T_B$ = Board temperature (measured 1.0 mm away from the package edge)

$T_C$ = Case temperature

P = Total power dissipated by the device

***Table 9 •*** **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices**

| | Still Air | 1.0 m/s | 2.5 m/s | | | |
|---|---|---|---|---|---|---|
| **Device** | | **$\theta_{JA}$** | | **$\theta_{JB}$** | **$\theta_{JC}$** | **Unit** |
| **005** | | | | | | |
| FG484 | 19.36 | 15.81 | 14.63 | 9.74 | 5.27 | °C/W |
| VF256 | 41.30 | 38.16 | 35.30 | 28.41 | 3.94 | °C/W |
| VF400 | 20.19 | 16.94 | 15.41 | 8.86 | 4.95 | °C/W |
| TQ144 | 42.80 | 36.80 | 34.50 | 37.20 | 10.80 | °C/W |
| **010** | | | | | | |
| FG484 | 18.22 | 14.83 | 13.62 | 8.83 | 4.92 | °C/W |
| VF256 | 37.36 | 34.26 | 31.45 | 24.84 | 7.89 | °C/W |
| VF400 | 19.40 | 15.75 | 14.22 | 8.11 | 4.22 | °C/W |
| TQ144 | 38.60 | 32.60 | 30.30 | 31.80 | 8.60 | °C/W |
| **025** | | | | | | |
| FG484 | 17.03 | 13.66 | 12.45 | 7.66 | 4.18 | °C/W |
| VF256 | 33.85 | 30.59 | 27.85 | 21.63 | 6.13 | °C/W |
| VF400 | 18.36 | 14.89 | 13.36 | 7.12 | 3.41 | °C/W |
| FCS325 | 29.17 | 24.87 | 23.12 | 14.44 | 2.31 | °C/W |
| **050** | | | | | | |
| FG484 | 15.29 | 12.19 | 10.99 | 6.27 | 3.24 | °C/W |
| FG896 | 14.70 | 12.50 | 10.90 | 7.20 | 4.90 | °C/W |
| VF400 | 17.53 | 14.17 | 12.63 | 6.32 | 2.81 | °C/W |
| FCS325 | 27.38 | 23.18 | 21.41 | 12.47 | 1.59 | °C/W |
| **060** | | | | | | |
| FG484 | 15.40 | 12.06 | 10.85 | 6.14 | 3.15 | °C/W |
| FG676 | 15.49 | 12.21 | 11.06 | 7.07 | 3.87 | °C/W |
| VF400 | 17.45 | 14.01 | 12.47 | 6.22 | 2.69 | °C/W |
| FCS325 | 27.03 | 22.91 | 21.25 | 12.33 | 1.54 | °C/W |
| **090** | | | | | | |
| FG484 | 14.64 | 11.37 | 10.16 | 5.43 | 2.77 | °C/W |
| FG676 | 14.52 | 11.19 | 10.37 | 6.17 | 3.24 | °C/W |
| FCS325 | 26.63 | 22.26 | 20.13 | 14.24 | 2.50 | °C/W |

***Table 9 •*** **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices *(continued)***

| | Still Air | 1.0 m/s | 2.5 m/s | | | |
|---|---|---|---|---|---|---|
| **Device** | | $\theta_{JA}$ | | $\theta_{JB}$ | $\theta_{JC}$ | **Unit** |
| **150** | | | | | | |
| FC1152 | 9.08 | 6.81 | 5.87 | 2.56 | 0.38 | °C/W |
| FCS536 | 15.01 | 12.06 | 10.76 | 3.69 | 1.55 | °C/W |
| FCV484 | 16.21 | 13.11 | 11.84 | 6.73 | 0.10 | °C/W |

#### 2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance ($\theta_{JA}$) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

*EQ 4*

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

$\theta_{JA}$ = 14.7 °C/W (taken from Table 9, page 10).

$T_A$ = 85 °C

$$\text{Maximum power allowed} = \frac{100\ °C - 85\ °C}{14.7\ °C/W} = 1.088\ W$$

*EQ 5*

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

#### 2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance ($\theta_{JB}$) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

#### 2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance ($\theta_{JC}$) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

### 2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

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## 2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

### 2.3.2.1 Quiescent Supply Current

***Table 10 •*** **Quiescent Supply Current Characteristics**

| | Modes and Configurations | |
|---|---|---|
| **Power Supplies/Blocks** | **Non-Flash*Freeze** | **Flash*Freeze** |
| FPGA Core | On | Off |
| $V_{DD}$/SERDES_[01]_VDD[1] | On | On |
| $V_{PP}$/$V_{PPNVM}$ | On | On |
| HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDDA | 0 V | 0 V |
| SERDES_[01]_PLL_VDDA[2] | 0 V | 0 V |
| SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5[2] | On | On |
| SERDES_[01]_L[0123]_VDDAIIO[2] | On | On |
| $V_{DDIx}$[3, 4] | On | On |
| $V_{REFx}$ | On | On |
| MSSDDR CLK | 32 kHz | 32 kHz |
| RAM | On | Sleep state |
| System controller | 50 MHz | 50 MHz |
| 50 MHz oscillator (enable/disable) | Enable | Disabled |
| 1 MHz oscillator (enable/disable) | Disabled | Disabled |
| Crystal oscillator (enable/disable) | Disabled | Disabled |

1. SERDES_[01]_VDD Power Supply is shorted to $V_{DD}$.
2. SerDes and DDR blocks to be unused.
3. $V_{DDIx}$ has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate $V_{DDI}$ bank supplies. For details on bank power supplies, see “Recommendation for Unused Bank Supplies” table in the *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

***Table 11 •*** **SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD}$ = 1.2 V) – Typical Process**

| Symbol | Modes | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC1 | Non-Flash*Freeze | 6.2 | 6.9 | 8.9 | 13.1 | 15.3 | 15.4 | 27.5 | mA | Typical ($T_J$ = 25 °C) |
| | | 24.0 | 28.4 | 40.6 | 67.8 | 80.6 | 81.4 | 144.7 | mA | Commercial ($T_J$ = 85 °C) |
| | | 35.2 | 41.9 | 60.5 | 102.1 | 121.4 | 122.6 | 219.1 | mA | Industrial ($T_J$ = 100 °C) |

***Table 11 •*** **SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD}$ = 1.2 V) – Typical Process**

| Symbol | Modes | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC2 | Flash*Freeze | 1.4 | 2.6 | 3.7 | 5.1 | 5.0 | 5.1 | 8.9 | mA | Typical ($T_J$ = 25 °C) |
| | | 12.0 | 20.0 | 26.6 | 35.3 | 35.4 | 35.7 | 57.8 | mA | Commercial ($T_J$ = 85 °C) |
| | | 18.5 | 30.8 | 41.0 | 54.5 | 54.5 | 55.0 | 89.0 | mA | Industrial ($T_J$ = 100 °C) |

***Table 12 •*** **SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD}$ = 1.26 V) – Worst-Case Process**

| Symbol | Modes | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC1 | Non-Flash*Freeze | 43.8 | 57.0 | 84.6 | 132.3 | 161.4 | 163.0 | 242.5 | mA | Commercial ($T_J$= 85 °C) |
| | | 65.3 | 85.7 | 127.8 | 200.9 | 245.4 | 247.8 | 369.0 | mA | Industrial ($T_J$ = 100 °C) |
| IDC2 | Flash*Freeze | 29.1 | 45.6 | 51.7 | 62.7 | 69.3 | 70.0 | 84.8 | mA | Commercial ($T_J$ = 85 °C) |
| | | 44.9 | 70.3 | 79.7 | 96.5 | 106.8 | 107.8 | 130.6 | mA | Industrial ($T_J$ = 100 °C) |

### 2.3.2.2 Programming Currents

The following tables represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

***Table 13 •*** **Currents During Program Cycle, 0 °C < = $T_J$ <= 85 °C – Typical Process**

| Power Supplies | Voltage (V) | 005 | 010 | 025 | 050 | 060 | 090 | 150[1] | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | 1.26 | 46 | 53 | 55 | 58 | 30 | 42 | 52 | mA |
| $V_{PP}$ | 3.46 | 8 | 11 | 6 | 10 | 9 | 12 | 12 | mA |
| $V_{PPNVM}$ | 3.46 | 1 | 2 | 2 | 3 | 3 | 3 | | mA |
| $V_{DDI}$ | 2.62 | 31 | 16 | 17 | 1 | 12 | 12 | 81 | mA |
| | 3.46 | 62 | 31 | 36 | 1 | 12 | 17 | 84 | mA |
| Number of banks | | 7 | 8 | 8 | 10 | 10 | 9 | 19 | |

1. $V_{PP}$ and $V_{PPNVM}$ are internally shorted.

***Table 14 •*** **Currents During Verify Cycle, 0 °C <= $T_J$ <= 85 °C – Typical Process**

| Power Supplies | Voltage (V) | 005 | 010 | 025 | 050 | 060 | 090 | 150[1] | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | 1.26 | 44 | 53 | 55 | 58 | 33 | 41 | 51 | mA |
| $V_{PP}$ | 3.46 | 6 | 5 | 3 | 15 | 8 | 11 | 12 | mA |
| $V_{PPNVM}$ | 3.46 | 1 | 0 | 0 | 1 | 1 | 1 | | mA |
| $V_{DDI}$ | 2.62 | 31 | 16 | 17 | 1 | 12 | 11 | 81 | mA |
| | 3.46 | 61 | 32 | 36 | 1 | 12 | 17 | 84 | mA |
| Number of banks | | 7 | 8 | 8 | 10 | 10 | 9 | 19 | |

1. $V_{PP}$ and $V_{PPNVM}$ are internally shorted.

***Table 15 •*** **Inrush Currents at Power up, –40 °C <= $T_J$ <= 100 °C – Typical Process**

| Power Supplies | Voltage (V) | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | 1.26 | 25 | 32 | 38 | 48 | 45 | 77 | 109 | mA |
| $V_{PP}$ | 3.46 | 33 | 49 | 36 | 180 | 13 | 36 | 51 | mA |
| $V_{DDI}$ | 2.62 | 134 | 141 | 161 | 187 | 93 | 272 | 388 | mA |
| Number of banks | | 7 | 8 | 8 | 10 | 10 | 9 | 19 | |

## 2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to $T_J$ = 85 °C, in worst-case $V_{DD}$ = 1.14 V.

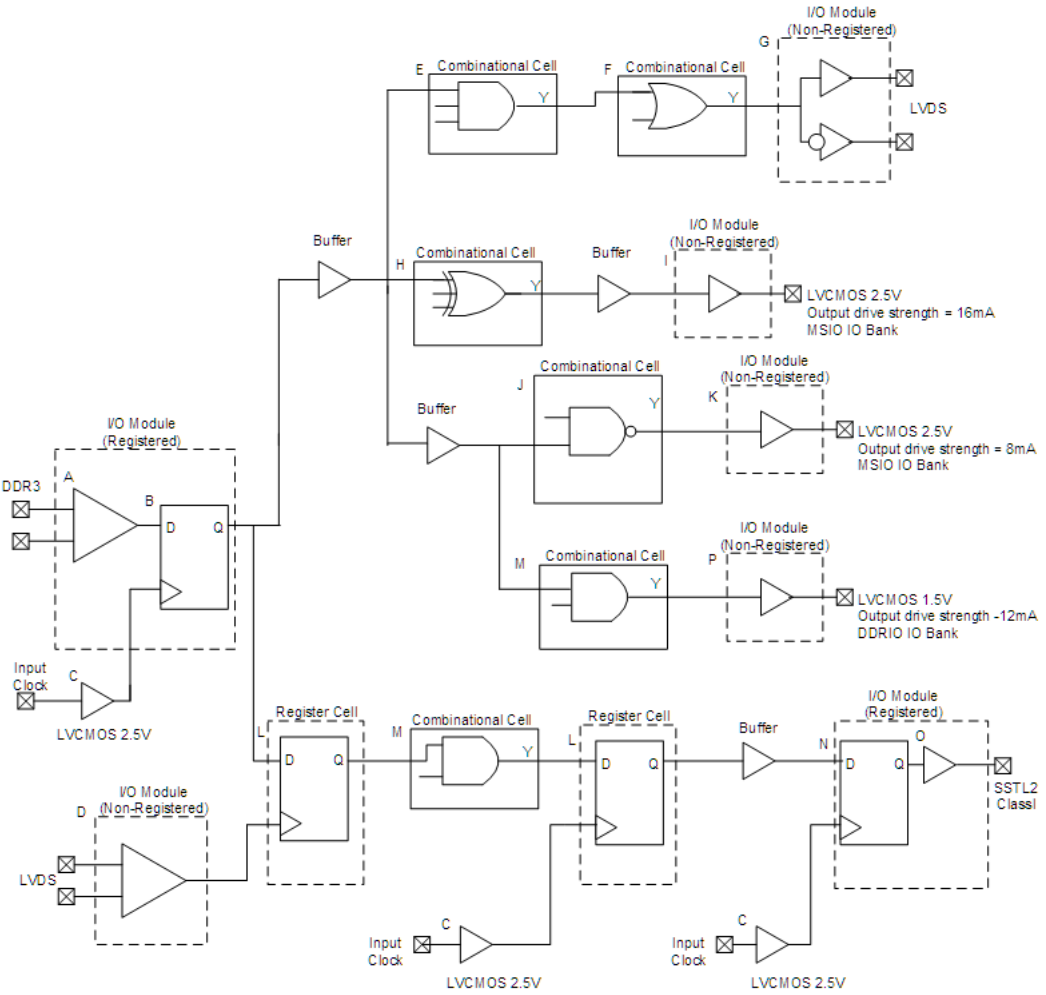
***Table 16 •*** **Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays**

| Array Voltage $V_{DD}$ (V) | –40 °C | 0 °C | 25 °C | 70 °C | 85 °C | 100 °C |
|---|---|---|---|---|---|---|
| 1.14 | 0.83 | 0.89 | 0.92 | 0.98 | **1.00** | 1.02 |
| 1.2 | 0.75 | 0.80 | 0.83 | 0.89 | 0.91 | 0.93 |
| 1.26 | 0.69 | 0.73 | 0.76 | 0.81 | 0.83 | 0.85 |

## 2.3.4 Timing Model

This section describes timing model and timing parameters.

***Figure 2 •*** **Timing Model**




The following table lists the timing model parameters in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 17 •*** **Timing Model Parameters**

| Index | Symbol | Description | –1 | Unit | For More Information |
|---|---|---|---|---|---|
| A | $T_{PY}$ | Propagation delay of DDR3 receiver | 1.605 | ns | See Table 137, page 50 |
| B | $T_{ICLKQ}$ | Clock-to-Q of the input data register | 0.16 | ns | See Table 221, page 71 |
| | $T_{ISUD}$ | Setup time of the input data register | 0.357 | ns | See Table 221, page 71 |
| C | $T_{RCKH}$ | Input high delay for global clock | 1.53 | ns | See Table 227, page 78 |
| | $T_{RCKL}$ | Input low delay for global clock | 0.897 | ns | See Table 227, page 78 |
| D | $T_{PY}$ | Input propagation delay of LVDS receiver | 2.774 | ns | See Table 167, page 56 |
| E | $T_{DP}$ | Propagation delay of a three-input AND gate | 0.198 | ns | See Table 223, page 76 |

***Table 17 •*** **Timing Model Parameters *(continued)***

| Index | Symbol | Description | –1 | Unit | For More Information |
|---|---|---|---|---|---|
| F | $T_{DP}$ | Propagation delay of an OR gate | 0.179 | ns | See Table 223, page 76 |
| G | $T_{DP}$ | Propagation delay of an LVDS transmitter | 2.136 | ns | See Table 169, page 57 |
| H | $T_{DP}$ | Propagation delay of a three-input XOR Gate | 0.241 | ns | See Table 223, page 76 |
| I | $T_{DP}$ | Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank | 2.412 | ns | See Table 46, page 27 |
| J | $T_{DP}$ | Propagation delay of a two-input NAND gate | 0.179 | ns | See Table 223, page 76 |
| K | $T_{DP}$ | Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank | 2.309 | ns | See Table 46, page 27 |
| L | $T_{CLKQ}$ | Clock-to-Q of the data register | 0.108 | ns | See Table 224, page 77 |
| | $T_{SUD}$ | Setup time of the data register | 0.254 | ns | See Table 224, page 77 |
| M | $T_{DP}$ | Propagation delay of a two-input AND gate | 0.179 | ns | See Table 223, page 76 |
| N | $T_{OCLKQ}$ | Clock-to-Q of the output data register | 0.263 | ns | See Table 220, page 69 |
| | $T_{OSUD}$ | Setup time of the output data register | 0.19 | ns | See Table 220, page 69 |
| O | $T_{DP}$ | Propagation delay of SSTL2, Class I transmitter on the MSIO bank | 2.055 | ns | See Table 114, page 45 |
| P | $T_{DP}$ | Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank | 3.316 | ns | See Table 70, page 34 |

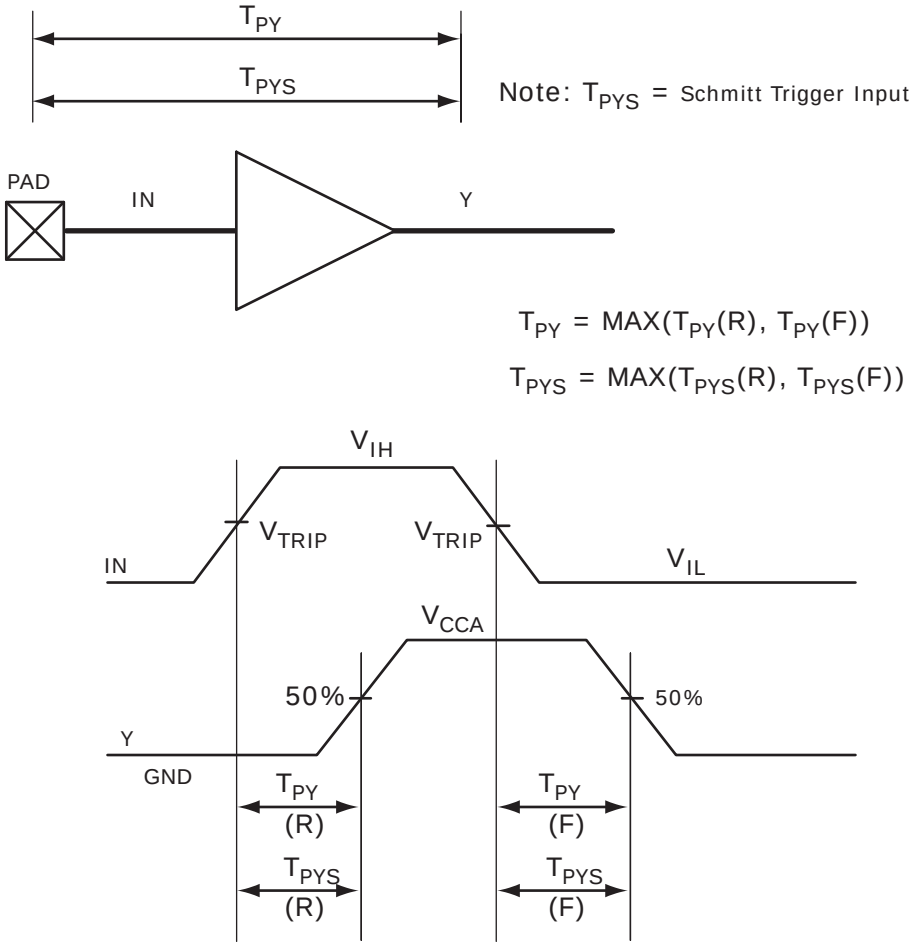
## 2.3.5 User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the I/Os section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

### 2.3.5.1 Input Buffer and AC Loading

The following figure shows the input buffer and AC loading.

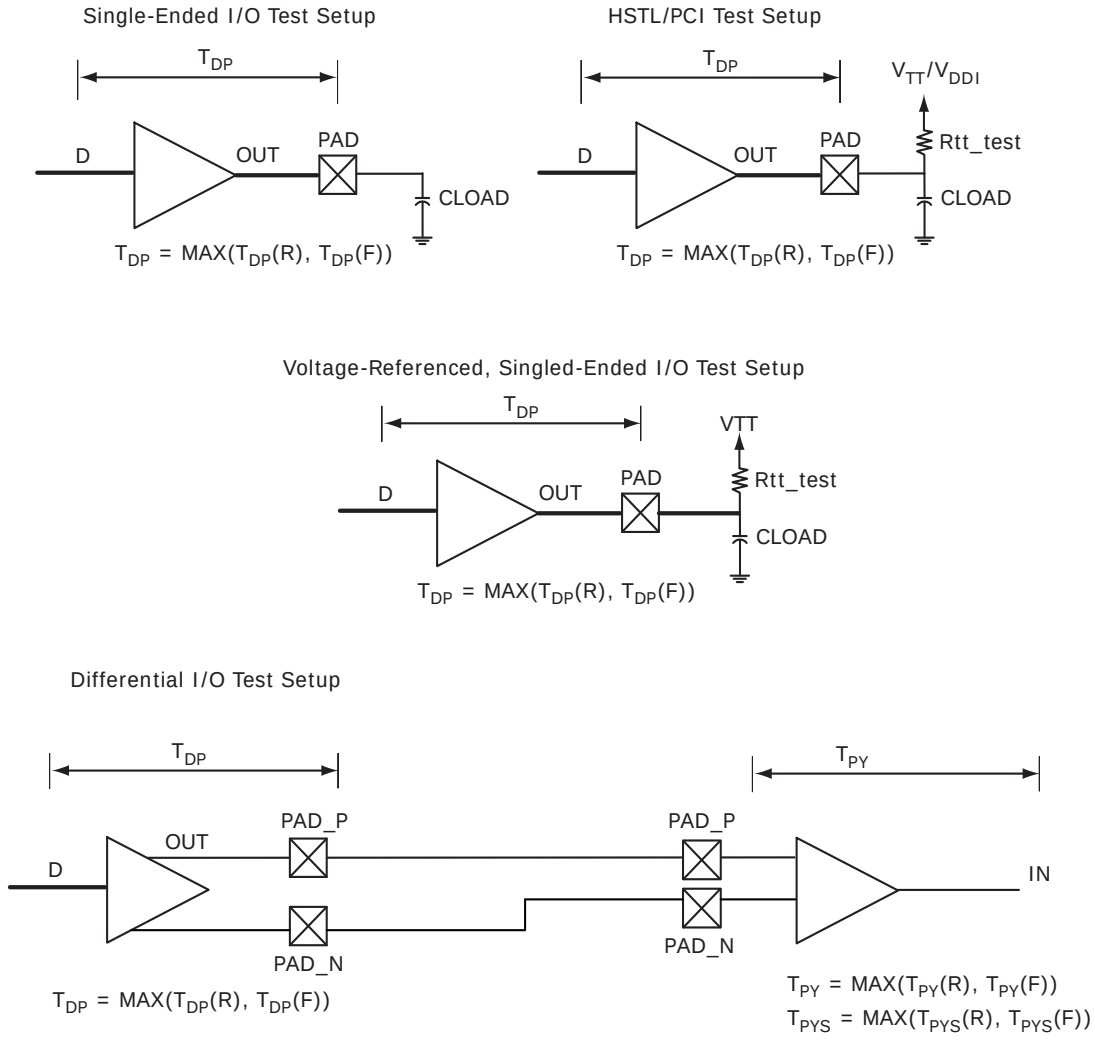
***Figure 3 •*** **Input Buffer AC Loading**



### 2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

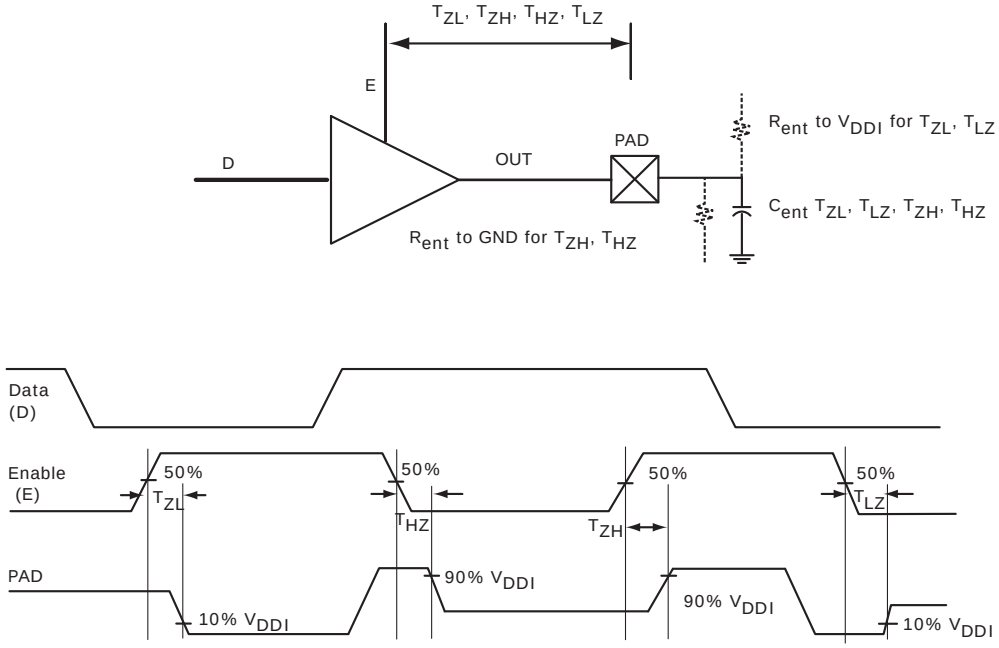
***Figure 4 •*** **Output Buffer AC Loading**



### 2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

***Figure 5 •*** **Tristate Buffer for Enable Path Test Point**




### 2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

***Table 18 •*** **Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| PCI 3.3 V | 630 | | | Mbps |
| LVTTL 3.3 V | 600 | | | Mbps |
| LVCMOS 3.3 V | 600 | | | Mbps |
| LVCMOS 2.5 V | 410 | 420 | 400 | Mbps |
| LVCMOS 1.8 V | 295 | 400 | 400 | Mbps |
| LVCMOS 1.5 V | 160 | 220 | 235 | Mbps |
| LVCMOS 1.2 V | 120 | 160 | 200 | Mbps |
| LPDDR-LVCMOS 1.8 V mode | | | 400 | Mbps |

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**Table 19 • Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| LPDDR | | | 400 | Mbps |
| HSTL1.5 V | | | 400 | Mbps |
| SSTL 2.5 V | 510 | 700 | 400 | Mbps |
| SSTL 1.8 V | | | 667 | Mbps |
| SSTL 1.5 V | | | 667 | Mbps |

**Table 20 • Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | Unit |
|---|---|---|---|
| LVPECL (input only) | 900 | | Mbps |
| LVDS 3.3 V | 535 | | Mbps |
| LVDS 2.5 V | 535 | 700 | Mbps |
| RSDS | 520 | 700 | Mbps |
| BLVDS | 500 | | Mbps |
| MLVDS | 500 | | Mbps |
| Mini-LVDS | 520 | 700 | Mbps |

**Table 21 • Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| PCI 3.3 V | 315 | | | MHz |
| LVTTL 3.3 V | 300 | | | MHz |
| LVCMOS 3.3 V | 300 | | | MHz |
| LVCMOS 2.5 V | 205 | 210 | 200 | MHz |
| LVCMOS 1.8 V | 147.5 | 200 | 200 | MHz |
| LVCMOS 1.5 V | 80 | 110 | 118 | MHz |
| LVCMOS 1.2 V | 60 | 80 | 100 | MHz |
| LPDDR– LVCMOS 1.8 V mode | | | 200 | MHz |

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***Table 22 •*** **Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| LPDDR | | | 200 | MHz |
| HSTL1.5 V | | | 200 | MHz |
| SSTL 2.5 V | 255 | 350 | 200 | MHz |
| SSTL 1.8 V | | | 334 | MHz |
| SSTL 1.5 V | | | 334 | MHz |

***Table 23 •*** **Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | Unit |
|---|---|---|---|
| LVPECL (input only) | 450 | | MHz |
| LVDS 3.3 V | 267.5 | | MHz |
| LVDS 2.5 V | 267.5 | 350 | MHz |
| RSDS | 260 | 350 | MHz |
| BLVDS | 250 | | MHz |
| MLVDS | 250 | | MHz |
| Mini-LVDS | 260 | 350 | MHz |

### 2.3.5.5 Detailed I/O Characteristics

***Table 24 •*** **Input Capacitance, Leakage Current, and Ramp Time**

| Symbol | Description | Maximum | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | 10 | pF | |
| $I_{IL}$ (dc) | Input current low (Applicable to HSTL/SSTL inputs only) | 400 | µA | $V_{DDI}$ = 2.5 V |
| | | 500 | µA | $V_{DDI}$ = 1.8 V |
| | | 600 | µA | $V_{DDI}$ = 1.5 V[1] |
| | Input current low (Applicable to all other digital inputs) | 10 | µA | |
| $I_{IH}$ (dc) | Input current high (Applicable to HSTL/SSTL inputs only) | 400 | µA | $V_{DDI}$ = 2.5 V |
| | | 500 | µA | $V_{DDI}$ = 1.8 V |
| | | 600 | µA | $V_{DDI}$ = 1.5 V[1] |
| | Input current high (Applicable to all other digital inputs) | 10 | µA | |
| $T_{RAMPIN}$[2] | Input ramp time (Applicable to all digital inputs) | 50 | ns | |

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at $V_{OH}/V_{OL}$ Level.

***Table 25 •*** **I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank**

| | R(WEAK PULL-UP) at $V_{OH}$ (Ω) | | R(WEAK PULL-DOWN) at $V_{OL}$ (Ω) | |
|---|---|---|---|---|
| $V_{DDI}$ Domain | Min | Max | Min | Max |
| 2.5 V[1, 2] | 10K | 17.8K | 9.98K | 18K |
| 1.8 V[1, 2] | 10.3K | 19.1K | 10.3K | 19.5K |
| 1.5 V[1, 2] | 10.6K | 20.2K | 10.6K | 21.1K |
| 1.2 V[1, 2] | 11.1K | 22.7K | 11.2K | 24.6K |

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at $V_{OH}/V_{OL}$ Level.

***Table 26 •*** **I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank**

| | R(WEAK PULL-UP) at $V_{OH}$ (Ω) | | R(WEAK PULL-DOWN) at $V_{OL}$ (Ω) | |
|---|---|---|---|---|
| **$V_{DDI}$ Domain** | **Min** | **Max** | **Min** | **Max** |
| 3.3 V | 9.9K | 17.1K | 9.98K | 17.5K |
| 2.5 V[1, 2] | 10K | 17.6K | 10.1K | 18.4K |
| 1.8 V[1, 2] | 10.4K | 19.1K | 10.4K | 20.4K |
| 1.5 V[1, 2] | 10.7K | 20.4K | 10.8K | 22.2K |
| 1.2 V[1, 2] | 11.3K | 23.2K | 11.5K | 26.7K |

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at $V_{OH}/V_{OL}$ Level.

***Table 27 •*** **I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank**

| | R(WEAK PULL-UP) at $V_{OH}$ (Ω) | | R(WEAK PULL-DOWN) at $V_{OL}$ (Ω) | |
|---|---|---|---|---|
| **$V_{DDI}$ Domain** | **Min** | **Max** | **Min** | **Max** |
| 2.5 V[1, 2] | 9.6K | 16.6K | 9.5K | 16.4K |
| 1.8 V[1, 2] | 9.7K | 17.3K | 9.7K | 17.1K |
| 1.5 V[1, 2] | 9.9K | 18K | 9.8K | 17.6K |
| 1.2 V[1, 2] | 10.3K | 19.6K | 10K | 19.1K |

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

***Table 28 •*** **Schmitt Trigger Input Hysteresis**

| Input Buffer Configuration | Hysteresis Value (Typical, unless otherwise noted) |
|---|---|
| 3.3 V LVTTL/LVCMOS/ PCI/PCI-X | 0.05 × $V_{DDI}$ (worst-case) |
| 2.5 V LVCMOS | 0.05 × $V_{DDI}$ (worst-case) |
| 1.8 V LVCMOS | 0.1 × $V_{DDI}$ (worst-case) |
| 1.5 V LVCMOS | 60 mV |
| 1.2 V LVCMOS | 20 mV |

### 2.3.5.6 Single-Ended I/O Standards

#### 2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

#### 2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 29 •*** **LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

***Table 30 •*** **LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | 2.0 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.8 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 31 •*** **LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high[1] | $V_{OH}$ | $V_{DDI}$ – 0.4 | | V |
| DC output logic low[1] | $V_{OL}$ | | 0.4 | V |

1. The $V_{OH}/V_{OL}$ test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

***Table 32 •*** **LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 2.4 | | V |
| DC output logic low | $V_{OL}$ | | 0.4 | V |

***Table 33 •*** **LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 600 | Mbps | AC loading: 17 pF load, maximum drive/slew |

**Table 34 • LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 1.4 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**Table 35 • LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank**

| Output Drive Selection | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) mA | IOL (at $V_{OL}$) mA |
|---|---|---|---|---|
| 2 mA | $V_{DDI}$ – 0.4 | 0.4 | 2 | 2 |
| 4 mA | $V_{DDI}$ – 0.4 | 0.4 | 4 | 4 |
| 8 mA | $V_{DDI}$ – 0.4 | 0.4 | 8 | 8 |
| 12 mA | $V_{DDI}$ – 0.4 | 0.4 | 12 | 12 |
| 16 mA | $V_{DDI}$ – 0.4 | 0.4 | 16 | 16 |
| 20 mA | $V_{DDI}$ – 0.4 | 0.4 | 20 | 20 |

**Note:** For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 3.0 V

**Table 36 • LVTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | Unit |
|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | |
| None | 2.262 | 2.663 | 2.289 | 2.695 | ns |

**Table 37 • LVTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 3.192 | 3.755 | 3.47 | 4.083 | 2.969 | 3.494 | 1.856 | 2.183 | 3.337 | 3.926 | ns |
| 4 mA | Slow | 2.331 | 2.742 | 2.673 | 3.145 | 2.526 | 2.973 | 3.034 | 3.569 | 4.451 | 5.236 | ns |
| 8 mA | Slow | 2.135 | 2.511 | 2.33 | 2.741 | 2.297 | 2.703 | 4.532 | 5.331 | 4.825 | 5.676 | ns |
| 12 mA | Slow | 2.052 | 2.414 | 2.107 | 2.479 | 2.162 | 2.544 | 5.75 | 6.764 | 5.445 | 6.406 | ns |
| 16 mA | Slow | 2.062 | 2.425 | 2.072 | 2.438 | 2.145 | 2.525 | 5.993 | 7.05 | 5.625 | 6.618 | ns |
| 20 mA | Slow | 2.148 | 2.527 | 1.999 | 2.353 | 2.088 | 2.458 | 6.262 | 7.367 | 5.876 | 6.913 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 38 •*** **LVCMOS 2.5 V DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

***Table 39 •*** **LVCMOS 2.5 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 1.7 | 2.625 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 1.7 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.7 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 40 •*** **LVCMOS 2.5 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$[1] | $V_{DDI}$ – 0.4 | – | V |
| DC output logic low | $V_{OL}$[2] | | 0.4 | V |

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

***Table 41 •*** **LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 410 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 420 | Mbps | AC loading: 17 pF load, maximum drive/slew |

***Table 42 •*** **LVCMOS 2.5 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | Rodt_cal | 75, 60, 50, 33, 25, 20 | Ω |

***Table 43 •*** **LVCMOS 2.5 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 1.2 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ωσ |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 44 •*** **LVCMOS 2.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank (With Software Default Fixed Code) | Min | Max | | |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ – 0.4 | 0.4 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ – 0.4 | 0.4 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ – 0.4 | 0.4 | 6 | 6 |
| 8 mA | 8 mA | 8 mA | $V_{DDI}$ – 0.4 | 0.4 | 8 | 8 |
| 12 mA | 12 mA | 12 mA | $V_{DDI}$ – 0.4 | 0.4 | 12 | 12 |
| 16 mA | | 16 mA | $V_{DDI}$ – 0.4 | 0.4 | 16 | 16 |

**Note:** For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at: www.microsemi.com/soc/download/ibis/default.aspx.

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

***Table 45 •*** **LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | Unit |
|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | |
| **LVCMOS 2.5 V (for DDRIO I/O bank)** | None | 1.823 | 2.145 | 1.932 | 2.274 | ns |
| **LVCMOS 2.5 V (for MSIO I/O bank)** | None | 2.486 | 2.925 | 2.495 | 2.935 | ns |
| **LVCMOS 2.5 V (for MSIOD I/O bank)** | None | 2.29 | 2.694 | 2.305 | 2.712 | ns |

***Table 46 •*** **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 3.657 | 4.302 | 3.393 | 3.991 | 3.675 | 4.323 | 3.894 | 4.582 | 3.552 | 4.18 | ns |
| | Medium | 3.374 | 3.97 | 3.139 | 3.693 | 3.396 | 3.995 | 3.635 | 4.277 | 3.253 | 3.828 | ns |
| | Medium fast | 3.239 | 3.811 | 3.036 | 3.572 | 3.261 | 3.836 | 3.519 | 4.141 | 3.128 | 3.681 | ns |
| | Fast | 3.224 | 3.793 | 3.029 | 3.563 | 3.246 | 3.818 | 3.512 | 4.132 | 3.119 | 3.67 | ns |

***Table 46 •*** **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers) *(continued)***

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 4 mA | Slow | 3.095 | 3.641 | 2.705 | 3.182 | 3.088 | 3.633 | 4.738 | 5.575 | 4.348 | 5.116 | ns |
| | Medium | 2.825 | 3.324 | 2.488 | 2.927 | 2.823 | 3.321 | 4.492 | 5.285 | 4.063 | 4.781 | ns |
| | Medium fast | 2.701 | 3.178 | 2.384 | 2.804 | 2.698 | 3.173 | 4.364 | 5.135 | 3.945 | 4.642 | ns |
| | Fast | 2.69 | 3.165 | 2.377 | 2.796 | 2.687 | 3.161 | 4.359 | 5.129 | 3.94 | 4.636 | ns |
| 6 mA | Slow | 2.919 | 3.434 | 2.491 | 2.93 | 2.902 | 3.414 | 5.085 | 5.983 | 4.674 | 5.5 | ns |
| | Medium | 2.65 | 3.118 | 2.279 | 2.681 | 2.642 | 3.108 | 4.845 | 5.701 | 4.375 | 5.148 | ns |
| | Medium fast | 2.529 | 2.975 | 2.176 | 2.56 | 2.521 | 2.965 | 4.724 | 5.558 | 4.259 | 5.011 | ns |
| | Fast | 2.516 | 2.96 | 2.168 | 2.551 | 2.508 | 2.95 | 4.717 | 5.55 | 4.251 | 5.002 | ns |
| 8 mA | Slow | 2.863 | 3.368 | 2.427 | 2.855 | 2.844 | 3.346 | 5.196 | 6.114 | 4.769 | 5.612 | ns |
| | Medium | 2.599 | 3.058 | 2.217 | 2.608 | 2.59 | 3.047 | 4.952 | 5.827 | 4.471 | 5.261 | ns |
| | Medium fast | 2.483 | 2.921 | 2.114 | 2.487 | 2.473 | 2.91 | 4.832 | 5.685 | 4.364 | 5.134 | ns |
| | Fast | 2.467 | 2.902 | 2.106 | 2.478 | 2.457 | 2.89 | 4.826 | 5.678 | 4.348 | 5.116 | ns |
| 12 mA | Slow | 2.747 | 3.232 | 2.296 | 2.701 | 2.724 | 3.204 | 5.39 | 6.342 | 4.938 | 5.81 | ns |
| | Medium | 2.493 | 2.934 | 2.102 | 2.473 | 2.483 | 2.921 | 5.166 | 6.078 | 4.65 | 5.471 | ns |
| | Medium fast | 2.382 | 2.803 | 2.006 | 2.36 | 2.371 | 2.789 | 5.067 | 5.962 | 4.546 | 5.349 | ns |
| | Fast | 2.369 | 2.787 | 1.999 | 2.352 | 2.357 | 2.773 | 5.063 | 5.958 | 4.538 | 5.339 | ns |
| 16 mA | Slow | 2.677 | 3.149 | 2.213 | 2.604 | 2.649 | 3.116 | 5.575 | 6.56 | 5.08 | 5.977 | ns |
| | Medium | 2.432 | 2.862 | 2.028 | 2.386 | 2.421 | 2.848 | 5.372 | 6.32 | 4.801 | 5.649 | ns |
| | Medium fast | 2.324 | 2.734 | 1.937 | 2.278 | 2.311 | 2.718 | 5.297 | 6.233 | 4.7 | 5.531 | ns |
| | Fast | 2.313 | 2.721 | 1.929 | 2.269 | 2.3 | 2.706 | 5.296 | 6.231 | 4.699 | 5.529 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 47 •*** **LVCMOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 3.48 | 4.095 | 3.855 | 4.534 | 3.785 | 4.453 | 2.12 | 2.494 | 3.45 | 4.059 | ns |
| 4 mA | Slow | 2.583 | 3.039 | 3.042 | 3.579 | 3.138 | 3.691 | 4.143 | 4.874 | 4.687 | 5.513 | ns |
| 6 mA | Slow | 2.392 | 2.815 | 2.669 | 3.139 | 2.82 | 3.317 | 4.909 | 5.775 | 5.083 | 5.98 | ns |
| 8 mA | Slow | 2.309 | 2.717 | 2.565 | 3.017 | 2.74 | 3.223 | 5.812 | 6.837 | 5.523 | 6.497 | ns |
| 12 mA | Slow | 2.333 | 2.745 | 2.437 | 2.867 | 2.626 | 3.089 | 6.131 | 7.213 | 5.712 | 6.72 | ns |
| 16 mA | Slow | 2.412 | 2.838 | 2.335 | 2.747 | 2.533 | 2.979 | 6.54 | 7.694 | 6.007 | 7.067 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 48 •*** **LVCMOS 2.5 V Transmitter Characteristics for MSIOD Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 2.206 | 2.596 | 2.678 | 3.15 | 2.64 | 3.106 | 4.935 | 5.805 | 4.74 | 5.576 | ns |
| 4 mA | Slow | 1.835 | 2.159 | 2.242 | 2.637 | 2.256 | 2.654 | 5.413 | 6.368 | 5.15 | 6.059 | ns |
| 6 mA | Slow | 1.709 | 2.01 | 2.132 | 2.508 | 2.167 | 2.549 | 5.813 | 6.838 | 5.499 | 6.469 | ns |
| 8 mA | Slow | 1.63 | 1.918 | 1.958 | 2.303 | 2.012 | 2.367 | 6.226 | 7.324 | 5.816 | 6.842 | ns |
| 12 mA | Slow | 1.648 | 1.939 | 1.86 | 2.187 | 1.921 | 2.259 | 6.519 | 7.669 | 6.027 | 7.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.8 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 49 •*** **LVCMOS 1.8 V DC Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **LVCMOS 1.8 V DC Recommended Operating Conditions** | | | | | |
| Supply voltage | $V_{DDI}$ | 1.710 | 1.8 | 1.89 | V |

***Table 50 •*** **LVCMOS 1.8 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 1.89 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.35 × $V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | – |
| Input current low[1] | $I_{IL}$ (DC) | | | – |

1. See Table 24, page 22.

***Table 51 •*** **LVCMOS 1.8 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | $V_{DDI}$ – 0.45 | | V |
| DC output logic low | $V_{OL}$ | | 0.45 | V |

***Table 52 •*** **LVCMOS 1.8 V Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank)[1] | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 295 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank)[1] | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |

1. Maximum Data Rate applies for Drive Strength 8 mA and above, All Slews.

**Table 53 • LVCMOS 1.8 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | Rodt_cal | 75, 60, 50, 33, 25, 20 | Ω |

**Table 54 • LVCMOS 1.8 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2k | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**Table 55 • LVCMOS 1.8 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) | IOL (at $V_{OL}$) |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min | Max | mA | mA |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ – 0.45 | 0.45 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ – 0.45 | 0.45 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ – 0.45 | 0.45 | 6 | 6 |
| 8 mA | 8 mA | 8 mA | $V_{DDI}$ – 0.45 | 0.45 | 8 | 8 |
| 10 mA | 10 mA | 10 mA | $V_{DDI}$ – 0.45 | 0.45 | 10 | 10 |
| 12 mA | | 12 mA | $V_{DDI}$ – 0.45 | 0.45 | 12 | 12 |
| | | 16 mA[1] | $V_{DDI}$ – 0.45 | 0.45 | 16 | 16 |

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.71 V

**Table 56 • LVCMOS 1.8 V Receiver Characteristics (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | Unit |
|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | |
| **LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)** | None | 1.968 | 2.315 | 2.099 | 2.47 | ns |
| **LVCMOS 1.8 V (for MSIO I/O bank)** | None | 2.898 | 3.411 | 2.883 | 3.393 | ns |
| | 50 | 3.05 | 3.59 | 3.044 | 3.583 | ns |
| | 75 | 2.999 | 3.53 | 2.987 | 3.516 | ns |
| | 150 | 2.947 | 3.469 | 2.933 | 3.452 | ns |
| **LVCMOS 1.8 V (for MSIOD I/O bank)** | None | 2.611 | 3.071 | 2.598 | 3.057 | ns |
| | 50 | 2.775 | 3.264 | 2.775 | 3.265 | ns |
| | 75 | 2.72 | 3.2 | 2.712 | 3.19 | ns |
| | 150 | 2.666 | 3.137 | 2.655 | 3.123 | ns |

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***Table 57 •*** **LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 4.234 | 4.981 | 3.646 | 4.29 | 4.245 | 4.995 | 4.908 | 5.774 | 4.434 | 5.216 | ns |
| | Medium | 3.824 | 4.498 | 3.282 | 3.861 | 3.834 | 4.511 | 4.625 | 5.441 | 4.116 | 4.843 | ns |
| | Medium fast | 3.627 | 4.267 | 3.111 | 3.66 | 3.637 | 4.279 | 4.481 | 5.272 | 3.984 | 4.687 | ns |
| | Fast | 3.605 | 4.241 | 3.097 | 3.644 | 3.615 | 4.253 | 4.472 | 5.262 | 3.973 | 4.674 | ns |
| 4 mA | Slow | 3.923 | 4.615 | 3.314 | 3.9 | 3.918 | 4.61 | 5.403 | 6.356 | 4.894 | 5.757 | ns |
| | Medium | 3.518 | 4.138 | 2.961 | 3.484 | 3.515 | 4.135 | 5.121 | 6.025 | 4.561 | 5.366 | ns |
| | Medium fast | 3.321 | 3.907 | 2.783 | 3.275 | 3.317 | 3.903 | 4.966 | 5.843 | 4.426 | 5.206 | ns |
| | Fast | 3.301 | 3.883 | 2.77 | 3.259 | 3.296 | 3.878 | 4.957 | 5.831 | 4.417 | 5.196 | ns |
| 6 mA | Slow | 3.71 | 4.364 | 3.104 | 3.652 | 3.702 | 4.355 | 5.62 | 6.612 | 5.08 | 5.977 | ns |
| | Medium | 3.333 | 3.921 | 2.779 | 3.27 | 3.325 | 3.913 | 5.346 | 6.289 | 4.777 | 5.62 | ns |
| | Medium fast | 3.155 | 3.712 | 2.62 | 3.083 | 3.146 | 3.702 | 5.21 | 6.13 | 4.657 | 5.479 | ns |
| | Fast | 3.134 | 3.688 | 2.608 | 3.068 | 3.125 | 3.677 | 5.202 | 6.12 | 4.648 | 5.468 | ns |
| 8 mA | Slow | 3.619 | 4.258 | 3.007 | 3.538 | 3.607 | 4.244 | 5.815 | 6.841 | 5.249 | 6.175 | ns |
| | Medium | 3.246 | 3.819 | 2.686 | 3.16 | 3.236 | 3.807 | 5.542 | 6.52 | 4.936 | 5.807 | ns |
| | Medium fast | 3.066 | 3.607 | 2.525 | 2.971 | 3.054 | 3.593 | 5.405 | 6.359 | 4.811 | 5.66 | ns |
| | Fast | 3.046 | 3.584 | 2.513 | 2.957 | 3.034 | 3.57 | 5.401 | 6.353 | 4.803 | 5.651 | ns |
| 10 mA | Slow | 3.498 | 4.115 | 2.878 | 3.386 | 3.481 | 4.096 | 6.046 | 7.113 | 5.444 | 6.404 | ns |
| | Medium | 3.138 | 3.692 | 2.569 | 3.023 | 3.126 | 3.678 | 5.782 | 6.803 | 5.129 | 6.034 | ns |
| | Medium fast | 2.966 | 3.489 | 2.414 | 2.841 | 2.951 | 3.472 | 5.666 | 6.665 | 5.013 | 5.897 | ns |
| | Fast | 2.945 | 3.464 | 2.401 | 2.826 | 2.93 | 3.448 | 5.659 | 6.658 | 5.003 | 5.886 | ns |
| 12 mA | Slow | 3.417 | 4.02 | 2.807 | 3.303 | 3.401 | 4.002 | 6.083 | 7.156 | 5.464 | 6.428 | ns |
| | Medium | 3.076 | 3.618 | 2.519 | 2.964 | 3.063 | 3.604 | 5.828 | 6.856 | 5.176 | 6.089 | ns |
| | Medium fast | 2.913 | 3.427 | 2.376 | 2.795 | 2.898 | 3.41 | 5.725 | 6.736 | 5.072 | 5.966 | ns |
| | Fast | 2.894 | 3.405 | 2.362 | 2.78 | 2.879 | 3.388 | 5.715 | 6.724 | 5.064 | 5.957 | ns |
| 16 mA | Slow | 3.366 | 3.96 | 2.751 | 3.237 | 3.348 | 3.939 | 6.226 | 7.324 | 5.576 | 6.56 | ns |
| | Medium | 3.03 | 3.565 | 2.47 | 2.906 | 3.017 | 3.55 | 5.981 | 7.036 | 5.282 | 6.214 | ns |
| | Medium fast | 2.87 | 3.377 | 2.328 | 2.739 | 2.854 | 3.358 | 5.895 | 6.935 | 5.18 | 6.094 | ns |
| | Fast | 2.853 | 3.357 | 2.314 | 2.723 | 2.837 | 3.338 | 5.889 | 6.929 | 5.177 | 6.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 58 •*** **LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 3.441 | 4.047 | 4.165 | 4.9 | 4.413 | 5.192 | 4.891 | 5.755 | 5.138 | 6.044 | ns |
| 4 mA | Slow | 3.218 | 3.786 | 3.642 | 4.284 | 3.941 | 4.636 | 5.665 | 6.665 | 5.568 | 6.551 | ns |
| 6 mA | Slow | 3.141 | 3.694 | 3.501 | 4.118 | 3.823 | 4.498 | 6.587 | 7.75 | 6.032 | 7.096 | ns |
| 8 mA | Slow | 3.165 | 3.723 | 3.319 | 3.904 | 3.654 | 4.298 | 6.898 | 8.115 | 6.216 | 7.313 | ns |
| 10 mA | Slow | 3.202 | 3.767 | 3.278 | 3.857 | 3.616 | 4.254 | 7.25 | 8.529 | 6.435 | 7.571 | ns |
| 12 mA | Slow | 3.277 | 3.855 | 3.175 | 3.736 | 3.519 | 4.139 | 7.392 | 8.697 | 6.538 | 7.692 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 59 •*** **LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 2.725 | 3.206 | 3.316 | 3.901 | 3.484 | 4.099 | 5.204 | 6.123 | 4.997 | 5.88 | ns |
| 4 mA | Slow | 2.242 | 2.638 | 2.777 | 3.267 | 2.947 | 3.466 | 5.729 | 6.74 | 5.448 | 6.41 | ns |
| 6 mA | Slow | 1.995 | 2.347 | 2.466 | 2.901 | 2.63 | 3.094 | 6.372 | 7.496 | 5.987 | 7.043 | ns |
| 8 mA | Slow | 2.001 | 2.354 | 2.44 | 2.87 | 2.6 | 3.058 | 6.633 | 7.804 | 6.193 | 7.286 | ns |
| 10 mA | Slow | 2.025 | 2.382 | 2.312 | 2.719 | 2.47 | 2.906 | 6.94 | 8.165 | 6.412 | 7.544 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.9 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 60 •*** **LVCMOS 1.5 V DC Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |

***Table 61 •*** **LVCMOS 1.5 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high for (MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 1.575 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.35 × $V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | – |
| Input current low[1] | $I_{IL}$ (DC | | | – |

1. See Table 24, page 22.

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**Table 62 • LVCMOS 1.5 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | VOH | $V_{DDI}$ × 0.75 | | V |
| DC output logic low | VOL | | $V_{DDI}$ × 0.25 | V |

**Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 235 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 160 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 220 | Mbps | AC loading: 17 pF load, maximum drive/slew |

**Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 40 | Ω |

**Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) | IOL (at $V_{OL}$) |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min | Max | mA | mA |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 6 | 6 |
| 8 mA | | 8 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 8 | 8 |
| | | 10 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 10 | 10 |
| | | 12 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 12 | 12 |

**Note:** For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

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### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.425 V

***Table 67 •*** **LVCMOS 1.5 V Receiver Characteristics for DDRIO I/O Bank with Fixed Codes (Input Buffers)**

| On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | Unit |
| None | 2.051 | 2.413 | 2.086 | 2.455 | ns |

***Table 68 •*** **LVCMOS 1.5 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | Unit |
| None | 3.311 | 3.896 | 3.285 | 3.865 | ns |
| 50 | 3.654 | 4.299 | 3.623 | 4.263 | ns |
| 75 | 3.533 | 4.156 | 3.501 | 4.119 | ns |
| 150 | 3.415 | 4.018 | 3.388 | 3.986 | ns |

***Table 69 •*** **LVCMOS 1.5 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

| On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | Unit |
| None | 2.959 | 3.481 | 2.93 | 3.447 | ns |
| 50 | 3.298 | 3.88 | 3.268 | 3.845 | ns |
| 75 | 3.162 | 3.719 | 3.128 | 3.68 | ns |
| 150 | 3.053 | 3.592 | 3.021 | 3.554 | ns |

***Table 70 •*** **LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 5.122 | 6.026 | 4.31 | 5.07 | 5.145 | 6.052 | 5.258 | 6.186 | 4.672 | 5.496 | ns |
| | Medium | 4.58 | 5.389 | 3.86 | 4.54 | 4.6 | 5.411 | 4.977 | 5.855 | 4.357 | 5.126 | ns |
| | Medium fast | 4.323 | 5.086 | 3.629 | 4.269 | 4.341 | 5.107 | 4.804 | 5.652 | 4.228 | 4.974 | ns |
| | Fast | 4.296 | 5.054 | 3.609 | 4.245 | 4.314 | 5.075 | 4.791 | 5.636 | 4.219 | 4.963 | ns |
| 4 mA | Slow | 4.449 | 5.235 | 3.707 | 4.361 | 4.443 | 5.227 | 6.058 | 7.127 | 5.458 | 6.421 | ns |
| | Medium | 3.961 | 4.66 | 3.264 | 3.839 | 3.954 | 4.651 | 5.778 | 6.797 | 5.116 | 6.018 | ns |
| | Medium fast | 3.729 | 4.387 | 3.043 | 3.579 | 3.72 | 4.376 | 5.63 | 6.624 | 4.981 | 5.86 | ns |
| | Fast | 3.704 | 4.358 | 3.027 | 3.56 | 3.695 | 4.347 | 5.624 | 6.617 | 4.973 | 5.851 | ns |

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***Table 70 •*** **LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers) *(continued)***

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 6 mA | Slow | 4.244 | 4.993 | 3.465 | 4.076 | 4.233 | 4.979 | 6.39 | 7.518 | 5.736 | 6.748 | ns |
| | Medium | 3.774 | 4.44 | 3.05 | 3.587 | 3.762 | 4.426 | 6.114 | 7.193 | 5.397 | 6.35 | ns |
| | Medium fast | 3.544 | 4.17 | 2.839 | 3.339 | 3.529 | 4.152 | 5.978 | 7.033 | 5.27 | 6.2 | ns |
| | Fast | 3.519 | 4.14 | 2.82 | 3.317 | 3.504 | 4.122 | 5.965 | 7.017 | 5.259 | 6.187 | ns |
| 8 mA | Slow | 4.099 | 4.823 | 3.311 | 3.894 | 4.087 | 4.807 | 6.584 | 7.746 | 5.854 | 6.888 | ns |
| | Medium | 3.656 | 4.301 | 2.927 | 3.443 | 3.642 | 4.284 | 6.311 | 7.425 | 5.553 | 6.533 | ns |
| | Medium fast | 3.437 | 4.044 | 2.731 | 3.213 | 3.42 | 4.023 | 6.182 | 7.273 | 5.435 | 6.394 | ns |
| | Fast | 3.41 | 4.012 | 2.715 | 3.193 | 3.393 | 3.991 | 6.178 | 7.269 | 5.425 | 6.383 | ns |
| 10 mA | Slow | 4.029 | 4.74 | 3.238 | 3.809 | 4.015 | 4.723 | 6.732 | 7.921 | 5.965 | 7.018 | ns |
| | Medium | 3.601 | 4.237 | 2.867 | 3.372 | 3.586 | 4.218 | 6.473 | 7.615 | 5.669 | 6.669 | ns |
| | Medium fast | 3.384 | 3.981 | 2.672 | 3.143 | 3.365 | 3.958 | 6.351 | 7.471 | 5.55 | 6.529 | ns |
| | Fast | 3.357 | 3.949 | 2.655 | 3.123 | 3.338 | 3.927 | 6.345 | 7.464 | 5.54 | 6.518 | ns |
| 12 mA | Slow | 3.974 | 4.675 | 3.196 | 3.759 | 3.958 | 4.656 | 6.842 | 8.049 | 6.068 | 7.139 | ns |
| | Medium | 3.55 | 4.176 | 2.827 | 3.326 | 3.534 | 4.157 | 6.584 | 7.746 | 5.751 | 6.766 | ns |
| | Medium fast | 3.345 | 3.935 | 2.638 | 3.103 | 3.325 | 3.911 | 6.488 | 7.633 | 5.641 | 6.637 | ns |
| | Fast | 3.316 | 3.902 | 2.621 | 3.083 | 3.297 | 3.878 | 6.486 | 7.63 | 5.626 | 6.619 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 71 •*** **LVCMOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 4.423 | 5.203 | 5.397 | 6.35 | 5.686 | 6.69 | 5.609 | 6.599 | 5.561 | 6.542 | ns |
| 4 mA | Slow | 4.05 | 4.765 | 4.503 | 5.298 | 4.92 | 5.788 | 7.358 | 8.657 | 6.525 | 7.677 | ns |
| 6 mA | Slow | 4.081 | 4.801 | 4.259 | 5.012 | 4.699 | 5.528 | 7.659 | 9.011 | 6.709 | 7.893 | ns |
| 8 mA | Slow | 4.234 | 4.98 | 4.068 | 4.786 | 4.521 | 5.319 | 8.218 | 9.668 | 7.05 | 8.294 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 72 •*** **LVCMOS 1.5 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 2.735 | 3.218 | 3.371 | 3.966 | 3.618 | 4.257 | 6.03 | 7.095 | 5.705 | 6.712 | ns |
| 4 mA | Slow | 2.426 | 2.854 | 2.992 | 3.521 | 3.221 | 3.79 | 6.738 | 7.927 | 6.298 | 7.41 | ns |
| 6 mA | Slow | 2.433 | 2.862 | 2.81 | 3.306 | 3.031 | 3.566 | 7.123 | 8.38 | 6.596 | 7.76 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.10 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 73 •*** **LVCMOS 1.2 V DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.140 | 1.2 | 1.26 | V |

***Table 74 •*** **LVCMOS 1.2 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 1.26 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.35 × $V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 75 •*** **LVCMOS 1.2 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | $V_{DDI}$ × 0.75 | | V |
| DC output logic low | $V_{OL}$ | | $V_{DDI}$ × 0.25 | V |

***Table 76 •*** **LVCMOS 1.2 V Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 200 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 120 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 160 | Mbps | AC loading: 17 pF load, maximum drive/slew |

**Table 77 • LVCMOS 1.2 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 40 | Ω |

**Table 78 • LVCMOS 1.2 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point | $V_{TRIP}$ | 0.6 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**Table 79 • LVCMOS 1.2 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) | IOL (at $V_{OL}$) |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min | Max | mA | mA |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 4 | 4 |
| | | 6 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 6 | 6 |

**Note:** For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.14 V

**Table 80 • LVCMOS 1.2 V Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

| | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | –1 | –Std | Unit |
| None | 2.448 | 2.88 | 2.466 | 2.901 | ns |

**Table 81 • LVCMOS 1.2 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| On-Die Termination ODT) | –1 | –Std | –1 | –Std | Unit |
| None | 4.714 | 5.545 | 4.675 | 5.5 | ns |
| 50 | 6.668 | 7.845 | 6.579 | 7.74 | ns |
| 75 | 5.832 | 6.862 | 5.76 | 6.777 | ns |
| 150 | 5.162 | 6.073 | 5.111 | 6.014 | ns |

***Table 82 •*** **LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

| | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| None | 4.154 | 4.887 | 4.114 | 4.84 | ns |
| 50 | 6.918 | 8.139 | 6.806 | 8.008 | ns |
| 75 | 5.613 | 6.603 | 5.533 | 6.509 | ns |
| 150 | 4.716 | 5.549 | 4.657 | 5.479 | ns |

***Table 83 •*** **LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| **Output Drive Selection** | **Slew Control** | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2 mA | Slow | 6.713 | 7.897 | 5.362 | 6.308 | 6.723 | 7.909 | 7.233 | 8.51 | 6.375 | 7.499 | ns |
| | Medium | 5.912 | 6.955 | 4.616 | 5.43 | 5.915 | 6.959 | 6.887 | 8.102 | 6.009 | 7.069 | ns |
| | Medium fast | 5.5 | 6.469 | 4.231 | 4.978 | 5.5 | 6.471 | 6.672 | 7.849 | 5.835 | 6.865 | ns |
| | Fast | 5.462 | 6.426 | 4.194 | 4.935 | 5.463 | 6.427 | 6.646 | 7.819 | 5.828 | 6.857 | ns |
| 4 mA | Slow | 6.109 | 7.186 | 4.708 | 5.539 | 6.098 | 7.174 | 8.005 | 9.418 | 7.033 | 8.274 | ns |
| | Medium | 5.355 | 6.299 | 4.034 | 4.746 | 5.338 | 6.28 | 7.637 | 8.985 | 6.672 | 7.849 | ns |
| | Medium fast | 4.953 | 5.826 | 3.685 | 4.336 | 4.932 | 5.802 | 7.44 | 8.752 | 6.499 | 7.646 | ns |
| | Fast | 4.911 | 5.777 | 3.658 | 4.303 | 4.89 | 5.754 | 7.427 | 8.737 | 6.488 | 7.632 | ns |
| 6 mA | Slow | 5.89 | 6.929 | 4.506 | 5.301 | 5.874 | 6.911 | 8.337 | 9.808 | 7.315 | 8.605 | ns |
| | Medium | 5.176 | 6.089 | 3.862 | 4.543 | 5.155 | 6.065 | 7.986 | 9.394 | 6.943 | 8.168 | ns |
| | Medium fast | 4.792 | 5.637 | 3.523 | 4.145 | 4.765 | 5.606 | 7.808 | 9.186 | 6.775 | 7.97 | ns |
| | Fast | 4.754 | 5.593 | 3.486 | 4.101 | 4.728 | 5.563 | 7.777 | 9.149 | 6.769 | 7.963 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 84 •*** **LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| **Output Drive Selection** | **Slew Control** | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2 mA | Slow | 6.746 | 7.937 | 7.458 | 8.774 | 8.172 | 9.614 | 9.867 | 11.608 | 8.393 | 9.874 | ns |
| 4 mA | Slow | 7.068 | 8.315 | 6.678 | 7.857 | 7.474 | 8.793 | 10.986 | 12.924 | 9.043 | 10.638 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 85 •*** **LVCMOS 1.2 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 3.883 | 4.568 | 4.868 | 5.726 | 5.329 | 6.269 | 7.994 | 9.404 | 7.527 | 8.855 | ns |
| 4 mA | Slow | 3.774 | 4.44 | 4.188 | 4.926 | 4.613 | 5.426 | 8.972 | 10.555 | 8.315 | 9.782 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.11 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

**Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to MSIO Bank Only)**

***Table 86 •*** **PCI/PCI-X DC Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

***Table 87 •*** **PCI/PCI-X DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 3.45 | V |
| Input current high[1] | $I_{IH}$(DC) | | | |
| Input current low[1] | $I_{IL}$(DC) | | | |

1. See Table 24, page 22.

***Table 88 •*** **PCI/PCI-X DC Output Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | | Per PCI specification | | V |
| DC output logic low | $V_{OL}$ | | Per PCI specification | | V |

***Table 89 •*** **PCI/PCI-X Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (MSIO I/O bank) | $D_{MAX}$ | 630 | Mbps | AC Loading: per JEDEC specifications |

***Table 90 •*** **PCI/PCI-X AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path (falling edge) | $V_{TRIP}$ | 0.615 × $V_{DDI}$ | V |
| Measuring/trip point for data path (rising edge) | $V_{TRIP}$ | 0.285 × $V_{DDI}$ | V |
| Resistance for data test path | RTT_TEST | 25 | Ω |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 10 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 3.0 V

***Table 91 •*** **PCI/PCIX AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| None | 2.229 | 2.623 | 2.238 | 2.633 | ns |

***Table 92 •*** **PCI/PCIX AC switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.146 | 2.525 | 2.043 | 2.404 | 2.084 | 2.452 | 6.095 | 7.171 | 5.558 | 6.539 | ns |

## 2.3.6 Memory Interface and Voltage Referenced I/O Standards

This section describes High-Speed Transceiver Logic (HSTL) memory interface and voltage reference I/O standards.

### 2.3.6.1 High-Speed Transceiver Logic (HSTL)

The HSTL standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to DDRIO Bank Only)**

***Table 93 •*** **HSTL Recommended DC Operating Conditions**

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |
| Termination voltage | $V_{TT}$ | 0.698 | 0.750 | 0.803 | V |
| Input reference voltage | $V_{REF}$ | 0.698 | 0.750 | 0.803 | V |

***Table 94 •*** **HSTL DC Input Voltage Specification**

| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | $V_{REF}$ + 0.1 | 1.575 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | $V_{REF}$ – 0.1 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 95 •*** **HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| | **HSTL Class I** | | | |
| DC output logic high | $V_{OH}$ | $V_{DDI}$ – 0.4 | | V |
| DC output logic low | $V_{OL}$ | | 0.4 | V |
| Output minimum source DC current (MSIO and DDRIO I/O banks) | $I_{OH}$ at $V_{OH}$ | –8.0 | | mA |
| Output minimum sink current (MSIO and DDRIO I/O banks) | $I_{OL}$ at $V_{OL}$ | 8.0 | | mA |
| | **HSTL Class II** | | | |
| DC output logic high | $V_{OH}$ | $V_{DDI}$ – 0.4 | | V |
| DC output logic low | $V_{OL}$ | | 0.4 | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | –16.0 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | 16.0 | | mA |

***Table 96 •*** **HSTL DC Differential Voltage Specification**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| DC input differential voltage | $V_{ID}$ (DC) | 0.2 | V |

***Table 97 •*** **HSTL AC Differential Voltage Specifications**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ | 0.4 | | V |
| AC differential cross point voltage | $V_x$ | 0.68 | 0.9 | V |

***Table 98 •*** **HSTL Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |

***Table 99 •*** **HSTL Impedance Specification**

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | $R_{REF}$ | 25.5, 47.8 | Ω | Reference resistance = 191 Ω |
| Effective impedance value (ODT for DDRIO I/O bank only) | $R_{TT}$ | 47.8 | Ω | Reference resistance = 191 Ω |

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***Table 100 •*** **HSTL AC Test Parameter Specification**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for HSTL15 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for HSTL15 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**AC Switching Characteristics**

Worst-case commercial conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, worst-case $V_{DDI}$.

***Table 101 •*** **HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| Pseudo differential | None | 1.605 | 1.888 | ns |
| | 47.8 | 1.614 | 1.898 | ns |
| True differential | None | 1.622 | 1.909 | ns |
| | 47.8 | 1.628 | 1.916 | ns |

***Table 102 •*** **HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| **HSTL Class I** | | | | | | | | | | | |
| Single-ended | 2.6 | 3.059 | 2.514 | 2.958 | 2.514 | 2.958 | 2.431 | 2.86 | 2.431 | 2.86 | ns |
| Differential | 2.621 | 3.083 | 2.648 | 3.115 | 2.647 | 3.113 | 2.925 | 3.442 | 2.923 | 3.44 | ns |
| **HSTL Class II** | | | | | | | | | | | |
| Single-ended | 2.511 | 2.954 | 2.488 | 2.927 | 2.49 | 2.93 | 2.409 | 2.833 | 2.411 | 2.836 | ns |
| Differential | 2.528 | 2.974 | 2.552 | 3.003 | 2.551 | 3.001 | 2.897 | 3.409 | 2.896 | 3.408 | ns |

### 2.3.6.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

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### 2.3.6.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 103 •*** **DDR1/SSTL2 DC Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |
| Termination voltage | $V_{TT}$ | 1.164 | 1.250 | 1.339 | V |
| Input reference voltage | $V_{REF}$ | 1.164 | 1.250 | 1.339 | V |

***Table 104 •*** **DDR1/SSTL2 DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | $V_{REF}$ + 0.15 | 2.625 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | VREF – 0.15 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 105 •*** **DDR1/SSTL2 DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **SSTL2 Class I (DDR Reduced Drive)** | | | | |
| DC output logic high | $V_{OH}$ | $V_{TT}$ + 0.608 | | V |
| DC output logic low | $V_{OL}$ | | $V_{TT}$ – 0.608 | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 8.1 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –8.1 | | mA |
| **SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Bank Only** | | | | |
| DC output logic high | $V_{OH}$ | $V_{TT}$ + 0.81 | | V |
| DC output logic low | $V_{OL}$ | | $V_{TT}$ – 0.81 | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 16.2 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –16.2 | | mA |

***Table 106 •*** **DDR1/SSTL2 DC Differential Voltage Specification**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| DC input differential voltage | $V_{ID}$ (DC) | 0.3 | V |

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***Table 107 •*** **SSTL2 AC Differential Voltage Specifications**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ (AC) | 0.7 | | V |
| AC differential cross point voltage | $V_x$ (AC) | 0.5 × $V_{DDI}$ – 0.2 | 0.5 × $V_{DDI}$ + 0.2 | V |

***Table 108 •*** **SSTL2 Minimum and Maximum AC Switching Speeds**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 575 | Mbps | AC loading: 17pF load |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 700 | Mbps | AC loading: 3 pF / 50 Ω load |
| | | 510 | Mbps | AC loading: 17pF load |

***Table 109 •*** **SSTL2 AC Impedance Specifications**

| Parameter | Typ | Unit | Conditions |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | 20, 42 | Ω | Reference resistor = 150 Ω |

***Table 110 •*** **DDR1/SSTL2 AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 1.25 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for SSTL2 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for SSTL2 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

***Table 111 •*** **SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | Unit |
|---|---|---|---|---|
| | | –1 | –Std | |
| Pseudo differential | None | 1.549 | 1.821 | ns |
| True differential | None | 1.589 | 1.87 | ns |

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**Table 112 • SSTL2 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | |
|---|---|---|---|---|
| | | –1 | –Std | Unit |
| Pseudo differential | None | 2.798 | 3.293 | ns |
| True differential | None | 2.733 | 3.215 | ns |

**Table 113 • DDR1/SSTL2 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | |
|---|---|---|---|---|
| | | –1 | –Std | Unit |
| Pseudo differential | None | 2.476 | 2.913 | ns |
| True differential | None | 2.475 | 2.911 | ns |

**Table 114 • SSTL2 Class I Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.26 | 2.66 | 1.99 | 2.341 | 1.985 | 2.335 | 2.135 | 2.512 | 2.13 | 2.505 | ns |
| Differential | 2.26 | 2.658 | 2.202 | 2.591 | 2.201 | 2.589 | 2.393 | 2.815 | 2.392 | 2.814 | ns |

**Table 115 • DDR1/SSTL2 Class I Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.055 | 2.417 | 2.037 | 2.396 | 2.03 | 2.388 | 2.068 | 2.433 | 2.061 | 2.425 | ns |
| Differential | 2.192 | 2.58 | 2.434 | 2.864 | 2.425 | 2.852 | 2.164 | 2.545 | 2.156 | 2.536 | ns |

**Table 116 • DDR1/SSTL2 Class I Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 1.512 | 1.779 | 1.462 | 1.72 | 1.462 | 1.72 | 1.676 | 1.972 | 1.676 | 1.971 | ns |
| Differential | 1.676 | 1.971 | 1.774 | 2.087 | 1.766 | 2.077 | 1.854 | 2.181 | 1.845 | 2.171 | ns |

**Table 117 • DDR1/SSTL2 Class II Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.122 | 2.497 | 1.906 | 2.243 | 1.902 | 2.237 | 2.061 | 2.424 | 2.056 | 2.418 | ns |
| Differential | 2.127 | 2.501 | 2.042 | 2.402 | 2.043 | 2.403 | 2.363 | 2.78 | 2.365 | 2.781 | ns |

**Table 118 • DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.29 | 2.693 | 1.988 | 2.338 | 1.978 | 2.326 | 1.989 | 2.34 | 1.979 | 2.328 | ns |
| Differential | 2.418 | 2.846 | 2.304 | 2.711 | 2.297 | 2.702 | 2.131 | 2.506 | 2.124 | 2.499 | ns |

### 2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double date rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

**Table 119 • SSTL18 DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.71 | 1.8 | 1.89 | V |
| Termination voltage | $V_{TT}$ | 0.838 | 0.900 | 0.964 | V |
| Input reference voltage | $V_{REF}$ | 0.838 | 0.900 | 0.964 | V |

**Table 120 • SSTL18 DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | $V_{REF}$ + 0.125 | 1.89 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | $V_{REF}$ – 0.125 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

**Table 121 • SSTL18 DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **SSTL18 Class I (DDR2 Reduced Drive)** | | | | |
| DC output logic high | $V_{OH}$ | $V_{TT}$ + 0.603 | | V |
| DC output logic low | $V_{OL}$ | | $V_{TT}$– 0.603 | V |
| Output minimum source DC current (DDRIO I/O bank only) | $I_{OH}$ at $V_{OH}$ | 6.5 | | mA |
| Output minimum sink current (DDRIO I/O bank only) | $I_{OL}$ at $V_{OL}$ | –6.5 | | mA |
| **SSTL18 Class II (DDR2 Full Drive)[1]** | | | | |
| DC output logic high | $V_{OH}$ | $V_{TT}$ + 0.603 | | V |
| DC output logic low | $V_{OL}$ | | $V_{TT}$– 0.603 | V |
| Output minimum source DC current (DDRIO I/O bank only) | $I_{OH}$ at $V_{OH}$ | 13.4 | | mA |
| Output minimum sink current (DDRIO I/O bank only) | $I_{OL}$ at $V_{OL}$ | –13.4 | | mA |

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

**Table 122 • SSTL18 DC Differential Voltage Specification**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| DC input differential voltage | $V_{ID}$ (DC) | 0.3 | V |

**Table 123 • SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ (AC) | 0.5 | | V |
| AC differential cross point voltage | $V_x$ (AC) | 0.5 × $V_{DDI}$ – 0.175 | 0.5 × $V_{DDI}$ + 0.175 | V |

**Table 124 • SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 667 | Mbps | AC loading: per JEDEC specification |

**Table 125 • SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)**

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | $R_{REF}$ | 20, 42 | Ω | Reference resistor = 150 Ω |
| Effective impedance value (ODT) | $R_{TT}$ | 50, 75, 150 | Ω | Reference resistor = 150 Ω |

**Table 126 • SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for SSTL18 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for SSTL18 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.71 V

**Table 127 • DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | On-Die Termination (ODT) | –1 | –Std | Unit |
| Pseudo differential | None | 1.567 | 1.844 | ns |
| True differential | None | 1.588 | 1.869 | ns |

***Table 128 •*** **DDR2/SSTL18 Transmitter Characteristics (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| **SSTL18 Class I (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.383 | 2.804 | 2.23 | 2.623 | 2.229 | 2.622 | 2.202 | 2.591 | 2.201 | 2.59 | ns |
| Differential | 2.413 | 2.84 | 2.797 | 3.29 | 2.797 | 3.29 | 2.282 | 2.685 | 2.282 | 2.685 | ns |
| **SSTL18 Class II (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.281 | 2.683 | 2.196 | 2.584 | 2.195 | 2.583 | 2.171 | 2.555 | 2.17 | 2.554 | ns |
| Differential | 2.315 | 2.724 | 2.698 | 3.173 | 2.698 | 3.173 | 2.242 | 2.639 | 2.242 | 2.639 | ns |

### 2.3.6.5 Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

The following table lists the SSTL15 DC voltage specifications for DDRIO bank.

***Table 129 •*** **SSTL15 DC Recommended DC Operating Conditions (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |
| Termination voltage | $V_{TT}$ | 0.698 | 0.750 | 0.803 | V |
| Input reference voltage | $V_{REF}$ | 0.698 | 0.750 | 0.803 | V |

***Table 130 •*** **SSTL15 DC Input Voltage Specification (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}(DC)$ | $V_{REF}$ + 0.1 | 1.575 | V |
| DC input logic low | $V_{IL}(DC)$ | –0.3 | $V_{REF}$ – 0.1 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

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***Table 131 •*** **SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **DDR3/SSTL15 Class I (DDR3 Reduced Drive)** | | | | |
| DC output logic high | $V_{OH}$ | 0.8 × $V_{DDI}$ | | V |
| DC output logic low | $V_{OL}$ | | 0.2 × $V_{DDI}$ | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 6.5 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –6.5 | | mA |
| **DDR3/SSTL15 Class II (DDR3 Full Drive)** | | | | |
| DC output logic high | $V_{OH}$ | 0.8 × $V_{DDI}$ | | V |
| DC output logic low | $V_{OL}$ | | 0.2 × $V_{DDI}$ | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 7.6 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –7.6 | | mA |

***Table 132 •*** **SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| DC input differential voltage | $V_{ID}$ | 0.2 | V |

**Note:** To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

***Table 133 •*** **SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ (AC) | 0.3 | | V |
| AC differential cross point voltage | $V_x$ (AC) | 0.5 × $V_{DDI}$ – 0.150 | 0.5 × $V_{DDI}$ + 0.150 | V |

***Table 134 •*** **SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 667 | Mbps | AC loading: per JEDEC specifications |

***Table 135 •*** **SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance | $R_{REF}$ | 34, 40 | Ω | Reference resistor = 240 Ω |
| Effective impedance value (ODT) | $R_{TT}$ | 20, 30, 40, 60, 120 | Ω | Reference resistor = 240 Ω |

***Table 136 •*** **SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for SSTL15 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for SSTL15 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.425 V

***Table 137 •*** **DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank – with Calibration Only**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| Pseudo differential | None | 1.605 | 1.888 | ns |
| | 20 | 1.616 | 1.901 | ns |
| | 30 | 1.613 | 1.897 | ns |
| | 40 | 1.611 | 1.895 | ns |
| | 60 | 1.609 | 1.893 | ns |
| | 120 | 1.607 | 1.89 | ns |
| True differential | None | 1.623 | 1.91 | ns |
| | 20 | 1.637 | 1.926 | ns |
| | 30 | 1.63 | 1.918 | ns |
| | 40 | 1.626 | 1.914 | ns |
| | 60 | 1.622 | 1.91 | ns |
| | 120 | 1.619 | 1.905 | ns |

***Table 138 •*** **DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| **DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.533 | 2.98 | 2.522 | 2.967 | 2.523 | 2.968 | 2.427 | 2.855 | 2.428 | 2.856 | ns |
| Differential | 2.555 | 3.005 | 3.073 | 3.615 | 3.073 | 3.615 | 2.416 | 2.843 | 2.416 | 2.843 | ns |
| **DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.53 | 2.977 | 2.514 | 2.958 | 2.516 | 2.96 | 2.422 | 2.849 | 2.425 | 2.852 | ns |
| Differential | 2.552 | 3.002 | 2.591 | 3.048 | 2.59 | 3.047 | 2.882 | 3.391 | 2.881 | 3.39 | ns |

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### 2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 139 •*** **LPDDR DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max |
|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.71 | 1.8 | 1.89 |
| Termination voltage | $V_{TT}$ | 0.838 | 0.900 | 0.964 |
| Input reference voltage | $V_{REF}$ | 0.838 | 0.900 | 0.964 |

***Table 140 •*** **LPDDR DC Input Voltage Specification**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | 0.7 × $V_{DDI}$ | 1.89 |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.3 × $V_{DDI}$ |
| Input current high[1] | $I_{IH}$ (DC) | | |
| Input current low[1] | $I_{IL}$ (DC) | | |

1. See Table 24, page 22.

***Table 141 •*** **LPDDR DC Output Voltage Specification Reduced Drive**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| DC output logic high | $V_{OH}$ | 0.9 × $V_{DDI}$ | |
| DC output logic low | $V_{OL}$ | | 0.1 × $V_{DDI}$ |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 0.1 | |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –0.1 | |

***Table 142 •*** **LPDDR DC Output Voltage Specification Full Drive[1]**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| DC output logic high | $V_{OH}$ | 0.9 × $V_{DDI}$ | |
| DC output logic low | $V_{OL}$ | | 0.1 × $V_{DDI}$ |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 0.1 | |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –0.1 | |

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

***Table 143 •*** **LPDDR DC Differential Voltage Specification**

| Parameter | Symbol | Min |
|---|---|---|
| DC input differential voltage | $V_{ID}$ (DC) | 0.4 × $V_{DDI}$ |

**Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ | 0.6 × $V_{DDI}$ | | V |
| AC differential cross point voltage | $V_x$ | 0.4 × $V_{DDI}$ | 0.6 × $V_{DDI}$ | V |

**Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |

**Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance | $R_{REF}$ | 20, 42 | Ω | Reference resistor = 150 Ω |
| Effective impedance value (ODT) | $R_{TT}$ | 50, 70, 150 | Ω | Reference resistor = 150 Ω |

**Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for LPDDR ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | Ω |

**AC Switching Characteristics**

Worst-case commercial conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, worst-case $V_{DDI}$.

**Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | On-Die Termination (ODT) | –1 | –Std | Unit |
| Pseudo differential | None | 1.568 | 1.845 | ns |
| True differential | None | 1.588 | 1.869 | ns |

**Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ENZL}$ | | $T_{ENZH}$ | | $T_{ENHZ}$ | | $T_{ENLZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.383 | 2.804 | 2.23 | 2.623 | 2.229 | 2.622 | 2.202 | 2.591 | 2.201 | 2.59 | ns |
| Differential | 2.396 | 2.819 | 2.764 | 3.252 | 2.764 | 3.252 | 2.255 | 2.653 | 2.255 | 2.653 | ns |

***Table 150 •*** **LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ENZL}$ | | $T_{ENZH}$ | | $T_{ENHZ}$ | | $T_{ENLZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| Single-ended | 2.281 | 2.683 | 2.196 | 2.584 | 2.195 | 2.583 | 2.171 | 2.555 | 2.17 | 2.554 | ns |
| Differential | 2.298 | 2.703 | 2.288 | 2.692 | 2.288 | 2.692 | 2.593 | 3.051 | 2.593 | 3.051 | ns |

**Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode**

***Table 151 •*** **LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.710 | 1.8 | 1.89 | V |

***Table 152 •*** **LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 1.89 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.35 × $V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 153 •*** **LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | $V_{DDI}$ – 0.45 | | V |
| DC output logic low | $V_{OL}$ | | 0.45 | V |

***Table 154 •*** **LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: 17pf load, 8 ma drive and above/all slew |

***Table 155 •*** **LPDDR-LVCMOS 1.8 V Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 33, 25, 20 | Ω |

***Table 156 •*** **LPDDR-LVCMOS 1.8 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 157 •*** **LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification for DDRIO Bank**

| Output Drive Selection | $V_{OH}$ (V) Min | $V_{OL}$ (V) Max | $I_{OH}$ (at $V_{OH}$) mA | $I_{OL}$ (at $V_{OL}$) mA |
|---|---|---|---|---|
| 2 mA | $V_{DDI}$ – 0.45 | 0.45 | 2 | 2 |
| 4 mA | $V_{DDI}$ – 0.45 | 0.45 | 4 | 4 |
| 6 mA | $V_{DDI}$ – 0.45 | 0.45 | 6 | 6 |
| 8 mA | $V_{DDI}$ – 0.45 | 0.45 | 8 | 8 |
| 10 mA | $V_{DDI}$ – 0.45 | 0.45 | 10 | 10 |
| 12 mA | $V_{DDI}$ – 0.45 | 0.45 | 12 | 12 |
| 16 mA[1] | $V_{DDI}$ – 0.45 | 0.45 | 16 | 16 |

1. 16 mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance.

***Table 158 •*** **LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (for DDRIO I/O Bank with Fixed Code - Input Buffers)**

| ODT (On Die Termination) | –1 | –Std | –1 | –Std | Unit |
|---|---|---|---|---|---|
| None | 1.968 | 2.315 | 2.099 | 2.47 | ns |

***Table 159 •*** **LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | slow | 4.234 | 4.981 | 3.646 | 4.29 | 4.245 | 4.995 | 4.908 | 5.774 | 4.434 | 5.216 | ns |
| | medium | 3.824 | 4.498 | 3.282 | 3.861 | 3.834 | 4.511 | 4.625 | 5.441 | 4.116 | 4.843 | ns |
| | medium_fast | 3.627 | 4.267 | 3.111 | 3.66 | 3.637 | 4.279 | 4.481 | 5.272 | 3.984 | 4.687 | ns |
| | fast | 3.605 | 4.241 | 3.097 | 3.644 | 3.615 | 4.253 | 4.472 | 5.262 | 3.973 | 4.674 | ns |
| 4 mA | slow | 3.923 | 4.615 | 3.314 | 3.9 | 3.918 | 4.61 | 5.403 | 6.356 | 4.894 | 5.757 | ns |
| | medium | 3.518 | 4.138 | 2.961 | 3.484 | 3.515 | 4.135 | 5.121 | 6.025 | 4.561 | 5.366 | ns |
| | medium_fast | 3.321 | 3.907 | 2.783 | 3.275 | 3.317 | 3.903 | 4.966 | 5.843 | 4.426 | 5.206 | ns |
| | fast | 3.301 | 3.883 | 2.77 | 3.259 | 3.296 | 3.878 | 4.957 | 5.831 | 4.417 | 5.196 | ns |
| 6 mA | slow | 3.71 | 4.364 | 3.104 | 3.652 | 3.702 | 4.355 | 5.62 | 6.612 | 5.08 | 5.977 | ns |
| | medium | 3.333 | 3.921 | 2.779 | 3.27 | 3.325 | 3.913 | 5.346 | 6.289 | 4.777 | 5.62 | ns |
| | medium_fast | 3.155 | 3.712 | 2.62 | 3.083 | 3.146 | 3.702 | 5.21 | 6.13 | 4.657 | 5.479 | ns |
| | fast | 3.134 | 3.688 | 2.608 | 3.068 | 3.125 | 3.677 | 5.202 | 6.12 | 4.648 | 5.468 | ns |
| 8 mA | slow | 3.619 | 4.258 | 3.007 | 3.538 | 3.607 | 4.244 | 5.815 | 6.841 | 5.249 | 6.175 | ns |

***Table 159 •*** **LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)** ***(continued)***

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | medium | 3.246 | 3.819 | 2.686 | 3.16 | 3.236 | 3.807 | 5.542 | 6.52 | 4.936 | 5.807 | ns |
| | medium_fast | 3.066 | 3.607 | 2.525 | 2.971 | 3.054 | 3.593 | 5.405 | 6.359 | 4.811 | 5.66 | ns |
| | fast | 3.046 | 3.584 | 2.513 | 2.957 | 3.034 | 3.57 | 5.401 | 6.353 | 4.803 | 5.651 | ns |
| 10 mA | slow | 3.498 | 4.115 | 2.878 | 3.386 | 3.481 | 4.096 | 6.046 | 7.113 | 5.444 | 6.404 | ns |
| | medium | 3.138 | 3.692 | 2.569 | 3.023 | 3.126 | 3.678 | 5.782 | 6.803 | 5.129 | 6.034 | ns |
| | medium_fast | 2.966 | 3.489 | 2.414 | 2.841 | 2.951 | 3.472 | 5.666 | 6.665 | 5.013 | 5.897 | ns |
| | fast | 2.945 | 3.464 | 2.401 | 2.826 | 2.93 | 3.448 | 5.659 | 6.658 | 5.003 | 5.886 | ns |
| 12 mA | slow | 3.417 | 4.02 | 2.807 | 3.303 | 3.401 | 4.002 | 6.083 | 7.156 | 5.464 | 6.428 | ns |
| | medium | 3.076 | 3.618 | 2.519 | 2.964 | 3.063 | 3.604 | 5.828 | 6.856 | 5.176 | 6.089 | ns |
| | medium_fast | 2.913 | 3.427 | 2.376 | 2.795 | 2.898 | 3.41 | 5.725 | 6.736 | 5.072 | 5.966 | ns |
| | fast | 2.894 | 3.405 | 2.362 | 2.78 | 2.879 | 3.388 | 5.715 | 6.724 | 5.064 | 5.957 | ns |
| 16 mA | slow | 3.366 | 3.96 | 2.751 | 3.237 | 3.348 | 3.939 | 6.226 | 7.324 | 5.576 | 6.56 | ns |
| | medium | 3.03 | 3.565 | 2.47 | 2.906 | 3.017 | 3.55 | 5.981 | 7.036 | 5.282 | 6.214 | ns |
| | medium_fast | 2.87 | 3.377 | 2.328 | 2.739 | 2.854 | 3.358 | 5.895 | 6.935 | 5.18 | 6.094 | ns |
| | fast | 2.853 | 3.357 | 2.314 | 2.723 | 2.837 | 3.338 | 5.889 | 6.929 | 5.177 | 6.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management).

## 2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

### 2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

**Minimum and Maximum Input and Output Levels**

***Table 160 •*** **LVDS Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V | 3.3 V range |

***Table 161 •*** **LVDS DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| DC Input voltage | $V_I$ | 0 | 2.925 | V | 2.5 V range |
| DC input voltage | $V_I$ | 0 | 3.45 | V | 3.3 V range |
| Input current high[1] | $I_{IH}$ (DC) | | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | | |

1. See Table 24, page 22.

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***Table 162 •*** **LVDS DC Output Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

***Table 163 •*** **LVDS DC Differential Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Differential output voltage swing | $V_{OD}$ | 250 | 350 | 450 | mV |
| Output common mode voltage | $V_{OCM}$ | 1.125 | 1.25 | 1.375 | V |
| Input common mode voltage | $V_{ICM}$ | 0.05 | 1.25 | 2.35 | V |
| Input differential voltage | $V_{ID}$ | 100 | 350 | 600 | mV |

***Table 164 •*** **LVDS Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 535 | Mbps | AC loading: 12 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) no pre-emphasis | $D_{MAX}$ | 620 | Mbps | AC loading: 10 pF / 100 Ω differential load |
| | | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

***Table 165 •*** **LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Termination resistance | RT | 100 | | Ω |

***Table 166 •*** **LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

**LVDS25 AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

***Table 167 •*** **LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.774 | 3.263 | ns |
| 100 | 2.775 | 3.264 | ns |

**Table 168 • LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.554 | 3.004 | ns |
| 100 | 2.549 | 2.999 | ns |

**Table 169 • LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2.136 | 2.513 | 2.416 | 2.842 | 2.402 | 2.825 | 2.423 | 2.85 | 2.409 | 2.833 | ns |

**Table 170 • LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| No pre-emphasis | 1.61 | 1.893 | 1.749 | 2.058 | 1.735 | 2.041 | 1.897 | 2.231 | 1.866 | 2.195 | ns |
| Min pre-emphasis | 1.527 | 1.796 | 1.757 | 2.067 | 1.744 | 2.052 | 1.905 | 2.241 | 1.876 | 2.207 | ns |
| Med pre-emphasis | 1.496 | 1.76 | 1.765 | 2.077 | 1.751 | 2.06 | 1.914 | 2.252 | 1.884 | 2.216 | ns |

### LVDS33 AC Switching Characteristics

**Table 171 • LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| On Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.572 | 3.025 | ns |
| 100 | 2.569 | 3.023 | ns |

**Table 172 • LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 1.942 | 2.284 | 1.98 | 2.33 | 1.97 | 2.318 | 1.953 | 2.298 | 1.96 | 2.307 | ns |

### 2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 173 •*** **B-LVDS Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

***Table 174 •*** **B-LVDS DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 2.925 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 175 •*** **B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

***Table 176 •*** **B-LVDS DC Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing (for MSIO I/O bank only) | $V_{OD}$ | 65 | 460 | mV |
| Output common mode voltage (for MSIO I/O bank only) | $V_{OCM}$ | 1.1 | 1.5 | V |
| Input common mode voltage | $V_{ICM}$ | 0.05 | 2.4 | V |
| Input differential voltage | $V_{ID}$ | 0.1 | $V_{DDI}$ | V |

***Table 177 •*** **B-LVDS Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 500 | Mbps | AC loading: 2 pF / 100 Ω differential load |

***Table 178 •*** **B-LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | $R_T$ | 27 | Ω |

***Table 179 •*** **B-LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

***Table 180 •*** **B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.738 | 3.221 | ns |
| 100 | 2.735 | 3.218 | ns |

***Table 181 •*** **B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.495 | 2.934 | ns |
| 100 | 2.495 | 2.935 | ns |

***Table 182 •*** **B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.258 | 2.656 | 2.343 | 2.756 | 2.329 | 2.74 | 2.12 | 2.494 | 2.123 | 2.497 | ns |

### 2.3.7.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

**Minimum and Maximum Input and Output Levels**

***Table 183 •*** **M-LVDS Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage[1] | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

1. Only M-LVDS TYPE I is supported.

***Table 184 •*** **M-LVDS DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 2.925 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[2] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

**Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

**Table 186 • M-LVDS Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing (for MSIO I/O bank only) | $V_{OD}$ | 300 | 650 | mV |
| Output common mode voltage (for MSIO I/O bank only) | $V_{OCM}$ | 0.3 | 2.1 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.2 | V |
| Input differential voltage | $V_{ID}$ | 50 | 2400 | mV |

**Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 500 | Mbps | AC loading: 2 pF / 100 Ω differential load |

**Table 188 • M-LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | $R_T$ | 50 | Ω |

**Table 189 • M-LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

**Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.738 | 3.221 | ns |
| 100 | 2.735 | 3.218 | ns |

**Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.495 | 2.934 | ns |
| 100 | 2.495 | 2.935 | ns |

**Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.258 | 2.656 | 2.348 | 2.762 | 2.334 | 2.746 | 2.123 | 2.497 | 2.125 | 2.5 | ns |

### 2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

**Mini-LVDS Minimum and Maximum Input and Output Levels**

**Table 193 • Mini-LVDS Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

**Table 194 • Mini-LVDS DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC Input voltage | $V_I$ | 0 | 2.925 | V |

**Table 195 • Mini-LVDS DC Output Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

**Table 196 • Mini-LVDS DC Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing | $V_{OD}$ | 300 | 600 | mV |
| Output common mode voltage | $V_{OCM}$ | 1 | 1.4 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.2 | V |
| Input differential voltage | $V_{ID}$ | 100 | 600 | mV |

**Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 520 | Mbps | AC loading: 2 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

**Table 198 • Mini-LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | $R_T$ | 100 | Ω |

**Table 199 • Mini-LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

**Table 200 • Mini-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.855 | 3.359 | ns |
| 100 | 2.85 | 3.353 | ns |
| None | 2.602 | 3.061 | ns |
| 100 | 2.597 | 3.055 | ns |

**Table 201 • Mini-LVDS AC Switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2.097 | 2.467 | 2.308 | 2.715 | 2.296 | 2.701 | 1.964 | 2.31 | 1.949 | 2.293 | ns |

**Table 202 • Mini-LVDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| No pre-emphasis | 1.614 | 1.899 | 1.562 | 1.837 | 1.553 | 1.826 | 1.593 | 1.874 | 1.578 | 1.856 | ns |
| Min pre-emphasis | 1.604 | 1.887 | 1.745 | 2.053 | 1.731 | 2.036 | 1.892 | 2.225 | 1.861 | 2.189 | ns |
| Med pre-emphasis | 1.521 | 1.79 | 1.753 | 2.062 | 1.737 | 2.043 | 1.9 | 2.235 | 1.868 | 2.197 | ns |
| Max pre-emphasis | 1.492 | 1.754 | 1.762 | 2.073 | 1.745 | 2.052 | 1.91 | 2.247 | 1.876 | 2.206 | ns |

### 2.3.7.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

**Minimum and Maximum Input and Output Levels**

***Table 203 •*** **RSDS Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

***Table 204 •*** **RSDS DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 2.925 | V |

***Table 205 •*** **RSDS DC Output Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

***Table 206 •*** **RSDS Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing | $V_{OD}$ | 100 | 600 | mV |
| Output common mode voltage | $V_{OCM}$ | 0.5 | 1.5 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.5 | V |
| Input differential voltage | $V_{ID}$ | 100 | 600 | mV |

***Table 207 •*** **RSDS Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 520 | Mbps | AC loading: 2 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

***Table 208 •*** **RSDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | RT | 100 | Ω |

***Table 209 •*** **RSDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

***Table 210 •*** **RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.855 | 3.359 | ns |
| 100 | 2.85 | 3.353 | ns |

***Table 211 •*** **RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.602 | 3.061 | ns |
| 100 | 2.597 | 3.055 | ns |

***Table 212 •*** **RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.097 | 2.467 | 2.303 | 2.709 | 2.291 | 2.695 | 1.961 | 2.307 | 1.947 | 2.29 | ns |

***Table 213 •*** **RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| No pre-emphasis | 1.614 | 1.899 | 1.559 | 1.834 | 1.55 | 1.823 | 1.59 | 1.87 | 1.575 | 1.852 | ns |
| Min pre-emphasis | 1.604 | 1.887 | 1.742 | 2.05 | 1.728 | 2.032 | 1.889 | 2.222 | 1.858 | 2.185 | ns |
| Med pre-emphasis | 1.521 | 1.79 | 1.753 | 2.062 | 1.737 | 2.043 | 1.9 | 2.235 | 1.868 | 2.197 | ns |
| Max pre-emphasis | 1.492 | 1.754 | 1.762 | 2.073 | 1.745 | 2.052 | 1.91 | 2.247 | 1.876 | 2.206 | ns |

### 2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

**Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)**

***Table 214 •*** **LVPECL Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

**Table 215 • LVPECL DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 3.45 | V |

**Table 216 • LVPECL DC Differential Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input common mode voltage | $V_{ICM}$ | 0.3 | | 2.8 | V |
| Input differential voltage | $V_{IDIFF}$ | 100 | 300 | 1,000 | mV |

**Table 217 • LVPECL Minimum and Maximum AC Switching Speeds**

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 900 | Mbps |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

**Table 218 • LVPECL Receiver Characteristics for MSIO I/O Bank**

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.572 | 3.025 | ns |
| 100 | 2.569 | 3.023 | ns |

## 2.3.8 I/O Register Specifications

This section describes input and output register specifications.

### 2.3.8.1 Input Register

**Figure 6 • Timing Model for Input Register**

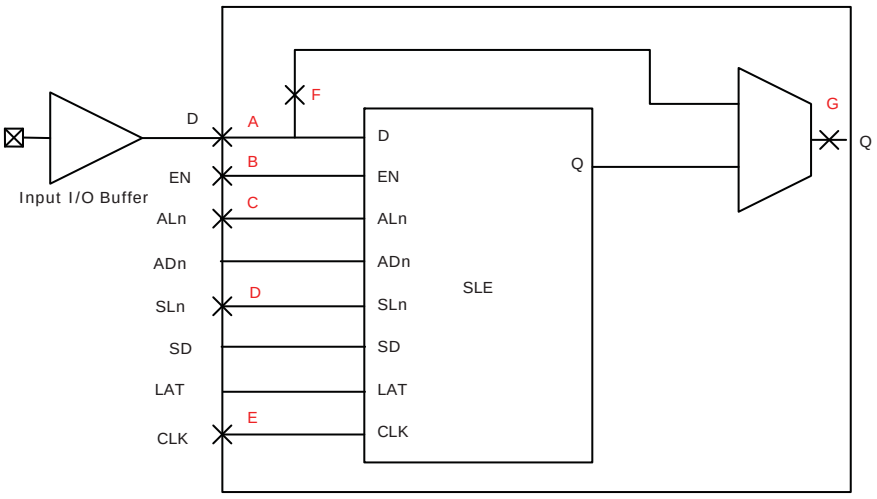
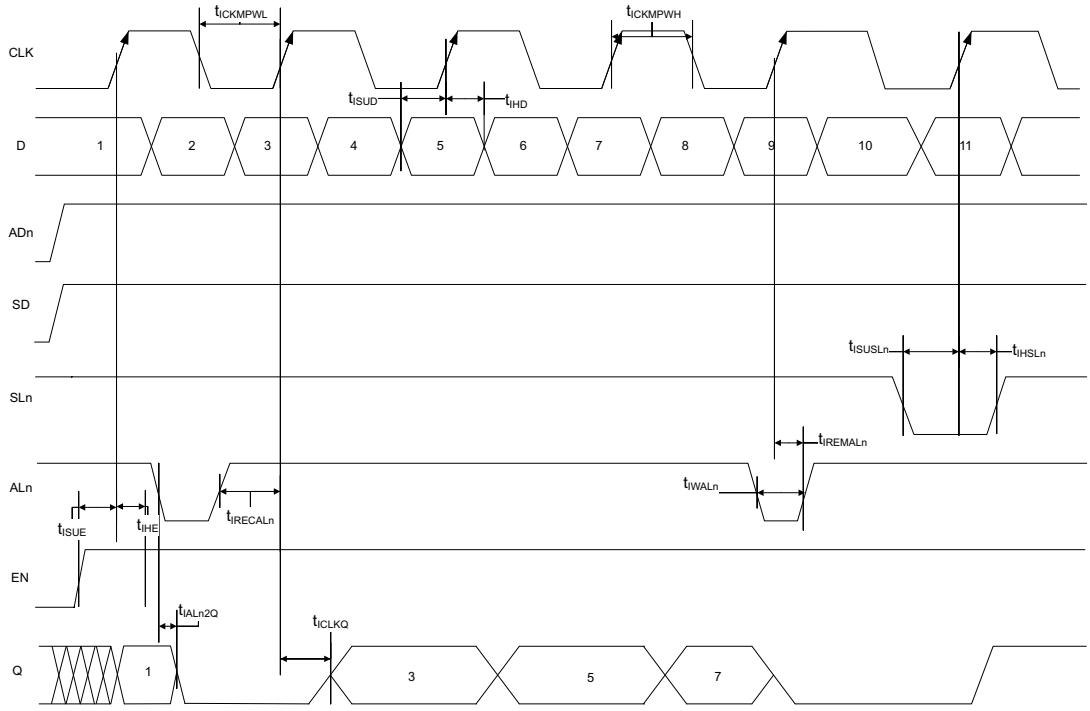


***Figure 7 •*** **I/O Register Input Timing Diagram**



The following table lists the input data register propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 219 •*** **Input Data Register Propagation Delays**

| Parameter | Symbol | Measuring Nodes (from, to)[1] | –1 | –Std | Unit |
|---|---|---|---|---|---|
| Bypass delay of the input register | $T_{IBYP}$ | F, G | 0.353 | 0.415 | ns |
| Clock-to-Q of the input register | $T_{ICLKQ}$ | E, G | 0.16 | 0.188 | ns |
| Data setup time for the input register | $T_{ISUD}$ | A, E | 0.357 | 0.421 | ns |
| Data hold time for the input register | $T_{IHD}$ | A, E | 0 | 0 | ns |
| Enable setup time for the input register | $T_{ISUE}$ | B, E | 0.46 | 0.542 | ns |
| Enable hold time for the input register | $T_{IHE}$ | B, E | 0 | 0 | ns |
| Synchronous load setup time for the input register | $T_{ISUSL}$ | D, E | 0.46 | 0.542 | ns |
| Synchronous load hold time for the input register | $T_{IHSL}$ | D, E | 0 | 0 | ns |
| Asynchronous clear-to-Q of the input register (ADn=1) | $T_{IALN2Q}$ | C, G | 0.625 | 0.735 | ns |
| Asynchronous preset-to-Q of the input register (ADn=0) | | C, G | 0.587 | 0.69 | ns |
| Asynchronous load removal time for the input register | $T_{IREMALN}$ | C, E | 0 | 0 | ns |
| Asynchronous load recovery time for the input register | $T_{IRECALN}$ | C, E | 0.074 | 0.087 | ns |
| Asynchronous load minimum pulse width for the input register | $T_{IWALN}$ | C, C | 0.304 | 0.357 | ns |
| Clock minimum pulse width high for the input register | $T_{ICKMPWH}$ | E, E | 0.075 | 0.088 | ns |
| Clock minimum pulse width low for the input register | $T_{ICKMPWL}$ | E, E | 0.159 | 0.187 | ns |

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

### 2.3.8.2 Output/Enable Register

***Figure 8 •*** **Timing Model for Output/Enable Register**

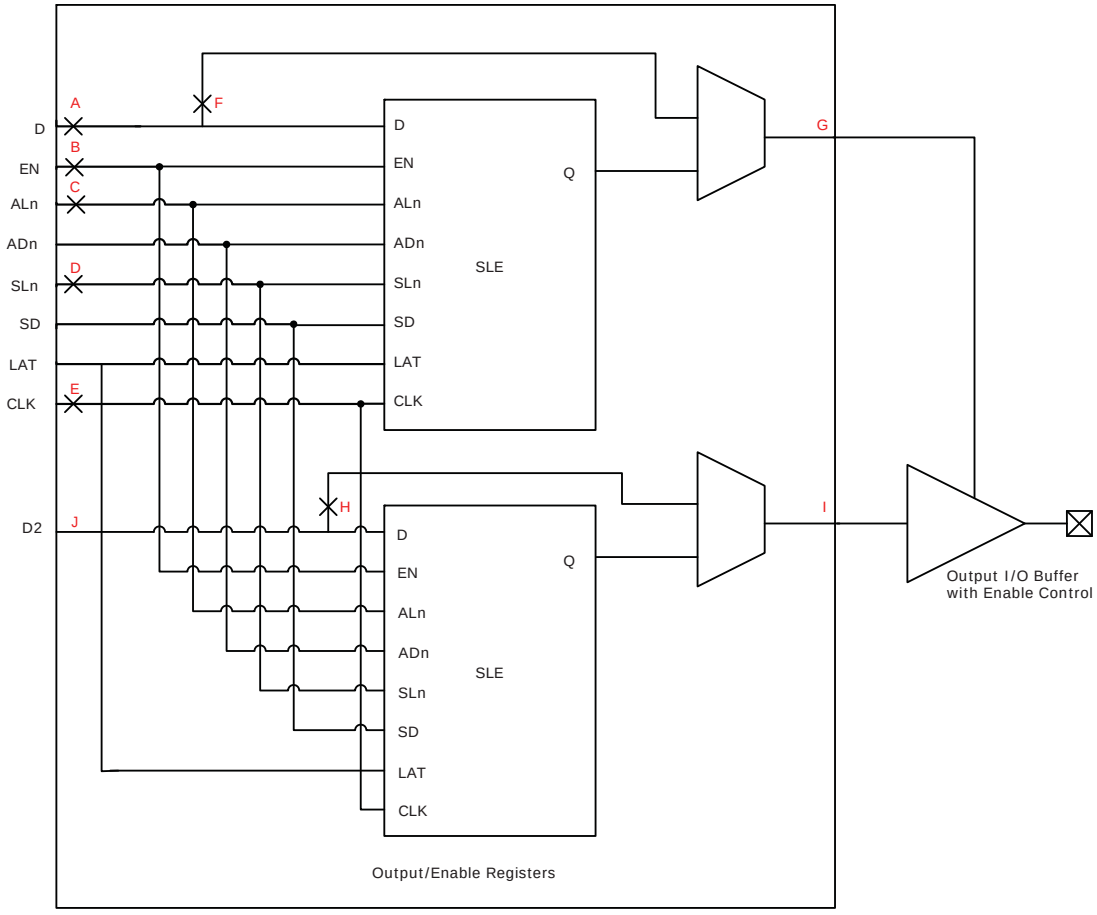
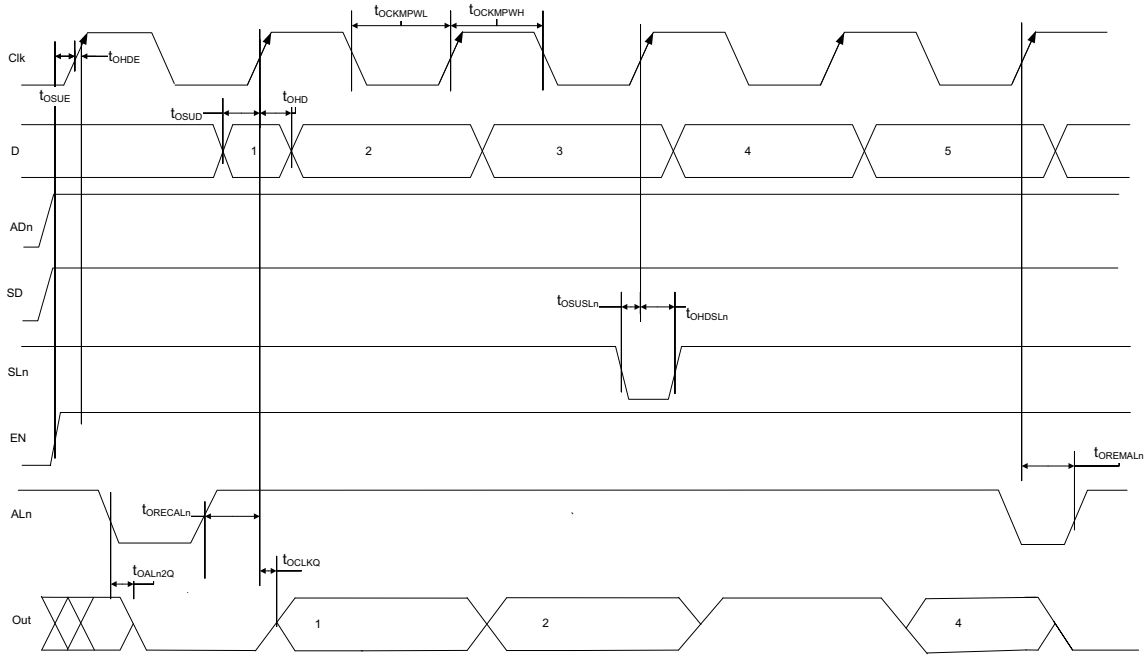


***Figure 9 •*** **I/O Register Output Timing Diagram**




The following table lists the output/enable propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 220 •*** **Output/Enable Data Register Propagation Delays**

| Parameter | Symbol | Measuring Nodes (from, to)[1] | –1 | –Std | Unit |
|---|---|---|---|---|---|
| Bypass delay of the output/enable register | $T_{OBYP}$ | F, G or H, I | 0.353 | 0.415 | ns |
| Clock-to-Q of the output/enable register | $T_{OCLKQ}$ | E, G or E, I | 0.263 | 0.309 | ns |
| Data setup time for the output/enable register | $T_{OSUD}$ | A, E or J, E | 0.19 | 0.223 | ns |
| Data hold time for the output/enable register | $T_{OHD}$ | A, E or J, E | 0 | 0 | ns |
| Enable setup time for the output/enable register | $T_{OSUE}$ | B, E | 0.419 | 0.493 | ns |
| Enable hold time for the output/enable register | $T_{OHE}$ | B, E | 0 | 0 | ns |
| Synchronous load setup time for the output/enable register | $T_{OSUSL}$ | D, E | 0.196 | 0.231 | ns |
| Synchronous load hold time for the output/enable register | $T_{OHSL}$ | D, E | 0 | 0 | ns |
| Asynchronous clear-to-q of the output/enable register (ADn = 1) | $T_{OALN2Q}$ | C, G or C, I | 0.505 | 0.594 | ns |
| Asynchronous preset-to-q of the output/enable register (ADn = 0) | | C, G or C, I | 0.528 | 0.621 | ns |
| Asynchronous load removal time for the output/enable register | $T_{OREMALN}$ | C, E | 0 | 0 | ns |
| Asynchronous load recovery time for the output/enable register | $T_{ORECALN}$ | C, E | 0.034 | 0.04 | ns |
| Asynchronous load minimum pulse width for the output/enable register | $T_{OWALN}$ | C, C | 0.304 | 0.357 | ns |
| Clock minimum pulse width high for the output/enable register | $T_{OCKMPWH}$ | E, E | 0.075 | 0.088 | ns |
| Clock minimum pulse width low for the output/enable register | $T_{OCKMPWL}$ | E, E | 0.159 | 0.187 | ns |

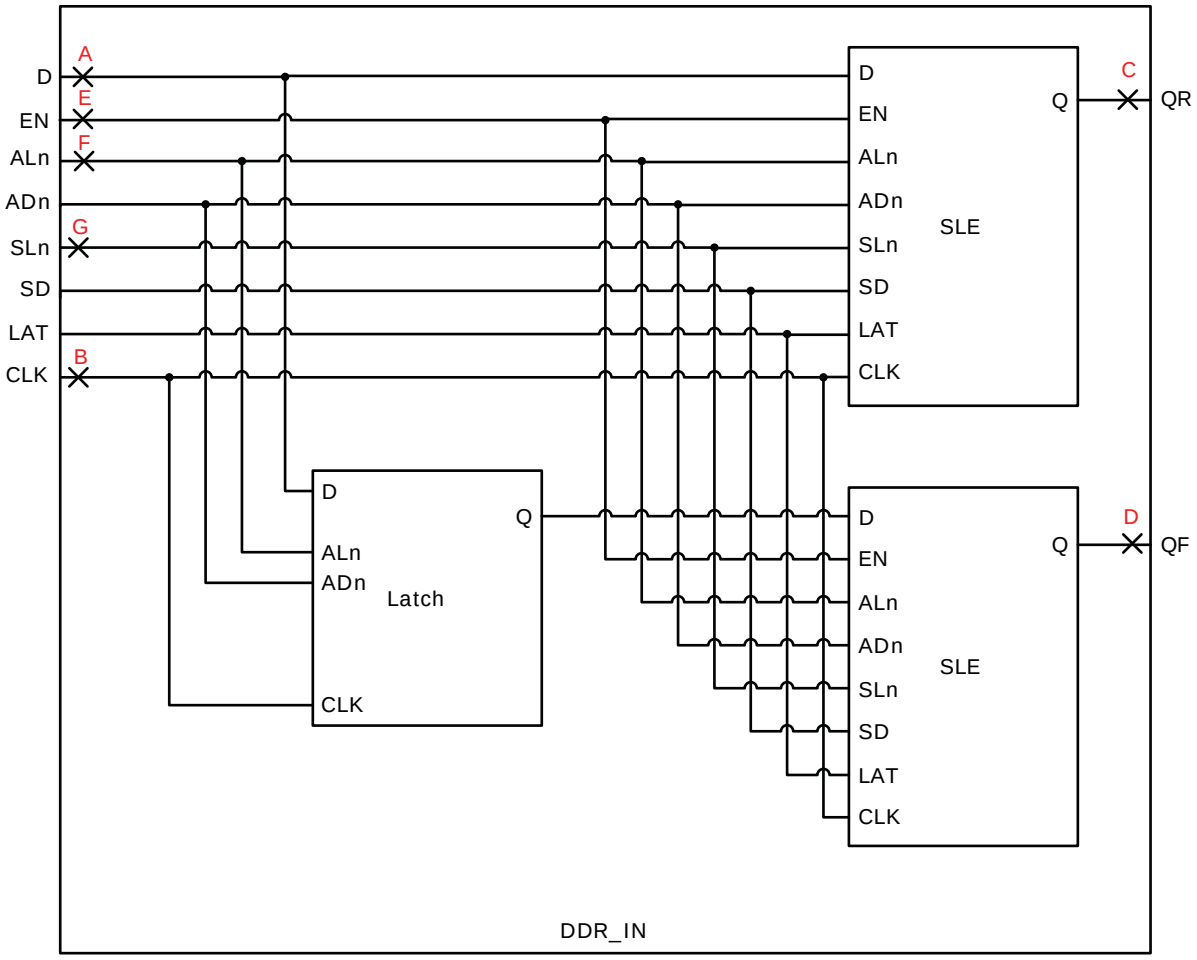
1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

## 2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

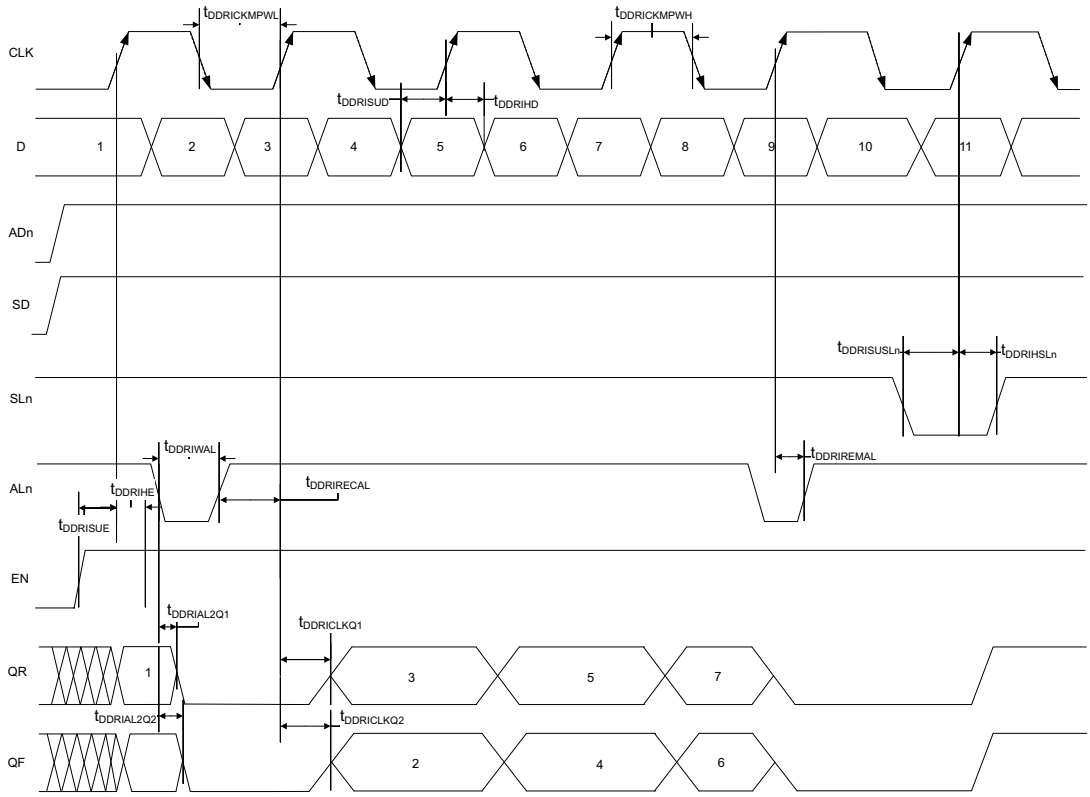
### 2.3.9.1 Input DDR Module

***Figure 10 •*** **Input DDR Module**



### 2.3.9.2 Input DDR Timing Diagram

***Figure 11 •*** **Input DDR Timing Diagram**




### 2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 221 •*** **Input DDR Propagation Delays**

| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDRICLKQ1}$ | Clock-to-Out Out_QR for input DDR | B, C | 0.16 | 0.188 | ns |
| $T_{DDRICLKQ2}$ | Clock-to-Out Out_QF for input DDR | B, D | 0.166 | 0.195 | ns |
| $T_{DDRISUD}$ | Data setup for input DDR | A, B | 0.357 | 0.421 | ns |
| $T_{DDRIHD}$ | Data hold for input DDR | A, B | 0 | 0 | ns |
| $T_{DDRISUE}$ | Enable setup for input DDR | E, B | 0.46 | 0.542 | ns |
| $T_{DDRIHE}$ | Enable hold for input DDR | E, B | 0 | 0 | ns |
| $T_{DDRISUSLN}$ | Synchronous load setup for input DDR | G, B | 0.46 | 0.542 | ns |
| $T_{DDRIHSLN}$ | Synchronous load hold for input DDR | G, B | 0 | 0 | ns |
| $T_{DDRIAL2Q1}$ | Asynchronous load-to-out QR for input DDR | F, C | 0.587 | 0.69 | ns |
| $T_{DDRIAL2Q2}$ | Asynchronous load-to-out QF for input DDR | F, D | 0.541 | 0.636 | ns |
| $T_{DDRIREMAL}$ | Asynchronous load removal time for input DDR | F, B | 0 | 0 | ns |
| $T_{DDRIRECAL}$ | Asynchronous load recovery time for input DDR | F, B | 0.074 | 0.087 | ns |

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***Table 221 •*** **Input DDR Propagation Delays *(continued)***

| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDRIWAL}$ | Asynchronous load minimum pulse width for input DDR | F, F | 0.304 | 0.357 | ns |
| $T_{DDRICKMPWH}$ | Clock minimum pulse width high for input DDR | B, B | 0.075 | 0.088 | ns |
| $T_{DDRICKMPWL}$ | Clock minimum pulse width low for input DDR | B, B | 0.159 | 0.187 | ns |

### 2.3.9.4 Output DDR Module

***Figure 12 •*** **Output DDR Module**

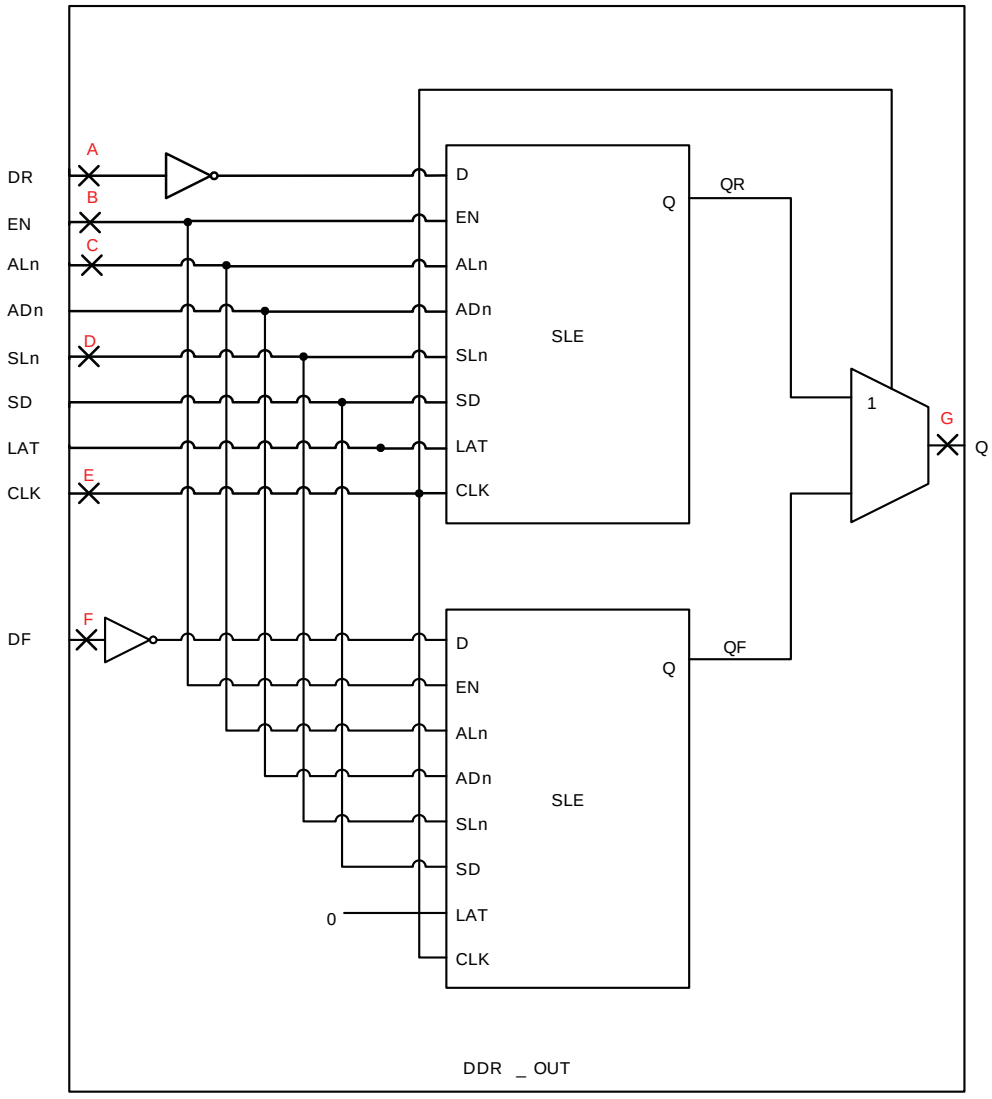
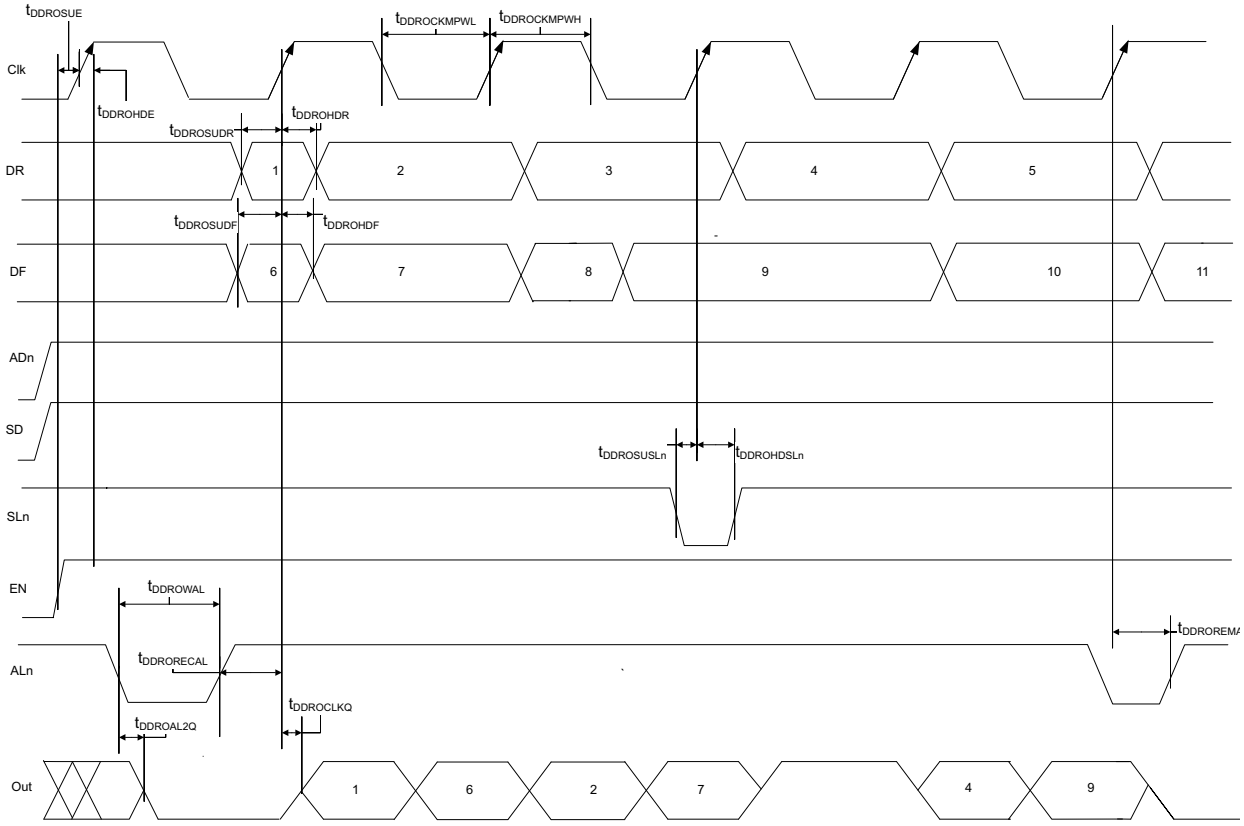


***Figure 13 •*** **Output DDR Timing Diagram**




### 2.3.9.5 Timing Characteristics

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 222 •*** **Output DDR Propagation Delays**

| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDROCLKQ}$ | Clock-to-out of DDR for output DDR | E, G | 0.263 | 0.309 | ns |
| $T_{DDROSUDF}$ | Data_F data setup for output DDR | F, E | 0.143 | 0.168 | ns |
| $T_{DDROSUDR}$ | Data_R data setup for output DDR | A, E | 0.19 | 0.223 | ns |
| $T_{DDROHDF}$ | Data_F data hold for output DDR | F, E | 0 | 0 | ns |
| $T_{DDROHDR}$ | Data_R data hold for output DDR | A, E | 0 | 0 | ns |
| $T_{DDROSUE}$ | Enable setup for input DDR | B, E | 0.419 | 0.493 | ns |
| $T_{DDROHE}$ | Enable hold for input DDR | B, E | 0 | 0 | ns |
| $T_{DDROSUSLN}$ | Synchronous load setup for input DDR | D, E | 0.196 | 0.231 | ns |
| $T_{DDROHSLN}$ | Synchronous load hold for input DDR | D, E | 0 | 0 | ns |
| $T_{DDROAL2Q}$ | Asynchronous load-to-out for output DDR | C, G | 0.528 | 0.621 | ns |
| $T_{DDROREMAL}$ | Asynchronous load removal time for output DDR | C, E | 0 | 0 | ns |
| $T_{DDRORECAL}$ | Asynchronous load recovery time for output DDR | C, E | 0.034 | 0.04 | ns |

***Table 222 •*** **Output DDR Propagation Delays *(continued)***

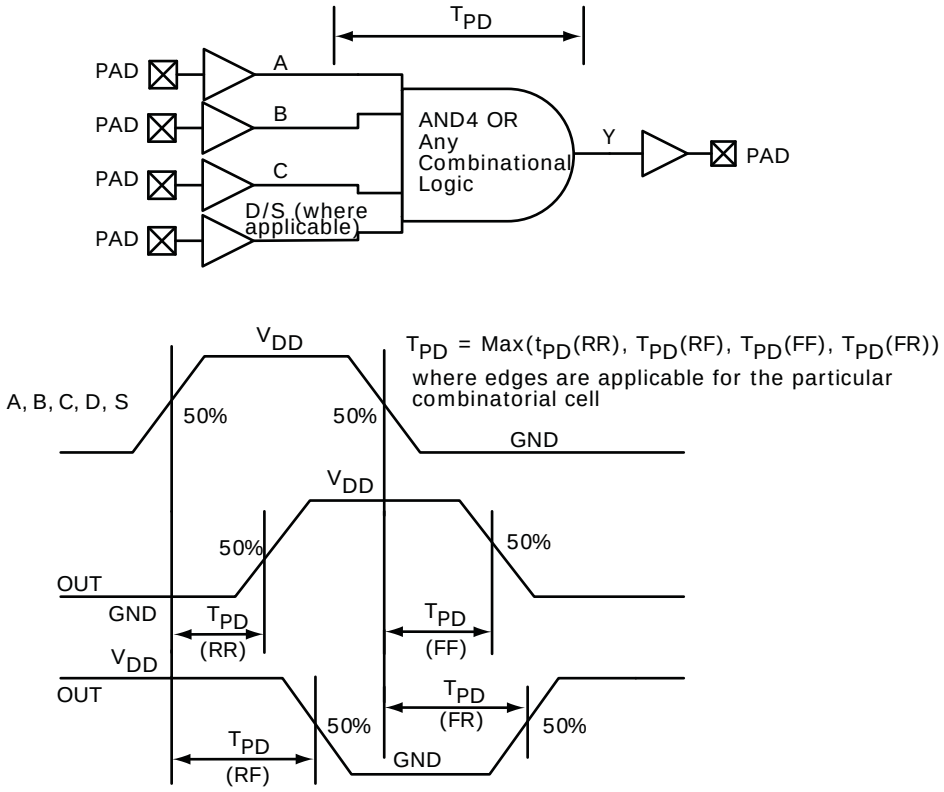
| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDROWAL}$ | Asynchronous load minimum pulse width for output DDR | C, C | 0.304 | 0.357 | ns |
| $T_{DDROCKMPWH}$ | Clock minimum pulse width high for the output DDR | E, E | 0.075 | 0.088 | ns |
| $T_{DDROCKMPWL}$ | Clock minimum pulse width low for the output DDR | E, E | 0.159 | 0.187 | ns |

## 2.3.10 Logic Element Specifications

### 2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see *SmartFusion2 and IGLOO2 Macro Library Guide*.

***Figure 14 •*** **LUT-4**



### 2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

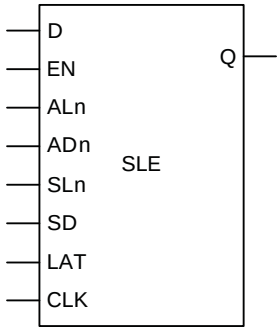
***Table 223 •*** **Combinatorial Cell Propagation Delays**

| Combinatorial Cell | Equation | Symbol | –1 | –Std | Unit |
|---|---|---|---|---|---|
| INV | Y = !A | $T_{PD}$ | 0.1 | 0.118 | ns |
| AND2 | Y = A · B | $T_{PD}$ | 0.164 | 0.193 | ns |
| NAND2 | Y = !(A · B) | $T_{PD}$ | 0.147 | 0.173 | ns |
| OR2 | Y = A + B | $T_{PD}$ | 0.164 | 0.193 | ns |
| NOR2 | Y = !(A + B) | $T_{PD}$ | 0.147 | 0.173 | ns |
| XOR2 | Y = A ⊕ B | $T_{PD}$ | 0.164 | 0.193 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $T_{PD}$ | 0.225 | 0.265 | ns |
| AND3 | Y = A · B · C | $T_{PD}$ | 0.209 | 0.246 | ns |
| AND4 | Y = A · B · C · D | $T_{PD}$ | 0.287 | 0.338 | ns |

### 2.3.10.3 Sequential Module

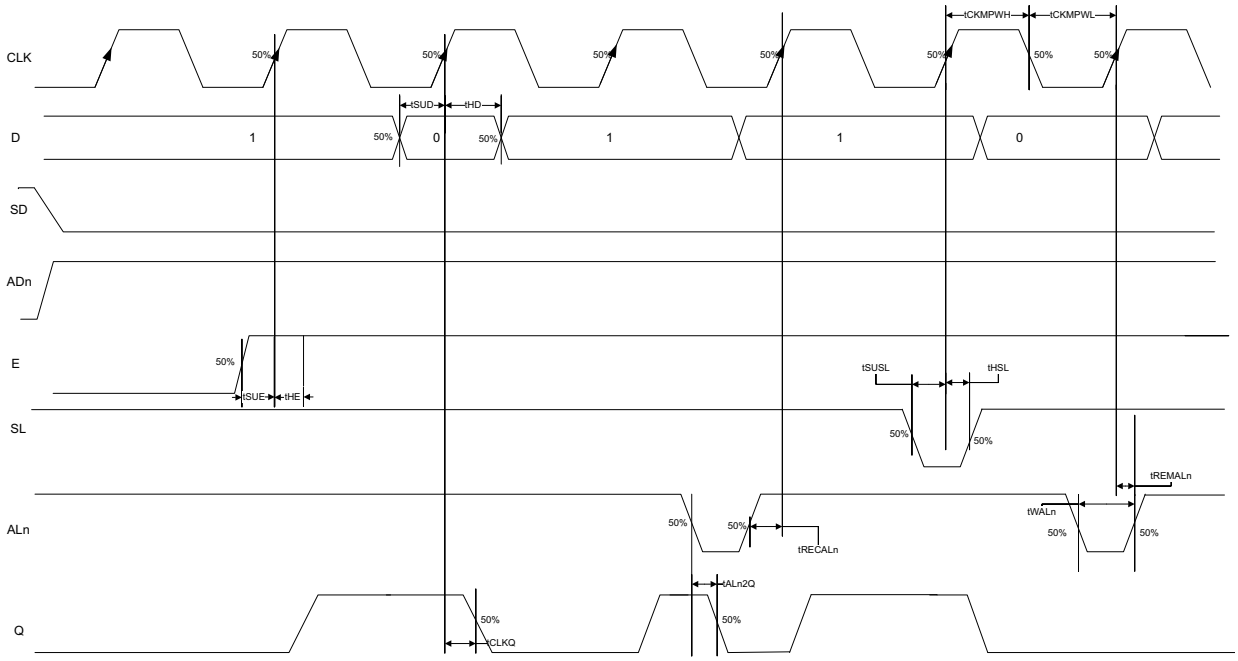
IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

***Figure 15 •*** **Sequential Module**



The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

***Figure 16 •*** **Sequential Module Timing Diagram**




## 2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 224 •*** **Register Delays**

| Parameter | Symbol | –1 | –Std | Unit |
|---|---|---|---|---|
| Clock-to-Q of the core register | $T_{CLKQ}$ | 0.108 | 0.127 | ns |
| Data setup time for the core register | $T_{SUD}$ | 0.254 | 0.298 | ns |
| Data hold time for the core register | $T_{HD}$ | 0 | 0 | ns |
| Enable setup time for the core register | $T_{SUE}$ | 0.335 | 0.394 | ns |
| Enable hold time for the core register | $T_{HE}$ | 0 | 0 | ns |
| Synchronous load setup time for the core register | $T_{SUSL}$ | 0.335 | 0.394 | ns |
| Synchronous load hold time for the core register | $T_{HSL}$ | 0 | 0 | ns |
| Asynchronous Clear-to-Q of the core register (ADn = 1) | $T_{ALN2Q}$ | 0.473 | 0.556 | ns |
| Asynchronous preset-to-Q of the core register (ADn = 0) | | 0.451 | 0.531 | ns |
| Asynchronous load removal time for the core register | $T_{REMALN}$ | 0 | 0 | ns |
| Asynchronous load recovery time for the core register | $T_{RECALN}$ | 0.353 | 0.415 | ns |
| Asynchronous load minimum pulse width for the core register | $T_{WALN}$ | 0.266 | 0.313 | ns |
| Clock minimum pulse width high for the core register | $T_{CKMPWH}$ | 0.065 | 0.077 | ns |
| Clock minimum pulse width low for the core register | $T_{CKMPWL}$ | 0.139 | 0.164 | ns |

## 2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 225 •*** **150 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.83 | 0.911 | 0.831 | 0.913 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.457 | 1.588 | 1.715 | 1.869 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.131 | | 0.154 | ns |

The following table lists the 090 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 226 •*** **090 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.835 | 0.888 | 0.833 | 0.886 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.405 | 1.489 | 1.654 | 1.752 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.084 | | 0.098 | ns |

The following table lists the 050 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 227 •*** **050 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.827 | 0.897 | 0.826 | 0.896 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.419 | 1.53 | 1.671 | 1.8 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.111 | | 0.129 | ns |

The following table lists the 025 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 228 •*** **025 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.747 | 0.799 | 0.745 | 0.797 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.294 | 1.378 | 1.522 | 1.621 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.084 | | 0.099 | ns |

The following table lists the 010 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 229 •*** **010 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.626 | 0.669 | 0.627 | 0.668 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.112 | 1.182 | 1.308 | 1.393 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.07 | | 0.085 | ns |

The following table lists the 005 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 230 •*** **005 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.625 | 0.66 | 0.628 | 0.66 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.126 | 1.187 | 1.325 | 1.397 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.061 | | 0.072 | ns |

## 2.3.12 FPGA Fabric SRAM

See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

### 2.3.12.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 1K × 18 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 231 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.273 | | 2.674 | ns |
| Access time with feed-through write timing | | | 1.529 | | 1.799 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.441 | | 0.519 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.341 | | 0.401 | | ns |
| Data hold time | $T_{DHD}$ | 0.107 | | 0.126 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |

***Table 231 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18 *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.449 | | 0.528 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.167 | | 0.197 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | – | 1.506 | – | 1.772 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.39 | | 0.458 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.242 | | 0.285 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 2K × 9 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 232 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.273 | | 2.674 | ns |
| Access time with feed-through write timing | | | 1.529 | | 1.799 | ns |

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***Table 232 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Address setup time | $T_{ADDRSU}$ | 0.475 | | 0.559 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.336 | | 0.395 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.485 | | 0.57 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.514 | | 1.781 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.415 | | 0.488 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 233 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |

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***Table 233 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4 *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.323 | | 0.38 | ns |
| Read access time without pipeline register | | | 2.273 | | 2.673 | ns |
| Access time with feed-through write timing | | | 1.511 | | 1.778 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.543 | | 0.638 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.334 | | 0.393 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.511 | | 1.778 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.516 | | 0.607 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.507 | | 1.773 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.458 | | 0.539 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 8K × 2 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 234 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.32 | | 0.377 | ns |
| Read access time without pipeline register | | | 2.272 | | 2.673 | ns |
| Access time with feed-through write timing | | | 1.511 | | 1.778 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.612 | | 0.72 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.33 | | 0.388 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.511 | | 1.778 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.529 | | 0.622 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.528 | | 1.797 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.488 | | 0.574 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 16K × 1 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 235 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.32 | | 0.377 | ns |
| Read access time without pipeline register | | | 2.269 | | 2.669 | ns |
| Access time with feed-through write timing | | | 1.51 | | 1.777 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.626 | | 0.737 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.322 | | 0.378 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.51 | | 1.777 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.53 | | 0.624 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.547 | | 1.82 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.454 | | 0.534 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

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The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 236 •*** **RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.25 | | 2.647 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.313 | | 0.368 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.337 | | 0.396 | | ns |
| Data hold time | $T_{DHD}$ | 0.111 | | 0.13 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.201 | | 0.237 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.25 | | 2.647 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.449 | | 0.528 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.167 | | 0.197 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.506 | | 1.772 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.39 | | 0.458 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.242 | | 0.285 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

### 2.3.12.2 FPGA Fabric Micro SRAM (µSRAM)

The following table lists the µSRAM in 64 × 18 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 237 •*** **µSRAM (RAM64x18) in 64 × 18 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | –0.778 | | –0.915 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.036 | | 2.396 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.023 | | –0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.839 | | 0.987 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |

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***Table 237 •*** **µSRAM (RAM64x18) in 64 × 18 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.026 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 64 × 16 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 238 •*** **µSRAM (RAM64x16) in 64 × 16 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | –0.778 | | –0.915 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.036 | | 2.396 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.023 | | –0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.835 | | 0.983 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |

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***Table 238 •*** **µSRAM (RAM64x16) in 64 × 16 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.026 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 128 × 9 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 239 •*** **µSRAM (RAM128x9) in 128 × 9 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | –0.778 | | –0.915 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.036 | | 2.396 | ns |

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***Table 239 •*** **µSRAM (RAM128x9) in 128 × 9 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.023 | | –0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.835 | | 0.982 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.026 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 128 × 8 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 240 •*** **µSRAM (RAM128x8) in 128 × 8 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |

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***Table 240 •*** **µSRAM (RAM128x8) in 128 × 8 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | –0.778 | | –0.915 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.036 | | 2.396 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.023 | | –0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.835 | | 0.982 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.026 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 256 × 4 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 241 •*** **µSRAM (RAM256x4) in 256 × 4 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | 1.75 | | 2.06 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.931 | | 2.272 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.121 | | 0.142 | | ns |
| Read address hold time in asynchronous mode | | –0.65 | | –0.76 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.09 | | 2.46 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.02 | | –0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.101 | | 0.118 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |

***Table 241 •*** **µSRAM (RAM256x4) in 256 × 4 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Write address hold time | $T_{ADDRCHD}$ | 0.245 | | 0.288 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.03 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 512 × 2 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 242 •*** **µSRAM (RAM512x2) in 512 × 2 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | 1.76 | | 2.08 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.96 | | 2.306 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.137 | | 0.161 | | ns |
| Read address hold time in asynchronous mode | | –0.58 | | –0.68 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.14 | | 2.52 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.02 | | –0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |

***Table 242 •*** **µSRAM (RAM512x2) in 512 × 2 Mode *(continued)***

| Parameter | Symbol | –1 | | –Std | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.101 | | 0.118 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.247 | | 0.29 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.03 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 1024 × 1 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 243 •*** **µSRAM (RAM1024x1) in 1024 × 1 Mode**

| Parameter | Symbol | –1 | | –Std | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | 1.78 | | 2.1 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.978 | | 2.327 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.137 | | 0.161 | | ns |
| Read address hold time in asynchronous mode | | –0.6 | | –0.71 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.16 | | 2.54 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.02 | | –0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |

***Table 243 •*** **µSRAM (RAM1024x1) in 1024 × 1 Mode *(continued)***

| Parameter | Symbol | –1 | | –Std | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.003 | | 0.004 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.247 | | 0.29 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.03 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

## 2.3.13 Programming Times

The following tables list the programming times in typical conditions when $T_J$ = 25 °C, $V_{DD}$ = 1.2 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

***Table 244 •*** **JTAG Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 302672 | 22 | 10 | Sec |
| 010 | 568784 | 28 | 18 | Sec |
| 025 | 1223504 | 51 | 26 | Sec |
| 050 | 2424832 | 66 | 54 | Sec |
| 060 | 2418896 | 77 | 54 | Sec |
| 090 | 3645968 | 113 | 126 | Sec |
| 150 | 6139184 | 155 | 193 | Sec |

***Table 245 •*** **JTAG Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 137536 | 39 | 4 | Sec |
| 010 | 274816 | 78 | 9 | Sec |
| 025 | 274816 | 78 | 9 | Sec |
| 050 | 278528 | 84 | 8 | Sec |
| 060 | 268480 | 76 | 8 | Sec |
| 090 | 544496 | 154 | 15 | Sec |
| 150 | 544496 | 155 | 15 | Sec |

***Table 246 •*** **JTAG Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 439296 | 59 | 11 | Sec |
| 010 | 842688 | 107 | 20 | Sec |
| 025 | 1497408 | 120 | 35 | Sec |
| 050 | 2695168 | 162 | 59 | Sec |
| 060 | 2686464 | 158 | 70 | Sec |
| 090 | 4190208 | 266 | 147 | Sec |
| 150 | 6682768 | 316 | 231 | Sec |

***Table 247 •*** **2 Step IAP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 4 | 17 | 6 | Sec |
| 010 | 568784 | 7 | 23 | 12 | Sec |
| 025 | 1223504 | 14 | 33 | 23 | Sec |
| 050 | 2424832 | 29 | 52 | 40 | Sec |
| 060 | 2418896 | 39 | 61 | 50 | Sec |
| 090 | 3645968 | 60 | 84 | 73 | Sec |
| 150 | 6139184 | 100 | 132 | 120 | Sec |

***Table 248 •*** **2 Step IAP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 2 | 37 | 5 | Sec |
| 010 | 274816 | 4 | 76 | 11 | Sec |
| 025 | 274816 | 4 | 78 | 10 | Sec |
| 050 | 278528 | 3 | 85 | 9 | Sec |
| 060 | 268480 | 5 | 76 | 22 | Sec |
| 090 | 544496 | 10 | 152 | 43 | Sec |
| 150 | 544496 | 10 | 153 | 44 | Sec |

***Table 249 •*** **2 Step IAP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 6 | 56 | 11 | Sec |
| 010 | 842688 | 11 | 100 | 21 | Sec |
| 025 | 1497408 | 19 | 113 | 32 | Sec |
| 050 | 2695168 | 32 | 136 | 48 | Sec |
| 060 | 2686464 | 43 | 137 | 70 | Sec |
| 090 | 4190208 | 68 | 236 | 115 | Sec |
| 150 | 6682768 | 109 | 286 | 162 | Sec |

***Table 250 •*** **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 6 | 19 | 8 | Sec |
| 010 | 568784 | 10 | 26 | 14 | Sec |
| 025 | 1223504 | 21 | 39 | 29 | Sec |
| 050 | 2424832 | 39 | 60 | 50 | Sec |
| 060 | 2418896 | 44 | 65 | 54 | Sec |
| 090 | 3645968 | 66 | 90 | 79 | Sec |
| 150 | 6139184 | 108 | 140 | 128 | Sec |

***Table 251 •*** **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 3 | 42 | 4 | Sec |
| 010 | 274816 | 4 | 82 | 7 | Sec |
| 025 | 274816 | 4 | 82 | 8 | Sec |
| 050 | 278528 | 4 | 80 | 8 | Sec |
| 060 | 268480 | 6 | 80 | 8 | Sec |
| 090 | 544496 | 10 | 157 | 15 | Sec |

***Table 251 •*** **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) *(continued)***

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 150 | 544496 | 10 | 158 | 15 | Sec |

***Table 252 •*** **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 9 | 61 | 11 | Sec |
| 010 | 842688 | 15 | 107 | 21 | Sec |
| 025 | 1497408 | 26 | 121 | 35 | Sec |
| 050 | 2695168 | 43 | 141 | 55 | Sec |
| 060 | 2686464 | 48 | 143 | 60 | Sec |
| 090 | 4190208 | 75 | 244 | 91 | Sec |
| 150 | 6682768 | 117 | 296 | 141 | Sec |

***Table 253 •*** **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

| M2S/M2GL Device | Auto Programming | Auto Update | Programming Recovery | Unit |
|---|---|---|---|---|
| | 100 kHz | 25 MHz | 12.5 MHz | |
| 005 | 47 | 27 | 28 | Sec |
| 010 | 77 | 35 | 35 | Sec |
| 025 | 150 | 42 | 41 | Sec |
| 050 | 33[1] | Not Supported | Not Supported | Sec |
| 060 | 291 | 83 | 82 | Sec |
| 090 | 427 | 109 | 108 | Sec |
| 150 | 708 | 157 | 160 | Sec |

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

***Table 254 •*** **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

| M2S/M2GL Device | Auto Programming | Auto Update | Programming Recovery | Unit |
|---|---|---|---|---|
| | 100 kHz | 25 MHz | 12.5 MHz | |
| 005 | 41 | 48 | 49 | Sec |
| 010 | 86 | 87 | 87 | Sec |
| 025 | 87 | 85 | 86 | Sec |
| 050 | 85 | Not Supported | Not Supported | Sec |
| 060 | 78 | 86 | 86 | Sec |
| 090 | 154 | 162 | 162 | Sec |

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**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only) (continued)**

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 150 | 161 | 161 | 161 | Sec |

**Table 255 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 005 | 47 | 27 | 28 | Sec |
| 010 | 77 | 35 | 35 | Sec |
| 025 | 150 | 42 | 41 | Sec |
| 050 | 33[1] | Not Supported | Not Supported | Sec |
| 060 | 291 | 83 | 82 | Sec |
| 090 | 427 | 109 | 108 | Sec |
| 150 | 708 | 157 | 160 | Sec |
| 005 | 41 | 48 | 49 | Sec |
| 010 | 86 | 87 | 87 | Sec |
| 025 | 87 | 85 | 86 | Sec |
| 050 | 85 | Not Supported | Not Supported | Sec |
| 060 | 78 | 86 | 86 | Sec |
| 090 | 154 | 162 | 162 | Sec |
| 150 | 161 | 161 | 161 | Sec |
| 005 | 87 | 67 | 66 | Sec |
| 010 | 161 | 113 | 113 | Sec |
| 025 | 229 | 120 | 121 | Sec |
| 050 | 112 | Not Supported | Not Supported | Sec |
| 060 | 368 | 161 | 158 | Sec |
| 090 | 582 | 261 | 260 | Sec |
| 150 | 867 | 309 | 310 | Sec |

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

The following table lists the programming times in worst-case conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

***Table 256 •*** **JTAG Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 302672 | 44 | 10 | Sec |
| 010 | 568784 | 50 | 18 | Sec |
| 025 | 1223504 | 73 | 26 | Sec |
| 050 | 2424832 | 88 | 54 | Sec |
| 060 | 2418896 | 99 | 54 | Sec |
| 090 | 3645968 | 135 | 126 | Sec |
| 150 | 6139184 | 177 | 193 | Sec |

***Table 257 •*** **JTAG Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 137536 | 61 | 4 | Sec |
| 010 | 274816 | 100 | 9 | Sec |
| 025 | 274816 | 100 | 9 | Sec |
| 050 | 2,78,528 | 106 | 8 | Sec |
| 060 | 268480 | 98 | 8 | Sec |
| 090 | 544496 | 176 | 15 | Sec |
| 150 | 544496 | 177 | 15 | Sec |

***Table 258 •*** **JTAG Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 439296 | 71 | 11 | Sec |
| 010 | 842688 | 129 | 20 | Sec |
| 025 | 1497408 | 142 | 35 | Sec |
| 050 | 2695168 | 184 | 59 | Sec |
| 060 | 2686464 | 180 | 70 | Sec |
| 090 | 4190208 | 288 | 147 | Sec |
| 150 | 6682768 | 338 | 231 | Sec |

***Table 259 •*** **2 Step IAP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 4 | 39 | 6 | Sec |
| 010 | 568784 | 7 | 45 | 12 | Sec |
| 025 | 1223504 | 14 | 55 | 23 | Sec |
| 050 | 2424832 | 29 | 74 | 40 | Sec |
| 060 | 2418896 | 39 | 83 | 50 | Sec |
| 090 | 3645968 | 60 | 106 | 73 | Sec |
| 150 | 6139184 | 100 | 154 | 120 | Sec |

***Table 260 •*** **2 Step IAP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 2 | 59 | 5 | Sec |
| 010 | 274816 | 4 | 98 | 11 | Sec |
| 025 | 274816 | 4 | 100 | 10 | Sec |
| 050 | 2,78,528 | 3 | 107 | 9 | Sec |
| 060 | 268480 | 5 | 98 | 22 | Sec |
| 090 | 544496 | 10 | 174 | 43 | Sec |
| 150 | 544496 | 10 | 175 | 44 | Sec |

***Table 261 •*** **2 Step IAP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 6 | 78 | 11 | Sec |
| 010 | 842688 | 11 | 122 | 21 | Sec |
| 025 | 1497408 | 19 | 135 | 32 | Sec |
| 050 | 2695168 | 32 | 158 | 48 | Sec |
| 060 | 2686464 | 43 | 159 | 70 | Sec |
| 090 | 4190208 | 68 | 258 | 115 | Sec |
| 150 | 6682768 | 109 | 308 | 162 | Sec |

***Table 262 •*** **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 6 | 41 | 8 | Sec |
| 010 | 568784 | 10 | 48 | 14 | Sec |
| 025 | 1223504 | 21 | 61 | 29 | Sec |
| 050 | 2424832 | 39 | 82 | 50 | Sec |
| 060 | 2418896 | 44 | 87 | 54 | Sec |
| 090 | 3645968 | 66 | 112 | 79 | Sec |
| 150 | 6139184 | 108 | 162 | 128 | Sec |

***Table 263 •*** **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 3 | 64 | 4 | Sec |
| 010 | 274816 | 4 | 104 | 7 | Sec |
| 025 | 274816 | 4 | 104 | 8 | Sec |
| 050 | 2,78,528 | 4 | 102 | 8 | Sec |
| 060 | 268480 | 6 | 102 | 8 | Sec |
| 090 | 544496 | 10 | 179 | 15 | Sec |
| 150 | 544496 | 10 | 180 | 15 | Sec |

***Table 264 •*** **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 9 | 83 | 11 | Sec |
| 010 | 842688 | 15 | 129 | 21 | Sec |
| 025 | 1497408 | 26 | 143 | 35 | Sec |
| 050 | 2695168 | 43 | 163 | 55 | Sec |
| 060 | 2686464 | 48 | 165 | 60 | Sec |
| 090 | 4190208 | 75 | 266 | 91 | Sec |
| 150 | 6682768 | 117 | 318 | 141 | Sec |

***Table 265 •*** **Programming Times with 100 kHz, 25 MHz. and 12.5 MHz SPI Clock Rates (Fabric Only)**

| | Auto Programming | Auto Update | Programming Recovery | |
|---|---|---|---|---|
| **M2S/M2GL Device** | **100 kHz** | **25 MHz** | **12.5 MHz** | **Unit** |
| 005 | 69 | 49 | 50 | Sec |
| 010 | 99 | 57 | 57 | Sec |
| 025 | 150 | 64 | 63 | Sec |
| 050 | 55[1] | Not Supported | Not Supported | Sec |
| 060 | 313 | 105 | 104 | Sec |
| 090 | 449 | 131 | 130 | Sec |
| 150 | 730 | 179 | 183 | Sec |

1. Auto programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

***Table 266 •*** **Programming Times with 100 kHz, 25 MHz. and 12.5 MHz SPI Clock Rates (eNVM Only)**

| | Auto Programming | Auto Update | Programming Recovery | |
|---|---|---|---|---|
| **M2S/M2GL Device** | **100 kHz** | **25 MHz** | **12.5 MHz** | **Unit** |
| 005 | 63 | 70 | 71 | Sec |
| 010 | 108 | 109 | 109 | Sec |
| 025 | 109 | 107 | 108 | Sec |
| 050 | 107 | Not Supported | Not Supported | Sec |
| 060 | 100 | 108 | 108 | Sec |
| 090 | 176 | 184 | 184 | Sec |
| 150 | 183 | 183 | 183 | Sec |

***Table 267 •*** **Programming Times with 100 kHz, 25 MHz. and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

| | Auto Programming | Auto Update | Programming Recovery | |
|---|---|---|---|---|
| **M2S/M2GL Device** | **100 kHz** | **25 MHz** | **12.5 MHz** | **Unit** |
| 005 | 109 | 89 | 88 | Sec |
| 010 | 183 | 135 | 135 | Sec |
| 025 | 251 | 142 | 143 | Sec |
| 050 | 134 | Not Supported | Not Supported | Sec |
| 060 | 390 | 183 | 180 | Sec |
| 090 | 604 | 283 | 282 | Sec |
| 150 | 889 | 331 | 332 | Sec |

## 2.3.14 Math Block Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC math block supports 18×18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 268 •*** **Math Blocks with all Registers Used**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input, control register setup time | $T_{MISU}$ | 0.149 | | 0.176 | | ns |
| Input, control register hold time | $T_{MIHD}$ | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.185 | | 0.218 | | ns |
| CDIN input hold time | $T_{MOCDINHD}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 | | –0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Output register clock to out delay | $T_{MOCQ}$ | | 0.232 | | 0.273 | ns |
| CLK minimum period | $T_{MCLKMP}$ | 2.245 | | 2.641 | | ns |

The following table lists the math blocks with input bypassed and output registers used in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 269 •*** **Math Block with Input Bypassed and Output Registers Used**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Output register setup time | $T_{MOSU}$ | 2.294 | | 2.699 | | ns |
| Output register hold time | $T_{MOHD}$ | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.115 | | 0.136 | | ns |
| CDIN input hold time | $T_{MOCDINHD}$ | –0.444 | | –0.522 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 | | –0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.014 | | 0.017 | | ns |
| Output register clock to out delay | $T_{MOCQ}$ | | 0.232 | | 0.273 | ns |
| CLK minimum period | $T_{MCLKMP}$ | 2.179 | | 2.563 | | ns |

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 270 •*** **Math Block with Input Register Used and Output in Bypass Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input register setup time | $T_{MISU}$ | 0.149 | | 0.176 | | ns |
| Input register hold time | $T_{MIHD}$ | 0.185 | | 0.218 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | –0.012 | | –0.014 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | –0.005 | | –0.005 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Input register clock to output delay | $T_{MICQ}$ | | 2.52 | | 2.964 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | | 1.951 | | 2.295 | ns |

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 271 •*** **Math Block with Input and Output in Bypass Mode**

| | | –1 | –Std | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Max** | **Max** | **Unit** |
| Input to output delay | $T_{MIQ}$ | 2.568 | 3.022 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | 1.951 | 2.295 | ns |

## 2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD}$ = 1.14 V, $V_{PPNVM}$ = $V_{PP}$ = 2.375 V.

***Table 272 •*** **eNVM Read Performance**

| | | Operating Temperature Range | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Description** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| $T_J$ | Junction temperature range | –55 °C to 125 °C | | –40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $F_{MAXREAD}$ | eNVM maximum read frequency | 25 | 25 | 25 | 25 | 25 | 25 | MHz |

The following table lists the eNVM page programming in worst-case conditions when $V_{DD}$ = 1.14 V, $V_{PPNVM}$ = $V_{PP}$ = 2.375 V.

***Table 273 •*** **eNVM Page Programming**

| | | Operating Temperature Range | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Description** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| $T_J$ | Junction temperature range | –55 °C to 125 °C | | –40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $T_{PAGEPGM}$ | eNVM page programming time | 40 | 40 | 40 | 40 | 40 | 40 | ms |

## 2.3.16 SRAM PUF

For more details on static random-access memory (SRAM) physical unclonable functions (PUF) services, see *AC434: Using SRAM PUF System Service in SmartFusion2 Application Note*.

The following table lists the SRAM PUF in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 274 •*** **SRAM PUF**

| | PUF Off | | PUF On | | |
|---|---|---|---|---|---|
| **Service** | **Typ** | **Max** | **Typ** | **Max** | **Unit** |
| Create activation code | 709.1 | 746.4 | 754.4 | 762.5 | ms |
| Delete activation code | 1329.3 | 1399.3 | 1414.1 | 1429.3 | ms |
| Create intrinsic keycode | 656.6 | 691.1 | 698.5 | 706.0 | ms |
| Create extrinsic keycode | 656.6 | 691.1 | 698.5 | 706.0 | ms |
| Get number of keys | 1.3 | 1.4 | 1.4 | 1.4 | ms |
| Export (Kc0, Kc1) | 998.0 | 1050.5 | 1061.7 | 1073.1 | ms |
| Export 2 keycodes | 2020.2 | 2126.5 | 2149.2 | 2172.3 | ms |
| Export 4 keycodes | 3065.7 | 3227.0 | 3261.3 | 3296.4 | ms |
| Export 8 keycodes | 5101.0 | 5369.5 | 5426.6 | 5485.0 | ms |
| Export 16 keycodes | 9212.1 | 9697.0 | 9800.1 | 9905.5 | ms |
| Import (Kc0, Kc1) | 39.7 | 41.8 | 42.2 | 42.7 | ms |
| Import 2 keycodes | 50.1 | 52.7 | 53.3 | 53.9 | ms |
| Import 4 keycodes | 60.6 | 63.8 | 64.5 | 65.2 | ms |
| Import 8 keycodes | 80.9 | 85.1 | 86.1 | 87.0 | ms |
| Import 16 keycodes | 123.8 | 130.4 | 131.7 | 133.2 | ms |
| Delete keycode | 552.5 | 581.6 | 587.8 | 594.1 | ms |
| Fetch key | 31.4 | 33.0 | 33.4 | 33.7 | ms |
| Fetch ecc key | 20.0 | 21.1 | 21.3 | 21.5 | ms |
| Get seed | 2.0 | 2.1 | 2.2 | 2.2 | ms |

## 2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see *AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note.* The following table lists the NRBG in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 275 •*** **Non-Deterministic Random Bit Generator (NRBG)**

| | | | Conditions | |
|---|---|---|---|---|
| **Service** | **Timing** | **Unit** | **Prediction Resistance** | **Additional Input** |
| Instantiate | 85 | ms | OFF | X |
| Generate (after Instantiate)[1] | 4.5 ms + (6.25 us/byte x No. of Bytes) | | OFF | 0 |
| | 6.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 64 |
| | 7.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 128 |
| Generate (after Instantiate) | 47 | ms | ON | X |
| Generate (subsequent)[1] | 0.5 ms + (6.25 us/byte x No. of Bytes) | | OFF | 0 |
| | 2.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 64 |
| | 3.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 128 |
| Generate (subsequent) | 43 | ms | ON | X |
| Reseed | 40 | ms | | |
| Uninstantiate | 0.16 | ms | | |
| Reset | 0.10 | ms | | |
| Self test | 20 | ms | First time after power-up | |
| | 6 | ms | Subsequent | |

1. If PUF_OFF, generate will incur additional PUF delay time for consecutive service calls.

## 2.3.18 Cryptographic Block Characteristics

For more information about cryptographic block and associated services, see *AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note* and *AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note*.

The following table lists the cryptographic block characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 276 •*** **Cryptographic Block Characteristics**

| **Service** | **Conditions** | **Timing** | **Unit** |
|---|---|---|---|
| Any service | First certificate check penalty at boot | 11.5 | ms |
| AES128/256 (encoding-/-decoding)[1] | 100 blocks up to 64k blocks | 700 | kbps |

***Table 276 •*** **Cryptographic Block Characteristics *(continued)***

| Service | Conditions | Timing | Unit |
|---|---|---|---|
| SHA256 | 512 bits | 540 | kbps |
| | 1024 bits | 780 | kbps |
| | 2048 bits | 950 | kbps |
| | 24 kbits | 1140 | kbps |
| HMAC | 512 bytes | 820 | kbps |
| | 1024 bytes | 890 | kbps |
| | 2048 bytes | 930 | kbps |
| | 24 kbytes | 980 | kbps |
| KeyTree | | 1.8 | ms |
| Challenge-response | PUF = OFF | 25 | ms |
| | PUF = ON | 7 | ms |
| ECC point multiplication | | 590 | ms |
| ECC point addition | | 8 | ms |

1. Using cypher block chaining (CBC) mode.

## 2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 20 | | MHz | |
| Accuracy | ACCXTAL | | | 0.0047 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.0058 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 200 | 300 | ps | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 200 | 300 | ps | 010, 025, 050, and 060 devices |
| | | | 250 | 410 | ps | 150 devices |
| | | | 250 | 550 | ps | 005 and 090 devices |
| Operating current | IDYNXTAL | | 1.5 | | mA | 010, 050, and 060 devices |
| | | | 1.65 | | mA | 005, 025, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)** ***(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 0.8 | ms | 005, 010, 025, and 050 devices |
| | | | | 1.0 | ms | 090 and 150 devices |

***Table 278 •*** **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 2 | | MHz | |
| Accuracy | ACCXTAL | | | 0.00105 | % | 050 devices |
| | | | | 0.003 | % | 005, 010, 025, 090, and 150 devices |
| | | | | 0.004 | % | 060 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 1 | 5 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 1 | 5 | ns | |
| Operating current | IDYNXTAL | | 0.3 | | mA | |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 4.5 | ms | 010 and 050 devices |
| | | | | 5 | ms | 005 and 025 devices |
| | | | | 7 | ms | 090 and 150 devices |

***Table 279 •*** **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 32 | | kHz | |
| Accuracy | ACCXTAL | | | 0.004 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.005 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 150 | 300 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 150 | 300 | ns | |
| Operating current | IDYNXTAL | | 0.044 | | mA | 010 and 050 devices |
| | | | 0.060 | | mA | 005, 025, 060, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 115 | ms | 005, 025, 050, 090, and 150 devices |
| | | | | 126 | ms | 010 devices |

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## 2.3.20 On-Chip Oscillator

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

***Table 280 •*** **Electrical Characteristics of the 50 MHz RC Oscillator**

| Parameter | Symbol | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| Operating frequency | F50RC | 50 | | MHz | |
| Accuracy | ACC50RC | 1 | 4 | % | 050 devices |
| | | 1 | 5 | % | 005, 025, and 060 devices |
| | | 1 | 6.3 | % | 090 devices |
| | | 1 | 7.1 | % | 010 and 150 devices |
| Output duty cycle | CYC50RC | 49–51 | 46.5–53.5 | % | |
| Output jitter (peak to peak) | JIT50RC | | | | Period Jitter |
| | | 200 | 300 | ps | 005, 010, 050, and 060 devices |
| | | 200 | 400 | ps | 150 devices |
| | | 300 | 500 | ps | 025 and 090 devices |
| | | | | | Cycle-to-Cycle Jitter |
| | | 200 | 300 | ps | 005 and 050 devices |
| | | 320 | 420 | ps | 010, 060, and 150 devices |
| | | 320 | 850 | ps | 025 and 090 devices |
| Operating current | IDYN50RC | 6.5 | | mA | |

***Table 281 •*** **Electrical Characteristics of the 1 MHz RC Oscillator**

| Parameter | Symbol | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| Operating frequency | F1RC | 1 | | MHz | |
| Accuracy | ACC1RC | 1 | 3 | % | 005, 010, 025, and 050 devices |
| | | 1 | 4.5 | % | 060, and 150 devices |
| | | 1 | 5.6 | % | 090 devices |
| Output duty cycle | CYC1RC | 49–51 | 46.5–53.5 | % | 005, 010, 025, 050, 090 and 150 devices |
| | | 49-51 | 46.0-54.0 | % | 060 devices |
| Output jitter (peak to peak) | JIT1RC | | | | Period Jitter |
| | | 10 | 20 | ns | 005, 010, 025, and 050 devices |
| | | 10 | 28 | ns | 060, 090 and 150 devices |
| | | | | | Cycle-to-Cycle Jitter |
| | | 10 | 20 | ns | 005, 010, and 050 devices |
| | | 10 | 35 | ns | 025, 060, and 150 devices |
| | | 10 | 45 | ns | 090 devices |
| Operating current | IDYN1RC | 0.1 | | mA | |
| Startup time | SU1RC | | 17 | µs | 050, 090, and 150 devices |
| | | | 18 | µs | 005, 010, and 025 devices |

## 2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 282 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Clock conditioning circuitry input frequency $F_{IN_CCC}$ | 1 | | 200 | MHz | All CCC |
| | 0.032 | | 200 | MHz | 32 kHz capable CCC |
| Clock conditioning circuitry output frequency $F_{OUT_CCC}$[1] | 0.078 | | 400 | MHz | |
| PLL VCO frequency[2] | 500 | | 1000 | MHz | |
| Delay increments in programmable delay blocks | | 75 | 100 | ps | |
| Number of programmable values in each programmable delay block | | | 64 | | |
| Acquisition time | | 70 | 100 | µs | $F_{IN}$ >= 1 MHz |
| | | 1 | 16 | ms | $F_{IN}$ = 32 kHz |
| Input duty cycle (reference clock) | | | | | Internal Feedback |
| | 10 | | 90 | % | 1 MHz ≤ $F_{IN_CCC}$ ≤ 25 MHz |
| | 25 | | 75 | % | 25 MHz ≤ $F_{IN_CCC}$≤ 100 MHz |
| | 35 | | 65 | % | 100 MHz ≤ $F_{IN_CCC}$ ≤ 150 MHz |
| | 45 | | 55 | % | 150 MHz ≤ $F_{IN_CCC}$ ≤ 200 MHz |
| | | | | | External Feedback (CCC, FPGA, Off-chip) |
| | 25 | | 75 | % | 1 MHz ≤ $F_{IN_CCC}$ ≤ 25 MHz |
| | 35 | | 65 | % | 25 MHz ≤ $F_{IN_CCC}$ ≤ 35 MHz |
| | 45 | | 55 | % | 35 MHz ≤ $F_{IN_CCC}$ ≤ 50 MHz |
| Output duty cycle | 48 | | 52 | % | 050 devices $F_{OUT}$ ≤ 400 MHz |
| | 48 | | 52 | % | 005, 010, and 025 devices $F_{OUT}$ < 350 MHz |
| | 46 | | 54 | % | 005, 010, and 025 devices 350 MHz ≤ $F_{out}$ ≤ 400 MHz |
| | 48 | | 52 | % | 060 and 090 devices $F_{OUT}$ ≤ 100 MHz |
| | 44 | | 52 | % | 060 and 090 devices 100 MHz ≤ $F_{OUT}$ ≤ 400 MHz |
| | 48 | | 52 | % | 150 devices $F_{OUT}$ ≤ 120 MHz |
| | 45 | | 52 | % | 150 devices 120 MHz ≤ $F_{OUT}$ ≤ 400 MHz |
| **Spread Spectrum Characteristics** | | | | | |
| Modulation frequency range | 25 | 35 | 50 | k | |
| Modulation depth range | 0 | | 1.5 | % | |
| Modulation depth control | | 0.5 | | % | |

1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 283 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**

| **CCC Output Maximum Peak-to-Peak Period Jitter $F_{OUT_CCC}$** | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Conditions/Package Combinations** | | | | | **Unit** |
| **10 FG484, 050 FG896/FG484/FCS325 Packages[1]** | SSO = 0 | 0 < SSO <= 2 | SSO <= 4 | SSO <= 8 | SSO <= 16 | |
| 20 MHz to 100 MHz | Max(110, ± 1% x ($1/F_{OUT_CCC}$)) | Max(150, ± 1% x ($1/F_{OUT_CCC}$)) | | | | ps |
| 100 MHz to 400 MHz | Max(120, ± 1% x ($1/F_{OUT_CCC}$)) | Max(150, ± 1% x ($1/F_{OUT_CCC}$)) | | | Max(170, ± 1% x ($1/F_{OUT_CCC}$)) | ps |
| **025 FG484/FCS325 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 74 MHz | ± 1% x ($1/F_{OUT_CCC}$)) | | | | | ps |
| 74 MHz to 400 MHz | 210 | | | | | ps |
| **005 FG484 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 53 MHz | ± 1% x ($1/F_{OUT_CCC}$)) | | | | | ps |
| 53 MHz to 400 MHz | 270 | | | | | ps |
| **090 FG676 and FC325 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x ($1/F_{OUT_CCC}$)) | | | | | ps |
| 100 MHz to 400 MHz | 150 | | | | | ps |
| **060 FG676 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x ($1/F_{OUT_CCC}$) | | | | | ps |
| 100 MHz to 400 MHz | 150 | | | | | |
| **150 FC1152 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x ($1/F_{OUT_CCC}$)) | | | | | ps |
| 100 MHz to 400 MHz | 120 | | | | | ps |

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

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## 2.3.22 JTAG

***Table 284 •*** **JTAG 1532 for 005, 010, 025, and 050 Devices**

| | | 005 | | 010 | | 025 | | 050 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | |
| Clock to Q (data out) | $T_{TCK2Q}$ | 7.47 | 8.79 | 7.73 | 9.09 | 7.75 | 9.12 | 7.89 | 9.28 | ns |
| Reset to Q (data out) | $T_{RSTB2Q}$ | 7.65 | 9 | 6.43 | 7.56 | 6.13 | 7.21 | 7.40 | 8.70 | ns |
| Test data input setup time | $T_{DISU}$ | –1.05 | –0.89 | –0.69 | –0.59 | –0.67 | –0.57 | –0.30 | –0.25 | ns |
| Test data input hold time | $T_{DIHD}$ | 2.38 | 2.8 | 2.38 | 2.8 | 2.42 | 2.85 | 2.09 | 2.45 | ns |
| Test mode select setup time | $T_{TMSSU}$ | –0.73 | –0.62 | –1.03 | –1.21 | –1.1 | –0.94 | 0.28 | 0.33 | ns |
| Test mode select hold time | $T_{TMDHD}$ | 1.36 | 1.6 | 1.43 | 1.68 | 1.93 | 2.27 | 0.16 | 0.19 | ns |
| ResetB removal time | $T_{TRSTREM}$ | –0.77 | –0.65 | –1.08 | –0.92 | –1.33 | –1.13 | –0.45 | –0.38 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | –0.76 | –0.65 | –1.07 | –0.91 | –1.34 | –1.14 | –0.45 | –0.38 | ns |
| TCK maximum frequency | $F_{TCKMAX}$ | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | 25.00 | 21.25 | MHz |

***Table 285 •*** **JTAG 1532 for 060, 090, and 150 Devices**

| | | 060 | | 090 | | 150 | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| Clock to Q (data out) | $T_{TCK2Q}$ | 8.38 | 9.86 | 8.96 | 10.54 | 8.66 | 10.19 | ns |
| Reset to Q (data out) | $T_{RSTB2Q}$ | 8.54 | 10.04 | 7.75 | 9.12 | 8.79 | 10.34 | ns |
| Test data input setup time | $T_{DISU}$ | –1.18 | –1 | –1.31 | –1.11 | –0.96 | –0.82 | ns |
| Test data input hold time | $T_{DIHD}$ | 2.52 | 2.97 | 2.68 | 3.15 | 2.57 | 3.02 | ns |
| Test mode select setup time | $T_{TMSSU}$ | –0.97 | –0.83 | –1.02 | –0.87 | –0.53 | –0.45 | ns |
| Test mode select hold time | $T_{TMDHD}$ | 1.7 | 2 | 1.67 | 1.96 | 1.02 | 1.2 | ns |
| ResetB removal time | $T_{TRSTREM}$ | –1.21 | –1.03 | –0.76 | –0.65 | –1.03 | –0.88 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | –1.21 | –1.03 | –0.77 | –0.65 | –1.03 | –0.88 | ns |
| TCK maximum frequency | $F_{TCKMAX}$ | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | MHz |

## 2.3.23 System Controller SPI Characteristics

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The following table lists the system controller characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 286 •*** **System Controller SPI Characteristics for All Devices**

| Symbol | Description | Conditions | Min | Typ | Unit |
|---|---|---|---|---|---|
| sp1 | SC_SPI_SCK minimum period | | 20 | | ns |
| sp2 | SC_SPI_SCK minimum pulse width high | | 10 | | ns |
| sp3 | SC_SPI_SCK minimum pulse width low | | 10 | | ns |
| sp4[1] | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%–90%) 1 | I/O configuration: LVTTL 3.3 V– 20 mA<br>AC loading: 35 pF<br>Test conditions: Typical voltage, 25 °C | | 1.239 | ns |
| sp5[1] | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%–90%) 1 | I/O configuration: LVTTL 3.3 V– 20 mA<br>AC loading: 35 pF<br>Test conditions: Typical voltage, 25 °C | | 1.245 | ns |
| sp6 | Data from master (SC_SPI_SDO) setup time | | 160 | | ns |
| sp7 | Data from master (SC_SPI_SDO) hold time | | 160 | | ns |
| sp8 | SC_SPI_SDI setup time | | 20 | | ns |
| sp9 | SC_SPI_SDI hold time | | 20 | | ns |

1. For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx. Use the supported I/O Configurations for the System Controller SPI in the following table.

***Table 287 •*** **Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)**

| Voltage Supply | I/O Drive Configuration | Unit |
|---|---|---|
| 3.3 V | 20 | mA |
| 2.5 V | 16 | mA |
| 1.8 V | 12 | mA |
| 1.5 V | 8 | mA |
| 1.2 V | 4 | mA |

## 2.3.24 Power-up to Functional Times

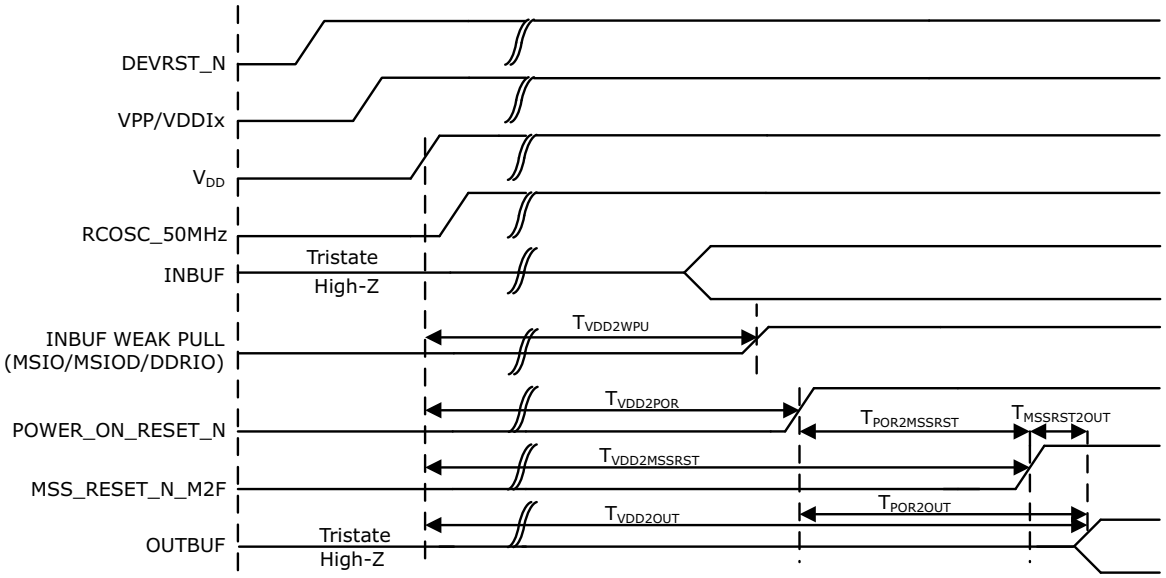
The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 288 •*** **Power-up to Functional Times for SmartFusion2**

| | | | | Maximum Power-up to Functional Time for SmartFusion2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 647 | 500 | 531 | 483 | 474 | 524 | 647 |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F | Fabric to MSS | 644 | 497 | 528 | 480 | 468 | 518 | 641 |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F | Output available at I/O | MSS to output | 3.6 | 3.6 | 3.6 | 3.4 | 4.9 | 4.8 | 4.8 |
| $T_{VDD2OUT}$ | $V_{DD}$ | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 3096 | 2975 | 3012 | 2959 | 2869 | 2992 | 3225 |
| $T_{VDD2POR}$ | $V_{DD}$ | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 2476 | 2487 | 2496 | 2486 | 2406 | 2563 | 2602 |
| $T_{VDD2MSSRST}$ | $V_{DD}$ | MSS_RESET_N_M2F | $V_{DD}$ at its minimum threshold level to MSS | 3093 | 2972 | 3008 | 2956 | 2864 | 2987 | 3220 |
| $T_{VDD2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2500 | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2504 | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2479 | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

**Note:** For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

***Figure 17 •*** **Power-up to Functional Timing Diagram for SmartFusion2**



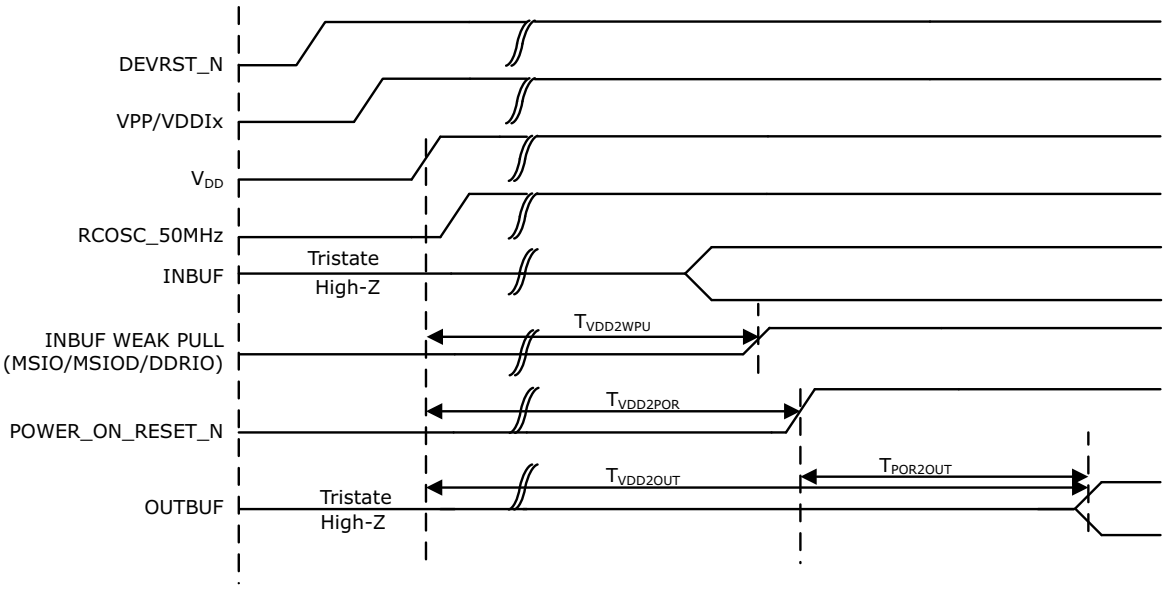

The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 289 •*** **Power-up to Functional Times for IGLOO2**

| | | | | Maximum Power-up to Functional Time for IGLOO2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 114 | 114 | 113 | 114 | 114 | 114 |
| $T_{VDD2OUT}$ | $V_{DD}$ | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 2587 | 2600 | 2607 | 2558 | 2591 | 2600 | 2699 |
| $T_{VDD2POR}$ | $V_{DD}$ | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 2474 | 2486 | 2493 | 2445 | 2477 | 2486 | 2585 |
| $T_{VDD2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2500 | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2504 | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2479 | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

**Note:** For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

***Figure 18 •*** **Power-up to Functional Timing Diagram for IGLOO2**




## 2.3.25 DEVRST_N Characteristics

***Table 290 •*** **DEVRST_N Characteristics for All Devices**

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| DEVRST_N ramp rate | $T_{RAMPDEVRSTN}$ | 1 | us |
| DEVRST_N cycling rate | $F_{MAXPDEVRSTN}$ | 100 | kHz |

## 2.3.26 DEVRST_N to Functional Times

The following table lists the SmartFusion2 DEVRST_N to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

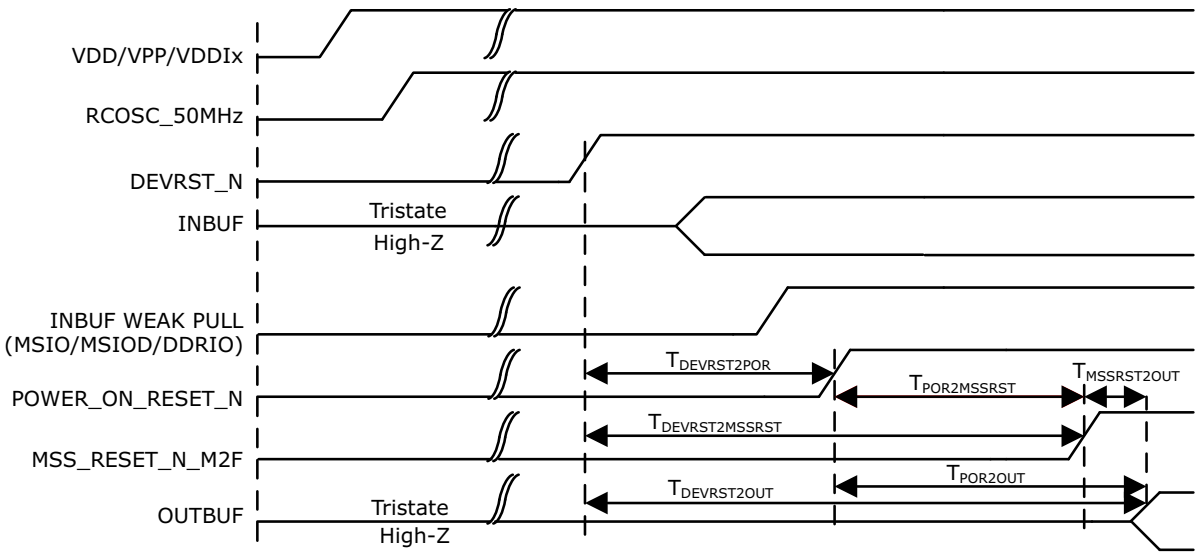
***Table 291 •*** **DEVRST_N to Functional Times for SmartFusion2**

| | | | | Maximum Power-up to Functional Time for SmartFusion2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 518 | 501 | 527 | 521 | 422 | 419 | 694 |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F | Fabric to MSS | 515 | 497 | 524 | 518 | 417 | 414 | 689 |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F | Output available at I/O | MSS to output | 3.5 | 3.5 | 3.5 | 3.3 | 4.8 | 4.8 | 4.8 |
| $T_{DEVRST2OUT}$ | DEVRST_N | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 706 | 768 | 715 | 691 | 641 | 635 | 871 |

***Table 291 •*** **DEVRST_N to Functional Times for SmartFusion2 *(continued)***

| | | | | Maximum Power-up to Functional Time for SmartFusion2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 233 | 289 | 216 | 213 | 237 | 234 | 219 |
| $T_{DEVRST2MSSRST}$ | DEVRST_N | MSS_RESET_N_M2F | $V_{DD}$ at its minimum threshold level to MSS | 702 | 765 | 712 | 688 | 636 | 630 | 866 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |

***Figure 19 •*** **DEVRST_N to Functional Timing Diagram for SmartFusion2**

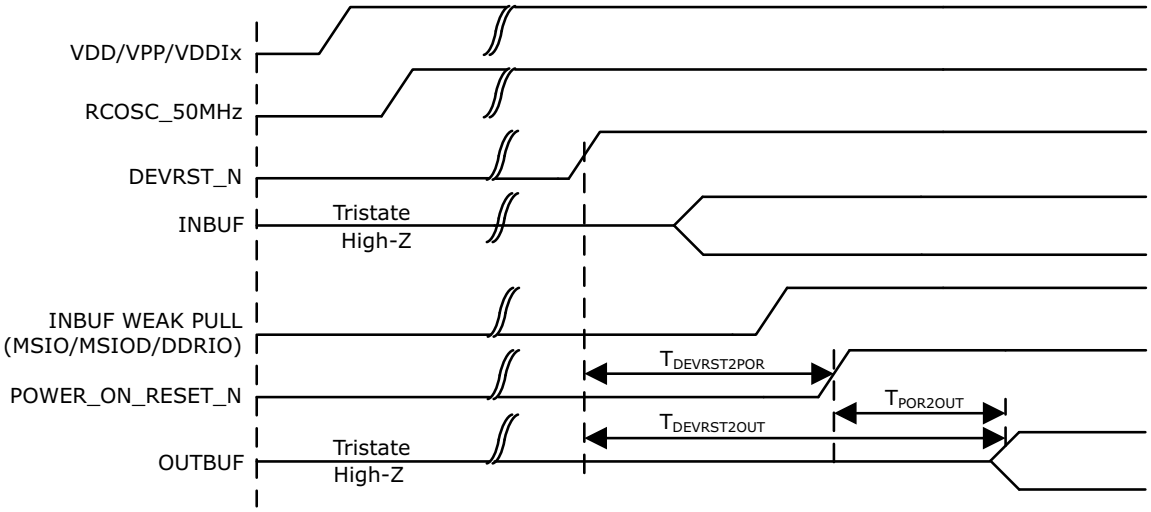


The following table lists the IGLOO2 DEVRST_N to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 292 •*** **DEVRST_N to Functional Times for IGLOO2**

| | | | | Maximum Power-up to Functional Time for IGLOO2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 116 | 113 | 113 | 115 | 115 | 114 |
| $T_{DEVRST2OUT}$ | DEVRST_N | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 314 | 353 | 314 | 307 | 343 | 341 | 341 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 200 | 238 | 201 | 195 | 230 | 229 | 227 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |

***Figure 20 •*** **DEVRST_N to Functional Timing Diagram for IGLOO2**




## 2.3.27 Flash*Freeze Timing Characteristics

The following table lists the Flash*Freeze entry and exit times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 293 •*** **Flash*Freeze Entry and Exit Times**

| | | Entry/Exit Timing FCLK = 100MHz | | Entry/Exit Timing FCLK = 3 MHz | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **005, 010, 025, 060, 090, and 150** | **050** | **All Devices** | **Unit** | **Conditions** |
| Entry time | TFF_ENTRY | 160 | 150 | 320 | µs | eNVM and MSS/HPMS PLL = ON |
| | | 215 | 200 | 430 | µs | eNVM and MSS/HPMS PLL= OFF |
| Exit time with respect to the MSS PLL Lock | TFF_EXIT | 100 | 100 | 140 | µs | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 136 | 120 | 190 | µs | eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit |
| | | 200 | 200 | 285 | µs | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |
| | | 200 | 200 | 285 | µs | eNVM = OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit |

***Table 293 •*** **Flash*Freeze Entry and Exit Times *(continued)***

| Parameter | Symbol | Entry/Exit Timing FCLK = 100MHz | | Entry/Exit Timing FCLK = 3 MHz | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | 005, 010, 025, 060, 090, and 150 | 050 | All Devices | | |
| Exit time with respect to the fabric PLL lock[1] | TFF_EXIT | 1.5 | 1.5 | 1.5 | ms | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 1.5 | 1.5 | 1.5 | ms | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |
| Exit time with respect to the fabric buffer output | TFF_EXIT | 21 | 15 | 21 | µs | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 65 | 55 | 65 | µs | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |

1. PLL Lock Delay set to 1024 cycles (default).

## 2.3.28 DDR Memory Interface Characteristics

The following table lists the DDR memory interface characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 294 •*** **DDR Memory Interface Characteristics**

| Standard | Supported Data Rate | | Unit |
|---|---|---|---|
| | Min | Max | |
| DDR3 | 667 | 667 | Mbps |
| DDR2 | 667 | 667 | Mbps |
| LPDDR | 50 | 400 | Mbps |

## 2.3.29 SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

The following table lists the SFP transceiver electrical characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 295 •*** **SFP Transceiver Electrical Characteristics**

| Pin | Direction | Differential Peak-Peak Voltage | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| RD+/-[1] | Output | 1600 | 2400 | mV |
| TD+/-[2] | Input | 350 | 2400 | mV |

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.

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## 2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 296 •*** **Transmitter Parameters**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| VTX-DIFF-PP | Differential swing (2.5 Gbps, 5.0 Gbps) | 0.8 | 1.2 | V |
| VTX-CM-AC-P | Output common mode voltage (2.5 Gbps) | | 20 | mV |
| VTX-CM-AC-PP | Output common mode voltage (5.0 Gbps) | | 100 | mV |
| VTX-RISE-FALL | Rise and fall time (20% to 80%, 2.5 Gbps) | 0.125 | | UI |
| | Rise and fall time (20% to 80%, 5.0 Gbps) | 0.15 | | UI |
| ZTX-DIFF-DC | Output impedance–differential | 80 | 120 | Ω |
| LTX-SKEW | Lane-to-lane TX skew within a SerDes block (2.5 Gbps) | | 500 ps + 2 UI | ps |
| | Lane-to-lane TX skew within a SerDes block (5.0 Gbps) | | 500 ps + 4 UI | ps |
| RLTX-DIFF | Return loss differential mode (2.5 Gbps) | –10 | | dB |
| | Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz | –10 | | dB |
| | 1.25 GHz to 2.5 GHz | –8 | | dB |
| RLTX-CM | Return loss common mode (2.5 Gbps, 5.0 Gbps) | –6 | | dB |
| TX-LOCK-RST | Transmit PLL lock time from reset | | 10 | µs |
| VTX-AMP | 100 mV setting | 90 | 150 | mV |
| | 400 mV setting | 320 | 480 | mV |
| | 800 mV setting | 660 | 940 | mV |
| | 1200 mV setting | 950 | 1400 | mV |

The following table lists the receiver pa in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 297 •*** **Receiver Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VRX-IN-PP-CC | Differential input peak-to-peak sensitivity (2.5 Gbps) | 0.238 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized) | 0.219 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (5.0 Gbps) | 0.300 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized) | 0.300 | | 1.2 | V |
| VRX-CM-AC-P | Input common mode range (AC coupled) | | | 150 | mV |
| ZRX-DIFF-DC | Differential input termination | 80 | 100 | 120 | Ω |
| REXT | External calibration resistor | 1,188 | 1,200 | 1,212 | Ω |
| CDR-LOCK-RST | CDR relock time from reset | | | 15 | µs |
| RLRX-DIFF | Return loss differential mode (2.5 Gbps) | –10 | | | dB |
| | Return loss differential mode (5.0 Gbps) | | | | |
| | 0.05 GHz to 1.25 GHz | –10 | | | dB |
| | 1.25 GHz to 2.5 GHz | –8 | | | dB |
| RLRX-CM | Return loss common mode (2.5 Gbps, 5.0 Gbps) | –6 | | | dB |
| RX-CID[1] | CID limit PCIe Gen1/2 | | | 200 | UI |
| VRX-IDLE-DET-DIFF-PP | Signal detect limit | 65 | | 175 | mV |

1. AC-coupled, BER = $e^{-12}$, using synchronous clock.

***Table 298 •*** **SerDes Protocol Compliance**

| Protocol | Maximum Data Rate (Gbps) | –1 | –Std |
|---|---|---|---|
| PCIe Gen 1 | 2.5 | Yes | Yes |
| PCIe Gen 2 | 5.0 | Yes | |
| XAUI | 3.125 | Yes | |
| Generic EPCS | 3.2 | Yes | |
| Generic EPCS | 2.5 | Yes | Yes |

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The following table lists the SerDes reference clock AC specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 299 •*** **SerDes Reference Clock AC Specifications**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Reference clock frequency | $F_{REFCLK}$ | 100 | 160 | MHz |
| Reference clock rise time | $T_{RISE}$ | 0.6 | 4 | V/ns |
| Reference clock fall time | $T_{FALL}$ | 0.6 | 4 | V/ns |
| Reference clock duty cycle | $T_{CYC}$ | 40 | 60 | % |
| Reference clock mismatch | $M_{MREFCLK}$ | –300 | 300 | ppm |
| Reference spread spectrum clock | SSCref | 0 | 5000 | ppm |

***Table 300 •*** **HCSL Minimum and Maximum DC Input Levels (Applicable to SerDes REFCLK Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | |
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |
| **HCSL DC Input Voltage Specification** | | | | | |
| DC Input voltage | $V_I$ | 0 | | 2.625 | V |
| **HCSL Differential Voltage Specification** | | | | | |
| Input common mode voltage | $V_{ICM}$ | 0.05 | | 2.4 | V |
| Input differential voltage | $V_{IDIFF}$ | 100 | | 1100 | mV |

***Table 301 •*** **HCSL Minimum and Maximum AC Switching Speeds (Applicable to SerDes REFCLK Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **HCSL AC Specifications** | | | | | |
| Maximum data rate (for MSIO I/O bank) | $F_{MAX}$ | | | 350 | Mbps |
| **HCSL Impedance Specifications** | | | | | |
| Termination resistance | Rt | | 100 | | Ω |

## 2.3.31 SmartFusion2 Specifications

### 2.3.31.1 MSS Clock Frequency

The following table lists the maximum frequency for MSS main clock in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 302 •*** **Maximum Frequency for MSS Main Clock**

| Symbol | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| M3_CLK | Maximum frequency for the MSS main clock | 166 | 142 | MHz |

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### 2.3.31.2 SmartFusion2 Inter-Integrated Circuit ($I^2C$) Characteristics

This section describes the DC and switching of the $I^2C$ interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the $I^2C$ characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

***Table 303 •*** **I2C Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | –0.3 | | 0.8 | V | See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive. |
| Input high voltage | $V_{IH}$ | 2 | | 3.45 | V | See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive. |
| Hysteresis of schmitt triggered inputs for $V_{DDI}$ > 2 V | $V_{HYS}$ | 0.05 × $V_{DDI}$ | | | V | See Table 28, page 23 for more information. |
| Input current high | $I_{IL}$ | | | 10 | µA | See Single-Ended I/O Standards, page 24 for more information. |
| Input current low | $I_{IH}$ | | | 10 | µA | See Single-Ended I/O Standards, page 24 for more information. |
| Input rise time | $T_{ir}$ | | | 1000 | ns | Standard mode |
| | | | | 300 | ns | Fast mode |
| Input fall time | $T_{if}$ | | | 300 | ns | Standard mode |
| | | | | 300 | ns | Fast mode |
| Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI}$ > 2 V | $V_{OL}$ | | | 0.4 | V | See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive. |
| Pin capacitance | Cin | | | 10 | pF | $V_{IN}$ = 0, f = 1.0 MHz |
| Output fall time from VIHMin to VILMax[1] | $t_{OF}$[1] | | 21.04 | | ns | $V_{IHmin}$ to $V_{ILMax}$, CLOAD = 400 pF |
| | | | 5.556 | | ns | $V_{IHmin}$ to $V_{ILMax}$, CLOAD = 100 pF |
| Output rise time from VILMax to VIHMin[1] | $t_{OR}$ [1] | | 19.887 | | ns | $V_{ILMax}$ to $V_{IHmin}$, CLOAD = 400 pF |
| | | | 5.218 | | ns | $V_{ILMax}$ to $V_{IHmin}$, CLOAD = 100 pF |
| Output buffer maximum pull-down resistance[2, 3] | $R_{pull\text{-}up}$[2,3] | | | 50 | Ω | |
| Output buffer maximum pull-up resistance[2, 4] | $R_{pull\text{-}down}$[2,4] | | | 131.25 | Ω | |

***Table 303 •*** **I2C Characteristics *(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | | | 400 | Kbps | Fast mode |
| | | | | 100 | Kbps | Standard mode |
| Pulse width of spikes which must be suppressed by the input filter | $T_{FILT}$ | | 50 | | ns | Fast mode |

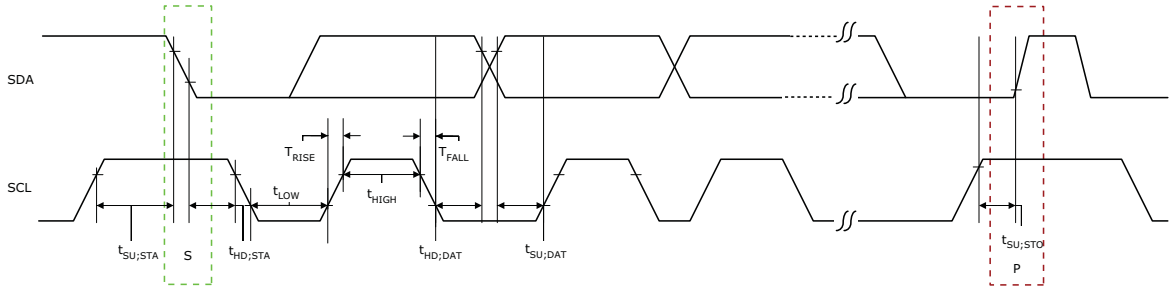
1. These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on $V_{DDIx}$, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
3. R(PULL-DOWN-MAX) = (VOLspec)/IOLspec.
4. R(PULL-UP-MAX) = (VDDImax–VOHspec)/IOHspec.

The following table lists the $I^2C$ switching characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

***Table 304 •*** **I2C Switching Characteristics**

| | | –1 | Std | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Min** | **Unit** |
| Low period of I2C_x_SCL | $T_{LOW}$ | 1 | 1 | PCLK cycles |
| High period of I2C_x_SCL | $T_{HIGH}$ | 1 | 1 | PCLK cycles |
| START hold time | $T_{HD;STA}$ | 1 | 1 | PCLK cycles |
| START setup time | $T_{SU;STA}$ | 1 | 1 | PCLK cycles |
| DATA hold time | $T_{HD;DAT}$ | 1 | 1 | PCLK cycles |
| DATA setup time | $T_{SU;DAT}$ | 1 | 1 | PCLK cycles |
| STOP setup time | $T_{SU;STO}$ | 1 | 1 | PCLK cycles |

***Figure 21 •*** **$I^2C$ Timing Parameter Definition**



### 2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, see Figure 22, page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

***Table 305 •*** **SPI Characteristics for All Devices**

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0\|1]_CLK minimum period | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.1 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.19 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.39 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.77 | | | µs | |
| sp2 | SPI_[0\|1]_CLK minimum pulse width high | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp3 | SPI_[0\|1]_CLK minimum pulse width low | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp4 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS rise time (10%–90%)[1] | | 2.77 | | ns | I/O Configuration: LVCMOS 2.5 V– 8 mA<br>AC loading: 35 pF<br>Test conditions: Typical voltage, 25 °C |

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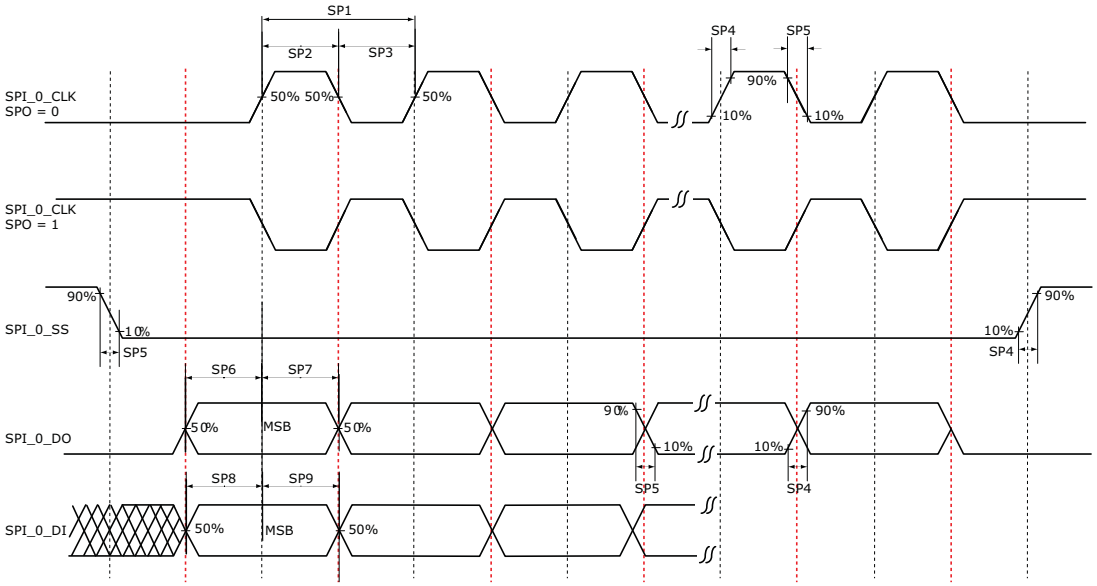
***Table 305 •*** **SPI Characteristics for All Devices *(continued)***

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| sp5 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS fall time (10%–90%)[1] | | 2.906 | | ns | IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C |
| SPI master configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 8.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 2.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 12 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |
| SPI slave configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 17.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) + 3.0 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 2 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 7 | | | ns | |
| SPI master configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 7.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 9.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 15 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | –2.5 | | | ns | |
| SPI slave configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 16.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) - 3.5 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 3 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

***Figure 22 •*** **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**




## 2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 306 •*** **CAN Controller Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FCANREFCLK[1] | Internally sourced CAN reference clock frequency | 160 | 136 | MHz |
| BAUDCANMAX | Maximum CAN performance baud rate | 1 | 1 | Mbps |
| BAUDCANMIN | Minimum CAN performance baud rate | 0.05 | 0.05 | Mbps |

1. PCLK to CAN controller must be a multiple of 8 MHz.

## 2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 307 •*** **USB Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FUSBREFCLK | Internally sourced USB reference clock frequency | 166 | 142 | MHz |
| TUSBCLK | USB clock period | 16.66 | 16.66 | ns |
| TUSBPD | Clock to USB data propagation delay | 9.0 | 9.0 | ns |
| TUSBSU | Setup time for USB data | 6.0 | 6.0 | ns |
| TUSBHD | Hold time for USB data | 0 | 0 | ns |

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## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 308 •*** **MMUART Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FMMUART_REF_CLK | Internally sourced MMUART reference clock frequency. | 166 | 142 | MHz |
| BAUDMMUARTTx | Maximum transmit baud rate | 10.375 | 8.875 | Mbps |
| BAUDMMUARTRx | Maximum receive baud rate | 10.375 | 8.875 | Mbps |

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 309 •*** **Maximum Frequency for HPMS Main Clock**

| Symbol | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| HPMS_CLK | Maximum frequency for the HPMS main clock | 166 | 142 | MHz |

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 310 •*** **SPI Characteristics for All Devices**

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0\|1]_CLK minimum period | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.1 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.19 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.39 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.77 | | | µs | |

***Table 310 •*** **SPI Characteristics for All Devices *(continued)***

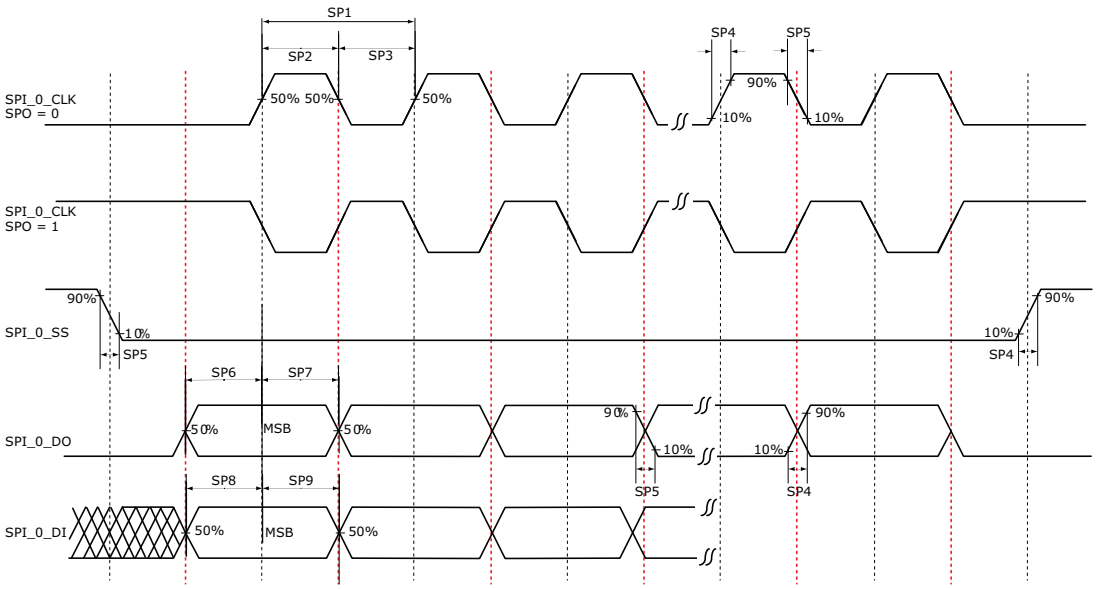
| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| sp2 | SPI_[0\|1]_CLK minimum pulse width high | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp3 | SPI_[0\|1]_CLK minimum pulse width low | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp4 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS rise time (10%–90%)[1] | | 2.77 | | ns | I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C |
| sp5 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS fall time (10%–90%)[1] | | 2.906 | | ns | I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C |
| SPI master configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 8.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 2.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 12 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |
| SPI slave configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 17.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) + 3.0 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 2 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 7 | | | ns | |

***Table 310 •*** **SPI Characteristics for All Devices *(continued)***

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPI master configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 7.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 9.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 15 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | –2.5 | | | ns | |
| SPI slave configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 16.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) - 3.5 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 3 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

***Figure 23 •*** **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**



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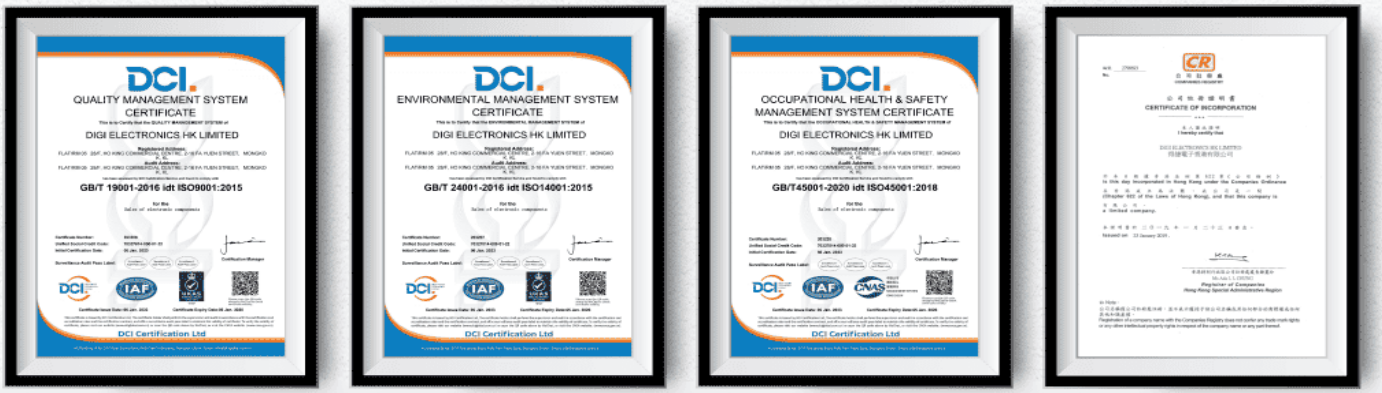

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