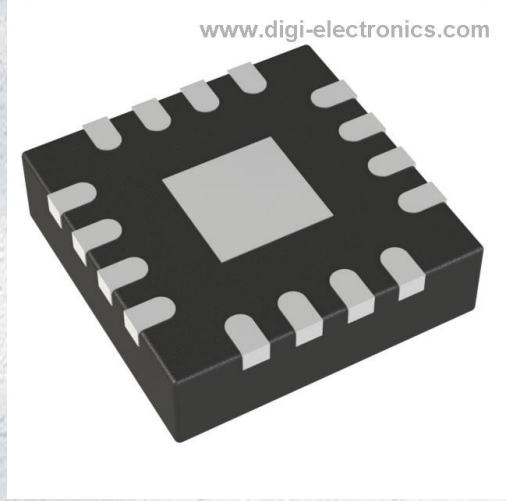
MCP47CVB11-E/MG Datasheet



DiGi Electronics Part Number	MCP47CVB11-E/MG-DG
Manufacturer	Microchip Technology
Manufacturer Product Number	MCP47CVB11-E/MG
Description	IC DAC 10BIT V-OUT 16QFN
Detailed Description	10 Bit Digital to Analog Converter 1 16-QFN (3x3)

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MCP47CVB11-E/MG	Microchip Technology
Series:	Product Status:
-	Active
DiGi-Electronics Programmable:	Number of Bits:
Not Verified	10
Number of D/A Converters:	Settling Time:
1	16µs (Typ)
Output Type:	Differential Output:
Voltage - Buffered	Yes
Data Interface:	Reference Type:
I2C	External, Internal
Voltage - Supply, Analog:	Voltage - Supply, Digital:
1.8V ~ 5.5V	1.8V ~ 5.5V
INL/DNL (LSB):	Architecture:
±0.25, ±0.25	Current Source
Operating Temperature:	Package / Case:
-40°C ~ 125°C	16-VFQFN Exposed Pad
Supplier Device Package:	Mounting Type:
16-QFN (3x3)	Surface Mount
Base Product Number:	
MCP47CVB11	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	3 (168 Hours)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

MCP47CXBX4/8

8/10/12-Bit Digital-to-Analog Converters, 1 LSb INL, Quad/Octal Voltage Output with I²C Interface

Features

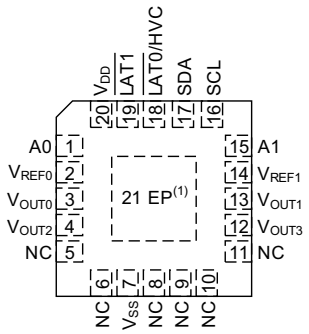
- Memory Options:
  - Volatile memory: MCP47CVBXX
  - Nonvolatile memory: MCP47CMBXX
- Operating Voltage Range:
  - 2.7V to 5.5V – full specifications
  - 1.8V to 2.7V – reduced device specifications
- Output Voltage Resolutions:
  - 8-bit: MCP47CXB0X (256 steps)
  - 10-bit: MCP47CXB1X (1024 steps)
  - 12-bit: MCP47CXB2X (4096 steps)
- Nonvolatile Memory (MTP) Size: 32 Locations
- 1 LSb Integral Nonlinearity (INL) Specification
- DAC Voltage Reference Source Options:
  - Device V_{DD}
  - External V_{REF} pin (buffered or unbuffered)
  - Internal band gap (1.214V typical)
- Output Gain Options:
  - 1x (unity)
  - 2x (available when not using internal V_{DD} as voltage source)
- Power-on/Brown-out Reset (POR/BOR) Protection
- Power-Down Modes:
  - Disconnects output buffer (high-impedance)
  - Selection of V_{OUT} pull-down resistors (100 kΩ or 1 kΩ)
- I²C Interface:
  - Options: two physical address select pins and register-defined address (for nonvolatile devices only)
  - Standard (100 kbps), Fast (400 kbps) and High-Speed (up to 3.4 Mbps) modes
- Package Types:
  - 20-lead 4 mm x 4 mm QFN, 20-lead TSSOP
- Extended Temperature Range: -40°C to +125°C

Applications

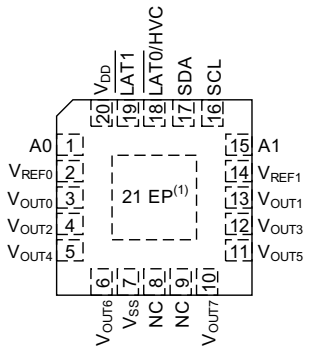
- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- Data Acquisition Systems
- Motor Control

Package Types

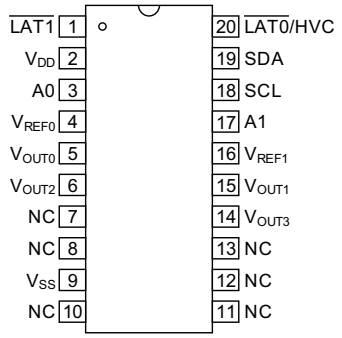
MCP47CXBX4 (Quad)
20-Lead QFN (4 x 4)



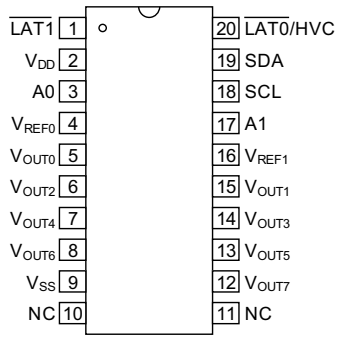
MCP47CXBX8 (Octal)
20-Lead QFN (4 x 4)



MCP47CXBX4 (Quad)
20-Lead TSSOP



MCP47CXBX8 (Octal)
20-Lead TSSOP



Note 1: Includes Exposed Thermal Pad (EP); see Table 3-1 and Table 3-2.

MCP47CXBX4/8

General Description

The MCP47CXBX4/8 devices are quad and octal channel 8-bit, 10-bit and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with volatile or MTP memory and an I^2C serial interface.

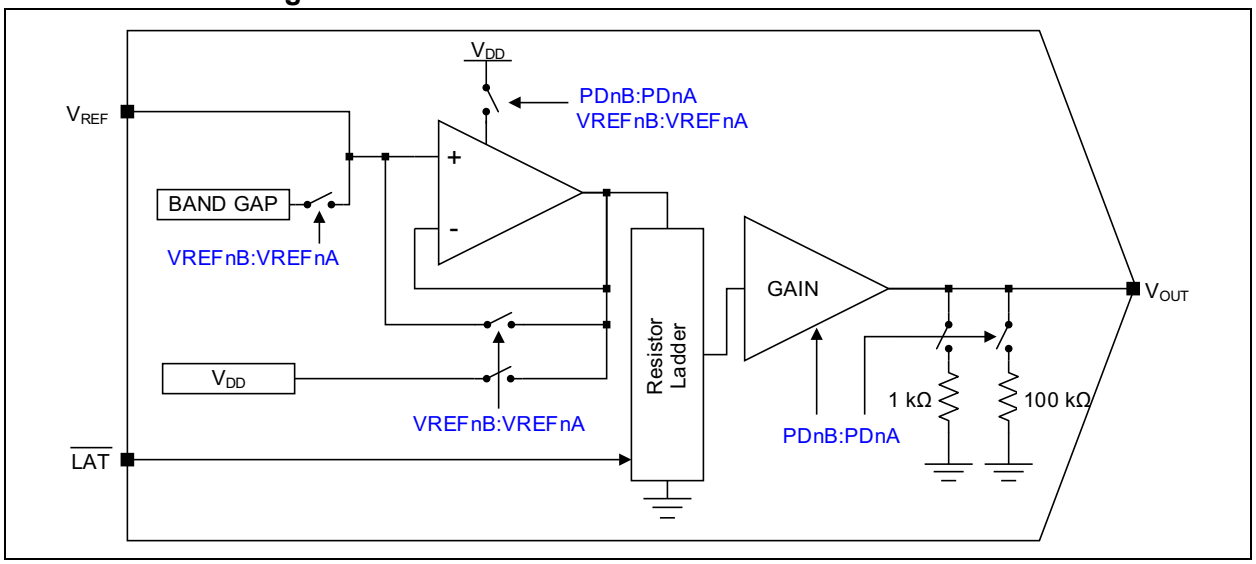
The MTP memory can be written by the user up to 32 times for each specific register. It requires a high-voltage level on the HVC pin, typically 7.5V, in order to successfully program the desired memory location. The nonvolatile memory consists of power-up output values, configuration registers and general purpose locations.

The V_{REF} pin, the device V_{DD} or the internal band gap voltage can be selected as the DAC's reference voltage. When V_{DD} is selected, V_{DD} is internally connected to the DAC reference circuit.

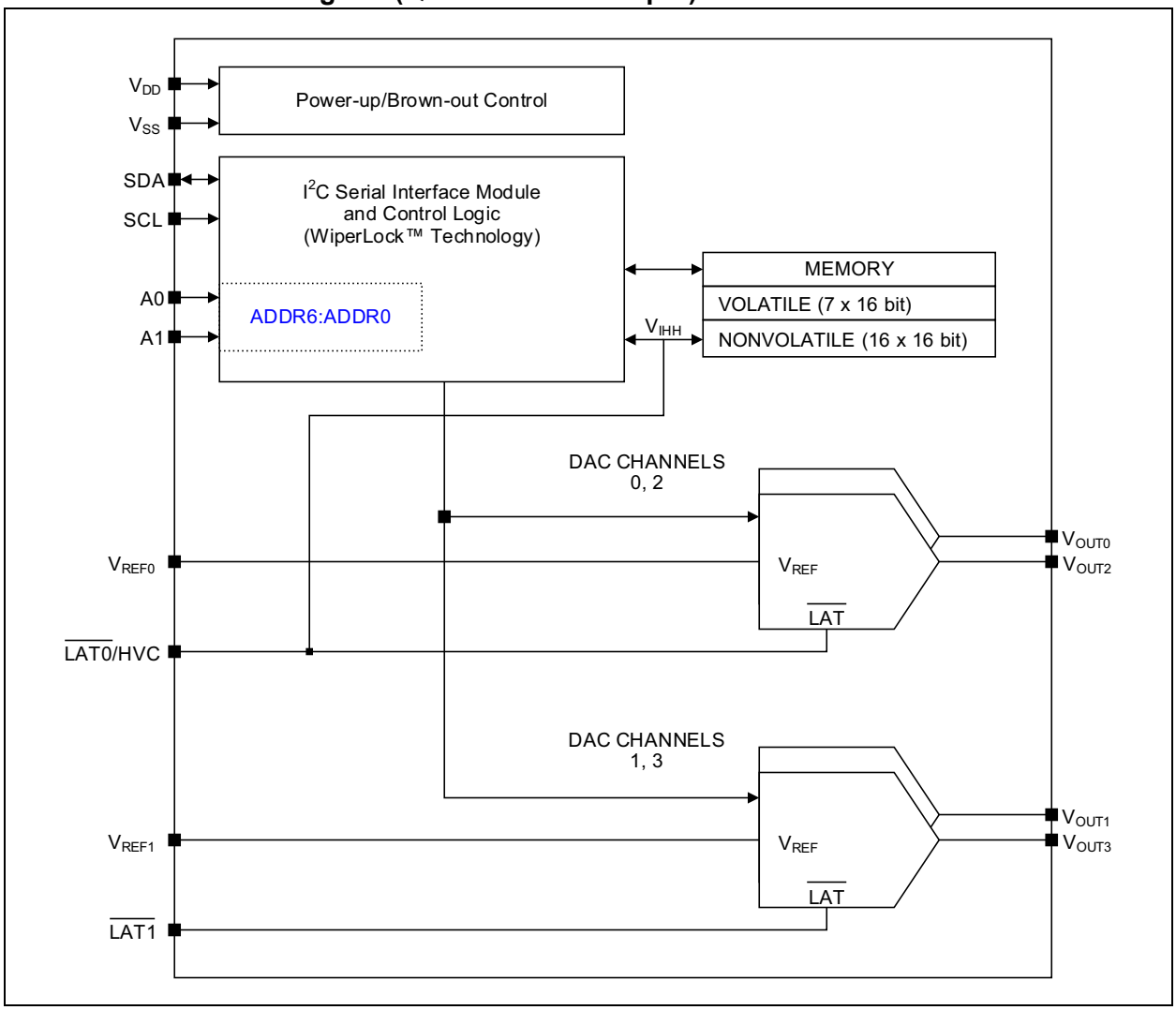
When the V_{REF} pin is used with an external voltage reference, the user can select between a gain of 1 or 2 and can have the reference buffer enabled or disabled. When the gain is 2, the V_{REF} pin voltage must be limited to a maximum of $V_{DD}/2$.

These devices have a two-wire I^2C compatible serial interface for Standard (100 kHz), Fast (400 kHz) or High-Speed (1.7 MHz and 3.4 MHz) modes.

DAC Core Block Diagram

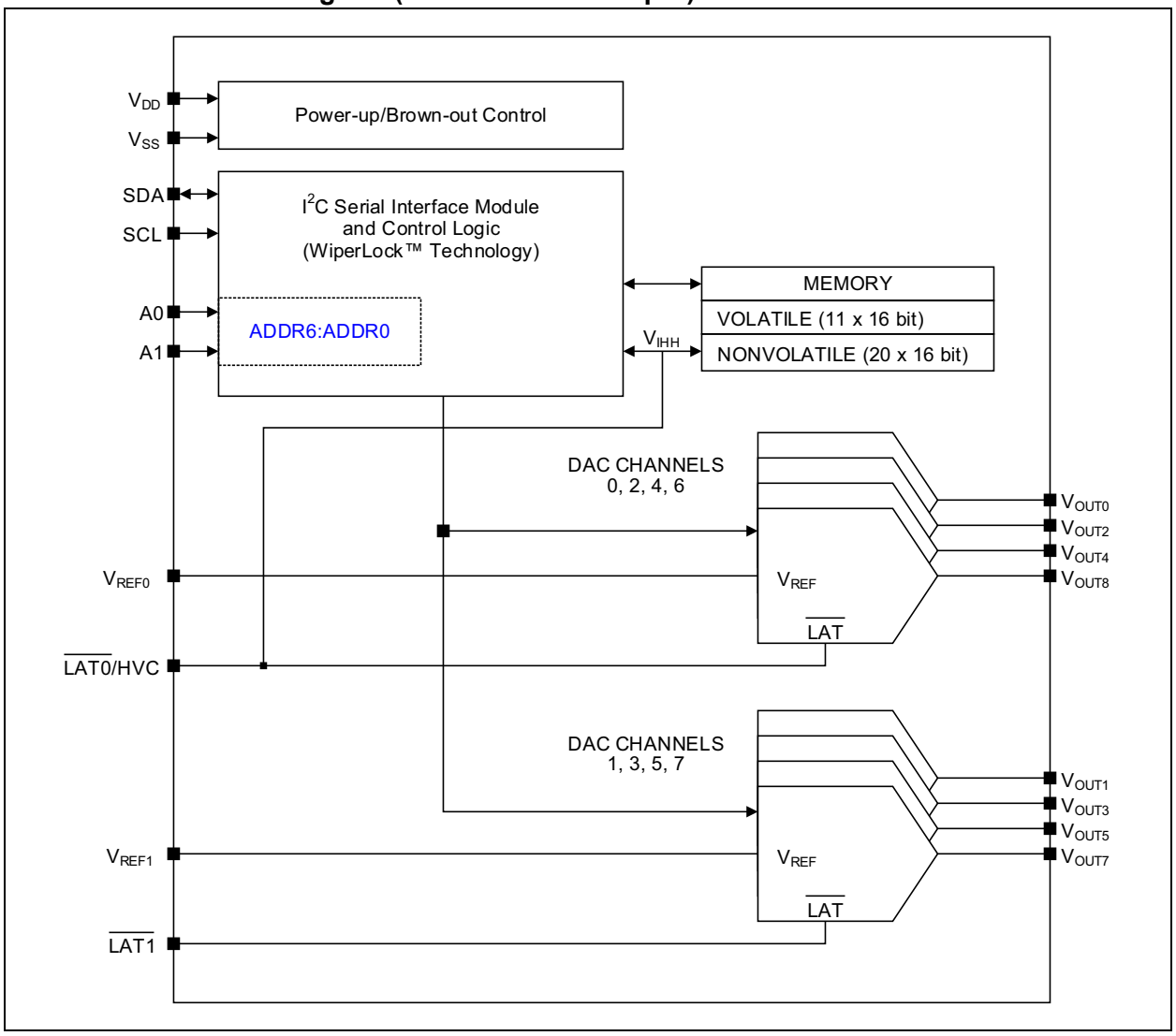


MCP47CXBX4 Block Diagram (Quad-Channel Output)



MCP47CXBX4/8

MCP47CXBX8 Block Diagram (Octal-Channel Output)



Family Device Features

Device	Package Type	# of Channels	Resolution (bits)	DAC Output POR/BOR Setting[1]	# of V_{REF} Inputs	# of $\overline{LAT}$ Inputs	# of Address Pins	Memory[2]	GP MTP Locations
MCP47CVB04	TSSOP, QFN	4	8	7Fh	2	2	2	RAM	—
MCP47CVB14	TSSOP, QFN	4	10	1FFh	2	2	2	RAM	—
MCP47CVB24	TSSOP, QFN	4	12	7FFh	2	2	2	RAM	—
MCP47CVB08	TSSOP, QFN	8	8	7Fh	2	2	2	RAM	—
MCP47CVB18	TSSOP, QFN	8	10	1FFh	2	2	2	RAM	—
MCP47CVB28	TSSOP, QFN	8	12	7FFh	2	2	2	RAM	—
MCP47CMB04	TSSOP, QFN	4	8	7Fh	2	2	2	MTP	8
MCP47CMB14	TSSOP, QFN	4	10	1FFh	2	2	2	MTP	8
MCP47CMB24	TSSOP, QFN	4	12	7FFh	2	2	2	MTP	8
MCP47CMB08	TSSOP, QFN	8	8	7Fh	2	2	2	MTP	8
MCP47CMB18	TSSOP, QFN	8	10	1FFh	2	2	2	MTP	8
MCP47CMB28	TSSOP, QFN	8	12	7FFh	2	2	2	MTP	8

Note 1: The factory default value.

2: Each nonvolatile memory location can be written 32 times. For subsequent writes to the MTP, the device will ignore the commands and the memory will not be modified.

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Voltage on V_{DD} with Respect to V_{SS} ..... -0.6V to +6.5V
Voltage on all Pins with Respect to V_{SS} ..... -0.6V to V_{DD} + 0.3V
Input Clamp Current, I_{IK} (V_I < 0, V_I > V_{DD}, V_I > V_{PP} on HV Pins) ..... ±20 mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum Current out of the V_{SS} Pin (Quad) ..... 50 mA
(Octal) ..... 100 mA
Maximum Current into the V_{DD} Pin (Quad) ..... 50 mA
(Octal) ..... 100 mA
Maximum Current Sourced by the V_{OUT} Pin ..... 20 mA
Maximum Current Sunk by the V_{OUT} Pin ..... 20 mA
Maximum Current Sourced/Sunk by the $V_{REF(0)}$ Pin (in Band Gap mode) ..... 20 mA
Maximum Current Sunk by the V_{REFX} Pin (when V_{REF} is in Unbuffered mode) ..... 350 µA
Maximum Current Sourced by the V_{REFX} Pin ..... 20 µA
Maximum Current Sunk by the V_{REF} Pin ..... 125 µA
Maximum Input Current Sourced/Sunk by the SDA, SCL Pins ..... 2 mA
Maximum Output Current Sunk by the SDA Output Pin ..... 25 mA
Total Power Dissipation(1) ..... 400 mW
ESD Protection on all Pins ..... ≥ ±8 kV (HBM)
..... ≥ ±400V (MM)
..... ≥ ±2 kV (CDM)
Latch-Up (per JEDEC® JESD78A) at +125°C ..... ±100 mA
Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -55°C to +125°C
Soldering Temperature of Leads (10 seconds) ..... +300°C
Maximum Junction Temperature (T_J) ..... +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.7	—	5.5	V	
		1.8	—	2.7	V	DAC operation (reduced analog specifications) and serial interface
V_{DD} Voltage (Rising) to Ensure Device Power-on Reset	V_{POR}	—	—	1.75	V	RAM retention voltage: (V_{RAM}) < V_{POR}, V_{DD} voltages greater than the V_{POR} limit ensure that the device is out of reset
V_{DD} Voltage (Falling) to Ensure Device Brown-out Reset	V_{BOR}	V_{RAM}	—	1.61	V	RAM retention voltage: (V_{RAM}) < V_{BOR}
V_{DD} Rise Rate to Ensure POR	V_{DDRR}	**Note 3**			V/ms	
POR to Output-Driven Delay(1)	T_{POR2OD}	—	—	175	µs	V_{DD} rising, V_{DD} > V_{POR}, quad output
		—	—	265	µs	V_{DD} rising, V_{DD} > V_{POR}, octal output

Note 1 This parameter is ensured by design.

Note 3 POR/BOR voltage trip point is not slope-dependent. Hysteresis is implemented with time delay.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions		
Supply Current	I_{DD}	—	—	550	µA	Quad	100 kHz(2)	Serial interface active, VRnB:VRnA = 10(4), V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Mid-Scale
		—	—	650			400 kHz	
		—	—	820			1.7 MHz(2)	
		—	—	1090			3.4 MHz(2)	
		—	—	900		Octal	100 kHz(2)	
		—	—	970			400 kHz	
		—	—	1110			1.7 MHz(2)	
		—	—	1380			3.4 MHz(2)	
		—	—	410		Quad	Serial interface inactive, VRnB:VRnA = 10, V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Mid-Scale	
		—	—	720		Octal		
$\overline{LAT}$/HVC Pin Write Current(1)	$I_{DD(MTP\_WR)}$	—	—	6.40	mA	—	Serial interface inactive (MTP write active), VRnB:VRnA = 10 (valid for all modes), V_{DD} = 5.5V, $\overline{LAT}$/HVC = V_{IHH}, write all '1's to nonvolatile DAC0, V_{OUT} pins are unloaded	
Power-Down Current	I_{DDP}	—	0.54	2.40	µA	—	PDnB:PDnA = 01(5), VRnB:VRnA = 10, V_{OUT} not connected	

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 4 Supply current is independent of current through the resistor ladder in mode VRnB:VRnA = 10.

Note 5 The PDnB:PDnA = 01, 10 and 11 configurations must have the same current.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Resistor Ladder Resistance[6]	R_L	62.475	73.5	84.525	kΩ	VRnB:VRnA = 10, V_{REF} = V_{DD}	
Resolution (# of resistors and # of taps), (see C.1, "Resolution")	N	256			Taps	8-bit	No missing codes
		1024			Taps	10-bit	No missing codes
		4096			Taps	12-bit	No missing codes
Nominal V_{OUT} Match[10]	$\lvert V_{OUT} - V_{OUTMEAN}\rvert / V_{OUTMEAN}$	—	0.026	0.300	%	1.8V ≤ V_{DD} ≤ 5.5V[2]	
V_{OUT} Temperature Coefficient[2] (see C.19, "V_{OUT} Temperature Coefficient")	$\Delta V_{OUT}/\Delta T$	—	3	—	ppm/°C	Code = Mid-Scale, VRnB:VRnA = 00, 10 and 11	
V_{REF} Pin Input Voltage Range[1]	V_{REF}	V_{SS}	—	V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V	

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 6 Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = 10) and the V_{SS} pin. This is the effective resistance of each resistor ladder. The resistance measurement is one of the resistor ladders measured in parallel.

Note 10 Variation of one output voltage to mean output voltage.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Zero-Scale Error (Code = 000h) (see **C.4, "Zero-Scale Error (E_{ZS})"**)	E_{ZS}	—	—	0.5	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		—	—	2	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		—	—	8	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
Offset Error (see **C.6, "Offset Error (E_{OS})"**)	E_{OS}	-9	±1.1	+9	mV	VRnB:VRnA = 10, Gn = 0, no load, 8-bit: Code = 4; 10-bit: Code = 16; 12-bit: Code = 64	
Offset Voltage Temperature Coefficient[2, 9]	V_{OSTC}	—	±9	—	µV/°C		
Full-Scale Error (see **C.5, "Full-Scale Error (E_{FS})"**)	E_{FS}	—	—	0.625	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		—	—	2.5	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		—	—	10	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
Gain Error (see **C.8, "Gain Error (E_G)"**)[7]	E_G	-0.6	±0.1	+0.6	% of FSR	8-bit	VRnB:VRnA = 10, G = 0, Code = 252, V_{REF} = V_{DD}, no load
		-0.6	±0.1	+0.6	% of FSR	10-bit	VRnB:VRnA = 10, G = 0, Code = 1008, V_{REF} = V_{DD}, no load
		-0.6	±0.1	+0.6	% of FSR	12-bit	VRnB:VRnA = 10, G = 0, Code = 4032, V_{REF} = V_{DD}, no load
Gain Error Drift[2, 9] (see **C.9, "Gain Error Drift (EG_D)"**)	ΔG/°C	—	-10	—	ppm/°C		

Note 2 This parameter is ensured by characterization.

Note 7 This gain error does not include the offset error.

Note 9 Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Total Unadjusted Error[2, 9] (see **C.10, "Total Unadjusted Error (E_T)"**)	E_T	-1.375	—	0.625	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-5.5	—	2.5	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-22	—	10	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 10, G = 1, V_{REF} = 0.5 × V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 01, G = 0, G = 1, V_{DD} = 1.8V-5.5V, no load
Integral Nonlinearity (see **C.11, "Integral Nonlinearity (INL)"**)[9]	INL	-0.1	—	+0.1	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-0.25	—	+0.25	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-1	—	+1	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 10, G = 1, V_{REF} = 0.5 × V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 01, G = 0, G = 1, V_{DD} = 1.8V-5.5V, no load
Differential Nonlinearity (see **C.12, "Differential Nonlinearity (DNL)"**)[9]	DNL	-0.1	—	+0.1	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-0.25	—	+0.25	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-1.0	—	+1.0	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 10, G = 1, V_{REF} = 0.5 × V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 01, G = 0, G = 1, V_{DD} = 1.8V-5.5V, no load

Note 2 This parameter is ensured by characterization.

Note 9 Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
-3 dB Bandwidth (see **C.16, "-3 dB Bandwidth"**)	BW	—	270	—	kHz	V_{REF} = 3.00V ± 2V, VRnB:VRnA = 10, Gn = 0	
		—	170	—		V_{REF} = 3.50V ± 1.5V, VRnB:VRnA = 10, Gn = 1	
Output Amplifier (Op Amp)							
Phase Margin[(1)]	PM	—	76	—	°C	R_L = ∞	
Slew Rate	SR	—	0.7	—	V/µs	R_L = 2 kΩ	
Load Regulation	—	—	147	—	µV/mA	1 mA ≤ I ≤ 6 mA	V_{DD} = 5.5V, DAC code = Mid-Scale
		—	176	—	µV/mA	-6 mA ≤ I ≤ -1 mA	
Short-Circuit Current	I_{SC_OA}	6	10	14	mA	Short to V_{SS}	DAC code = Full Scale
		6	10	14	mA	Short to V_{DD}	DAC code = Zero Scale
Settling Time[(8)]	$t_{SETTLING}$	—	4	—	µs	R_L = 2 kΩ	
Internal Band Gap							
Band Gap Voltage	V_{BG}	1.180	1.214	1.260	V	1.8V ≤ V_{DD} ≤ 5.5V	
Short-Circuit Current	I_{SC_BG}	6	10	14	mA	Short to V_{SS}	
		6	10	14	mA	Short to V_{DD}	
Band Gap Voltage Temperature Coefficient	V_{BGTC}	—	18	—	ppm/°C	1.8V ≤ V_{DD} ≤ 5.5V	
Band Gap Mode, V_{REF} Pin Load Regulation	I_{BG}	—	38	—	µV/mA	1 mA ≤ I ≤ 6 mA	V_{DD} = 5.5V
		—	363	—	µV/mA	-6 mA ≤ I ≤ -1 mA	

Note 1 This parameter is ensured by design.

Note 8 Within 1/2 LSb of the final value, when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device.)

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
External Reference (V_{REF})						
Input Range(1)	V_{REF}	V_{SS}	—	V_{DD}	V	VRnB:VRnA = 10 (Unbuffered mode)
Input Capacitance	C_{REF}	—	29	—	pF	VRnB:VRnA = 10 (Unbuffered mode)
Input Impedance	R_L	See **Resistor Ladder Resistance(6)**			kΩ	2.7V ≤ V_{DD} ≤ 5.5V, VRnB:VRnA = 10, V_{REF} = V_{DD}
Current through V_{REF}(1)	I_{VREF}	—	—	353.1	µA	Mathematically from $R_{VREF(min)}$ spec (at 5.5V)
Total Harmonic Distortion(1)	THD	—	-76	—	dB	V_{REF} = 2.048V ± 0.1V, VRnB:VRnA = 10, Gn = 0, Frequency = 1 kHz
Dynamic Performance						
Major Code Transition Glitch (see **C.14, "Major Code Transition Glitch"**)	—	—	60	—	nV-s	1 LSb change around major carry (7FFh to 800h)
Digital Feedthrough (see **C.15, "Digital Feedthrough"**)	—	—	< 2	—	nV-s	

Note 1 This parameter is ensured by design.

Note 6 Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = 10) and the V_{SS} pin. This is the effective resistance of each resistor ladder. The resistance measurement is one of the resistor ladders measured in parallel.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Digital Inputs/Outputs ($\overline{LAT0}$/HVC, $\overline{LAT1}$, A0, A1)						
Schmitt Trigger High Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 5.5V (allows 2.7V digital V_{DD} with 5.5V analog V_{DD} or 1.8V digital V_{DD} with 3.0V analog V_{DD})
Schmitt Trigger Low Input Threshold	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_{DD}	—	V	
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	
Digital Interface (SDA, SCL)						
Output Low Voltage	V_{OL}	—	—	0.4	V	V_{DD} ≥ 2.0V, I_{OL} = 3 mA
		—	—	0.2 V_{DD}	V	V_{DD} < 2.0V, I_{OL} = 1 mA
Input High Voltage (SDA and SCL pins)	V_{IH}	0.7 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 5.5V
Input Low Voltage (SDA and SCL pins)	V_{IL}	—	—	0.3 V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V
Input Leakage	I_L	-1	—	1	µA	SCL = SDA = V_{SS} or SCL = SDA = V_{DD}
Pin Capacitance	C_{PIN}	—	10	—	pF	
RAM Value						
Value Range	N	0h	—	FFh	Hex	8-bit
			—	3FFh		10-bit
			—	FFFh		12-bit
DAC Register POR/BOR Value	N	See Table 4-2			Hex	8-bit
						10-bit
						12-bit
PDCON Initial Factory Setting	—	See Table 4-2			Hex	
Power Requirements						
Power Supply Sensitivity	PSS	—	0.0010	0.0070	%/%	8-bit Code = Mid-Scale
		—				10-bit
		—				12-bit

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Multi-Time Programming Memory (MTP)						
MTP Programming Voltage(1)	V_{PG_MTP}	2.0	—	5.5	V	HVC = V_{IHH}, -20°C ≤ T_A ≤ +125°C
$\overline{LAT}$/HVC Pin Voltage for MTP Programming (high-voltage commands)	V_{IHH}	7.25	7.5	7.75V	V	The $\overline{LAT}$/HVC pin will be at one of the three input levels (V_{IL}, V_{IH} or V_{IHH})(1, 11) The $\overline{LAT}$/HVC pin must supply the required MTP programming current (up to 6.4 mA)
Writes Cycles	—	—	—	32(12)	Cycles	Note 1
Data Retention	DR_{MTP}	10	—	—	Years	At +125°C(1)
MTP Range	N	0h	—	FFh	Hex	8-bit
		0h	—	3FFh	Hex	10-bit
		0h	—	FFFh	Hex	12-bit
		0000h		7FFFh	Hex	All general purpose memory
Initial Factory Setting	N	See Table 4-2			—	
MTP Programming Write Cycle Time(1)	$t_{WC(MTP)}$	—	—	250	µs	V_{DD} = +2.0V to 5.5V, -20°C ≤ T_A ≤ +125°C

Note 1 This parameter is ensured by design.

Note 11 High-voltage on the LAT/HVC pin must be limited to the command plus programming time. After the programming cycle, the LAT/HVC pin voltage must be returned to 5.5V or lower.

Note 12 After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).

DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope-dependent. Hysteresis is implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRnB:VRnA = `10`.
5. The PDnB:PDnA = `01`, `10` and `11` configurations must have the same current.
6. Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = `10`) and the V_{SS} pin. This is the effective resistance of each resistor ladder. The resistance measurement is one of the resistor ladders measured in parallel.
7. This gain error does not include the offset error.
8. Within 1/2 LSb of the final value, when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device.)
9. Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.
10. Variation of one output voltage to mean output voltage.
11. High-voltage on the $\overline{LAT}$/HVC pin must be limited to the command plus programming time. After the programming cycle, the $\overline{LAT}$/HVC pin voltage must be returned to 5.5V or lower.
12. After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).

1.1 Timing Waveforms and Requirements

1.1.1 WIPER SETTLING TIME

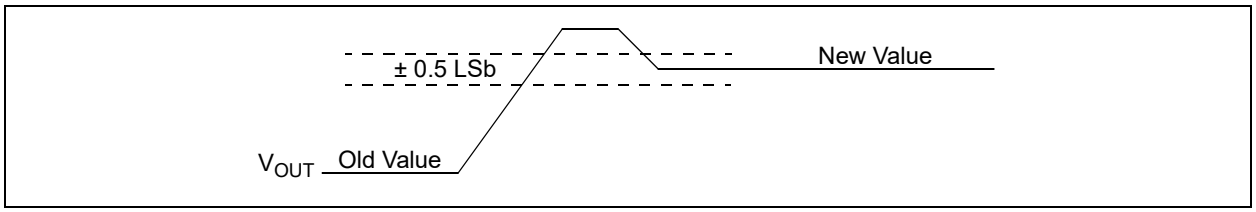


FIGURE 1-1: *V_{OUT} Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges, unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_{OUT} Settling Time (see **C.13, "Settling Time"**)	t_S	—	4	—	µs	12-bit	Code = 400h → C00h; C00h → 400h **(2)**

Note 2 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR.

1.1.2 LATCH PIN ($\overline{LAT}$) TIMING

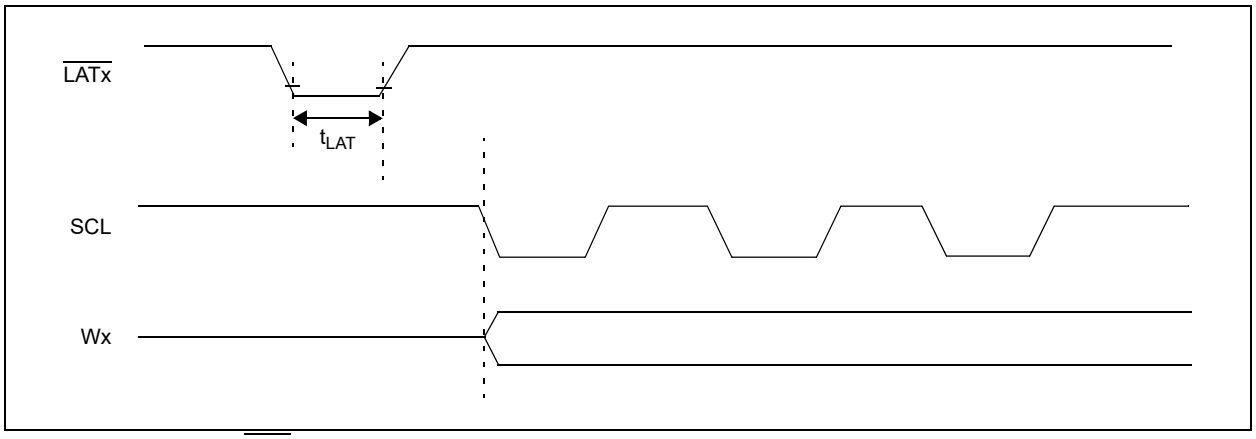


FIGURE 1-2: *$\overline{LAT}$ Pin Waveforms.*

TABLE 1-2: $\overline{LAT}$ PIN TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges, unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, RL = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
$\overline{LATx}$ Pin Pulse Width	t_{LAT}	20	—	—	ns	

1.2 I²C Mode Timing Waveforms and Requirements

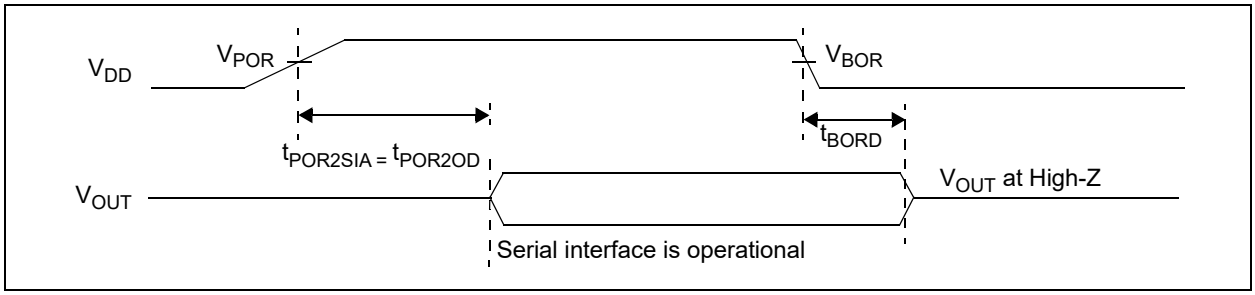


FIGURE 1-3: *Power-on and Brown-out Reset Waveforms.*

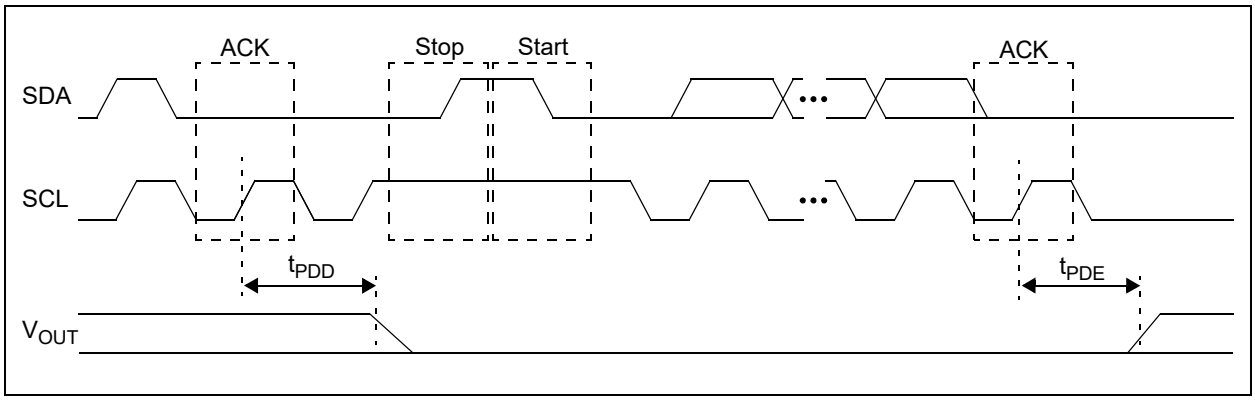


FIGURE 1-4: *I²C Power-Down Command Timing.*

TABLE 1-3: RESET TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)**: Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges, unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Power-on Reset Delay(10)	$t_{POR2SIA}$	—	—	175	µs	Quad	Monitor the ACK bit response to ensure the device responds to the command.
		—	—	265		Octal	
Brown-out Reset Delay	t_{BORD}	—	30	—	µs	V_{DD} transitions from $V_{DD(MIN)} \rightarrow V_{DD} > V_{POR}$, V_{OUT} driven to V_{OUT} disabled	
Power-Down Output Disable Time Delay	T_{PDD}	—	0.4	—	µs	PDnB:PDnA = 00 → 11, 10 or 01 started from the rising edge of the ACK bit; V_{OUT} = V_{OUT} – 10 mV, V_{OUT} not connected	
Power-Down Output Enable Time Delay	T_{PDE}	—	7	—	µs	PDnB:PDnA = 11, 10, or 01 → 00 started from the rising edge of the ACK bit; Volatile DAC register = FFFh, V_{OUT} = 10 mV, V_{OUT} not connected	

Note 10 Not tested. This parameter is ensured by design.

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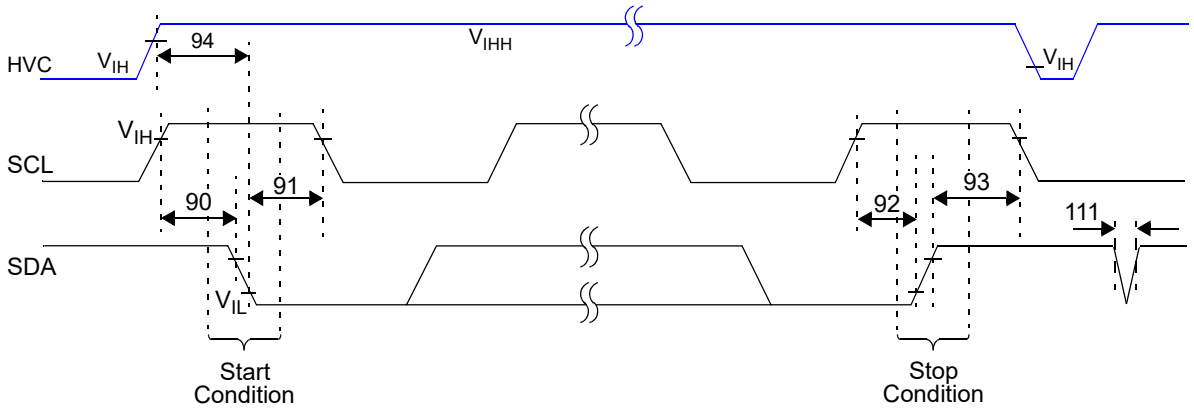

Note 1: The HVC pin must be at V_{IHH} until the MTP write cycle is complete.

FIGURE 1-5: *I^2C Bus Start/Stop Bits and HVC Timing Waveforms.*

TABLE 1-4: I^2C BUS START/STOP BITS AND $\overline{LAT}$ REQUIREMENTS

I^2C AC Characteristics			**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended). The operating voltage range is described in **DC Characteristics**.				
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
—	F_{SCL}	SCL Pin Frequency	Standard mode	0	100	kHz	C_b = 400 pF, 1.8V-5.5V(1)
			Fast mode	0	400	kHz	C_b = 400 pF, 2.7V-5.5V
			High Speed 1.7	0	1.7	MHz	C_b = 400 pF, 4.5V-5.5V(1)
			High Speed 3.4	0	3.4	MHz	C_b = 100 pF, 4.5V-5.5V(1)
90	$T_{SU:STA}$	Start Condition Setup Time (only relevant for a repeated Start condition)	100 kHz mode	4700	—	ns	**Note 1**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	**Note 1**
			3.4 MHz mode	160	—	ns	
91	$T_{HD:STA}$	Start Condition Hold Time (after this period, the first clock pulse is generated)	100 kHz mode	4000	—	ns	**Note 1**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	**Note 1**
			3.4 MHz mode	160	—	ns	
92	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	4000	—	ns	**Note 1**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	**Note 1**
			3.4 MHz mode	160	—	ns	
93	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	4000	—	ns	**Note 1**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	**Note 1**
			3.4 MHz mode	160	—	ns	
94	T_{HVCSU}	HVC High to Start Condition (setup time)		0	—	µs	Not tested, specification ensured by the host

Note 1 Not tested. This parameter is ensured by characterization.

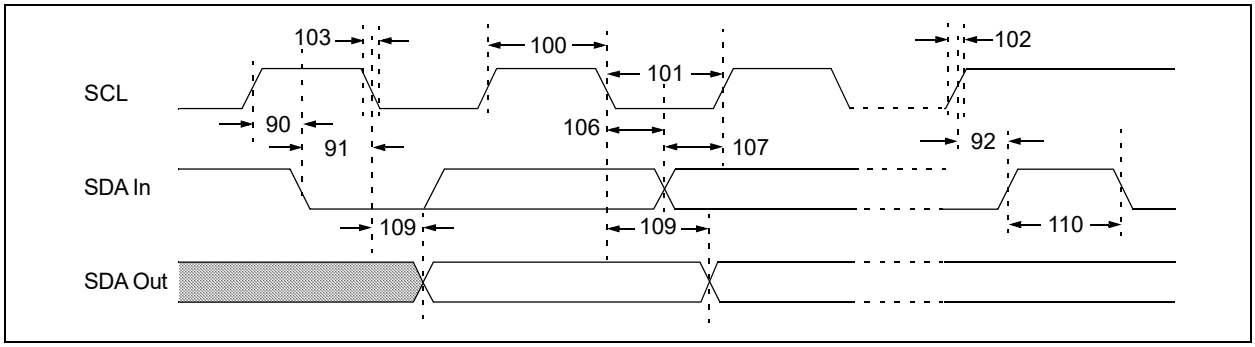

FIGURE 1-6: *I^2C Bus Data Timing Waveforms.*

I^2C BUS REQUIREMENTS (CLIENT MODE)

I^2C AC Characteristics				**Standard Operating Conditions (unless otherwise specified)**: Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended). The operating voltage range is described in **DC Characteristics**.			
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
100	T_{HIGH}	Clock High Time	100 kHz mode	4000	—	ns	1.8V-5.5V(1)
			400 kHz mode	600	—	ns	2.7V-5.5V
			1.7 MHz mode	120	—	ns	4.5V-5.5V(1)
			3.4 MHz mode	60	—	ns	4.5V-5.5V(1)
101	T_{LOW}	Clock Low Time	100 kHz mode	4700	—	ns	1.8V-5.5V(1)
			400 kHz mode	1300	—	ns	2.7V-5.5V
			1.7 MHz mode	320	—	ns	4.5V-5.5V(1)
			3.4 MHz mode	160	—	ns	4.5V-5.5V(1)
102A(10)	T_{RSCL}	SCL Rise Time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1C_b(4)	300	ns	
			1.7 MHz mode	20	80	ns	
			1.7 MHz mode	20	160	ns	After a repeated Start condition or an Acknowledge bit
			3.4 MHz mode	10	40	ns	
			3.4 MHz mode	10	80	ns	After a repeated Start condition or an Acknowledge bit
102B(10)	T_{RSDA}	SDA Rise Time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
103A(10)	T_{FSCL}	SCL Fall Time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	80	ns	
			3.4 MHz mode	10	40	ns	

Note 1 Not tested. This parameter is ensured by characterization.

Note 4 Use Cb in pF for the calculations.

Note 10 Not tested. This parameter is ensured by design.

I²C BUS REQUIREMENTS (CLIENT MODE) (CONTINUED)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended). The operating voltage range is described in DC Characteristics.			
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
103B(10)	T_{FSDA}	SDA Fall Time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
106	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	ns	1.8V-5.5V(1, 5)
			400 kHz mode	0	—	ns	2.7V-5.5V(5)
			1.7 MHz mode	0	—	ns	4.5V-5.5V(1, 5)
			3.4 MHz mode	0	—	ns	4.5V-5.5V(1, 5)
107	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	Notes 1, 6
			400 kHz mode	100	—	ns	Note 6
			1.7 MHz mode	10	—	ns	Notes 1, 6
			3.4 MHz mode	10	—	ns	Notes 1, 6
109	T_{AA}	Output Valid from Clock	100 kHz mode	—	3450	ns	Notes 1, 5, 7, 9
			400 kHz mode	—	900	ns	Notes 5, 7, 9
			1.7 MHz mode	—	310	ns	C_b = 400 pF(1, 9)
			3.4 MHz mode	—	150	ns	C_b = 100 pF(1, 9)
110	T_{BUF}	Bus Free Time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start(1)
			400 kHz mode	1300	—	ns	
			1.7 MHz mode	N.A.	—	ns	
			3.4 MHz mode	N.A.	—	ns	
111	T_{SP}	Input Filter Spike Suppression (SDA and SCL)	100 kHz mode	—	50	ns	NXP Spec states N.A.(1)
			400 kHz mode	—	50	ns	NXP Spec states N.A.
			1.7 MHz mode	—	10	ns	NXP Spec states N.A.(1)
			3.4 MHz mode	—	10	ns	NXP Spec states N.A.(1)

Note 1 Not tested. This parameter is ensured by characterization.

Note 4 Use Cb in pF for the calculations.

Note 5 A host transmitter must provide a delay to ensure that the difference between SDA and SCL fall times does not unintentionally create a Start or a Stop condition.

Note 6 A Fast mode (400 kHz) I²C bus device can be used in a standard mode (100 kHz) I²C bus system, but the requirement, $t_{SU:DAT} \geq 250$ ns, must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line, T_R max.+ $t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.

Note 7 As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

Note 8 Ensured by the T_{AA} 3.4 MHz specification test.

Note 9 The specification is not part of the I²C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or T_{RSDA}).

Note 10 Not tested. This parameter is ensured by design.

Timing Notes:

1. Not tested. This parameter is ensured by characterization.
2. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR.
3. The transition of the $\overline{LAT}$ signal, between 10 ns before the rising edge (Spec 94) and 250 ns after the rising edge (Spec 95) of the SCL signal, is indeterminate whether the change in V_{OUT} is delayed or not.
4. Use C_b in pF for the calculations.
5. A host transmitter must provide a delay to ensure that the difference between SDA and SCL fall times does not unintentionally create a Start or a Stop condition.
6. A Fast mode (400 kHz) I^2C bus device can be used in a standard mode (100 kHz) I^2C bus system, but the requirement, $t_{SU:DAT} \geq 250$ ns, must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line, T_R max.+ $t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
7. As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
8. Ensured by the T_{AA} 3.4 MHz specification test.
9. The specification is not part of the I^2C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or T_{RSDA}).
10. Not tested. This parameter is ensured by design.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 20L-TSSOP	θ_{JA}	—	90	—	°C/W	
Thermal Resistance, 20L-QFN (4 x 4)	θ_{JA}	—	30	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

2.1 Device Currents

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

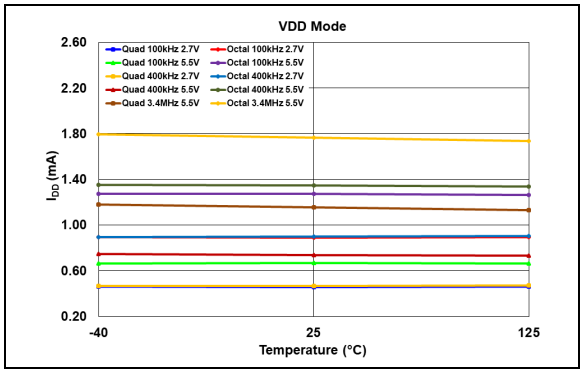

FIGURE 2-1: *Average Supply Current vs. F_{SCL} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA =* `00`.

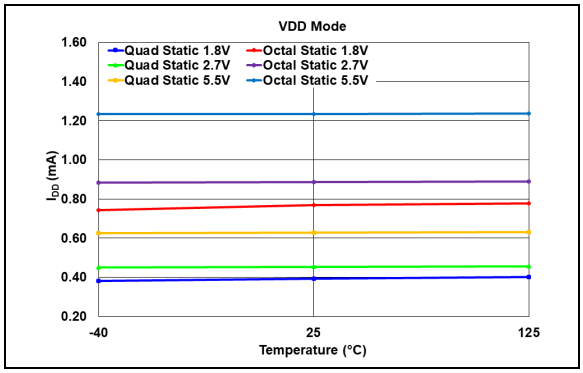

FIGURE 2-4: *Average Supply Current vs. Voltage and Temperature – Inactive Interface (SCL = V_{IH} or V_{IL}), VRnB:VRnA =* `00`.

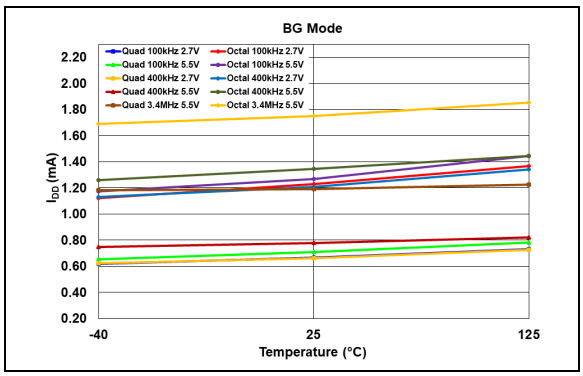

FIGURE 2-2: *Average Supply Current vs. F_{SCL} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA =* `01`.

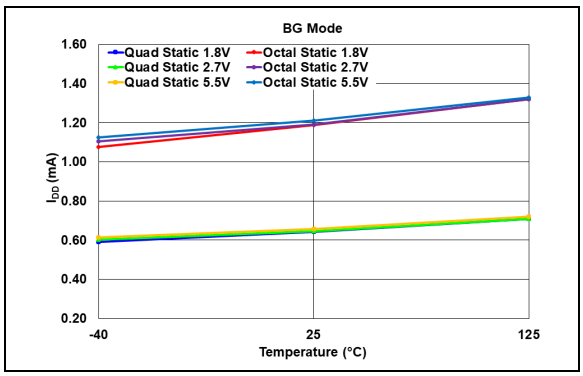

FIGURE 2-5: *Average Supply Current – Inactive Interface (SCL = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA =* `01`.

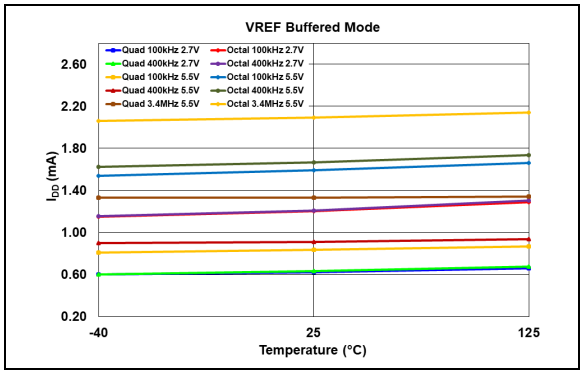

FIGURE 2-3: *Average Supply Current vs. F_{SCL} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA =* `11`.

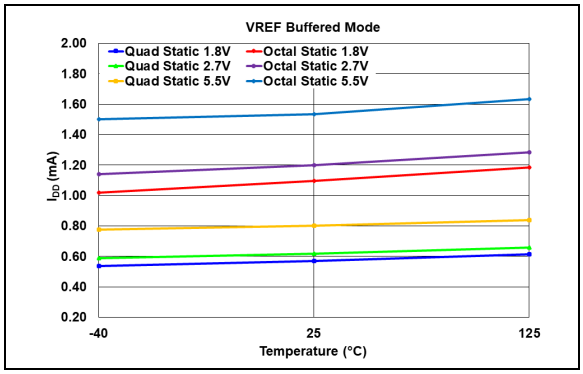

FIGURE 2-6: *Average Supply Current – Inactive Interface (SCL = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA =* `11`.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

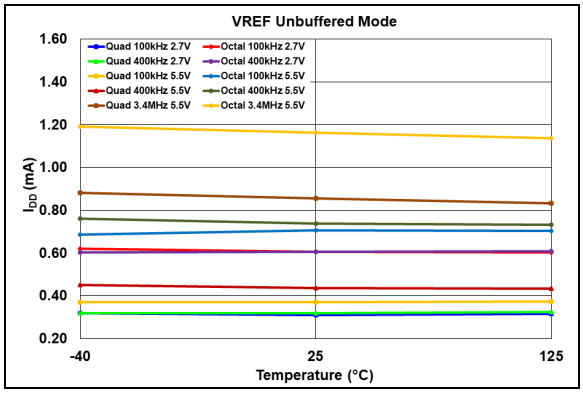

FIGURE 2-7: *Average Device Supply Current vs. F_{SCL} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA =* `10`*.*

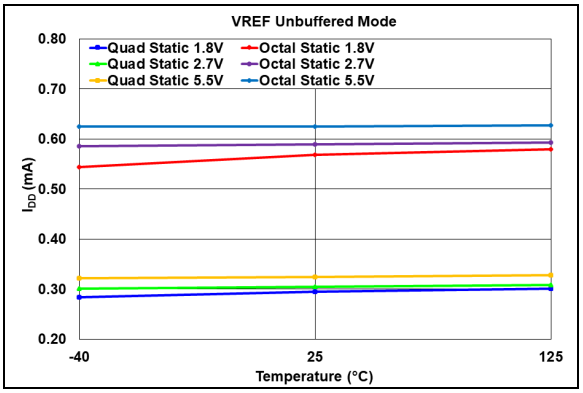

FIGURE 2-9: *Average Device Supply vs. Voltage and Temperature Current – Inactive Interface (SCL = V_{IH} or V_{IL}), VRnB:VRnA =* `10`*.*

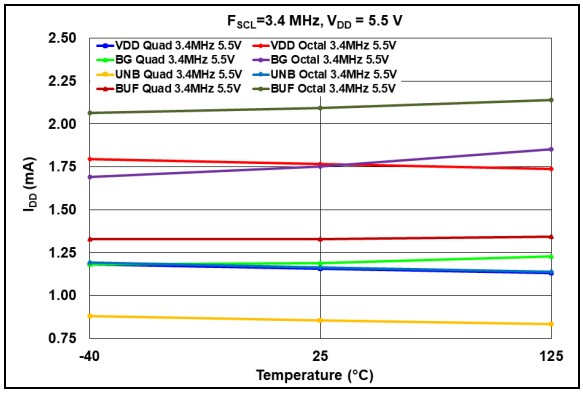

FIGURE 2-8: *Average Device Supply Active Current (I_{DDA}) vs. Temperature and DAC Reference Voltage Mode, V_{DD} = 5.5V and F_{SCL} = 3.4 MHz.*

2.2 Linearity Data

2.2.1 TOTAL UNADJUSTED ERROR (TUE) – MCP47CXB2X (12-BIT), VRnB:VRnA = 10, $V_{REF} = V_{DD}$, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

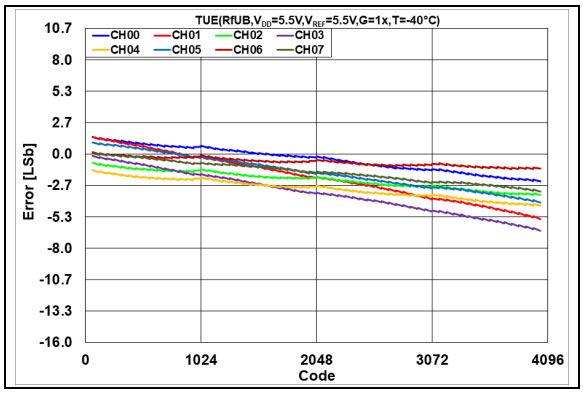

FIGURE 2-10: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

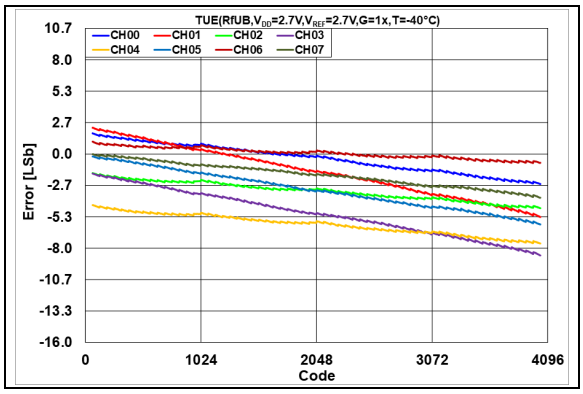

FIGURE 2-13: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

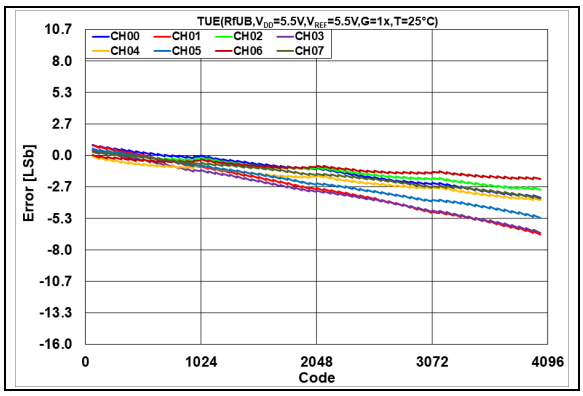

FIGURE 2-11: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

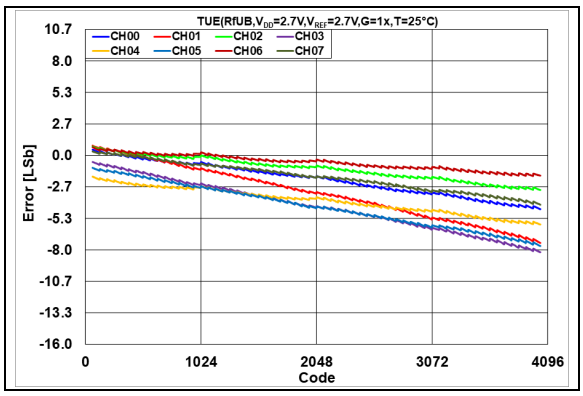

FIGURE 2-14: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

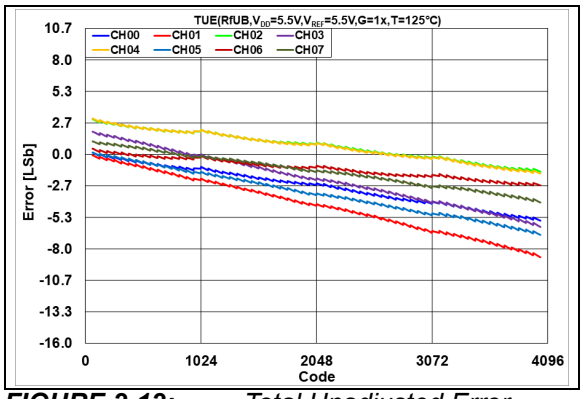

FIGURE 2-12: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

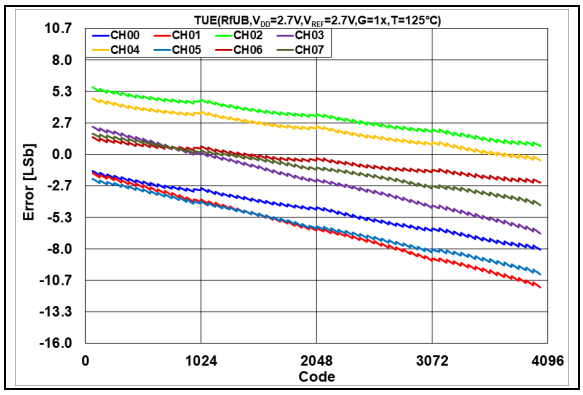

FIGURE 2-15: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

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Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

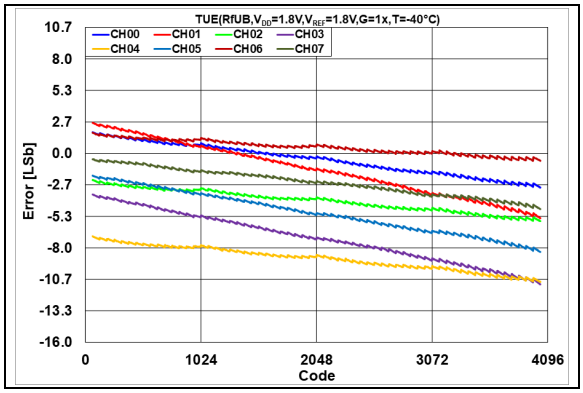

FIGURE 2-16: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

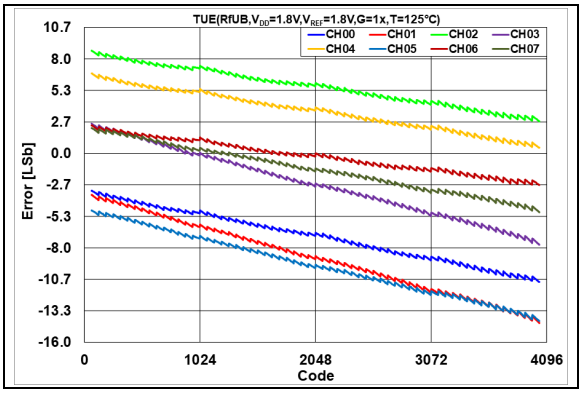

FIGURE 2-18: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

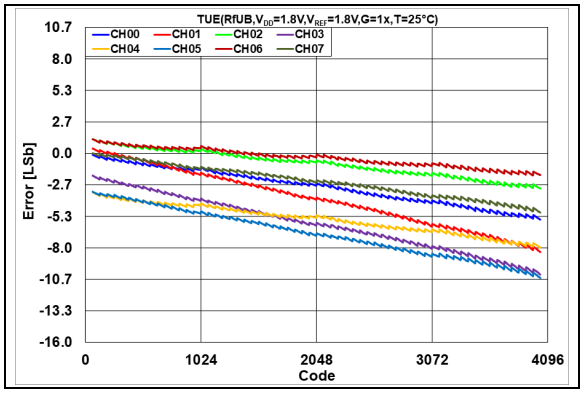

FIGURE 2-17: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

2.2.2 INTEGRAL NONLINEARITY (INL) – MCP47CXB2X (12-BIT), VRnB:VRnA = 10, $V_{REF} = V_{DD}$, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

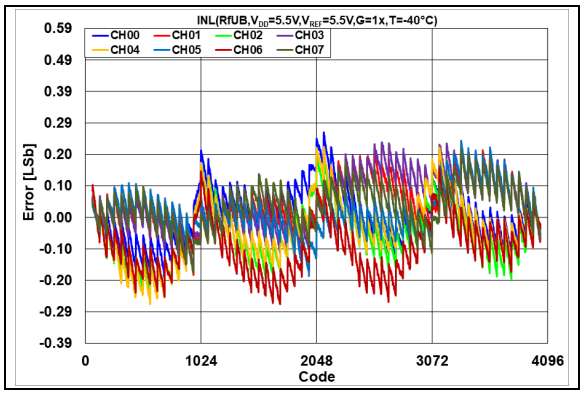

FIGURE 2-19: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

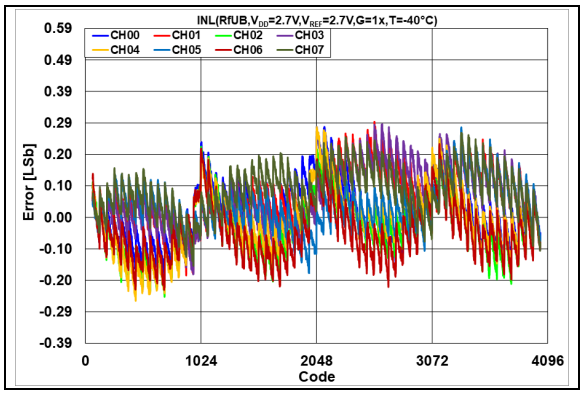

FIGURE 2-22: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

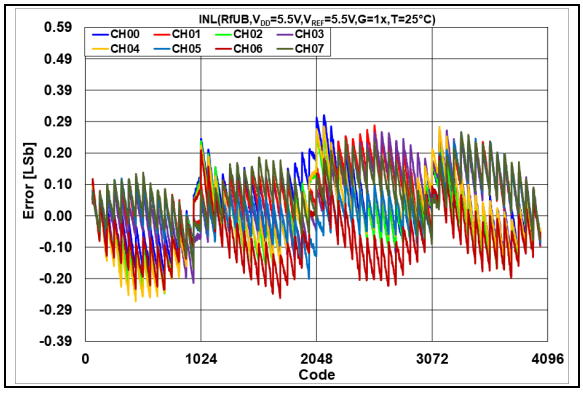

FIGURE 2-20: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

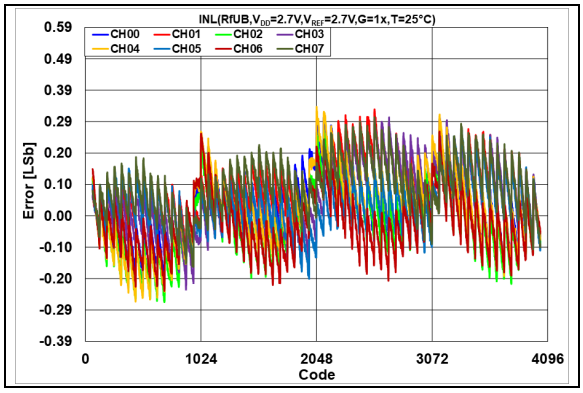

FIGURE 2-23: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

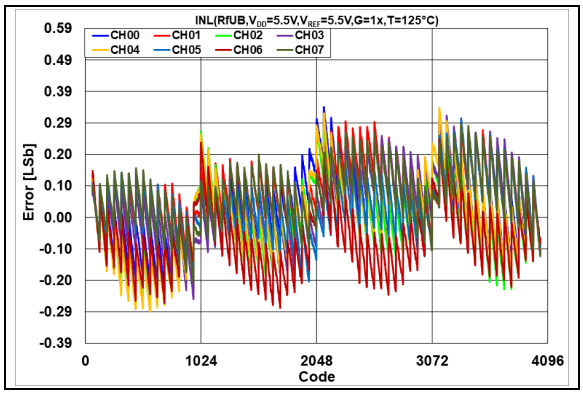

FIGURE 2-21: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

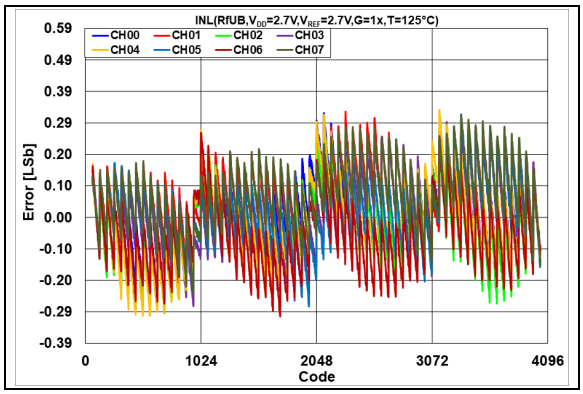

FIGURE 2-24: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

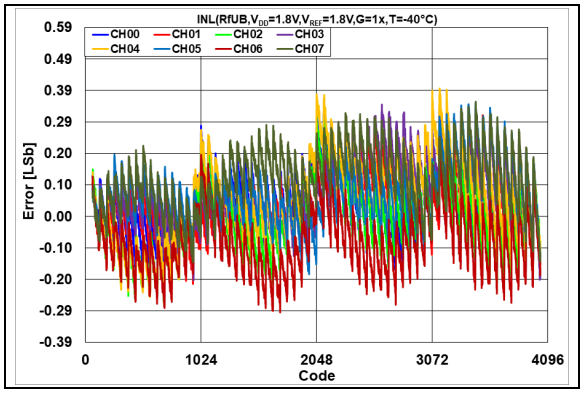

FIGURE 2-25: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

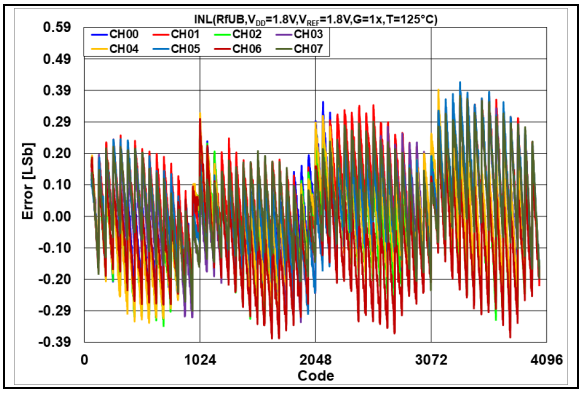

FIGURE 2-27: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

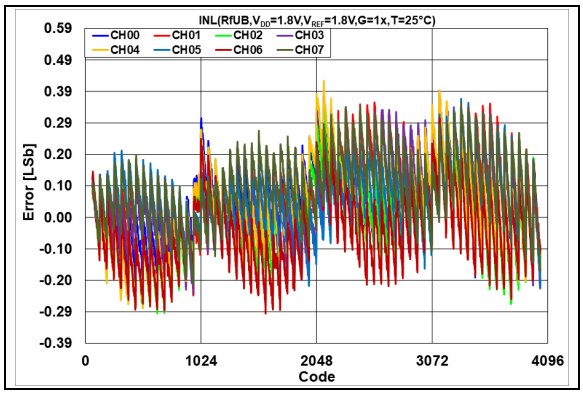

FIGURE 2-26: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

2.2.3 DIFFERENTIAL NONLINEARITY (DNL) – MCP47CXB2X (12-BIT), VRnB:VRnA = 10, $V_{REF} = V_{DD}$, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

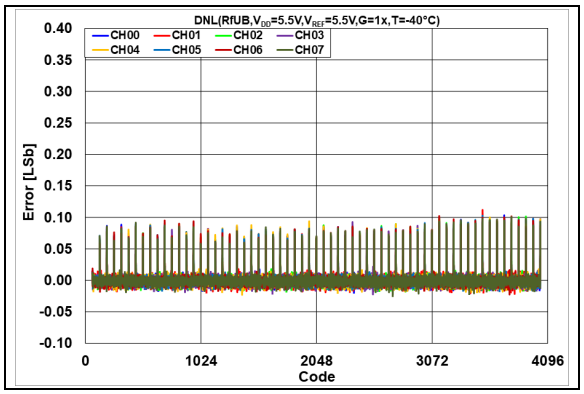

FIGURE 2-28: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

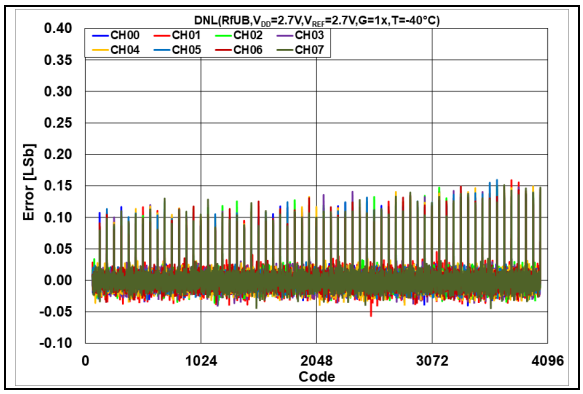

FIGURE 2-31: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

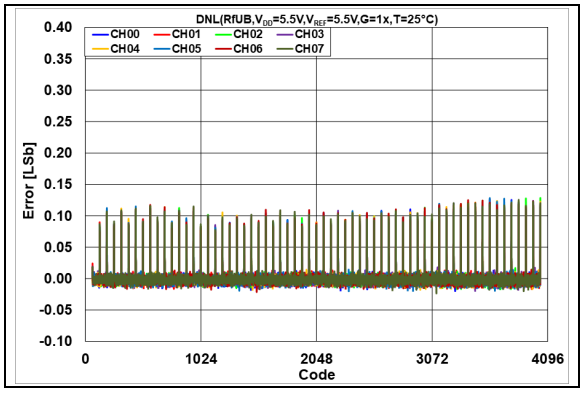

FIGURE 2-29: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

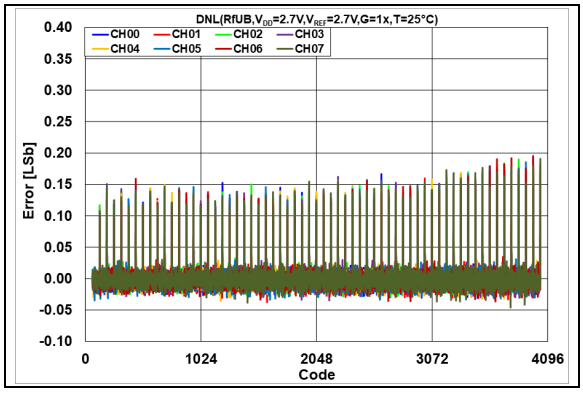

FIGURE 2-32: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

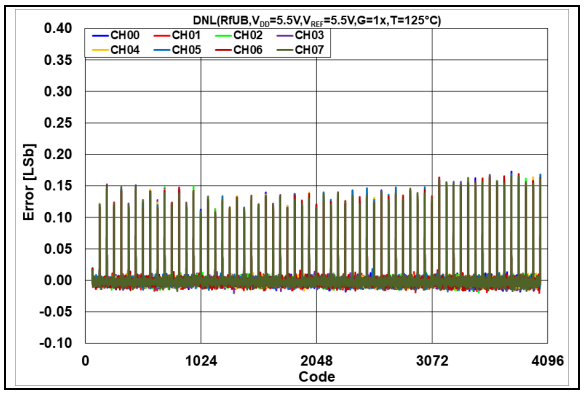

FIGURE 2-30: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

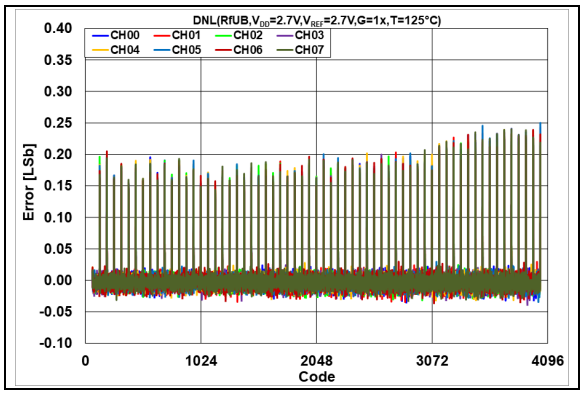

FIGURE 2-33: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

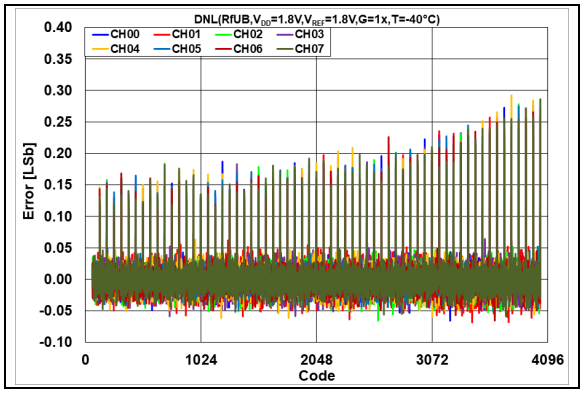

FIGURE 2-34: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

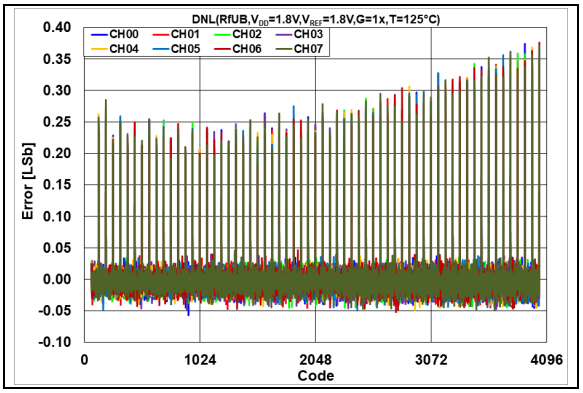

FIGURE 2-36: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

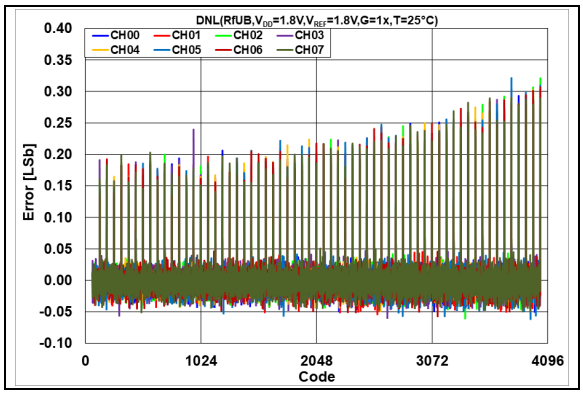

FIGURE 2-35: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

2.2.4 TOTAL UNADJUSTED ERROR (TUE) – MCP47CXB2X (12-BIT), VRnB:VRnA = 10, V_{REF} = 0.5 x V_{DD}, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

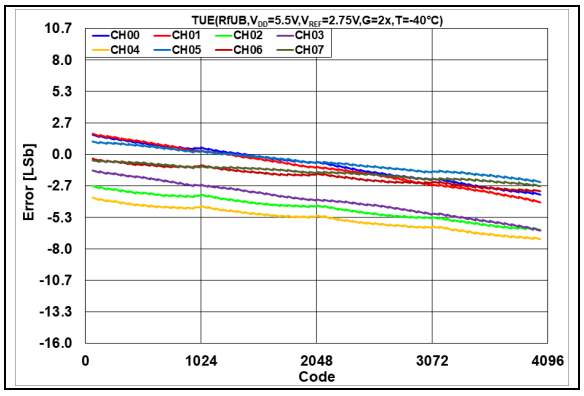

FIGURE 2-37: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = -40°C.*

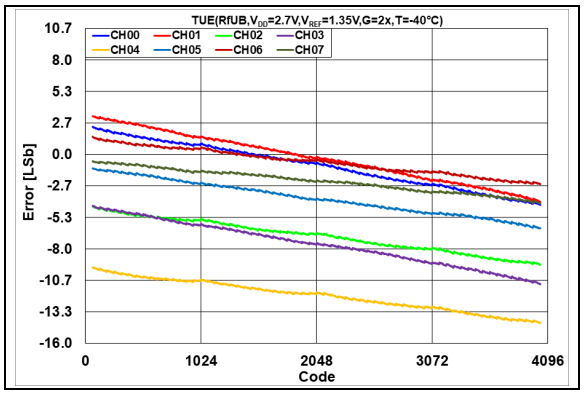

FIGURE 2-40: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = -40°C.*

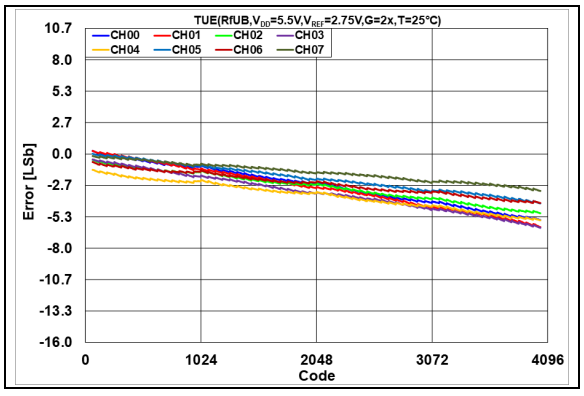

FIGURE 2-38: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +25°C.*

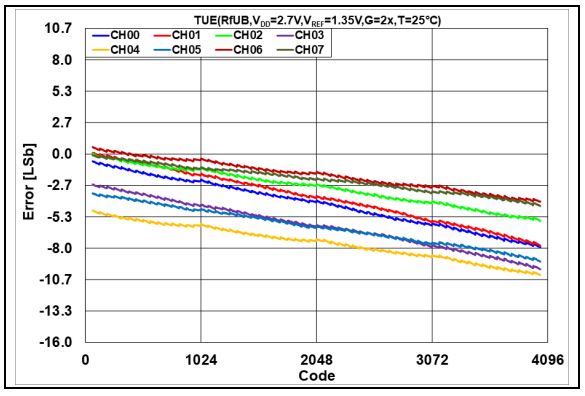

FIGURE 2-41: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +25°C.*

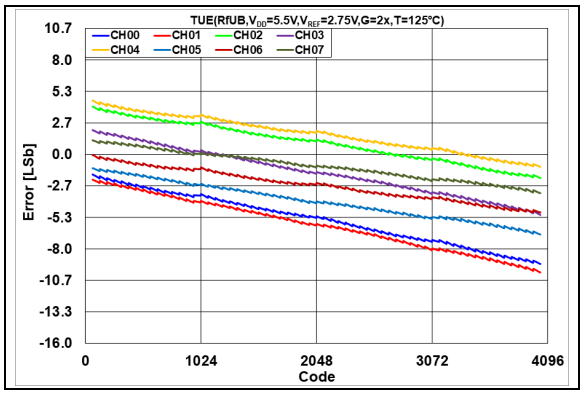

FIGURE 2-39: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +125°C.*

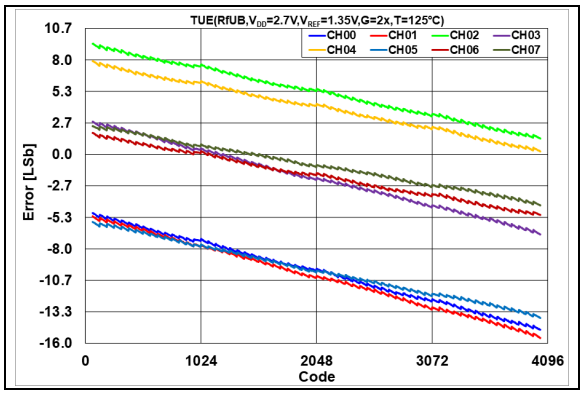

FIGURE 2-42: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +125°C.*

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2.2.5 INTEGRAL NONLINEARITY (INL) – MCP47CXB2X (12-BIT), VRnB:VRnA = 10, V_{REF} = 0.5 x V_{DD}, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

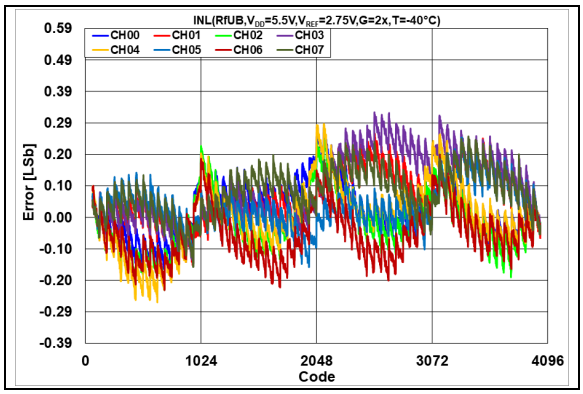

FIGURE 2-43: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = -40°C.*

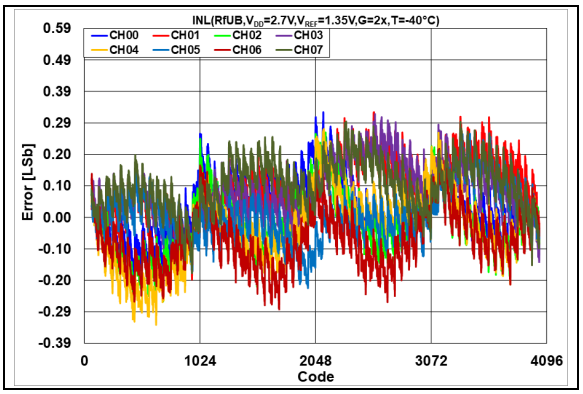

FIGURE 2-46: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = -40°C.*

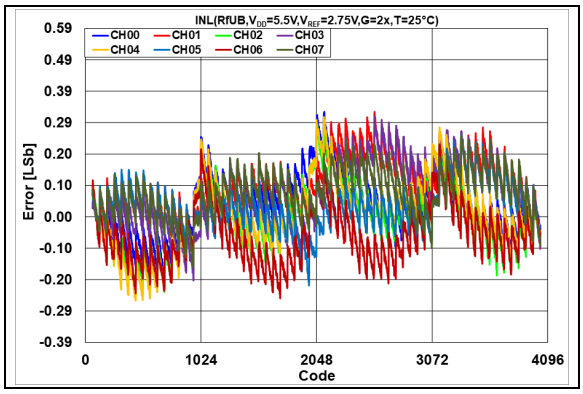

FIGURE 2-44: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +25°C.*

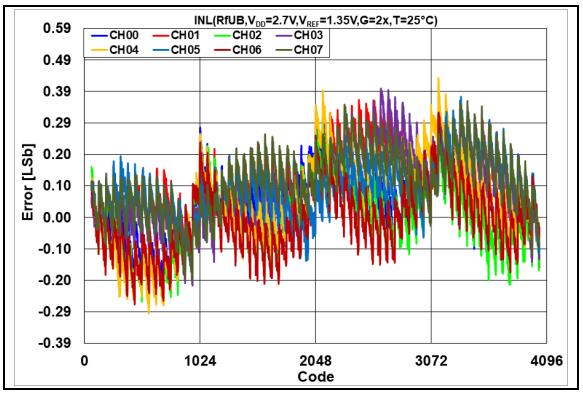

FIGURE 2-47: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +25°C.*

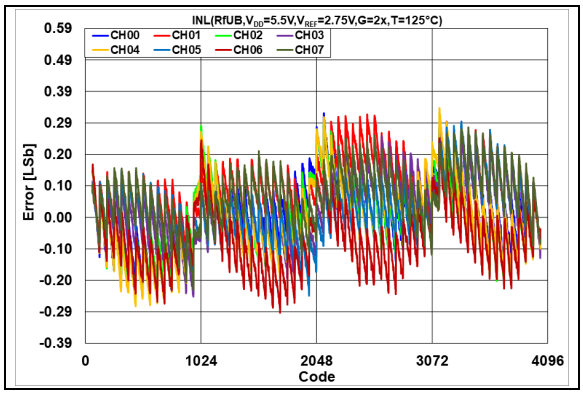

FIGURE 2-45: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +125°C.*

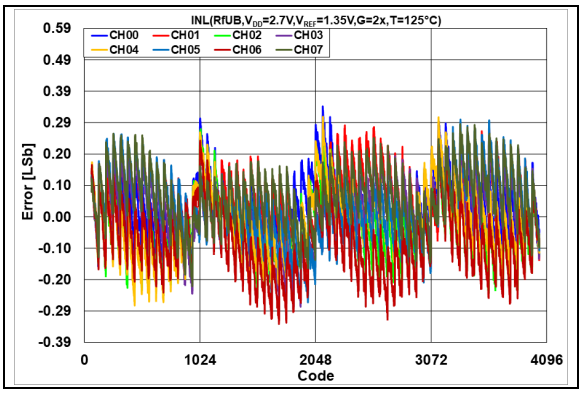

FIGURE 2-48: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +125°C.*

2.2.6 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP47CXB2X (12-BIT), VRnB:VRnA = 10, V_{REF} = 0.5 x V_{DD}, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

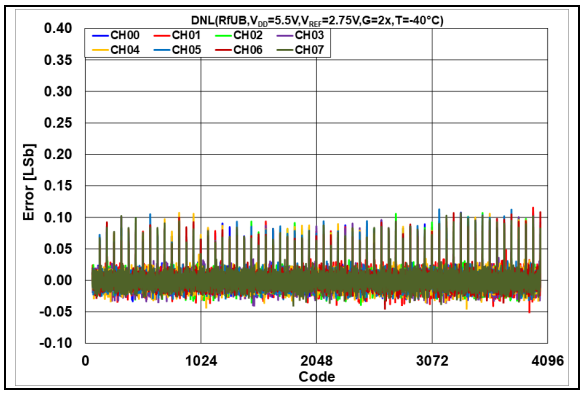

FIGURE 2-49: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = -40°C.*

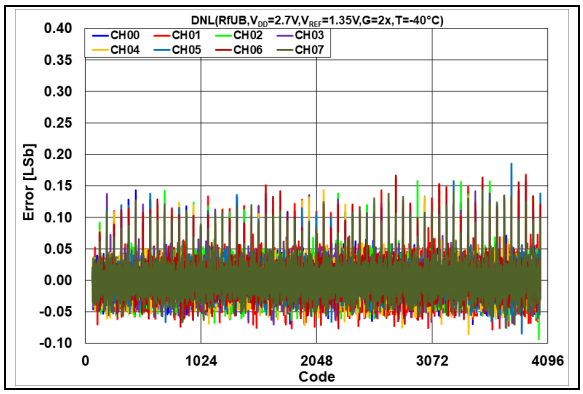

FIGURE 2-52: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +125°C.*

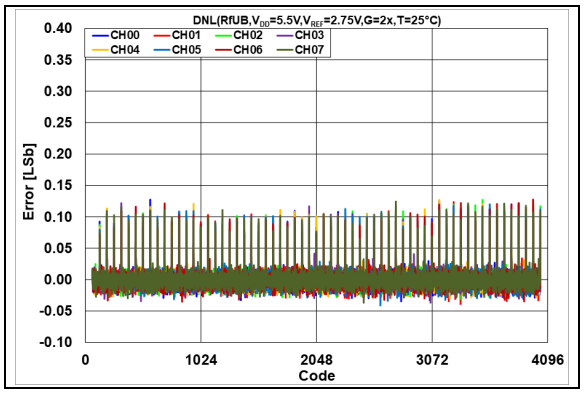

FIGURE 2-50: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +25°C.*

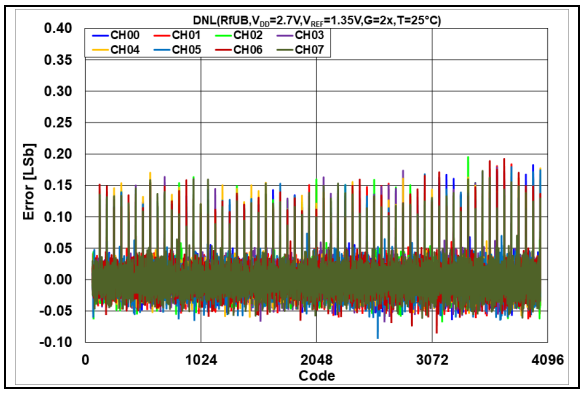

FIGURE 2-53: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +25°C.*

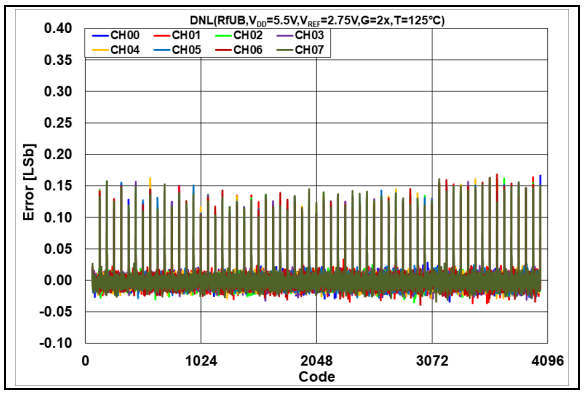

FIGURE 2-51: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +125°C.*

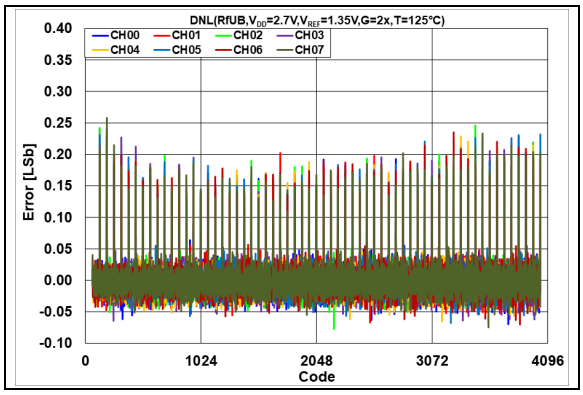

FIGURE 2-54: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +125°C.*

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2.2.7 TOTAL UNADJUSTED ERROR (TUE) – MCP47CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

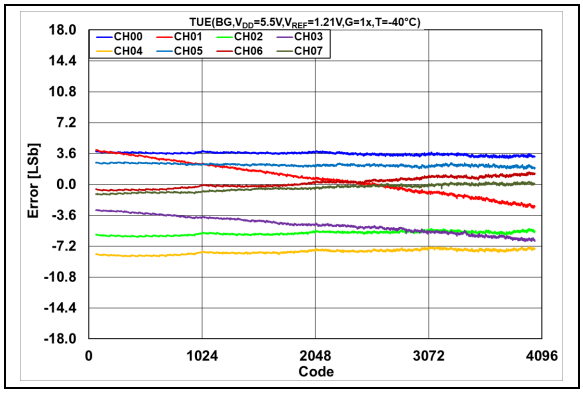

FIGURE 2-55: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

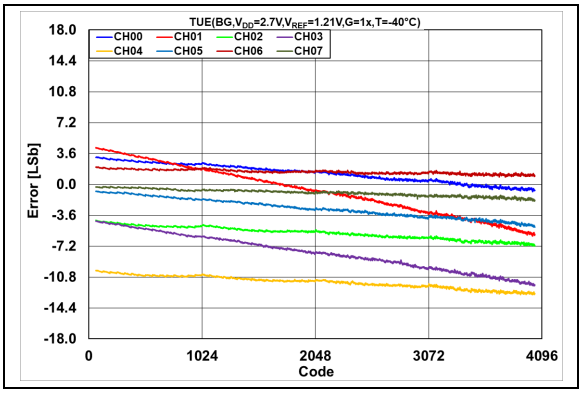

FIGURE 2-58: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

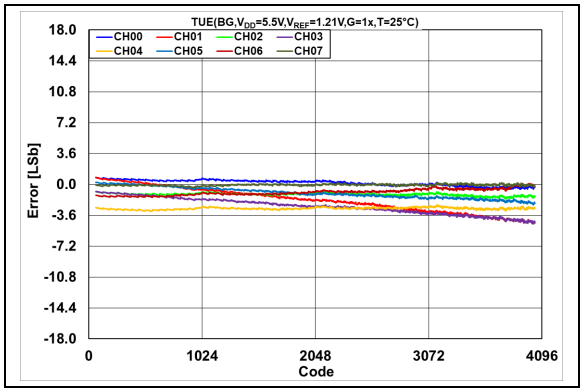

FIGURE 2-56: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

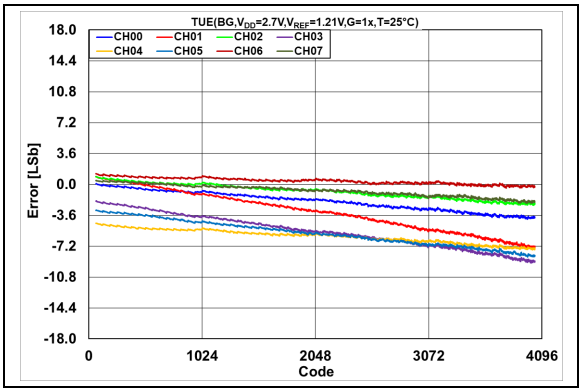

FIGURE 2-59: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

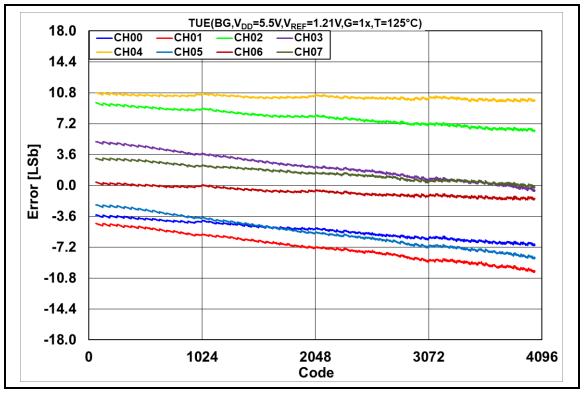

FIGURE 2-57: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

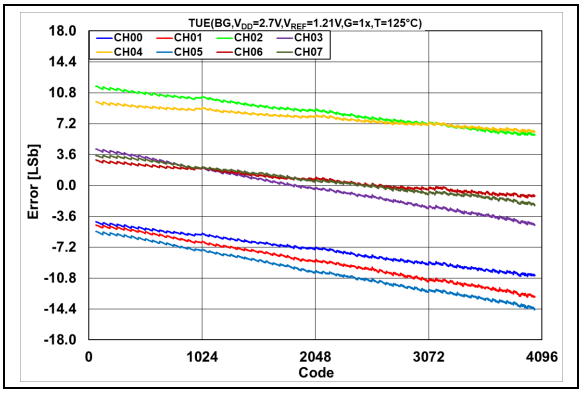

FIGURE 2-60: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

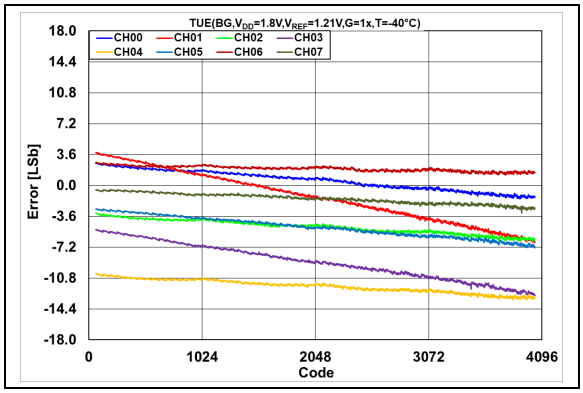

FIGURE 2-61: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

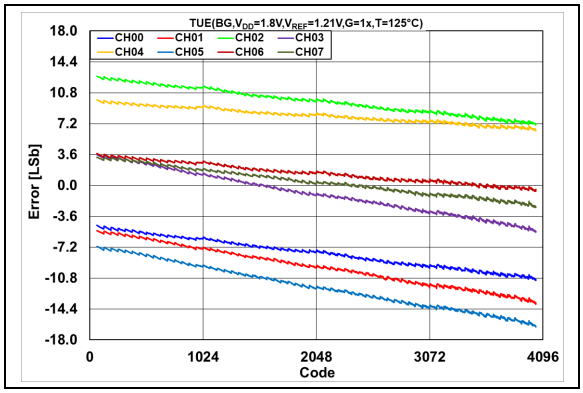

FIGURE 2-63: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

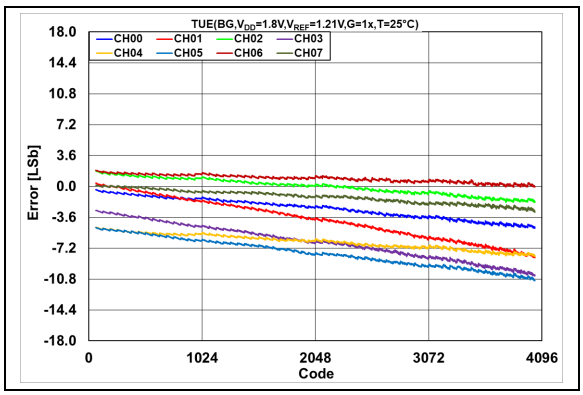

FIGURE 2-62: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

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2.2.8 TOTAL UNADJUSTED ERROR (TUE) – MCP47CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

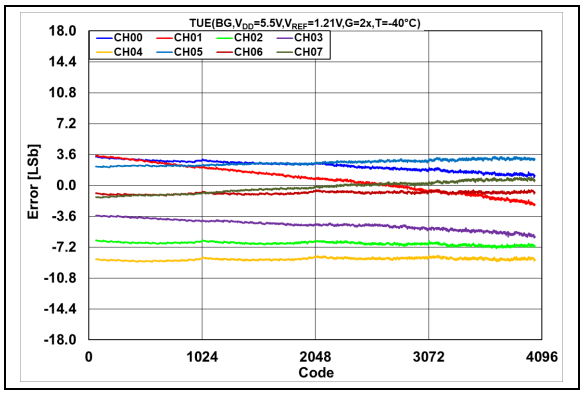

FIGURE 2-64: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

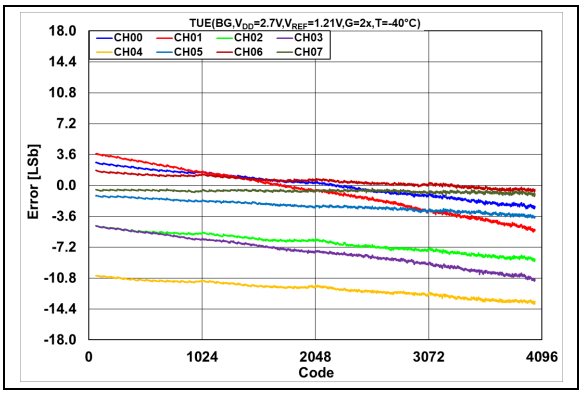

FIGURE 2-67: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

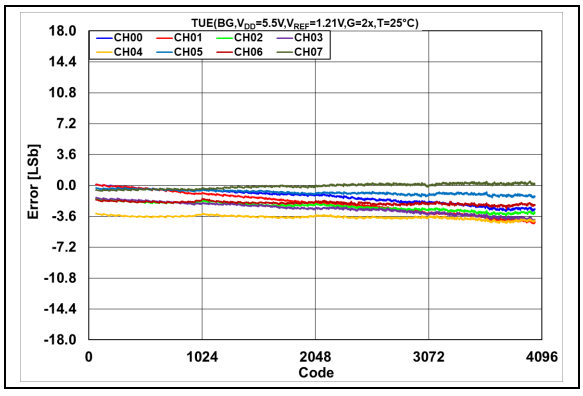

FIGURE 2-65: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

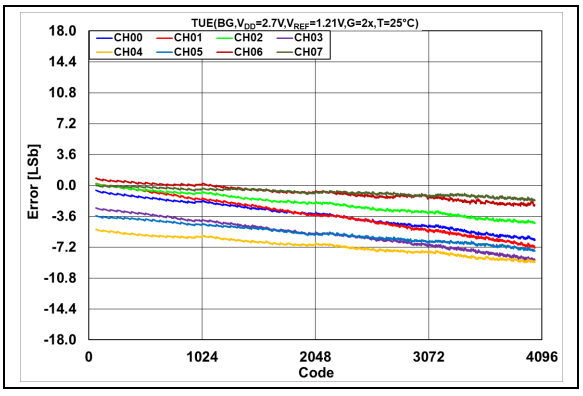

FIGURE 2-68: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

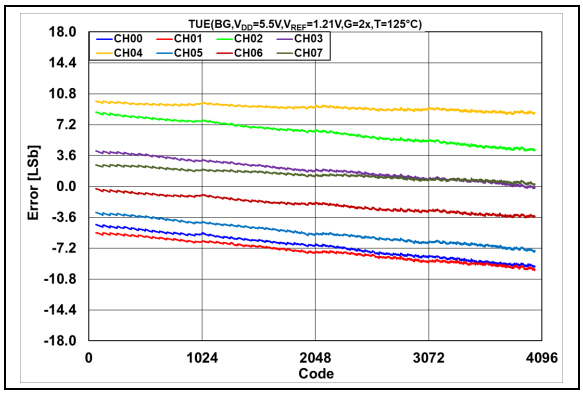

FIGURE 2-66: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

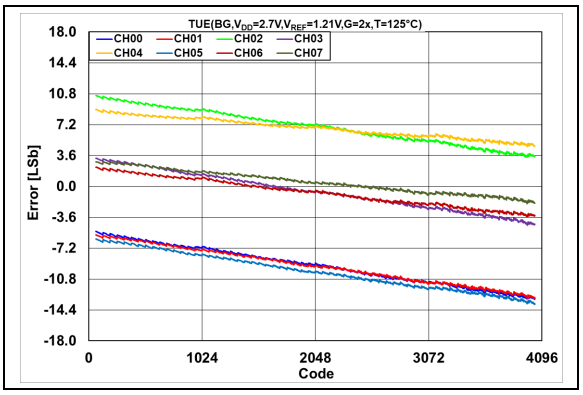

FIGURE 2-69: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

2.2.9 INTEGRAL NONLINEARITY ERROR (INL) – MCP47CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

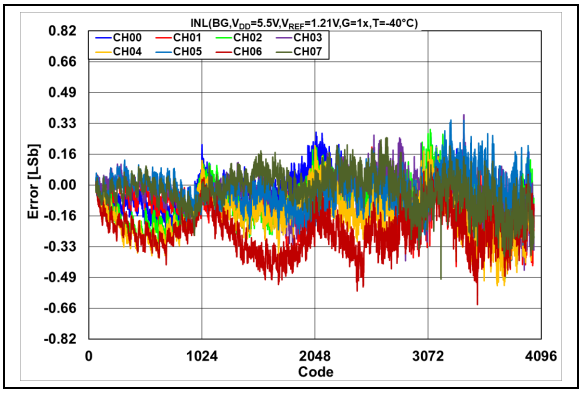

FIGURE 2-70: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

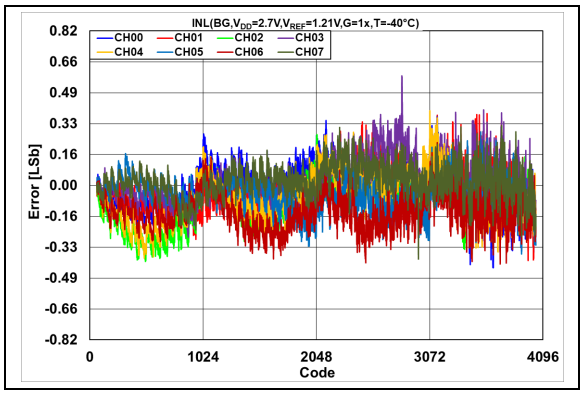

FIGURE 2-73: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

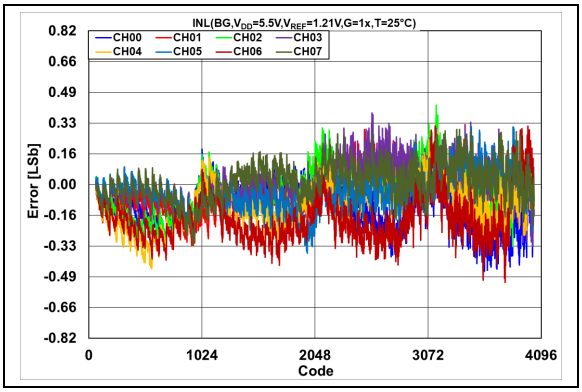

FIGURE 2-71: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

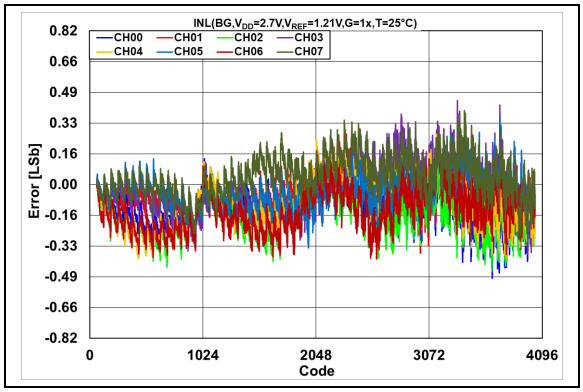

FIGURE 2-74: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

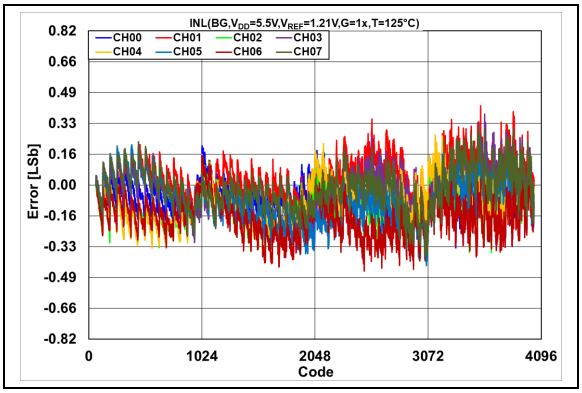

FIGURE 2-72: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

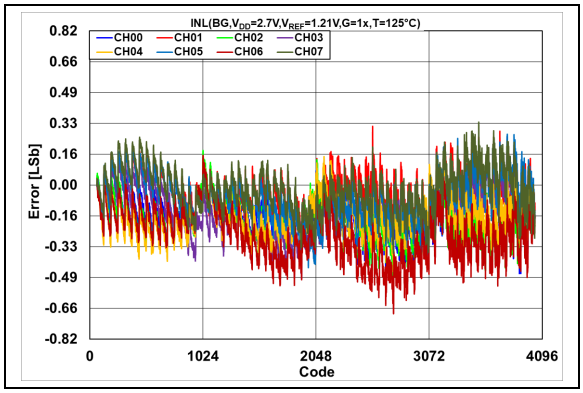

FIGURE 2-75: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

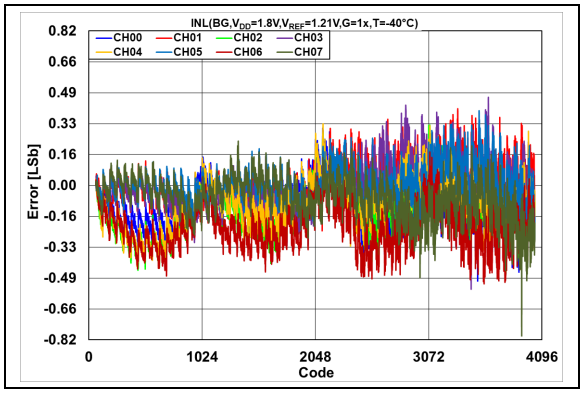

FIGURE 2-76: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

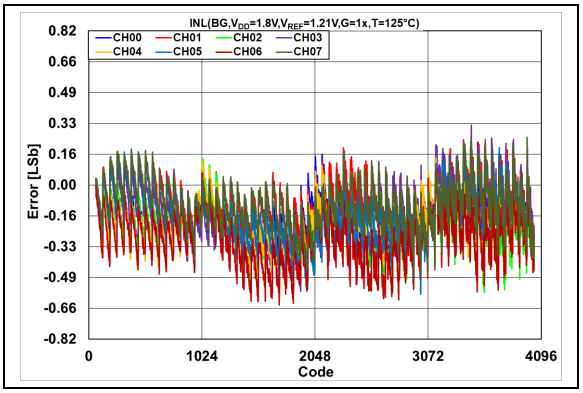

FIGURE 2-78: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

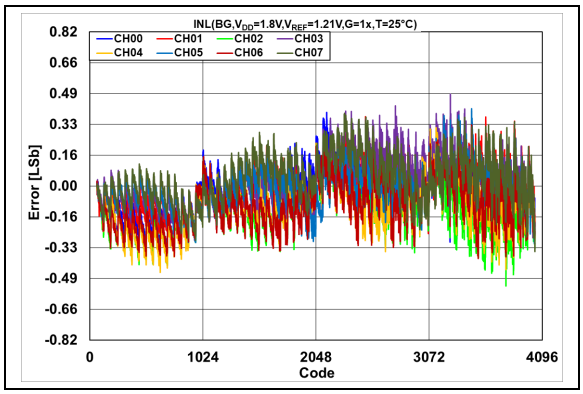

FIGURE 2-77: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

2.2.10 INTEGRAL NONLINEARITY ERROR (INL) – MCP47CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

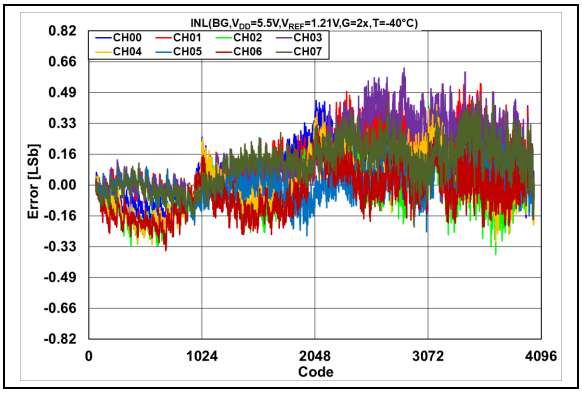

FIGURE 2-79: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

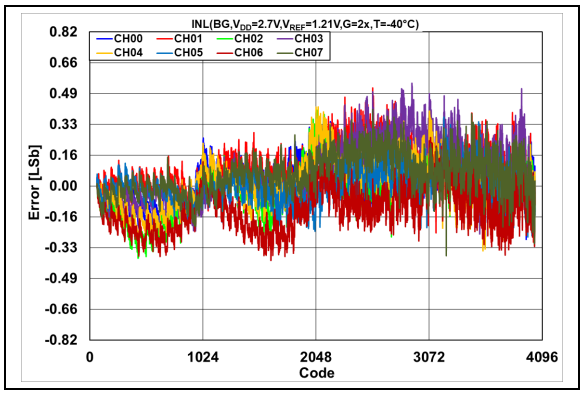

FIGURE 2-82: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

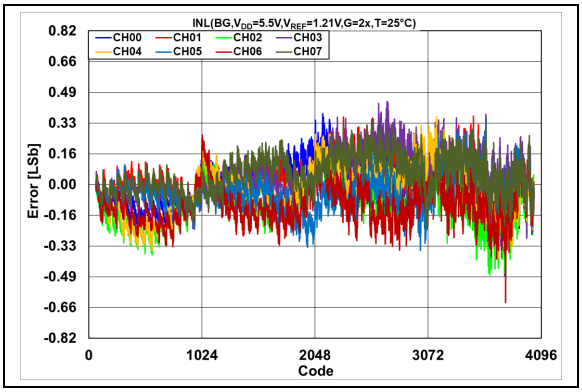

FIGURE 2-80: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

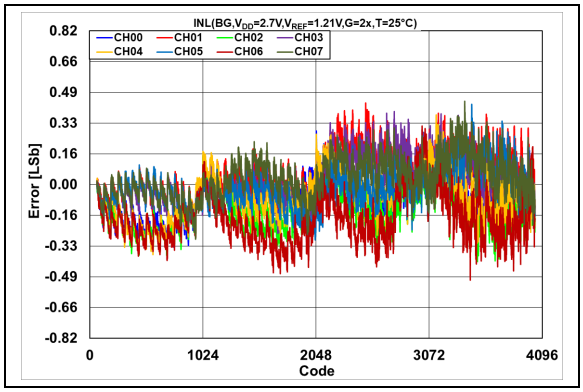

FIGURE 2-83: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

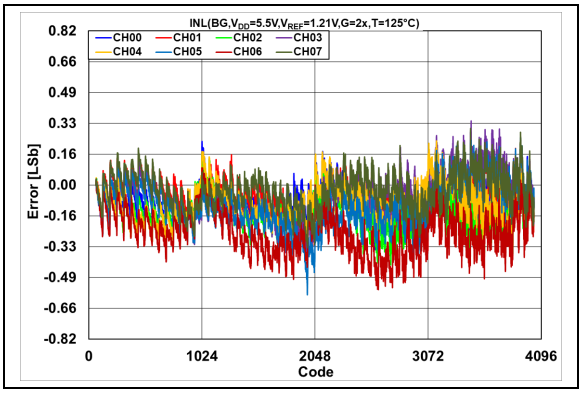

FIGURE 2-81: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

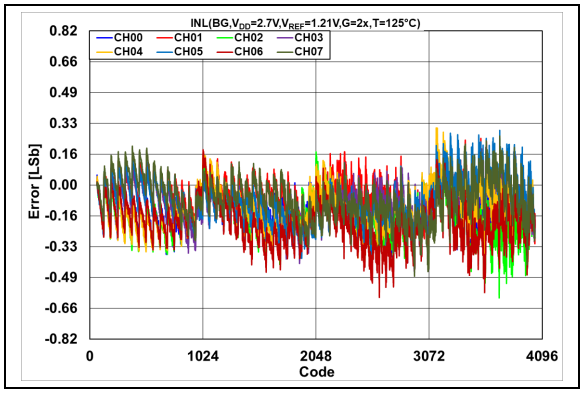

FIGURE 2-84: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

2.2.11 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP47CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

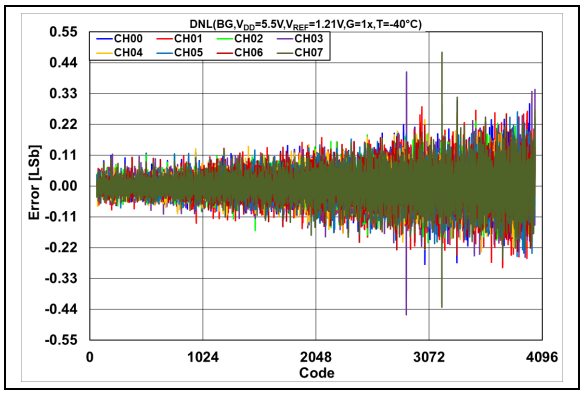

FIGURE 2-85: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

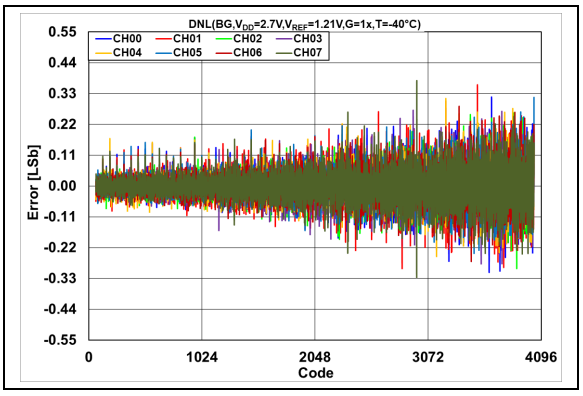

FIGURE 2-88: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

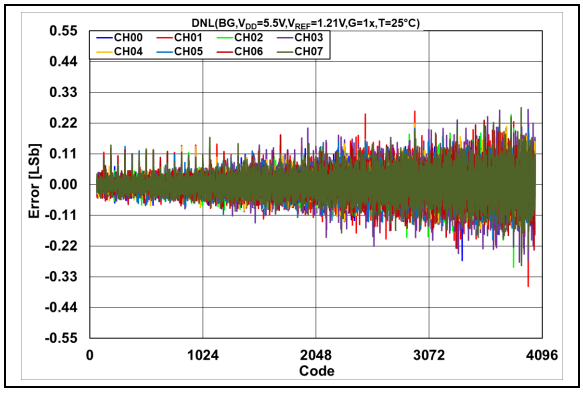

FIGURE 2-86: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

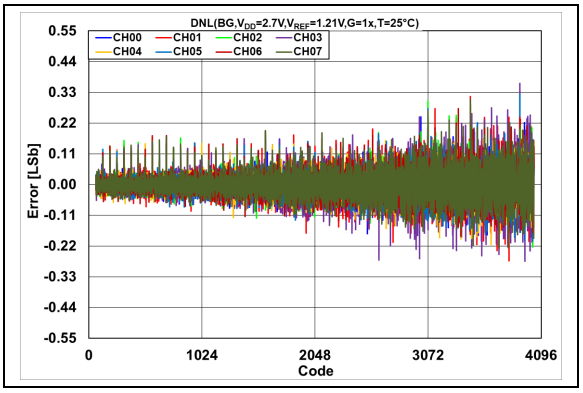

FIGURE 2-89: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

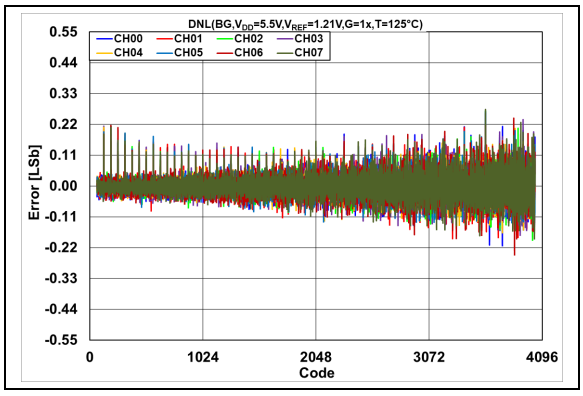

FIGURE 2-87: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

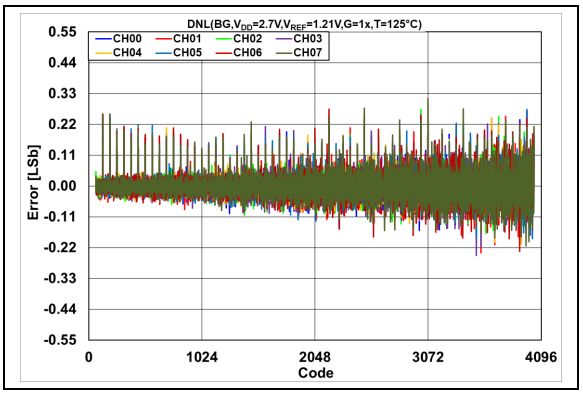

FIGURE 2-90: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

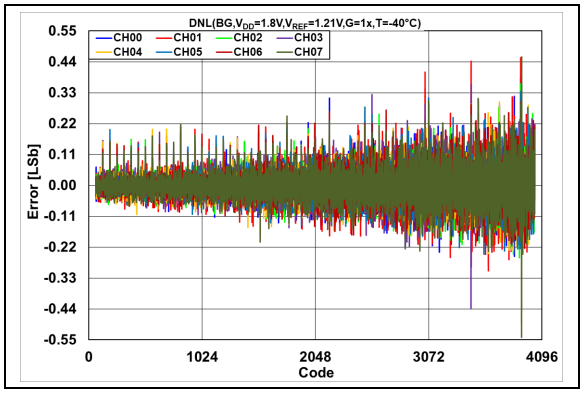

FIGURE 2-91: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

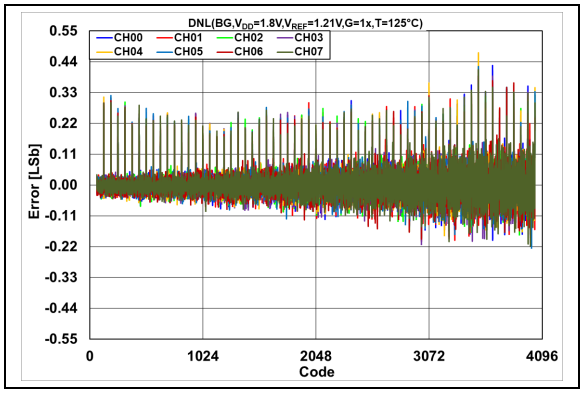

FIGURE 2-93: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

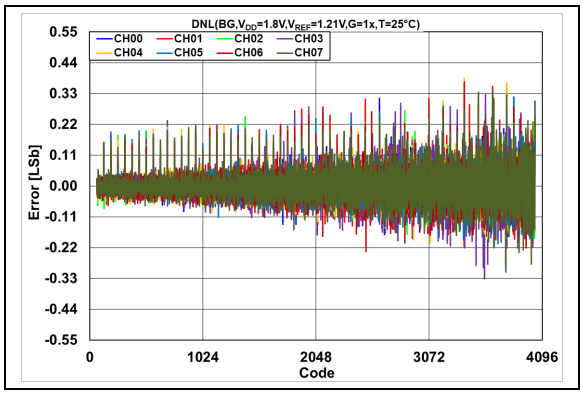

FIGURE 2-92: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

MCP47CXBX4/8

2.2.12 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP47CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

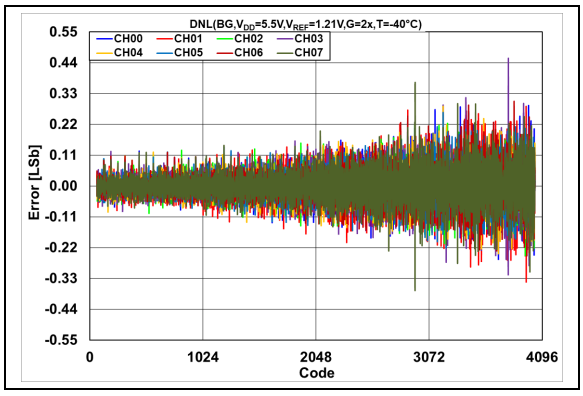

FIGURE 2-94: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

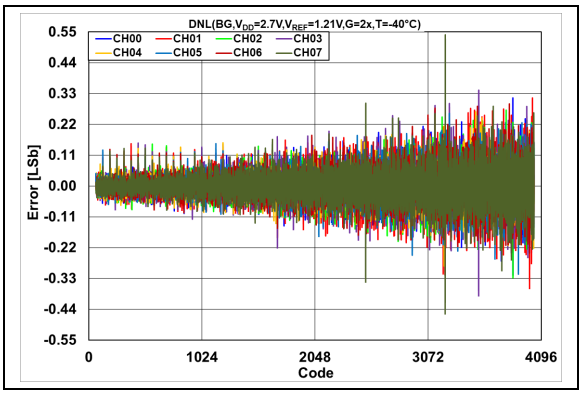

FIGURE 2-97: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

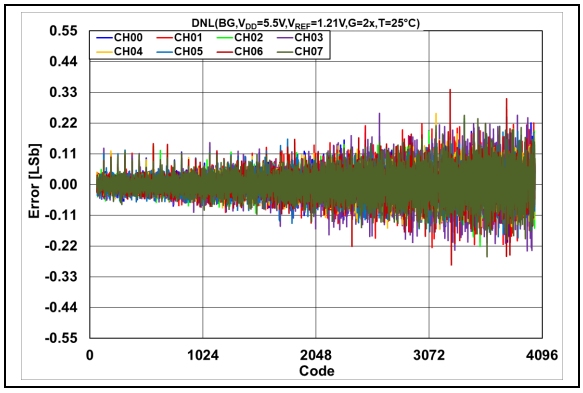

FIGURE 2-95: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

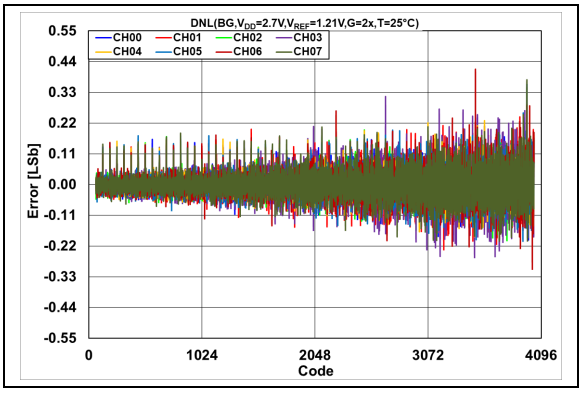

FIGURE 2-98: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

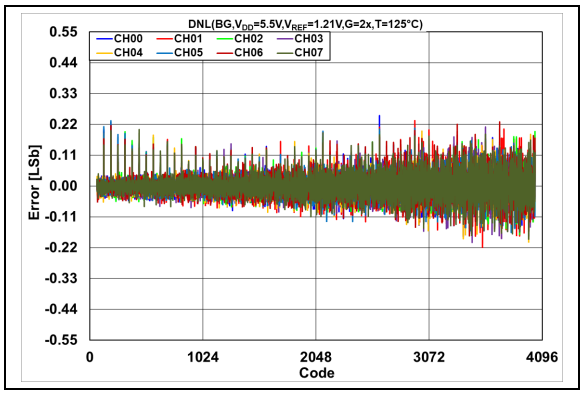

FIGURE 2-96: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

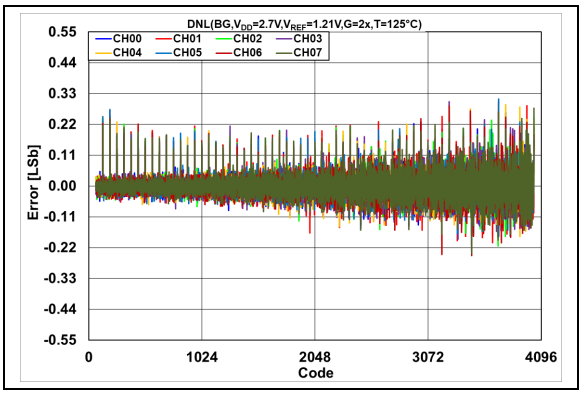

FIGURE 2-99: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

3.0 PIN DESCRIPTIONS

Overviews of the pin functions are provided in **Section 3.1, "Positive Power Supply Input (VDD)"** through **Section 3.9, "I²C Client Address Pins (A0, A1)"**.

The descriptions of the pins for the quad-DAC output devices are listed in Table 3-1 and descriptions for the octal-DAC output devices are listed in Table 3-2.

TABLE 3-1: MCP47CXBX4 (QUAD-DAC) PIN FUNCTION TABLE

Pin		Symbol	I/O	Buffer Type	Description
20-Lead TSSOP	20-Lead QFN				
1	19	$\overline{LAT1}$	I	ST	DAC Register Latch 1 Pin. The Latch 1 pin allows the values in the volatile DAC1/DAC3 registers to be transferred to the V_{OUT1}/ V_{OUT3} output pins.
2	20	V_{DD}	—	P	Supply Voltage Pin
3	1	A0	I	ST	I²C Client Address Bit 0 Pin
4	2	V_{REF0}	A	A	Voltage Reference Input 0 Pin
5	3	V_{OUT0}	A	A	Buffered Analog Voltage Output – Channel 0 Pin
6	4	V_{OUT2}	A	A	Buffered Analog Voltage Output – Channel 2 Pin
7, 8, 10, 11, 12, 13	5, 6, 8, 9, 10, 11	NC	—	—	Not Internally Connected
9	7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
14	12	V_{OUT3}	A	A	Buffered Analog Voltage Output - Channel 3 Pin
15	13	V_{OUT1}	A	A	Buffered Analog Voltage Output - Channel 1 Pin
16	14	V_{REF1}	A	A	Voltage Reference Input 1 Pin
17	15	A1	I	ST	I²C Client Address Bit 1 Pin
18	16	SCL	I	ST	I²C Serial Clock Pin
19	17	SDA	I/O	ST	I²C Serial Data Pin
20	18	$\overline{LAT0}$/HVC	I	ST	DAC Wiper Register Latch 0/High-Voltage Command Pin. The Latch 0 pin allows the values in the volatile DAC0/DAC2 registers to be transferred to the V_{OUT0}/V_{OUT2} output pins. High-voltage commands allow the MTP Configuration bits to be written.
—	21	EP	—	P	Exposed Thermal Pad – it must be connected to V_{SS}

Note 1: A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power

TABLE 3-2: MCP47CXBX8 (OCTAL-DAC) PIN FUNCTION TABLE

Pin		Symbol	I/O	Buffer Type	Description
20-Lead TSSOP	20-Lead QFN				
1	19	$\overline{LAT1}$	I	ST	DAC Register Latch 1 Pin. The Latch 1 pin allows the values in the volatile DAC1/DAC3/DAC5/DAC7 registers to be transferred to the $V_{OUT1}/V_{OUT3}/V_{OUT5}/V_{OUT7}$ output pins.
2	20	V_{DD}	—	P	Supply Voltage Pin
3	1	A0	I	ST	I^2C Client Address Bit 0 Pin
4	2	V_{REF0}	A	A	Voltage Reference Input 0 Pin
5	3	V_{OUT0}	A	A	Buffered Analog Voltage Output – Channel 0 Pin
6	4	V_{OUT2}	A	A	Buffered Analog Voltage Output – Channel 2 Pin
7	5	V_{OUT4}	A	A	Buffered Analog Voltage Output – Channel 4 Pin
8	6	V_{OUT6}	A	A	Buffered Analog Voltage Output – Channel 6 Pin
9	7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
10, 11	8, 9	NC	—	—	Not Internally Connected
12	10	V_{OUT7}	A	A	Buffered Analog Voltage Output – Channel 7 Pin
13	11	V_{OUT5}	A	A	Buffered Analog Voltage Output – Channel 5 Pin
14	12	V_{OUT3}	A	A	Buffered Analog Voltage Output – Channel 3 Pin
15	13	V_{OUT1}	A	A	Buffered Analog Voltage Output – Channel 1 Pin
16	14	V_{REF1}	A	A	Voltage Reference Input 1 Pin
17	15	A1	I	ST	I^2C Client Address Bit 1 Pin
18	16	SCL	I	ST	I^2C Serial Clock Pin
19	17	SDA	I/O	ST	I^2C Serial Data Pin
20	18	$\overline{LAT0}$/HVC	I	ST	DAC Wiper Register Latch 0/High-Voltage Command Pin. The Latch 0 pin allows the values in the volatile DAC0/DAC2/DAC4/DAC6 registers to be transferred to the $V_{OUT0}/V_{OUT2}/V_{OUT4}/V_{OUT6}$ output pins. High-voltage commands allow the MTP Configuration bits to be written.
—	21	EP	—	P	Exposed Thermal Pad – it must be connected to V_{SS}

Note 1: A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power

3.1 Positive Power Supply Input (V_{DD})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS}.

The power supply at the V_{DD} pin must be as clean as possible for a good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground as close as possible to the pin. An additional 10 µF capacitor in parallel can be added to further attenuate noise present in application boards.

3.2 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application Printed Circuit Board (PCB), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Voltage Reference Pins (V_{REFn})

The V_{REFn} pins are either an input or an output. When the DAC's voltage reference is configured as the V_{REF} pin, the pin is an input. When the DAC's voltage reference is configured as the internal band gap, the pin is an output.

When the DAC's voltage reference is configured as the V_{REF} pin, there are two options for this voltage input: the V_{REF} pin voltage is buffered or unbuffered. The buffered option is offered in cases where the external reference voltage does not have sufficient current capability to not drop its voltage when connected to the internal resistor ladder circuit.

When the DAC's voltage reference is configured as the device V_{DD}, the V_{REF} pin is disconnected from the internal circuit.

When the DAC's voltage reference is configured as the internal band gap, the V_{REF} pin's drive capability is minimal, so the output signal must be buffered.

See **Section 4.4.2, "Voltage Reference Selection"** and Register 4-2 for more details on the Configuration bits.

3.4 No Connect (NC)

The NC pins are not internally connected to the device.

3.5 Analog Output Voltage Pins (V_{OUTn})

V_{OUTn} are the DAC analog voltage output pins. Each DAC output has an output amplifier. The DAC output range depends on the selection of the voltage reference source (and potential output gain selection):

- Device V_{DD} – The Full-Scale Range (FSR) of the DAC output is from V_{SS} to approximately V_{DD}.
- V_{REF} pin – The FSR of the DAC output is from V_{SS} to G × V_{RL}, where G is the gain selection option (1x or 2x).
- Internal Band Gap – The FSR of the DAC output is from V_{SS} to G × V_{BG}, where G is the gain selection option (1x or 2x).

In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 100 kΩ or open. The power-down selection bits settings are shown in Register 4-3 (Table 4-7).

3.6 Latch Pins ($\overline{LATn}$)/High-Voltage Command Pin (HVC)

The DAC output value update event can be controlled and synchronized using the $\overline{LAT}$ pin, for individual channels, on single or multiple devices.

The $\overline{LAT}$ pin controls the effect of the Volatile Wiper registers, VRnB:VRnA, PDnB:PDnA and Gn bits on the DAC output. If the $\overline{LAT}$ pin is held at V_{IH}, the values sent to the Volatile Wiper registers and Configuration bits have no effect on the DAC outputs. After the Volatile Wiper registers and Configuration bits are loaded with the desired data, once the voltage on the pin transitions to V_{IL}, the values in the Volatile Wiper registers and Configuration bits are transferred to the DAC outputs. Pulling $\overline{LAT}$ low during writes to the output registers could lead to unpredictable DAC output voltage values and must be avoided. To clear such a situation, a low-to-high followed by a high-to-low transition on the $\overline{LAT}$ pin is required. The pin is level-sensitive, so writing to the Volatile Wiper registers and Configuration bits while it is being held at V_{IL} will trigger an immediate change in the outputs.

$\overline{LAT0}$ is multiplexed with a HVC pin functionality. The HVC pin allows the device's MTP memory to be programmed for the MCP47CMBXX devices. The programming voltage supply should provide 7.5V and at least 6.4 mA.

Note:	The HVC pin must have voltages greater than 5.5V present only during the MTP programming operation. Using voltages greater than 5.5V for an extended time on the pin may cause device reliability issues.

3.7 I²C – Serial Clock Pin (SCL)

The SCL pin is the serial clock pin of the I²C interface. The MCP47CXBX4/8 I²C interface only acts as a client and the SCL pin accepts only external serial clocks. The input data from the host device are shifted into the SDA pin on the rising edges of the SCL clock and output from the device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the V_{DD} line to the SCL pin. See **Section 4.5, "Serial Communication Interface"** for more details on the I²C serial interface communication.

3.8 I²C – Serial Data Pin (SDA)

The SDA pin is the serial data pin of the I²C interface. The SDA pin is used to write or read the DAC registers and Configuration bits. The SDA pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the V_{DD} line to the SDA pin. Except for Start and Stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. See **Section 4.5, "Serial Communication Interface"**.

3.9 I²C Client Address Pins (A0, A1)

The state of these pins determines the device's I²C Client Address bit 0 and bit 1 values, overriding the values of the ADD0 and ADD1 bits in Register 4-5. The address pins must be directly connected to V_{SS} or V_{DD} to set the value of the corresponding address bit. V_{SS} corresponds to a value of '0', while V_{DD} corresponds to a value of '1'.

Note:	The ADD0 and ADD1 bits are used in single and dual devices in the 1 LSb family, where external address pins are not available, on specific packages. This enhances code compatibility and helps with migration between devices in the family.

4.0 DEVICE OPERATION

4.1 General Description

The MCP47CXBX4 (MCP47CXB04, MCP47CXB14 and MCP47CXB24) devices are quad-channel voltage output devices.

MCP47CXBX8 (MCP47CXB08, MCP47CXB18 and MCP47CXB28) are octal-channel voltage output devices.

These devices are offered with 8-bit (MCP47CXB0X), 10-bit (MCP47CXB1X) and 12-bit (MCP47CXB2X) resolutions.

The family offers two memory options: the MCP47CVBXX devices have volatile memory, while the MCP47CMBXX have 32-times programmable nonvolatile memory (MTP).

All devices include an I^2C serial interface and write latch ($\overline{LAT}$) pins to control the update of the analog output voltage value from the value written in the volatile DAC output registers.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software-selectable voltage reference source. The source can be either the device's internal V_{DD}, an external V_{REF} pin voltage (buffered or unbuffered) or an internal band gap voltage source.

The DAC output is buffered with a low-power and precision output amplifier. This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain (1x or 2x) of the output buffer is software configurable.

The devices operate from a single supply voltage. This voltage is specified from 2.7V to 5.5V for full specified operation and from 1.8V to 5.5V for digital operation. The device operates between 1.8V and 2.7V, but some device parameters are not specified.

The MCP47CMBXX devices also have user-programmable nonvolatile configuration memory (MTP). This allows the device's desired POR values to be saved or the I^2C address to be changed. The device also has general purpose MTP memory locations for storing system-specific information (calibration data, serial numbers, system ID information). A high-voltage requirement for programming on the HVC pin ensures that these device settings are not accidentally modified during normal system operation.

The MCP47CXBX4/8 device architecture is composed of the following functional units:

- **Power-on Reset/Brown-out Reset Module**
- **Device Memory**
- **DAC Circuitry**
- **Serial Communication Interface**

4.2 Power-on Reset/Brown-out Reset Module

The internal POR/BOR circuit monitors the power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events.

The device's RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

The POR and BOR trip points are at the same voltage and the condition is determined by whether the V_{DD} voltage is rising or falling (see Figure 4-1). What occurs is different depending on whether the Reset is a POR or BOR.

POR occurs as the voltage rises (typically from 0V), while BOR occurs as the voltage falls (typically from $V_{DD(MIN)}$ or higher).

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its volatile memory if the proper serial command is executed.

4.2.1 POWER-ON RESET

The POR is the case where the device's V_{DD} has power applied to it from the V_{SS} voltage level. As the device powers up, the V_{OUT} pin floats to an unknown value. When the device's V_{DD} is above the transistor threshold voltage of the device, the output starts to be pulled low.

After the V_{DD} is above the POR/BOR trip point (V_{BOR}/V_{POR}), the resistor network's wiper is loaded with the POR value. The POR value is either mid-scale (MCP47CVBXX) or the user's MTP programmed value (MCP47CMBXX).

Note:	In order to have the MCP47CMBXX devices load the values from nonvolatile memory locations at POR, they have to be programmed at least once by the user. Otherwise, the loaded values will be the default ones. After MTP programming, a POR event is required to load the written values from the nonvolatile memory.

MCP47CXBX4/8

The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered up, the user can update the device memory.

When the rising V_{DD} voltage crosses the V_{POR} trip point, the following occur:

- The default DAC POR value is latched into the volatile DAC register.
- The default DAC POR Configuration bit values are latched into the volatile Configuration bits.
- The POR status bit is set ('1').
- The Reset Delay Timer (t_{PORD}) starts; when the Reset Delay Timer (t_{PORD}) times out, the I^2C serial interface is operational. During this delay time, the I^2C interface will not accept commands.
- The Device Memory Address pointer is forced to 00h.

The Analog Output (V_{OUT}) state is determined by the state of the volatile Configuration bits and the DAC register. This is called a Power-on Reset (event).

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

4.2.2 BROWN-OUT RESET

A BOR occurs when a device has power applied to it and that power (voltage) drops below the specified range. If the V_{DD} voltage decreases below the V_{RAM} voltage, all volatile memory may become corrupted. Serial commands not completed due to a Brown-out condition may cause the memory location to become corrupted.

When the falling V_{DD} voltage crosses the V_{POR} trip point (BOR event), the following occur:

- The serial interface is disabled.
- The MTP writes are disabled.
- The device is forced into a Power-Down state (PDnB:PDnA = 11). Analog circuitry is turned off.
- The volatile DAC register is forced to 000h.
- The volatile Configuration bits, VRnB:VRnA and Gn, are forced to '0'.

As the voltage recovers and crosses above the V_{POR}/V_{BOR} voltage threshold, see **Section 4.2.1, "Power-on Reset"** for further details.

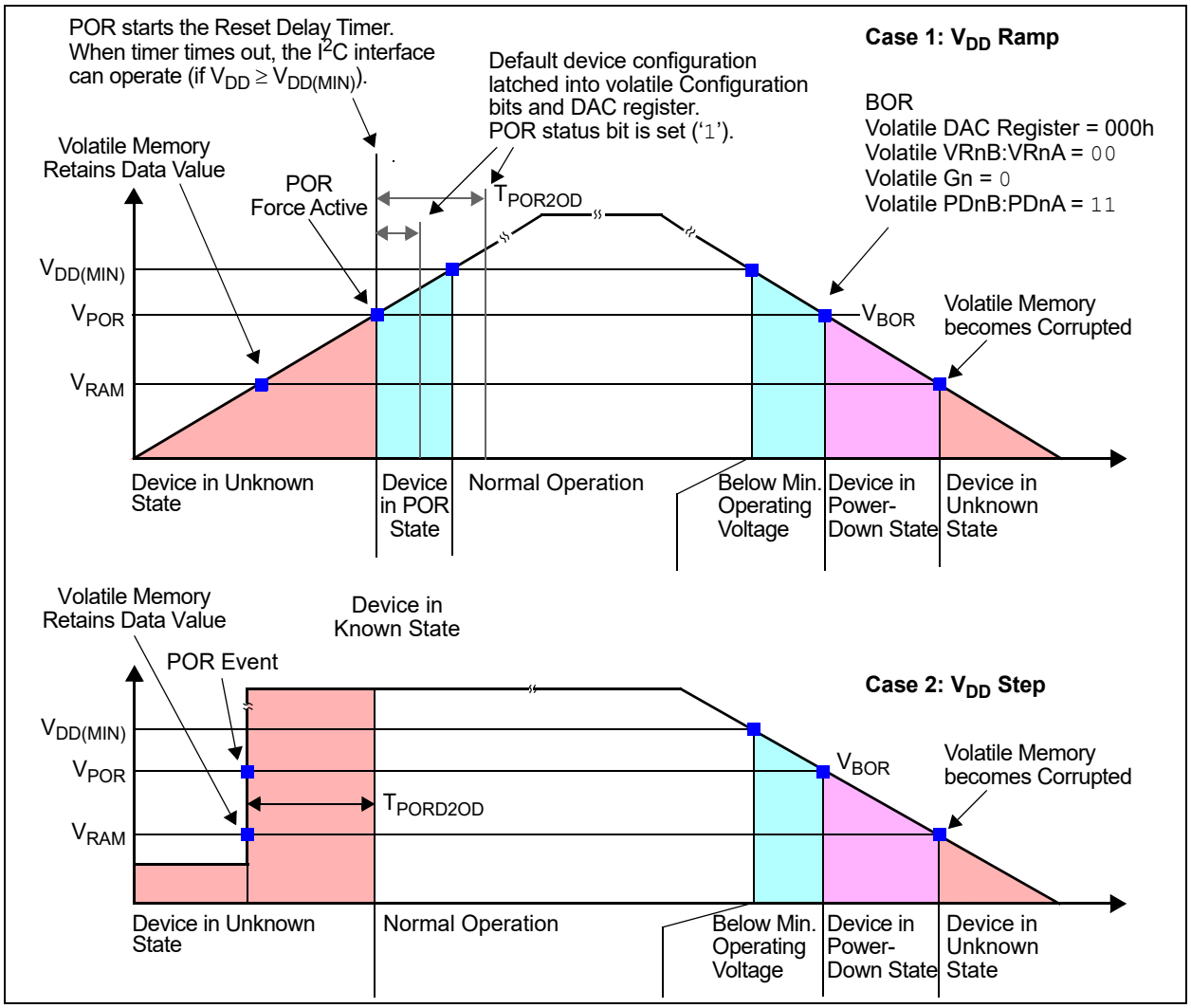

FIGURE 4-1: *Power-on/Brown-out Reset Operation.*

4.3 Device Memory

The user memory includes the following types:

- **Volatile Register Memory (RAM)**
- **Nonvolatile Register Memory (MTP)**

MTP memory is present just for the MCP47CMBXX devices and has three groupings:

- NV DAC output values (loaded on POR event)
- Device configuration memory
- General purpose NV memory

Each memory location is up to 16 bits wide. The memory-mapped register space is shown in Table 4-1.

The I^2C interface depends on how this memory is read and written. Refer to **Section 4.5, "Serial Communication Interface"** and **Section 4.6, "Device Commands"** for more details on reading and writing the device's memory.

4.3.1 VOLATILE REGISTER MEMORY (RAM)

The MCP47CXBX4/8 devices have volatile memory to directly control the operation of the DACs. There are up to eleven volatile memory locations:

- DACn Output Value registers
- VREF Select register
- Power-Down Configuration register
- Gain and Status register

The volatile memory starts functioning when the device V_{DD} is at (or above) the RAM retention voltage (V_{RAM}). The volatile memory will be loaded with the default device values when the V_{DD} rises across the V_{POR}/V_{BOR} voltage trip point.

After the device is powered-up, the user can update the device memory. Table 4-2 shows the volatile memory locations and their interaction due to a POR event.

TABLE 4-1: MCP47CXBX4/8 MEMORY MAP (16-BIT)

Address	Function	Quad(1)	Octal(1)	Address	Function	Quad(1)	Octal(1)
00h	Volatile DAC Wiper Register 0	Y	Y	10h	Nonvolatile DAC Wiper Register 0	Y	Y
01h	Volatile DAC Wiper Register 1	Y	Y	11h	Nonvolatile DAC Wiper Register 1	Y	Y
02h	Volatile DAC Wiper Register 2	Y	Y	12h	Nonvolatile DAC Wiper Register 2	Y	Y
03h	Volatile DAC Wiper Register 3	Y	Y	13h	Nonvolatile DAC Wiper Register 3	Y	Y
04h	Volatile DAC Wiper Register 4	—	Y	14h	Nonvolatile DAC Wiper Register 4	—	Y
05h	Volatile DAC Wiper Register 5	—	Y	15h	Nonvolatile DAC Wiper Register 5	—	Y
06h	Volatile DAC Wiper Register 6	—	Y	16h	Nonvolatile DAC Wiper Register 6	—	Y
07h	Volatile DAC Wiper Register 7	—	Y	17h	Nonvolatile DAC Wiper Register 7	—	Y
08h	Volatile VREF Register	Y	Y	18h	Nonvolatile VREF Register	Y	Y
09h	Volatile Power-Down Register	Y	Y	19h	Nonvolatile Power-Down Register	Y	Y
0Ah	Volatile Gain and Status Register	Y	Y	1Ah	NV Gain and I^2C 7-Bit Client Address	Y	Y
0Bh	Reserved	—	—	1Bh	NV WiperLock™ Technology Register	Y	Y
0Ch	General Purpose MTP	**Note 1**		1Ch	General Purpose MTP	**Note 1**	
0Dh	General Purpose MTP	**Note 1**		1Dh	General Purpose MTP	**Note 1**	
0Eh	General Purpose MTP	**Note 1**		1Eh	General Purpose MTP	**Note 1**	
0Fh	General Purpose MTP	**Note 1**		1Fh	General Purpose MTP	**Note 1**	

Legend:

	Volatile Memory Addresses
	MTP Memory Addresses
	Memory Locations Not Implemented

Note 1: On nonvolatile memory devices only (MCP47CMBXX).

4.3.2 NONVOLATILE REGISTER MEMORY (MTP)

This memory option is available only for the MCP47CMBXX devices.

The MTP memory starts functioning below the device's V_{POR}/V_{BOR} trip point and, once the V_{POR} event occurs, the volatile memory registers are loaded with the corresponding MTP register memory values.

Memory addresses, 0Ch through 1Fh, are nonvolatile memory locations. These registers contain the DAC POR/BOR wiper values, the DAC POR/BOR Configuration bits, the I^2C client address and eight general purpose memory addresses for storing user-defined data as calibration constants or identification numbers. The nonvolatile DAC Wiper registers and Configuration bits contain the user's DAC Output and configuration values for the POR event.

The Nonvolatile DAC Wiper registers contain the user's DAC output and configuration values for the POR event. These nonvolatile values will overwrite the factory default values. If these MTP addresses are unprogrammed, the factory default values define the output state.

The nonvolatile DAC registers enable the stand-alone operation of the device (without microcontroller control) after being programmed to the desired values.

To program nonvolatile memory locations, a high-voltage source on the $\overline{LAT}$/HVC pin is required. Each register/MTP location can be programmed 32 times. After 32 writes, a new write operation will not be possible and the last successful value written will remain associated with the memory location.

The device starts writing the MTP memory cells at the completion of the serial interface command at the rising edge of the last data bit. The high voltage must remain present on the $\overline{LAT}$/HVC pin until the write cycle is complete; otherwise, the write is unsuccessful and the location is compromised (cannot be used again and the number of available writes decreases by one).

To recover from an aborted MTP write operation, the following procedure must be used:

1. Write any valid value to the same address again.
2. Force a POR condition.
3. Write the desired value to the MTP location again.

It is recommended to keep high voltage on only during the MTP write command and programming cycle; otherwise, the reliability of the device could be affected.

4.3.3 POR/BOR OPERATION WITH WIPERLOCK TECHNOLOGY ENABLED

Regardless of the WiperLock technology state, a POR event will load the volatile DACn Wiper register value with the nonvolatile DACn Wiper register value. See **Section 4.2, "Power-on Reset/Brown-out Reset Module"** for further information.

4.3.4 UNIMPLEMENTED LOCATIONS

4.3.4.1 Unimplemented Register Bits

When issuing read commands to a valid memory location with unimplemented bits, the unimplemented bits will be read as '0'.

4.3.4.2 Unimplemented (RESERVED) Registers

There are a number of unimplemented memory locations that are reserved for future use. Normal (voltage) commands (read or write) to any unimplemented memory address will result in a command error condition (I^2C NACK).

High-voltage commands to any unimplemented Configuration bit(s) will also result in a command error condition.

TABLE 4-2: FACTORY DEFAULT POR/BOR VALUES (MTP MEMORY UNPROGRAMMED)

Address	Function	POR/BOR Value		
		8-Bit	10-Bit	12-Bit
00h	Volatile DAC0 Wiper Register	7Fh	1FFh	7FFh
01h	Volatile DAC1 Wiper Register	7Fh	1FFh	7FFh
02h	Volatile DAC2 Wiper Register	7Fh	1FFh	7FFh
03h	Volatile DAC3 Wiper Register	7Fh	1FFh	7FFh
04h	Volatile DAC4 Wiper Register	7Fh	1FFh	7FFh
05h	Volatile DAC5 Wiper Register	7Fh	1FFh	7FFh
06h	Volatile DAC6 Wiper Register	7Fh	1FFh	7FFh
07h	Volatile DAC7 Wiper Register	7Fh	1FFh	7FFh
08h	Volatile VREF Register	0000h	0000h	0000h
09h	Volatile Power-Down Register	0000h	0000h	0000h
0Ah	Volatile Gain and Status Register(4)	0080h	0080h	0080h
0Bh	Reserved(3)	0000h	0000h	0000h
0Ch	General Purpose MTP(1)	0000h	0000h	0000h
0Dh	General Purpose MTP(1)	0000h	0000h	0000h
0Eh	General Purpose MTP(1)	0000h	0000h	0000h
0Fh	General Purpose MTP(1)	0000h	0000h	0000h
10h	Nonvolatile DAC0 Wiper Register(1)	7Fh	1FFh	7FFh
11h	Nonvolatile DAC1 Wiper Register(1)	7Fh	1FFh	7FFh
12h	Nonvolatile DAC2 Wiper Register(1)	7Fh	1FFh	7FFh
13h	Nonvolatile DAC3 Wiper Register(1)	7Fh	1FFh	7FFh
14h	Nonvolatile DAC4 Wiper Register(1)	7Fh	1FFh	7FFh
15h	Nonvolatile DAC5 Wiper Register(1)	7Fh	1FFh	7FFh
16h	Nonvolatile DAC6 Wiper Register(1)	7Fh	1FFh	7FFh
17h	Nonvolatile DAC7 Wiper Register(1)	7Fh	1FFh	7FFh
18h	Nonvolatile VREF Register(1)	0000h	0000h	0000h
19h	Nonvolatile Power-Down Register(1)	0000h	0000h	0000h
1Ah	NV Gain and I^2C 7-Bit Client Address(1, 2)	0060h	0060h	0060h
1Bh	NV WiperLock™ Technology Register(1)	0000h	0000h	0000h
1Ch	General Purpose MTP(1)	0000h	0000h	0000h
1Dh	General Purpose MTP(1)	0000h	0000h	0000h
1Eh	General Purpose MTP(1)	0000h	0000h	0000h
1Fh	General Purpose MTP(1)	0000h	0000h	0000h

Legend:

- Volatile Memory Address Range
- Nonvolatile Memory Address Range
- Not Implemented

Note 1: On nonvolatile devices only (MCP47CMBXX).

2: The default I^2C 7-bit client address is '110 00xx', ADD1:ADD0 bits are determined from the A1 and A0 pins.

3: Reading a reserved memory location will result in the I^2C command to Not ACK the command byte. The device data bits will output all '1's. A Start condition will reset the I^2C interface.

4: The '1' bit is the POR status bit, which is set after the POR event and cleared after address 0Ah is read.

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4.3.5 DEVICE REGISTERS

Register 4-1 shows the format of the DAC Output Value registers for the volatile memory locations. These registers are 8 bits, 10 bits or 12 bits wide. The values are right justified.

REGISTER 4-1: DAC0 TO DAC7 OUTPUT VALUE REGISTERS ADDRESSES 00H THROUGH 07H/10H THROUGH 17H (VOLATILE/NONVOLATILE)

	U-0	U-0	U-0	U-0	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
12-bit	—	—	—	—	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
10-bit	—	—	—	—	—(1)	—(1)	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
8-bit	—	—	—	—	—(1)	—(1)	—(1)	—(1)	D07	D06	D05	D04	D03	D02	D01	D00
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= 12-bit device	= 10-bit device	= 8-bit device	

12-bit	**10-bit**	**8-bit**	
bit 15-12	bit 15-10	bit 15-8	**Unimplemented:** Read as '0'
bit 11-0	—	—	**D11:D00:** DAC Output Value bits – 12-bit devices FFFh = Full-Scale output value 7FFh = Mid-Scale output value 000h = Zero-Scale output value
—	bit 9-0	—	**D09:D00:** DAC Output Value bits – 10-bit devices 3FFh = Full-Scale output value 1FFh = Mid-Scale output value 000h = Zero-Scale output value
—	—	bit 7-0	**D07:D00:** DAC Output Value bits – 8-bit devices FFh = Full-Scale output value 7Fh = Mid-Scale output value 00h = Zero-Scale output value

Note 1: Unimplemented bit, read as '0'.

Register 4-2 shows the format of the Voltage Reference Control register. Each DAC has two bits to control the source of the DAC's voltage reference. This register is for the volatile memory locations. The width of this register is two times the number of DACs for the device.

REGISTER 4-2: VOLTAGE REFERENCE (VREF) CONTROL REGISTER ADDRESSES 08H/18H (VOLATILE/NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	VR7B	VR7A	VR6B	VR6A	VR5B	VR5A	VR4B	VR4A	VR3B	VR3A	VR2B	VR2A	VR1B	VR1A	VR0B	VR0A
Quad	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	VR3B	VR3A	VR2B	VR2A	VR1B	VR1A	VR0B	VR0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	Quad	
—	bit 15-8	**Unimplemented:** Read as '0'
bit 15-0	bit 7-0	**VRnB:VRnA:** DAC Voltage Reference Control bits 11 = V_{REF} pin (buffered); V_{REF} buffer enabled 10 = V_{REF} pin (unbuffered); V_{REF} buffer disabled 01 = Internal band gap; V_{REF} buffer enabled, V_{REF} voltage driven when powered down(2) 00 = V_{DD} (unbuffered); V_{REF} buffer disabled, use this state with power-down bits for lowest current

Note 1: Unimplemented bit, read as '0'.

2: When the internal band gap is selected, the band gap voltage source will continue to output the voltage on the V_{REF} pin in any of the Power-Down modes. To reduce the power consumption to its lowest level (band gap disabled), after selecting the desired Power-Down mode, the voltage reference must be changed to V_{DD} or the V_{REF} pin unbuffered ('00' or '10'), which turns off the internal band gap circuitry. After wake-up, the user needs to reselect the internal band gap ('01') for the voltage reference source.

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Register 4-3 shows the format of the Power-Down Control register. Each DAC has two bits to control the Power-Down state of the DAC. This register is for both volatile and nonvolatile memory locations. The width of this register is two times the number of DACs for the device.

REGISTER 4-3: POWER-DOWN CONTROL REGISTER ADDRESSES 09H/19H (VOLATILE/NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	PD7B	PD7A	PD6B	PD6A	PD5B	PD5A	PD4B	PD4A	PD3B	PD3A	PD2B	PD2A	PD1B	PD1A	PD0B	PD0A
Quad	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	PD3B	PD3A	PD2B	PD2A	PD1B	PD1A	PD0B	PD0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	Quad	
—	bit 15-8	**Unimplemented:** Read as '0'
bit 15-0	bit 7-0	**PDnB:PDnA:** DAC Power-Down Control bits(2) 11 =Powered down – V_{OUT} is open circuit 10 =Powered down – V_{OUT} is loaded with a 100 kΩ resistor to ground 01 =Powered down – V_{OUT} is loaded with a 1 kΩ resistor to ground 00 =Normal operation (not powered down)

Note 1: Unimplemented bit, read as '0'.

2: See Table 4-7 for more details.

Register 4-4 shows the format of the Gain Control and System Status register. Each DAC has one bit to control the gain of the DAC and two Status bits.

REGISTER 4-4: GAIN CONTROL AND SYSTEM STATUS REGISTER ADDRESS 0AH (VOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/C-1	R	U-0	U-0	U-0	U-0	U-0	U-0
Octal	G7	G6	G5	G4	G3	G2	G1	G0	POR	MTPMA	—	—	—	—	—	—
Quad	—(1)	—(1)	—(1)	—(1)	G3	G2	G1	G0	POR	MTPMA	—	—	—	—	—	—
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	Quad	
—	bit 15-12	**Unimplemented:** Read as '0'
bit 15-8	bit 11-8	**Gn:** DAC Channel n Output Driver Gain Control bit 1 = 2x gain; not applicable when V_{DD} is used as V_{RL} (2) 0 = 1x gain
bit 7	bit 7	**POR:** Power-on Reset (Brown-out Reset) Status bit This bit indicates if a POR or BOR event has occurred since the last read command of this register. Reading this register clears the state of the POR Status bit. 1 = A POR (BOR) event has occurred since the last read of this register; reading this register clears this bit. 0 = A POR (BOR) event has not occurred since the last read of this register.
bit 6	bit 6	**MTPMA:** MTP Memory Access Status bit(3) This bit indicates if the MTP memory access occurs. 1 = An MTP memory access is currently occurring (during the POR MTP read cycle or an MTP write cycle is occurring); only serial commands addressing the volatile memory are allowed. 0 = An MTP memory access is NOT currently occurring.
bit 5-0	bit 5-0	**Unimplemented:** Read as '0'

Note 1: Unimplemented bit, read as '0'.

2: The DAC's Gain bit is ignored and the gain is forced to 1x (Gn = 0) when the DAC voltage reference is selected as V_{DD} (VRnB:VRnA = 00).

3: For devices configured as volatile memory, this bit is read as '0'.

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Register 4-5 shows the format of the Nonvolatile Gain Control and Client Address register. Each DAC has one bit to control the gain of the DAC. I^2C devices also have five bits that determine, together with the address pins A1 and A0, the I^2C client address(3).

REGISTER 4-5: GAIN CONTROL AND CLIENT ADDRESS REGISTER ADDRESS 1AH (NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	U-0	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	G7	G6	G5	G4	G3	G2	G1	G0	—	ADD6	ADD5	ADD4	ADD3	ADD2	—(4)	—(4)
Quad	—(1)	—(1)	—(1)	—(1)	G3	G2	G1	G0	—	ADD6	ADD5	ADD4	ADD3	ADD2	—(4)	—(4)
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	**Quad**	
—	bit 15-12	**Unimplemented:** Read as '0'
bit 15-8	bit 11-8	**Gn**: DAC Channel n Output Driver Gain Control bit(2) 1 = 2x gain 0 = 1x gain
bit 7	bit 7	**Unimplemented:** Read as '0'
bit 6-2	bit 6-2	**ADD6:ADD2**: I^2C 7-bit Client Address bits(3)
bit 1-0	bit 1-0	**Unimplemented:** Read as '0'

Note 1: Unimplemented bit, read as '0'.

2: When the DAC voltage reference is selected as V_{DD} (VRnB:VRnA = 00), the DAC's Gain bit is ignored and the gain is forced to 1x (Gn = 0).

3: The 7-bit client address is given by ADD6:ADD2 + A1:A0.

4: These bits (ADD1 and ADD0) can be read and written, but the value of A1 and A0 pins will take precedence, so their value will be disregarded by the I^2C communication module. They are used for compatibility with single/dual devices in the 1 LSb family, where packages do not have external address pins.

Register 4-6 shows the format of the DAC WiperLock Technology Status register. The width of this register is two times the number of DACs for the device.

WiperLock technology bits only control access to volatile memory. Nonvolatile memory write access is controlled by the requirement of high voltage on the HVC pin, which is recommended to not be available during normal device operation.

REGISTER 4-6: WiperLock™ TECHNOLOGY CONTROL REGISTER ADDRESS 1Bh (NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	WL7B	WL7A	WL6B	WL6B	WL5A	WL5B	WL4A	WL4B	WL3A	WL3B	WL2A	WL2B	WL1B	WL1A	WL0B	WL0A
Quad	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	WL3A	WL3B	WL2A	WL2B	WL1B	WL1A	WL0B	WL0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad channel device	= Octal channel device		

Octal	**Quad**	
—	bit 15-8	**Unimplemented:** Read as '0'
bit 15-0	bit 7-0	**WLnB:WLnA:** WiperLock™ Technology Status bits(2) 11 = Volatile DAC Wiper register and volatile DAC Configuration bits are locked 10 = Volatile DAC Wiper register is locked and volatile DAC Configuration bits are unlocked 01 = Volatile DAC Wiper register is unlocked and volatile DAC Configuration bits are locked 00 = Volatile DAC Wiper register and volatile DAC Configuration bits are unlocked

Note 1: Unimplemented bit, read as '0'.

2: The volatile PDnB:PDnA bits are NOT locked due to the requirement of being able to exit Power-Down mode.

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4.4 DAC Circuitry

The Digital-to-Analog Converter circuitry converts a digital value into its analog representation. This section describes the functional operation of the device.

The DAC architecture is based on a resistor ladder implementation. Devices have up to eight DACs. Figure 4-2 shows the functional block diagram for the MCP47CXBX4/8 DAC circuitry.

The functional blocks of the DAC circuitry include:

- **Resistor Ladder**
- **Voltage Reference Selection**
- **Output Driver**
- **Latch Pins (LATn)**
- **Power-Down Control**

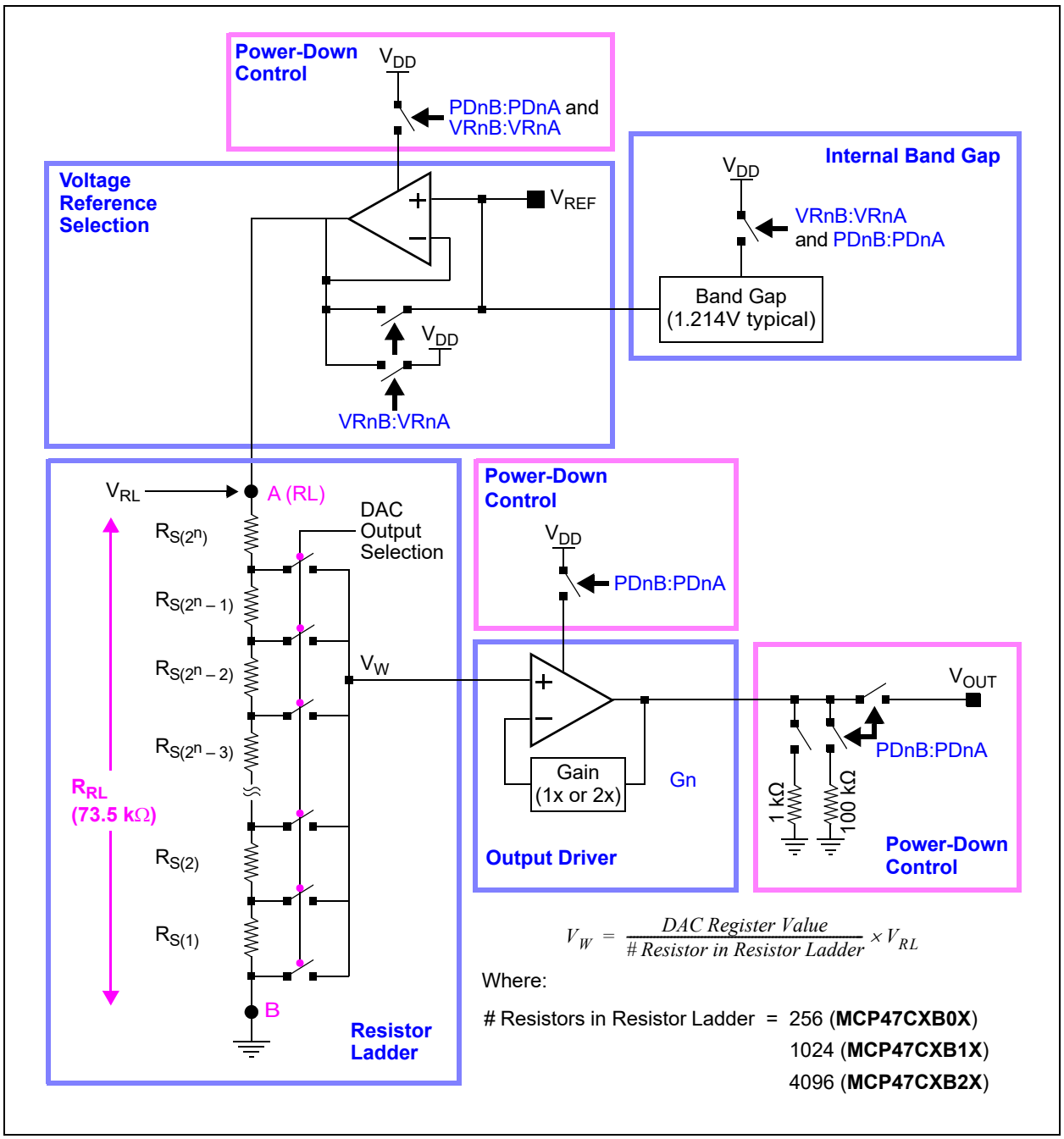
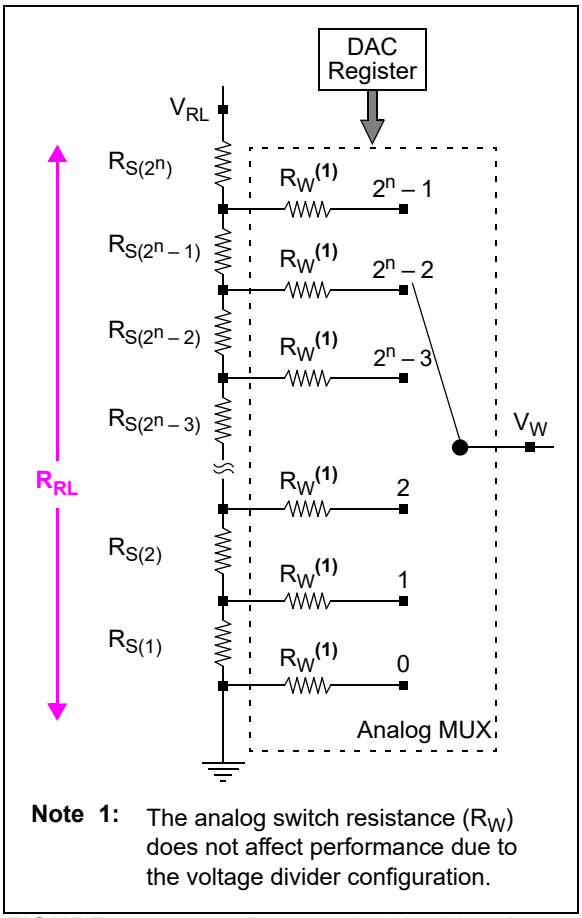


FIGURE 4-2: *MCP47CXBX4/8 DAC Circuitry Functional Block Diagram.*

4.4.1 RESISTOR LADDER

The resistor ladder is a digital potentiometer with the A Terminal connected to the selected reference voltage and the B Terminal internally grounded (see Figure 4-3). The volatile DAC register controls the wiper position. The wiper voltage (V_W) is proportional to the DAC register value divided by the number of resistor elements (R_S) in the ladder (256, 1024 or 4096) related to the V_{RL} voltage.



Note 1: The analog switch resistance (R_W) does not affect performance due to the voltage divider configuration.

FIGURE 4-3: *Resistor Ladder Model Block Diagram.*

The output of the resistor network will drive the input of an output buffer.

The resistor network has three parts:

- Resistor ladder (string of R_S elements)
- Wiper switches
- DAC register decode

The resistor ladder has a typical impedance (R_{RL}) of approximately 73.5 kΩ. This resistor ladder resistance (R_{RL}) may vary from device to device, up to ±15%. Since this is a voltage divider configuration, the actual R_{RL} resistance does not affect the output, given a fixed voltage at V_{RL}.

Equation 4-1 shows the calculation for the step resistance.

EQUATION 4-1: R_S CALCULATION

$$R_S = \frac{R_{RL}}{(256)} \quad \textit{8-bit Device}$$

$$R_S = \frac{R_{RL}}{(1024)} \quad \textit{10-bit Device}$$

$$R_S = \frac{R_{RL}}{(4096)} \quad \textit{12-bit Device}$$

Note: The maximum wiper position is $2^n - 1$, while the number of resistors in the resistor ladder is 2^n. This means that when the DAC register is at full scale, there is one resistor element (R_S) between the wiper and the V_{RL} voltage.

If the unbuffered V_{REF} pin is used as the V_{RL} voltage source, the external voltage source must have a low output impedance.

When the DAC is powered down, the resistor ladder is disconnected from the selected reference voltage.

4.4.2 VOLTAGE REFERENCE SELECTION

The resistor ladder has up to four sources for the reference voltage. The selection of the voltage reference source is specified with the volatile VRnB:VRnA Configuration bits (see Register 4-2). The selected voltage source is connected to the V_{RL} node (see Figure 4-3 and Figure 4-4).

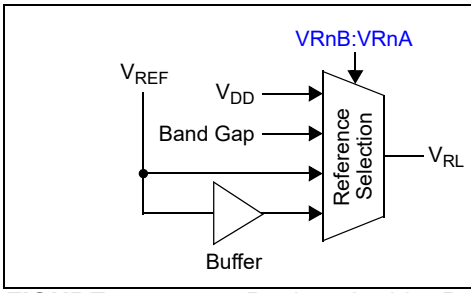
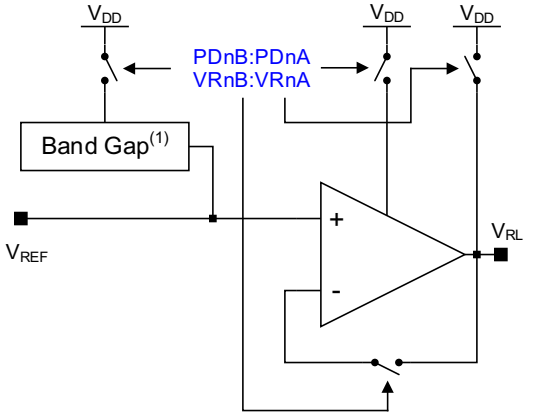


FIGURE 4-4: *Resistor Ladder Reference Voltage Selection Block Diagram.*

The four voltage source options for the resistor ladder are:

1. V_{DD} pin voltage
2. Internal band gap voltage reference (V_{BG})
3. V_{REF} pin voltage – unbuffered
4. V_{REF} pin voltage – internally buffered

On a POR/BOR event, the default configuration state or the value written in the nonvolatile register is latched into the volatile VRnB:VRnA Configuration bits.



Note 1: The band gap voltage (V_{BG}) is 1.214V (typical). The band gap output goes through the buffer with a 2x gain to create the V_{RL} voltage. See Table 4-3 for additional information on the band gap circuit.

FIGURE 4-5: *Reference Voltage Selection Implementation Block Diagram.*

If the V_{REF} pin is used with an external voltage source, then the user must select between Buffered or Unbuffered mode.

4.4.2.1 Using V_{DD} as V_{REF}

When the user selects the V_{DD} as reference, the V_{REF} pin voltage is not connected to the resistor ladder. The V_{DD} voltage is internally connected to the resistor ladder.

4.4.2.2 Using an External V_{REF} Source in Unbuffered Mode

In this case, the V_{REF} pin voltage may vary from V_{SS} to V_{DD}. The voltage source must have a low output impedance. If the voltage source has a high output impedance, then the voltage on the V_{REF} pin could be lower than expected. The resistor ladder has a typical impedance of 73.5 kΩ and a typical capacitance of 29 pF.

If a single V_{REF} pin supplies multiple DACs, the V_{REF} pin source must have adequate current capability to support the number of DACs. It must be assumed that the resistor ladder resistance (R_{RL}) of each DAC is at the minimum specified resistance and these resistances are in parallel.

If the V_{REF} pin is tied to the V_{DD} voltage, selecting the V_{DD} Reference mode (VREF1:VREF0 = `00`) is recommended.

4.4.2.3 Using an External V_{REF} Source in Buffered Mode

The V_{REF} pin voltage may be from 0V to V_{DD}. The input buffer (amplifier) provides low offset voltage, low noise and a very high input impedance, with only minor limitations on the input range and frequency response.

Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.

4.4.2.4 Using the Internal Band Gap as Voltage Reference

The internal band gap is designed to drive the resistor ladder buffer.

If the internal band gap is selected, the band gap voltage source will drive the external V_{REF} pins. The V_{REF0} pin can source up to 1 mA of current without affecting the DAC output specifications. The V_{REF1} pin must be left unloaded in this mode. The voltage reference source can be independently selected, but restrictions apply:

- The V_{DD} mode can be used without issues on any channel.
- When the internal band gap is selected as the voltage source, all the V_{REF} pins are connected to its output. The use of the Unbuffered mode is only possible on V_{REF0}, because it's the only one that can be loaded.
- When using the Internal Band Gap mode on Channel 0, Channels 1, 3, 5 and 7 must be put in Buffered External V_{REF} mode or V_{DD} Reference mode and the V_{REF1} pin must be left unloaded.

The resistance of the resistor ladder (R_{RL}) is targeted to be 73.5 kΩ (±15%), which means a minimum resistance of 62.475 kΩ. The band gap selection can be used across the V_{DD} voltages while maximizing the V_{OUT} voltage ranges. For V_{DD} voltages below the Gain ∗ V_{BG} voltage, the output for the upper codes will be clipped to the V_{DD} voltage.

Table 4-3 shows the maximum DAC register code given device V_{DD} and Gain bit setting.

TABLE 4-3: V_{OUT} USING BAND GAP

V_{DD}	DAC Gain	Max DAC Code(1)			Comment
		12-Bit	10-Bit	8-Bit	
5.5	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 1.214V(3)
	2	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.428V(3)
2.7	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 1.214V(3)
	2	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.428V
1.8	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 1.214V
	2(2)	BBCh	2EFh	BBh	1.8V

Note 1: Without the V_{OUT} pin voltage being clipped.
2: Recommended to use the Gain = `1` setting.
3: When V_{BG} = 1.214V typical.

4.4.3 OUTPUT DRIVER

The output driver buffers the wiper voltage (V_W) of the resistor ladder. Figure 4-6 shows a block diagram of the output driver circuit.

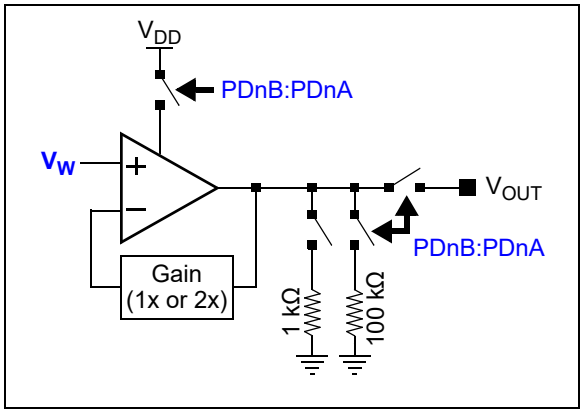


FIGURE 4-6: *Output Driver Block Diagram.*

The DAC output is buffered with a low-power, precision output amplifier with selectable gain. This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier's output can drive the resistive and high-capacitive loads without oscillation.

Note:	The load resistance must be kept higher than 2 kΩ to maintain stability of the analog output and have it meet electrical specifications.

The amplifier provides a maximum load current, which is enough for most programmable voltage reference applications. See **Section 1.0, "Electrical Characteristics"** for the specifications of the output amplifier. Power-down logic also controls the output buffer operation (see **Section 4.4.5, "Power-Down Control"** for additional information on power-down). In any of the three Power-Down modes, the output amplifier is powered down and its output becomes a high-impedance to the V_{OUT} pin.

4.4.3.1 Programmable Gain

The amplifier's gain is controlled by the Gain (Gn) Configuration bits (see Register 4-4) and the V_{RL} reference selection (see Register 4-2).

The gain options are:

a) Gain of 1, with either the V_{DD} or the V_{REF} pin used as the reference voltage.

b) Gain of 2, only when the V_{REF} pin or the internal band gap is used as the reference voltage. The V_{REF} pin voltage must be limited to $V_{DD}/2$. When the reference voltage selection (V_{RL}) is the device's V_{DD} voltage, the Gn bit is ignored and a gain of 1 is used.

Table 4-4 shows the gain bit operation.

TABLE 4-4: OUTPUT DRIVER GAIN

Gain Bit	Gain	Comment
0	1	
1	2	Limits V_{REF} pin voltages relative to device V_{DD} voltage.

The volatile G bit value can be modified by:

- POR event
- BOR event
- I^2C write commands
- I^2C General Call Reset command

4.4.3.2 Output Voltage

The volatile DAC register values, along with the device's Configuration bits, control the analog V_{OUT} voltage. The volatile DAC register's value is unsigned binary. The formula for the output voltage is provided in Equation 4-2.

EQUATION 4-2: CALCULATING OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{V_{RL} \times DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

 # Resistors in R Ladder = 4096 (MCP47CXB2X)
1024 (MCP47CXB1X)
256 (MCP47CXB0X)

Examples of volatile DAC register values and the corresponding theoretical V_{OUT} voltage for the MCP47CXBX4/8 devices are shown in Table 4-8.

When Gain = 2 ($V_{RL} = V_{REF}$), if $V_{REF} > V_{DD}/2$, the V_{OUT} voltage is limited to V_{DD}. So if $V_{REF} = V_{DD}$, the V_{OUT} voltage does not change for Volatile DAC register values mid-scale and greater, since the output amplifier is at full-scale output.

The following events update the DAC register value, and therefore, the analog voltage output (V_{OUT}):

- POR
- BOR
- I^2C write command (to volatile registers) on the rising edge of the last write command bit
- I^2C General Call Reset command; the output is updated with default POR data or MTP values
- I^2C General Call Wake-Up command; the output is updated with default POR data or MTP values

Next, the V_{OUT} voltage starts driving to the new value after the event has occurred.

4.4.3.3 Output Slew Rate

Figure 4-7 shows an example of the slew rate of the V_{OUT} pin.

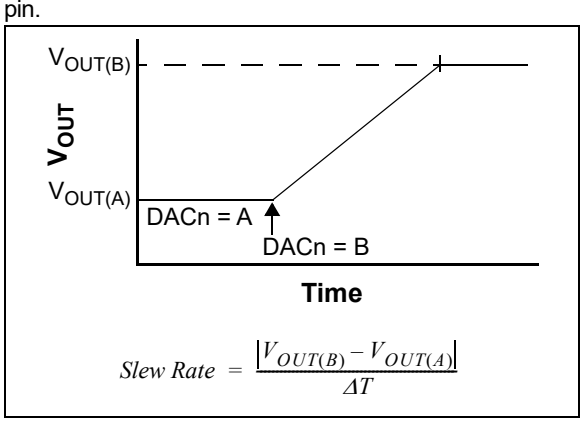


FIGURE 4-7: *V_{OUT} Pin Slew Rate.*

The slew rate can be affected by the characteristics of the circuit connected to the V_{OUT} pin.

4.4.3.4 Driving Small Capacitive Loads

With a small capacitive load, the output buffer's current is not affected by the capacitive load (C_L). But still, the V_{OUT} pin's voltage is not a step transition from one output value (DAC register value) to the next output value. The change of the V_{OUT} voltage is limited by the output buffer's characteristics, so the V_{OUT} pin voltage will have a slope from the old voltage to the new voltage. This slope is fixed for the output buffer and is referred to as the buffer slew rate (SR_{BUF}).

4.4.3.5 Driving Large Capacitive Loads

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer's short-circuit current (I_{SC})
- The V_{OUT} pin's external load

I_{OUT} cannot exceed the output buffer's short-circuit current (I_{SC}), which fixes the output buffer slew rate (SR_{BUF}). The voltage on the capacitive load (C_L), V_{CL}, changes at a rate proportional to I_{OUT}, which fixes a capacitive load slew rate (SR_{CL}).

The V_{CL} voltage slew rate is limited to the slower of the output buffer's internally set slew rate (SRBUF) and the capacitive load slew rate (SR_{CL}).

4.4.3.6 Step Voltage (V_S)

The step voltage can easily be calculated by using Equation 4-3 (the DAC register value is equal to '1').

EQUATION 4-3: V_S CALCULATION

$$V_S = \frac{V_{RL}}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

 # Resistors in R Ladder = 4096 (12-bit)
1024 (10-bit)
256 (8-bit)

The step voltage depends on the device resolution and the calculated output voltage range. One LSb is defined as the ideal voltage difference between two successive codes. Theoretical step voltages are shown in Table 4-5 for several V_{REF} voltages.

TABLE 4-5: THEORETICAL STEP VOLTAGE (V_S)(1)

Step Voltage	V_{REF}					
	5.0	**2.7**	**1.8**	**1.5**	**1.0**	
V_S	1.22 mV	659 uV	439 uV	366 uV	244 uV	12-bit
	4.88 mV	2.64 mV	1.76 mV	1.46 mV	977 uV	10-bit
	19.5 mV	10.5 mV	7.03 mV	5.86 mV	3.91 mV	8-bit

Note 1: When Gain = 1x, $V_{FS} = V_{RL}$ and $V_{ZS} = 0V$.

4.4.4 LATCH PINS ($\overline{LAT}$n)

The Latch pin controls when the volatile DAC register value is transferred to the DAC wiper. This is useful for applications that need to synchronize the wiper(s) updates to an external event, such as zero crossing or updates to the other wipers on the device. The $\overline{LAT}$ pin is asynchronous to the serial interface operation.

When the $\overline{LAT}$ pin is high, transfers from the volatile DAC register to the DAC wiper are inhibited. The volatile DAC register value(s) can continue to be updated.

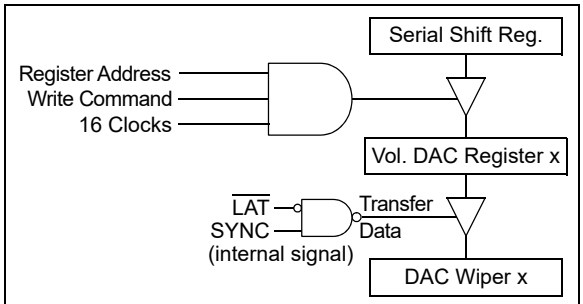
When the $\overline{LAT}$ pin is low, the volatile DAC register value is transferred to the DAC wiper.

This allows all the volatile wiper registers to be updated while the $\overline{LAT}$ pin is high and to have outputs synchronously updated as the $\overline{LAT}$ pin is driven low.

Figure 4-8 shows the interaction of the $\overline{LAT}$ pin and the loading of the DAC wiper x (from the volatile DAC register x). The transfers are level-driven. If the $\overline{LAT}$ pin is held low, the corresponding DAC wiper is updated as soon as the volatile DAC register value is updated.

The $\overline{LAT}$ pin allows the DAC wiper to be updated to an external event and to have multiple DAC channels/devices updated at a common event.

Since the DAC wiper x is updated from the volatile DAC register x, all DACs that are associated with a given $\overline{LAT}$ pin can be updated synchronously.



$\overline{LAT}$	SYNC	Transfer Data	Comment
1	1	0	No Transfer
1	0	0	No Transfer
0	1	1	Vol. DAC Register x → DAC Wiper x
0	0	0	No Transfer

FIGURE 4-8: *$\overline{LAT}$ and DAC Interaction.*

If the application does not require synchronization, this signal must be tied low.

Figure 4-9 shows two cases of using the $\overline{LAT}$ pin to control when the wiper register is updated, relative to the amplitude of a sine wave signal.

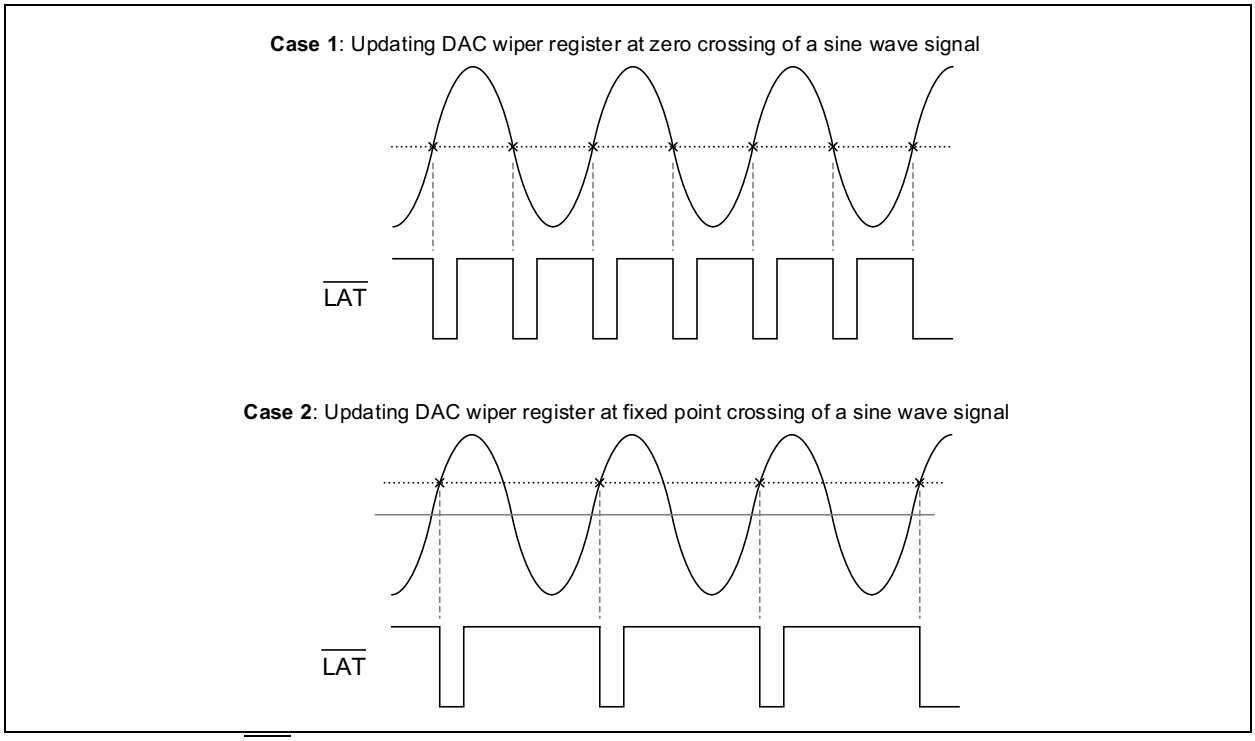


FIGURE 4-9: *$\overline{LAT}$ Pin Operation Example.*

4.4.5 POWER-DOWN CONTROL

To allow the application to conserve power when DAC operation is not required, three Power-Down modes are available. On devices with multiple DACs, each DAC's Power-Down mode is individually controllable.

All Power-Down modes do the following:

- Turn off most of the DAC module's internal circuits
- Op amp output becomes high-impedance to the V_{OUT} pin
- Retain the value of the volatile DAC register and Configuration bits

Depending on the selected Power-Down mode, the following will occur:

- V_{OUT} pin is switched to one of the two resistive pull-downs:
  - 100 kΩ (typical)
  - 1 kΩ (typical)
- Op amp is powered down and the V_{OUT} pin becomes high-impedance

The power-down Configuration bits (PDnB:PDnA) control the power-down operation (Table).

TABLE 4-6: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD

PDnB	PDnA	Function
0	0	Normal operation
0	1	1 kΩ resistor to ground
1	0	100 kΩ resistor to ground
1	1	Open circuit

There is a delay (T_{PDD}) between the PD1:PD0 bits changing from '00' to either '01', '10' or '11' and the op amp no longer driving the V_{OUT} output and the pull-down resistor's sinking current.

Table 4-7 shows the current sources for the DAC based on the selected source of the DAC's reference voltage and if the device is in normal operating mode or one of the Power-Down modes. In any of the Power-Down modes, where the V_{OUT} pin is not externally connected (sinking or sourcing current), as the number of DACs increases, the device's power-down current will also increase.

TABLE 4-7: DAC CURRENT SOURCES

Device V_{DD} Current Source	PDnB:nA = 00, VRnB:nA =				PDnB:nA ≠ 00, VRnB:nA =			
	00	01	10	11	00	01	10	11
Output Op Amp	Y	Y	Y	Y	N	N	N	N
Resistor Ladder	Y	Y	N(1)	Y	N	N	N(1)	N
V_{REF} Selection Buffer	N	Y	N	Y	N	N	N	N
Band Gap	N	Y	N	N	N(2)	Y(2)	N(2)	N(2)

Note 1: The current is sourced from the V_{REF} pin, not the device V_{DD}.
2: If DAC0 and DAC1 are in one of the Power-Down modes, MTP write operations are not recommended.

The power-down bits are modified by using commands that write to the volatile power-down register or a POR event, which transfers the nonvolatile power-down register to the volatile power-down register.

Section 4.6, "Device Commands" describes the I^2C commands for writing the power-down bits. The commands that can update the volatile PDnB:PDnA bits are:

- Write
- General Call Reset
- General Call Wake-Up

Note 1: The I^2C serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the I^2C host device.
2: A General Call Reset will do the POR event sequence, except that the MTP shadow memory values will be transfered to the volatile memory registers.

4.4.5.1 Exiting Power-Down

The following events change the PD1:PD0 bits to '00' and therefore exit the Power-Down mode. These are:

- Any I^2C write command, where the PD1:PD0 bits are '00'
- I^2C General Call Wake-Up command
- I^2C General Call Reset command

When the device exits Power-Down mode, the following occur:

- Disabled internal circuits are turned on
- Resistor ladder is connected to the selected reference voltage (V_{RL})
- Selected pull-down resistor is disconnected
- The V_{OUT} output is driven to the voltage represented by the volatile DAC register's value and Configuration bits

The DAC wiper register and DAC wiper value may be different due to the DAC wiper register being modified while the $\overline{LAT}$ pin was driven to (and remaining at) V_{IH}.

The V_{OUT} output signal requires time as these circuits are powered up and the output voltage is driven to the specified value, as determined by the volatile DAC register and Configuration bits.

Note: Since the op amp and resistor ladder are powered off (0V), the op amp's input voltage (V_W) can be considered as 0V. There is a delay (T_{PDE}) between the PDnB:PDnA bits updating to '00' and the op amp driving the V_{OUT} output. The op amp's settling time (from 0V) needs to be taken into account to ensure the V_{OUT} voltage reflects the selected value.

TABLE 4-8: DAC INPUT CODE VS. CALCULATED ANALOG OUTPUT (V_{OUT}) (V_{DD} = 5.0V)

Device	Volatile DAC Register Value	V_{RL} (1)	LSb		Gain Selection (2)	V_{OUT} (3)	
			Equation	µV		Equation	V
MCP47CVB2X (12-bit)	1111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} * (4095/4096) * 1	4.998779
		2.5V	2.5V/4096	610.4	1x	V_{RL} * (4095/4096) * 1	2.499390
					2x (2)	V_{RL} * (4095/4096) * 2)	4.998779
	0111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} * (2047/4096) * 1)	2.498779
		2.5V	2.5V/4096	610.4	1x	V_{RL} * (2047/4096) * 1)	1.249390
					2x (2)	V_{RL} * (2047/4096) * 2)	2.498779
	0011 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} * (1023/4096) * 1)	1.248779
		2.5V	2.5V/4096	610.4	1x	V_{RL} * (1023/4096) * 1)	0.624390
					2x (2)	V_{RL} * (1023/4096) * 2)	1.248779
	0000 0000 0000	5.0V	5.0V/4096	1,220.7	1x	V_{RL} * (0/4096) * 1)	0
		2.5V	2.5V/4096	610.4	1x	V_{RL} * (0/4096) * 1)	0
					2x (2)	V_{RL} * (0/4096) * 2)	0
MCP47CVB1X (10-bit)	11 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} * (1023/1024) * 1	4.995117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} * (1023/1024) * 1	2.497559
					2x (2)	V_{RL} * (1023/1024) * 2	4.995117
	01 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} * (511/1024) * 1	2.495117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} * (511/1024) * 1	1.247559
					2x (2)	V_{RL} * (511/1024) * 2	2.495117
	00 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} * (255/1024) * 1	1.245117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} * (255/1024) * 1	0.622559
					2x (2)	V_{RL} * (255/1024) * 2	1.245117
	00 0000 0000	5.0V	5.0V/1024	4,882.8	1x	V_{RL} * (0/1024) * 1	0
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} * (0/1024) * 1	0
					2x (2)	V_{RL} * (0/1024) * 1	0
MCP47CVB0X (8-bit)	1111 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} * (255/256) * 1	4.980469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} * (255/256) * 1	2.490234
					2x (2)	V_{RL} * (255/256) * 2	4.980469
	0111 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} * (127/256) * 1	2.480469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} * (127/256) * 1	1.240234
					2x (2)	V_{RL} * (127/256) * 2	2.480469
	0011 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} * (63/256) * 1	1.230469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} * (63/256) * 1	0.615234
					2x (2)	V_{RL} * (63/256) * 2	1.230469
	0000 0000	5.0V	5.0V/256	19,531.3	1x	V_{RL} * (0/256) * 1	0
		2.5V	2.5V/256	9,765.6	1x	V_{RL} * (0/256) * 1	0
					2x (2)	V_{RL} * (0/256) * 2	0

Note 1: V_{RL} is the resistor ladder's reference voltage. It is independent of the VRnB:VRnA selection.

2: Gain selection of 2x (Gn = 1) requires the voltage reference source to come from the V_{REF} pin (VRnB:VRnA = 10 or 11) and requires the V_{REF} pin voltage (or V_{RL}) ≤ V_{DD}/2 or from the internal band gap (VRnB:VRnA = 01).

3: These theoretical calculations do not take into account the offset, gain and nonlinearity errors.

4.5 Serial Communication Interface

4.5.1 I²C SERIAL INTERFACE MODULE

4.5.1.1 Overview

The MCP47CXBX4/8's I²C serial interface module supports the I²C serial protocol specification. This I²C interface is a two-wire interface (clock and data). Figure 4-10 shows a typical I²C interface connection.

The I²C specification only defines the field types, lengths, timings, etc., of a frame. The frame content defines the behavior of the device. The frame content (commands) for the MCP47CXBX4/8 is defined in **Section 4.6, "Device Commands"**.

An overview of the I²C protocol is available in **Appendix B:, "I²C Serial Interface"**.

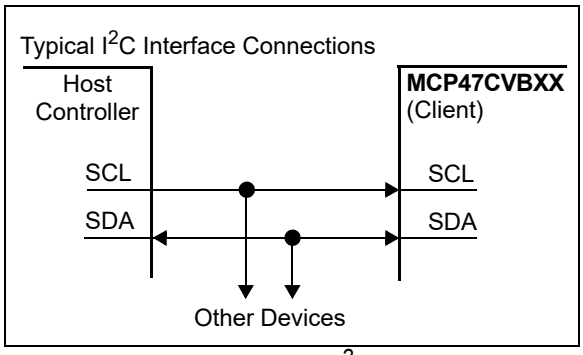


FIGURE 4-10: *Typical I²C Interface.*

This section discusses some of the specific characteristics of the MCP47CXBX4/8 devices' I²C serial interface module. This is to assist in the development of your application.

The following sections discuss some of these device-specific characteristics.

- **Interface Pins (SCL and SDA)**
- **Communication Data Rates**
- **POR/BOR**
- **Device Memory Address**
- **General Call Commands**
- **Device I²C Client Addressing**
- **Custom I²C Client Address Options**

4.5.1.2 Interface Pins (SCL and SDA)

The MCP47CXBX4/8 I²C module SCL pin does not generate the serial clock since the device operates in Client mode. Also, the MCP47CXBX4/8 will not stretch the clock signal (SCL) since memory read access occurs fast enough.

The MCP47CXBX4/8 I²C module implements slope control on the SDA pin output driver.

4.5.1.3 Communication Data Rates

The I²C interface specifies different communication bit rates. These are referred to as Standard, Fast or High-Speed modes. The MCP47CXBX4/8 supports these three modes. The clock rates (bit rate) of these modes are:

- Standard mode: up to 100 kHz (Kbit/s)
- Fast mode: up to 400 kHz (Kbit/s)
- High-Speed mode (HS mode): up to 3.4 MHz (Mbit/s)

A description on how to enter High-Speed mode is in **Section 4.5.1.12, "Entering High-Speed (HS) Mode"**.

4.5.1.4 POR/BOR

On a POR/BOR event, the I²C serial interface module state machine is reset, which includes forcing the device's memory address pointer to 00h.

4.5.1.5 Device Memory Address

The memory address is the 5-bit value that specifies the location in the device's memory that the specified command will operate on.

On a POR/BOR event, the device's memory address pointer is forced to 00h.

The MCP47CXBX4/8 retains the last received device memory address. That is, the MCP47CXBX4/8 does not corrupt the device memory address after repeated Start or Stop conditions.

4.5.1.6 General Call Commands

The General Call commands utilize the I²C specification reserved General Call command address and command codes. The MCP47CXBX4/8 also implements a nonstandard General Call command.

The General Call commands are:

- **General Call Reset**
- **General Call Wake-Up** (MCP47CXBX4/8 defined)

The General Call Wake-Up command will cause all the MCP47CXBX4/8 devices to exit their Power-Down state.

4.5.1.7 Multi-Host Systems

The MCP47CXBX4/8 is not a host device (generates the interface clock), but it can be used in multi-host applications.

4.5.1.8 Slope Control

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed Clock modes of the interface.

4.5.1.9 Pulse Gobbler

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes < 10 ns during HS mode.

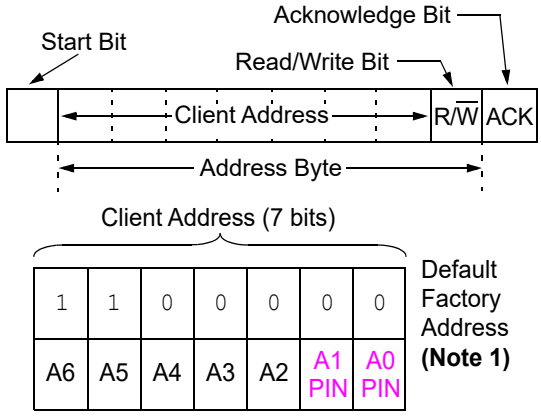
4.5.1.10 Device I²C Client Addressing

The address byte is the first byte received following the Start (or Repeated Start) condition from the host device (see Figure 4-11).

The default address for all devices is '110 0000'. The lower two bits of the address are determined by the state of the A1 and A0 pins. Leaving the pins not connected will default for a value of '0'.

For volatile devices (MCP47CVBXX), the I²C client address bits, A6:A2, are fixed ('110 00'). The user still has client address programmability with the A1:A0 address pins.

For nonvolatile devices, the five upper bits of the I²C client address are MTP and can be programmed during the user's manufacturing flow.



Note 1: Address bits (A6:A2) can be programmed by the user on nonvolatile devices. Bits A1 and A0 are determined by the A0 and A1 pin values.

FIGURE 4-11: *Client Address Bits in the I²C Control Byte.*

4.5.1.11 Custom I²C Client Address Options

Custom I²C client address options can be requested. Users can request the custom I²C client address via the Nonstandard Customer Authorization Request (NSCAR) process.

Note: Non-Recurring Engineering (NRE) charges and minimum ordering requirements for custom orders. Please contact Microchip sales for additional information.
A custom device will be assigned custom device marking.

MCP47CXBX4/8

4.5.1.12 Entering High-Speed (HS) Mode

The I^2C specification requires that a High-Speed mode device be activated to operate in High-Speed (3.4 Mbit/s) mode. This is done by the host sending a special address byte following the Start bit.

The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next Stop condition.

The host code is sent as follows:

1. Start condition (S).
2. High-Speed Host Mode Code ('0000 1xxx'); the 'xxx' bits are unique to the High-Speed (HS) Host mode.
3. No Acknowledge ($\overline{A}$).

After switching to High-Speed mode, the next transferred byte is the I^2C Control byte, which specifies the device to communicate with and any number of data bytes plus acknowledgments. The host device can then either issue a repeated Start bit to address a different device (at High-Speed mode) or a Stop bit to return to the bus Fast/Standard Speed mode. After the Stop bit, any other host device (in a multi-host system) can arbitrate for the I^2C bus.

The MCP47CXBX4/8 device does not acknowledge the HS select byte. However, upon receiving this command, the device switches to HS mode.

See Figure 4-12 for an illustration of the HS mode command sequence.

For more information on the HS mode, or other I^2C modes, refer to the *"NXP I^2C Specification"*.

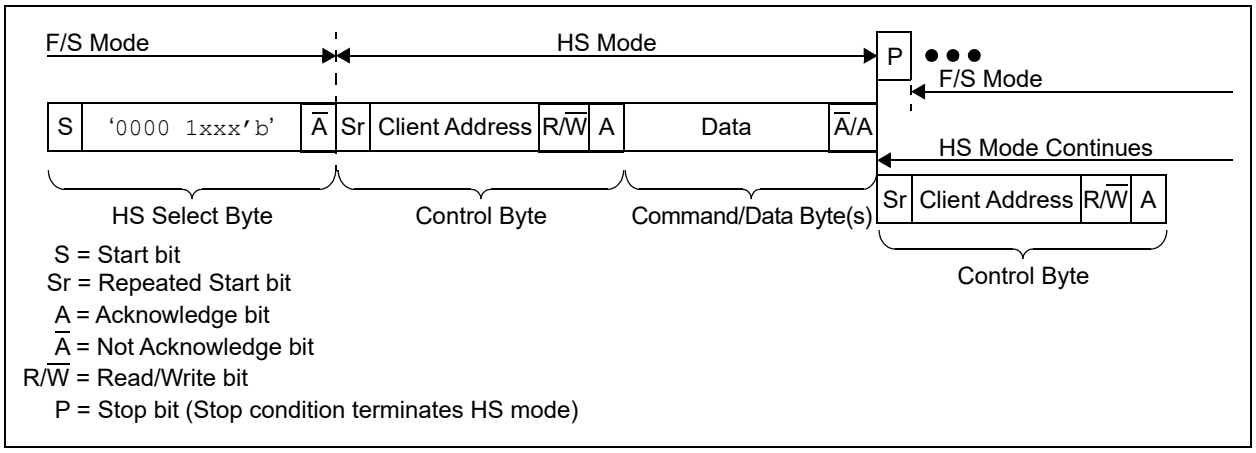


FIGURE 4-12: *HS Mode Sequence.*

4.6 Device Commands

4.6.1 OVERVIEW

The I²C protocol does not specify how commands are formatted, so this section specifies the MCP47CXBX4/8 device's I²C command formats and operation.

The commands can be grouped into the following categories:

- Write commands (C1:C0 = 00)
- Read commands (C1:C0 = 11)
- General Call commands

The supported commands are shown in Table 4-9. These commands allow both single data or continuous data operation. Continuous data operation means that the I²C host does not generate a Stop bit but repeats the required data/clocks. This allows faster updates since the overhead of the I²C control byte is removed. Table 5-1 also shows the required number of bit clocks for each command's different mode of operation and the estimated maximum output update rate.

TABLE 4-9: DEVICE COMMANDS

Command	Code		Mode
	C1	C0	
Write Command	0	0	Single
	0	0	Continuous
Read Command	1	1	Single
	1	1	Continuous
	1	1	Last Address
General Call Reset	—	—	Single
General Call Wake-Up	—	—	Single

4.6.1.1 Read Commands

Read commands are used to transfer data from the desired memory location to the host controller. The read command format writes two bytes (Control byte (R/$\overline{W}$ bit) = 0) and the read command byte (desired memory address and the read command). Then, a Restart condition is followed by a second Control byte, but this Control byte indicates an I²C read operation (R/$\overline{W}$ bit = 1). The host will then supply 16 clocks so the specified address data are transfered. See **Section 4.6.3, "Read Command"** for a full description of the read commands.

4.6.1.2 Write Commands

Write commands are used to transfer data to the desired memory location (from the host controller). The modes are Single or Continuous. The Continuous mode format allows the fastest data update rate for the device's memory locations.

See **Section 4.6.2, "Write Command"** for a full description of the write commands.

Note:	The 8-bit data devices use the same format as 10-bit and 12-bit devices. This allows code migration compatibility at the cost of nine extra clock cycles per data byte transferred.

4.6.1.3 General Call Commands

The General Call commands utilize the I²C specification reserved General Call command address and command codes. The General Call Reset command format is specified by the *"NXP I²C Specification"*. The General Call Wake-Up command is a Microchip-defined format.

I²C devices acknowledge the general call address command (0x00 in the first byte). The meaning of the general call address is always specified in the second byte. The I²C specification does not allow '00000000' (00h) in the second byte. Also, the '00000100' and '00000110' functionality is defined by the *"NXP I²C Specification"*. Lastly, a data byte with a '1' in the LSb indicates a "Hardware General Call".

Refer to the *"NXP I²C Specification"* for more details on the general call specifications.

The MCP47CXBX4/8 devices support the following I²C general calls:

- General Call Reset
- General Call Wake-Up

See **Section 4.6.4.1, "General Call Reset"** for a full description of the General Call Reset command and the General Call Wake-Up command.

4.6.1.4 Aborting a Transmission

A Restart or Stop condition in an expected data bit position will abort the current command sequence and if the command is a write, that data word will not be written to the MCP47CXBX4/8. Also, the I²C state machine will be reset.

4.6.2 WRITE COMMAND

The write command can be issued to both volatile and nonvolatile memory locations. Write commands can also be structured as either single or continuous. The continuous format allows the fastest data update rate for the device's memory locations.

Writing to volatile or nonvolatile memory uses the same command format, shown in Figure 4-13 (single) and Figure 4-15 (continuous); for example, ACK/NACK behavior (see Figure 4-14). During device communication, if the device address/command combination is invalid or an unimplemented device address is specified, then the MCP47CXBX4/8 will NACK that byte. To reset the I^2C internal state machine, the I^2C communication module must detect a Start bit.

4.6.2.1 Single Write to Volatile Memory

For volatile memory locations, data are written to the MCP47CXBX4/8 after every data word transfer (16 bits), during the rising edge of the last data bit. If a Stop or Restart condition is generated during a data transfer, before the last data bit is received, the data will not be written to the MCP47CXBX4/8. After the A bit, the host can initiate the next sequence with a Stop or Restart condition.

A write command to a volatile memory location changes that location after a properly formatted write command is received and the rising edge of the D00 bit (last data bit) clock is detected.

Writes to volatile memory locations depend on the state of their respective WiperLock technology bits.

Writes to a volatile DAC register will not transfer to the output register until the associated $\overline{LAT}$n pin is transitioned to the V_{IL} voltage.

4.6.2.2 Single Write to Nonvolatile Memory (HVC Pin = V_{IL} or V_{IH})

During normal operation, the MTP memory addresses cannot be written. Writing to the MTP address space, while the HVC pin is not at V_{IHH}, does not have any effect; the command is acknowledged but the memory is not modified.

4.6.2.3 Single Write to Nonvolatile Memory (HVC Pin = V_{IHH})

Writing to the MTP memory requires to have the HVC pin at V_{IHH}= 7.5V. This is designed for factory programming of configuration parameters and is not considered a normal operating condition of the device.

The sequence to write to a single nonvolatile memory location is the same as a single write to volatile memory, with the exception that the MTP write cycle (t_{wc}) is started after a properly formatted command, including the Stop bit, is received. After the Stop condition occurs, the serial interface may immediately be re-enabled by initiating a Start condition.

The HVC pin voltage must be held at V_{IHH} until the completion of the MTP write cycle (t_{wc}).

During an MTP write cycle, access to the volatile memory is allowed, when using the appropriate command sequence. Commands that address nonvolatile memory are ignored until the MTP write cycle (t_{wc}) completes. This allows the host controller to operate on the volatile DAC registers.

Once a write command to a nonvolatile memory location is received, no other commands must be received before the Stop condition occurs. If a Stop condition does not occur, then the NV write command is not executed and all following commands will have an error condition ($\overline{A}$). Also, writes to a NV memory location while an MTP write cycle is occurring will force an error condition ($\overline{A}$).

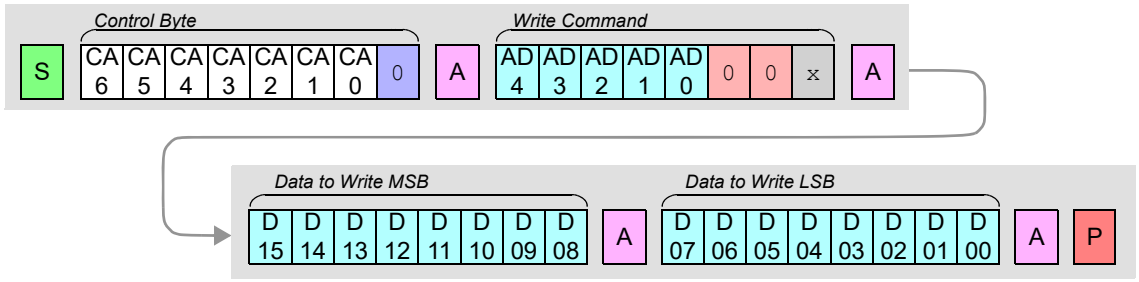
A Start bit is required to reset the command state machine.

4.6.2.4 Continuous Writes to Volatile Memory

A Continuous Write mode of operation is possible when writing to the device's volatile memory registers (see Table 4-1). This Continuous Write mode allows writes without a Stop or Restart condition or repeated transmissions of the I^2C Control byte. Figure 4-15 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address. The sequence ends with the host sending a Stop or Restart condition.

4.6.2.5 Continuous Writes to Nonvolatile Memory

If a continuous write is attempted on nonvolatile memory, the missing Stop condition will cause the command to be an error condition ($\overline{A}$) on all following bytes. A Start bit is required to reset the command state machine. All bytes are ignored and not transferred to memory.



Legend:

S	I^2C Start Bit	A	I^2C ACK bit(1)	x	Reserved, must be set to '0'
CA *n*	I^2C Client Address	AD *n*	Memory Address	D *nn*	Register Data (to be written)(2)
0	I^2C Write Bit	0 0	Write Command	P	I^2C Stop Bit(3)

Note 1: The Acknowledge bit is generated by the MCP47CXBX4/8.

2: At the rising edge of the SCL signal for the last bit (D00) of the write command, the device updates the value of the specified device register. For DAC output registers, the output voltage depends on the state of the $\overline{LAT}$ pin.

3: This command sequence does not need to terminate (using the Stop bit) and the write command can be repeated (see the continuous write format, **Section 4.6.2.4, "Continuous Writes to Volatile Memory"**).

FIGURE 4-13: *Write Single Address Command Format.*

Write 1 Word Command

	S	Client Address							R/W	ACK	Command									ACK	Data Byte									ACK	Data Byte									ACK	P
Host	S	CA6	CA5	CA4	CA3	CA2	CA1	CA0	0	A/A	AD4	AD3	AD2	AD1	AD0	C1	C0	x	A/A	D15	D14	D13	D12	D11	D10	D09	D08	A/A	D07	D06	D05	D04	D03	D02	D01	D00	A/A	P

Example 1 (No Command Error)

Host	S	1	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	x	1	d	d	d	d	d	d	d	d	1	d	d	d	d	d	d	d	d	1	P
MCP47CXBX4/8									0										0									0									0		
I^2C Bus	S	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	x	0	d	d	d	d	d	d	d	d	0	d	d	d	d	d	d	d	d	0	P

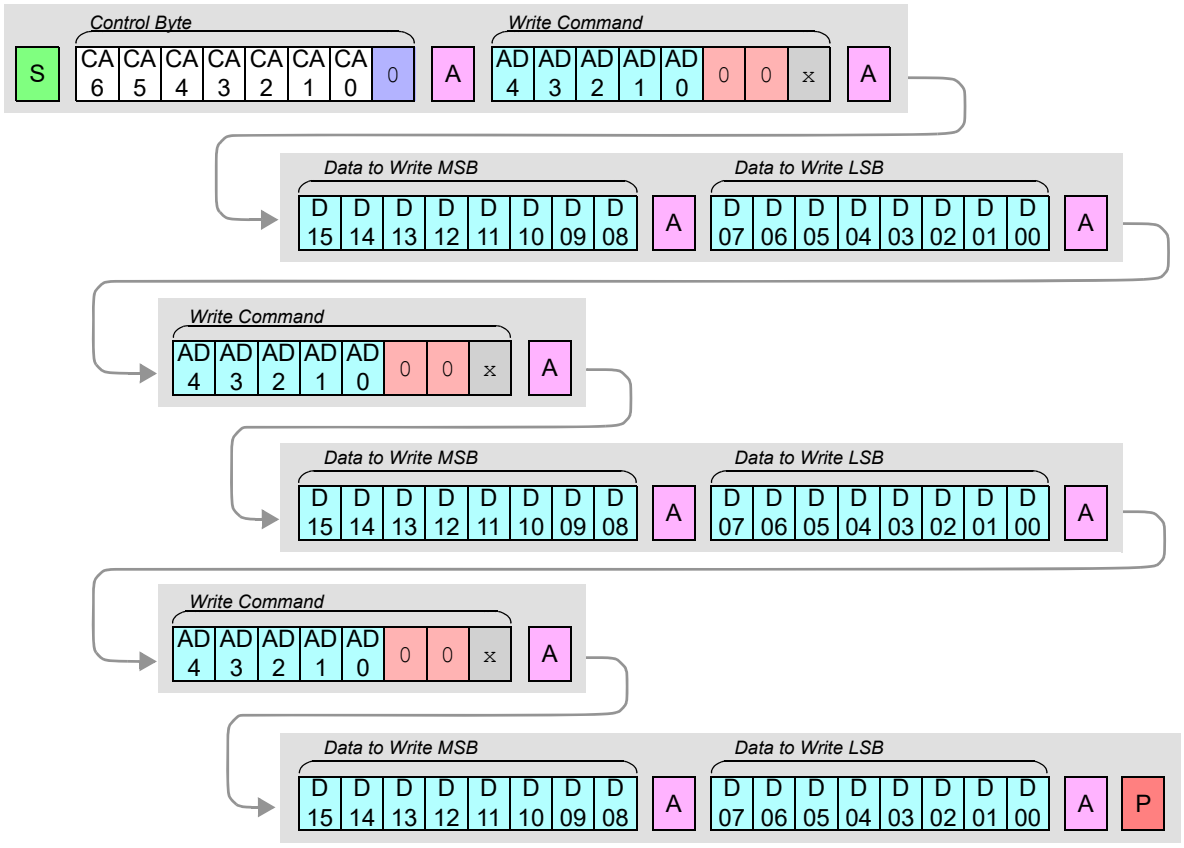
Example 2 (Command Error)

Host	S	1	1	0	0	0	0	0	0	1	0	1	1	1	1	0	0	x	1	d	d	d	d	d	d	d	d	1	d	d	d	d	d	d	d	d	1	P
MCP47CXBX4/8									0										1									1									1		
I^2C Bus	S	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	x	0	d	d	d	d	d	d	d	d	1	d	d	d	d	d	d	d	d	1	P

Note: Once a command error occurs (Example 2), the MCP47CVBXX will NACK until a Start condition occurs.

FIGURE 4-14: *I^2C ACK/NACK Behavior (Write Single Address Command Example).*

MCP47CXBX4/8



Legend:

S	I²C Start Bit	A	I²C ACK Bit(1)	x	Reserved, must be set to '0'
CA *n*	I²C Client Address	AD *n*	Memory Address	D *nn*	Register Data (to be written)(2)
0	I²C Write Bit	0 0	Write Command	P	I²C Stop Bit(3)

Note 1: The Acknowledge bit is generated by the MCP47CXBX4/8.

2: At the falling edge of the SCL pin for the write command ACK bit, the MCP47CXBX4/8 device updates the value of the specified device register.

3: This command sequence does not need to terminate (using the Stop bit) and the write command can be repeated (see the continuous write format, **Section 4.6.2.4, "Continuous Writes to Volatile Memory"**).

4: Only functions when writing to volatile registers (AD4:AD0 = 00h through 0Ah).

FIGURE 4-15: *Continuous Write Command Format (Volatile Memory Only).*

4.6.3 READ COMMAND

Read commands are used to transfer data from the specified memory location to the host controller.

The read command can be issued to both volatile and nonvolatile memory locations.

The read command formats include:

- **Read Single Memory Address**
  - **Read Single Memory Address**
  - **Read Last Accessed Memory Address**
- **Continuous Read Commands**

During an MTP memory write cycle, the read command can only read the volatile memory locations. By reading the Status register (0Ah), the host controller can determine when the write cycle (t_{WC}) is completed (via the state of the MTPMA bit).

The MCP47CXBX4/8 retains the last received device memory address. This means the MCP47CXBX4/8 does not corrupt the device memory address after repeated Start or Stop conditions.

The read commands operate the same regardless of the state of the High-Voltage command (HVC) signal.

If a $\overline{LAT}$ pin is high (V_{IH}), reads of the corresponding volatile DAC wiper register return the current output value, not the internal register value.

During device communication, if the device address/command combination is invalid or an unimplemented address is specified, the MCP47CXBX4/8 will NACK that byte. To reset the I^2C state machine, the I^2C communication module must detect a Start bit.

4.6.3.1 Read Single Memory Address

The read single specified memory address command writes two bytes, the Control byte and the Read Command byte (desired internal memory location address and the read command bits), and then a Restart condition must be issued. Then, a second Control byte is transmitted, but this control byte indicates an I^2C read operation (R/$\overline{W}$ bit = 1).

Figure 4-16 shows the sequence for reading a single specified memory address.

4.6.3.2 Read Last Accessed Memory Address

This is useful for checking the status of the MTPMA bit or when writes to other I^2C devices on the bus must occur between these memory reads. The host must send a Stop or Restart condition after the data word is sent from the client. Figure 4-17 shows the waveforms for a single read of the last memory location accessed.

4.6.3.3 Continuous Read Commands

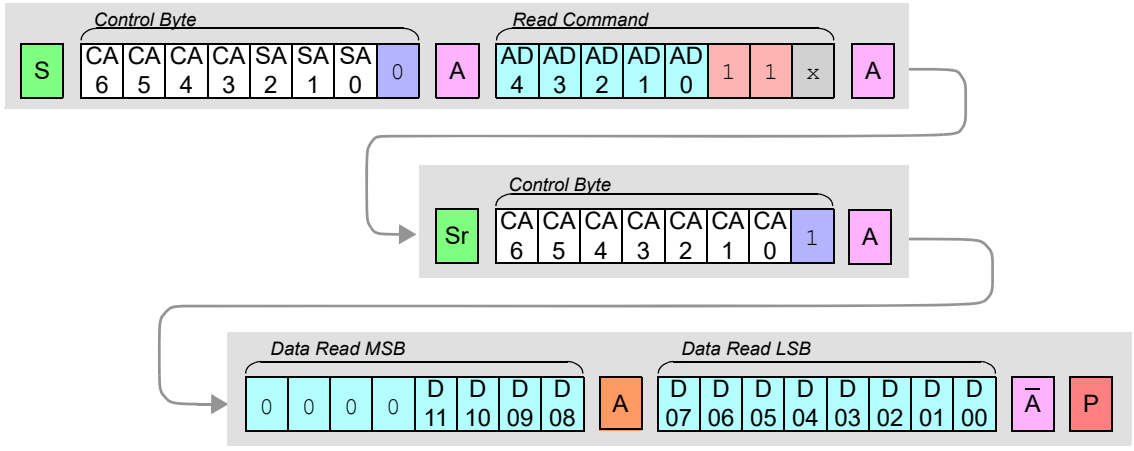
Continuous read commands allow the device's memory to be read quickly and are valid for all memory locations. Figure 4-19 shows the sequence for three continuous reads.

For continuous reads, instead of transmitting a Stop or Restart condition after the data transfer, the host continually reads the data byte. The sequence ends with the host Not Acknowledging and then sending a Stop or Restart.

4.6.3.4 Ignoring an I^2C Transmission and "Falling Off" the Bus

The MCP47CXBX4/8 expects to receive complete, valid I^2C commands and will assume any command not defined as a valid command is due to a bus corruption, thus entering a passive high condition on the SDA signal. All signals will be ignored until the next valid Start condition and Control byte are received.

MCP47CXBX4/8



Legend:

S	I²C Start Bit	AD *n*	Memory Address(5)	1	I²C Read Bit	P	I²C Stop Bit(3)
CA *n*	I²C Client Address	1 1	Read Command	D *nn*	Data (read from memory)		
0	I²C Write Bit	x	Reserved, set to '0'	A	I²C ACK Bit(2)		
A	I²C ACK Bit(1)	Sr	I²C Start Bit, Repeated	Ā	I²C NACK Bit(4)		

Note 1: The host device is responsible for the A/Ā signal. If an Ā signal occurs, the MCP47CXBX4/8 will abort this transfer and release the bus.

2: This Acknowledge bit is generated by the host device.

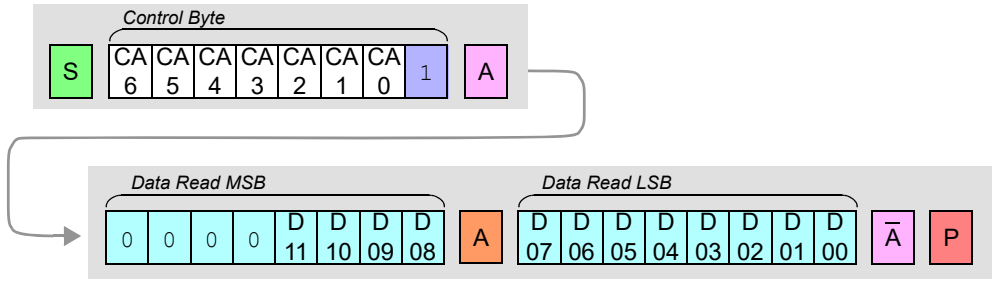
3: This command sequence does not need to terminate (using the Stop bit) and the read command can be repeated (see **Section 4.6.3.3, "Continuous Read Commands"**).

4: The host device will Not Acknowledge and the MCP47CXBX4/8 will release the bus so the host device can generate a Stop or a repeated Start condition.

5: The MCP47CXBX4/8 retains the last received device memory address.

6: The non-data bits of the Read Data Word will be output as '0's:
for 12-bit devices, bits D15:D12 are '0'
for 10-bit devices, bits D15:D10 are '0'
for 8-bit devices, bits D15:D08 are '0'

FIGURE 4-16: *Read Single Specified Memory Address Command Format.*



Legend:

S	I²C Start Bit	1	I²C Read Bit	Ā	I²C NACK Bit(4)
CA *n*	I²C Client Address	D *nn*	Data (read from memory)	P	I²C Stop Bit(3)
A	I²C ACK Bit(1)	A	I²C ACK Bit(2)		

Note 1: The host device is responsible for the A/Ā signal. If an Ā signal occurs, the MCP47CXBX4/8 will abort this transfer and release the bus.

2: This Acknowledge bit is generated by the host device.

3: This command sequence does not need to terminate (using the Stop bit) and the read command can be repeated (see **Section 4.6.3.3, "Continuous Read Commands"**).

4: The host device will Not Acknowledge and the MCP47CXBX4/8 will release the bus so the host device can generate a Stop or a repeated Start condition.

5: The MCP47CXBX4/8 retains the last received device memory address.

6: The non-data bits of the Read Data Word will be output as '0's:
for 12-bit devices, bits D15:D12 are '0'
for 10-bit devices, bits D15:D10 are '0'
for 8-bit devices, bits D15:D08 are '0'

7: If the last device address written (via the read or write command) is invalid for a read, then the read last memory address command will NACK due to the invalid device memory address.

FIGURE 4-17: *Read Last Memory Address Accessed Command Format.*

MCP47CXBX4/8

Read 1 Word Command

	S	Client Address	R/W	ACK	Command	ACK
Host	S	CA6 CA5 CA4 CA3 CA2 CA1 CA0	0	1	AD4 AD3 AD2 AD1 AD0 C1 C0 x	1

	Sr	Client Address	R/W	ACK	Data Byte	ACK	Data Byte	ACK	P
Host (Continued)	Sr	CA6 CA5 CA4 CA3 CA2 CA1 CA0	1	1	D15 D14 D13 D12 D11 D10 D09 D08	1	D07 D06 D05 D04 D03 D02 D01 D00	1	P

Example 1 (No Command Error)

Host	S	1 1 0 0 0 0 0	0	1	0 0 0 0 1 1 1 x	1
MCP47CXBX4/8				0		0
I²C Bus	S	1 1 0 0 0 0 0	0	0	0 0 0 0 0 1 1 x	0

Host (Continued)	S	0 0 0 0 1 0 0	1	1		1		1	P
MCP47CXBX4/8 (Continued)				0	d d d d d d d d	0	d d d d d d d d	0	
I²C Bus (Continued)	S	0 0 0 0 0 0 0	1	0	d d d d d d d d	0	d d d d d d d d	0	P

Example 2 (Command Error)

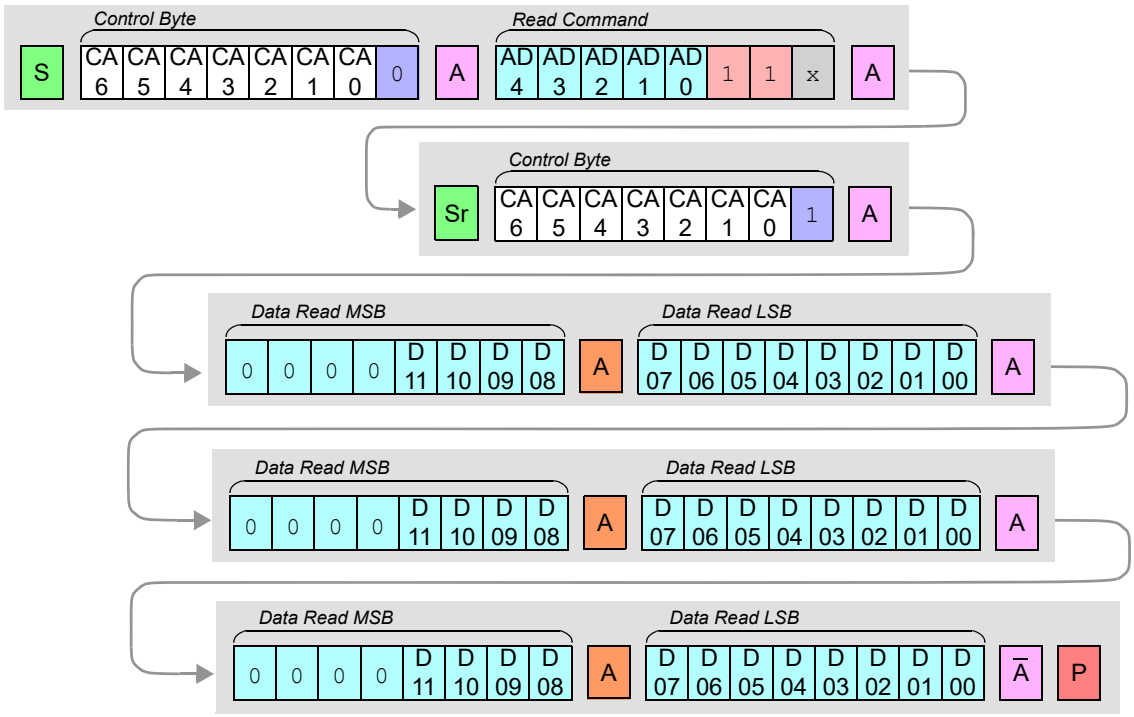
Host	S	1 1 0 0 0 0 0	0	1	0 1 1 1 1 0 0 x	1
MCP47CXBXX				0		1
I²C Bus	S	1 1 0 0 0 0 0	0	0	0 1 1 1 1 0 0 x	1

Host (Continued)	S	1 1 0 0 0 0 0	1	1		1		1	P
MCP47CXBX4/8 (Continued)				0	? ? ? ? ? ? ? ?	0	? ? ? ? ? ? ? ?	1	
I²C Bus (Continued)	S	1 1 0 0 0 0 0	1	0	? ? ? ? ? ? ? ?	0	? ? ? ? ? ? ? ?	1	P

Note 1: Once a command error occurs (Example 2), the MCP47CXBX4/8 will NACK until a Start condition occurs.

2: For a command error case (Example 2), the data read is from the register of the last valid address loaded into the device.

FIGURE 4-18: *I^2C ACK/NACK Behavior (Read Command Example).*



Legend:

S	I^2C Start Bit	AD *n*	Memory Address(5)	1	I^2C Read Bit	P	I^2C Stop Bit(3)
CA *n*	I^2C Client Address	1 1	Read Command	D *nn*	Data (read from memory)		
0	I^2C Write Bit	x	Reserved, set to '0'	A	I^2C ACK Bit(2)		
A	I^2C ACK Bit(1)	Sr	I^2C Start Bit, Repeated	Ā	I^2C NACK Bit(4)		

Note 1: The host device is responsible for the A/$\overline{A}$ signal. If an $\overline{A}$ signal occurs, the MCP47CXBX4/8 will abort this transfer and release the bus.

2: This Acknowledge bit is generated by the host device.

3: This command sequence does not need to terminate (using the Stop bit) and the read command can be repeated (see **Section 4.6.3.3, "Continuous Read Commands"**).

4: The host device will Not Acknowledge and the MCP47CXBX4/8 will release the bus so the host device can generate a Stop or repeated Start condition.

5: The MCP47CXBX4/8 retains the last received device memory address.

6: The non-data bits of the Read Data Word will be output as '0's:
for 12-bit devices, bits D15:D12 are '0'
for 10-bit devices, bits D15:D10 are '0'
for 8-bit devices, bits D15:D08 are '0'

FIGURE 4-19: *Continuous Read of Specified Address Command Format.*

MCP47CXBX4/8

4.6.4 GENERAL CALL COMMANDS

The MCP47CXBX4/8 acknowledges the General Call Address command (00h in the first byte). General Call commands can be used to communicate to all devices on the I²C bus (at the same time) that understand the General Call command. The meaning of the general call address is always specified in the second byte (see Figure 4-20).

If the second byte has a '1' in the LSb, the specification intends this to indicate a "Hardware General Call". The MCP47CXBX4/8 will ignore this byte and all following bytes (and $\overline{A}$), until a Stop bit (P) is encountered.

The MCP47CXBX4/8 devices support the following I²C General Call commands:

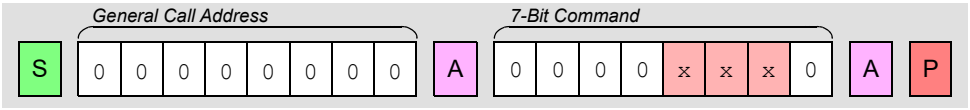
- **General Call Reset** (06h)
- **General Call Wake-Up** (0Ah)

The General Call Reset command format is specified by the I²C specification. The General Call Wake-Up command is a Microchip-defined format. The General Call Wake-Up command will have all devices wake up (that is, exit the Power-Down mode).

The other two I²C specification command codes (04h and 00h) are not supported and therefore, those commands are Not Acknowledged.

If these 7-bit commands conflict with other I²C devices on the bus, the user will need two I²C buses to ensure that the devices are on the correct bus for their desired application functionality.

Note: Refer to the *"NXP Specification"*, #UM10204, Rev. 6 document for more details on the general call specifications. The I²C specification does not allow '00000000' (00h) in the second byte.



Legend:

S I²C Start Bit — A I²C ACK Bit(1) — x x x GC Command — P I²C Stop Bit(2,3)

Note 1: The Acknowledge bit is generated by the MCP47CXBX4/8.

2: This command sequence does not need to terminate (using the Stop bit) and the General Call command can be repeated or another General Call command can be sent. Only the first command will be accepted by the MCP47CXBX4/8.

FIGURE 4-20: *General Call Formats.*

4.6.4.1 General Call Reset

The I²C General Call Reset command forces a reset event. This is similar to the Power-On Reset, except that the Reset Delay Timer is not started. This command allows multiple devices to be reset synchronously.

The device performs a General Call Reset if the second byte is '00000110' (06h). At the acknowledgment of this byte, the device will perform the following tasks:

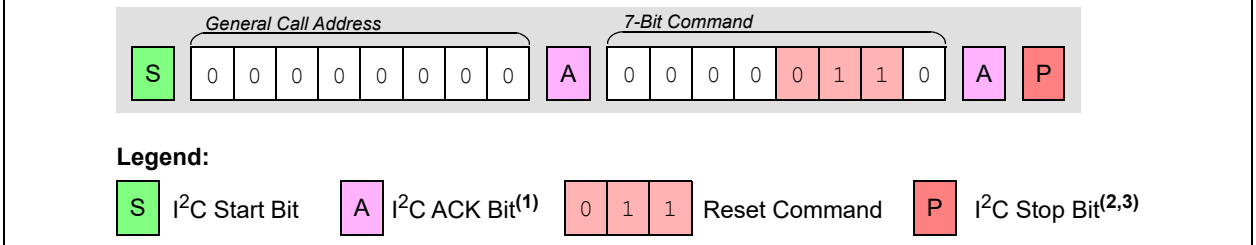
- Internal reset similar to a POR. The contents of the MTP are loaded into the DAC registers.
- Analog output (V_{OUT}) is available after the POR sequence is completed.

4.6.4.2 General Call Wake-Up

The I²C General Call Wake-Up command forces the device to exit its Power-Down state (forces the PDnB:PDnA bits to '00'). This command allows multiple MCP47CXBX4/8 devices to wake up synchronously.

The device performs a General Call Wake-Up if the second byte (after the general call address) is '00001010' (0Ah). At the acknowledgment of this byte, the device will perform the following task:

- The device's volatile power-down bits (PDnB:PDnA) are forced to '00'.

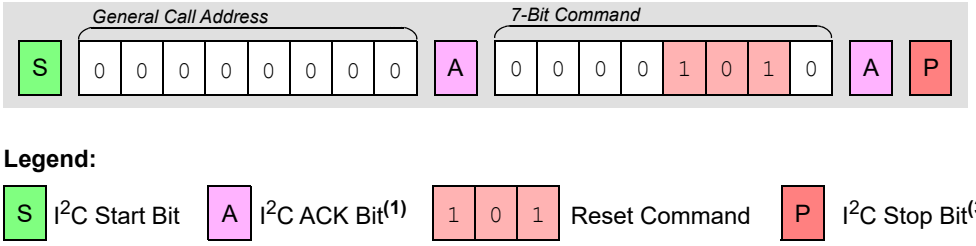


Note 1: The Acknowledge bit is generated by the MCP47CXBX4/8.

2: At the falling edge of the SCL pin for the General Call Reset command ACK bit, the MCP47CXBX4/8 device is reset.

3: This command sequence does not need to terminate (using the Stop bit) and the General Call Reset command can be repeated or the General Call Wake-Up command can be sent. Only the first command will be accepted by the MCP47CXBX4/8.

FIGURE 4-21: *General Call Reset Command.*



Note 1: The Acknowledge bit is generated by the MCP47CXBX4/8.

2: At the rising edge of the last data bit for the General Call Wake-Up command, the volatile power-down bits (PDnB:PDnA) are forced to '00'.

3: This command sequence does not need to terminate (using the Stop bit) and the General Call Wake-Up command can be repeated or the General Call Reset command can be sent.

FIGURE 4-22: *General Call Wake-Up Command.*

NOTES:

5.0 APPLICATIONS INFORMATION

The MCP47CXBX4/8 devices are general purpose, quad/octal-channel voltage output DACs for various applications where a precision operation with low power and nonvolatile memory is needed.

Since the devices include an MTP memory, they can be utilized in applications that require the output to return to the previous setup value on subsequent power-ups. The 32-times programmable MTP memory offers the possibility of factory or field calibration of the DAC, in the application circuit. The configurable I^2C address, combined with the dedicated pins, offers the possibility of having more than one DAC on the same bus, while increasing the interconnection compatibility with other device types, which do not have a user-programmable address.

Applications generally suited for the devices are:

- Digitally Controlled Power Supplies
- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery-Powered)
- Motor Control

5.1 I^2C Bus Connection Considerations

5.1.1 CONNECTING TO THE I^2C BUS USING PULL-UP RESISTORS

The SCL and SDA pins of the MCP47CXBX4/8 devices are open-drain configurations. These pins require a pull-up resistor, as shown in Figure 5-3.

The pull-up resistor values (R_1 and R_2) for SCL and SDA pins depend on the operating speed (standard, fast and high speed) and loading capacitance of the I^2C bus line. A higher value of the pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus line. Therefore, it can limit the bus operating speed. The lower resistor value, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long metal traces or multiple device connections to the bus line, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for Standard and Fast modes and less than 1 kΩ for High-Speed mode.

5.1.2 DEVICE CONNECTION TEST

The user can test the presence of the device on the I^2C bus line using a simple I^2C command. This test can be achieved by checking an acknowledge response from the device after sending a read or write command.

Figure 5-1 shows an example with a read command.

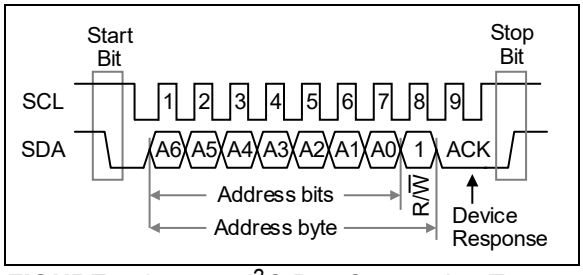


FIGURE 5-1: *I^2C Bus Connection Test.*

The steps are:

1. Set the R/$\overline{W}$ bit "High" in the device's address byte.
2. Check the ACK bit of the address byte. If the device acknowledges (ACK = 0) the command, the device is connected. Otherwise, it is not connected.
3. Send the Stop bit.

5.1.3 SOFTWARE I^2C INTERFACE RESET SEQUENCE

Note: This technique is documented in AN1028.

At times, it may become necessary to perform a Software Reset Sequence to ensure the device is in a correct and known I^2C interface state. This technique only resets the I^2C state machine.

This is useful if the device powers-up in an incorrect state (due to excessive bus noise, etc) or if the host device is reset during communication. Figure 5-2 shows the communication sequence to software reset the device.

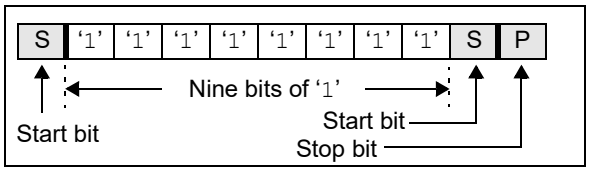


FIGURE 5-2: *Software Reset Sequence Format.*

The first Start bit will cause the device to reset from a state in which it is expecting to receive data from the host device. In this mode, the device monitors the data bus in Receive mode and can detect if the Start bit forces an internal reset.

The nine bits of '1' are used to force a reset of those devices that could not be reset by the previous Start bit. This occurs only if the device is driving an A bit on the I^2C bus or is in Output mode (from a read command) and is driving a data bit of '0' onto the I^2C bus. In both cases, the previous Start bit could not be generated due to the device holding the bus low. By sending out nine '1' bits, it is ensured that the device will see an $\overline{A}$ bit (the host device does not drive the I^2C bus low to acknowledge the data sent by the MCP47CXBX4/8), which also forces the device to reset.

The second Start bit is sent to address the rare possibility of an erroneous write. This can occur if the host device is reset while sending a write command to the MCP47CXBX4/8 and then as the host device returns to normal operation and issues a Start condition, while the MCP47CXBX4/8 is issuing an acknowledge. In this case, if the second Start bit is not sent (and the Stop bit was sent), the MCP47CXBX4/8 can initiate a write cycle.

Note:	The potential for this erroneous write ONLY occurs if the host device is reset while sending a write command to the MCP47CXBX4/8.

The Stop bit terminates the current I^2C bus activity. The MCP47CXBX4/8 waits to detect the next Start condition.

This sequence does not affect any other I^2C devices which may be on the bus, as they should disregard this as an invalid command.

5.1.4 OUTPUT UPDATE RATE

The supported commands and their associate clock cycles are shown in Table 5-1. The table also indicates the theoretical maximum update rate for different I^2C bus speeds.

Note:	The output update rate also depends on the slew rate and output load. The values in the table are calculated neglecting other influencing factors and must be used for orientation only.

TABLE 5-1: DEVICE COMMANDS – NUMBER OF CLOCKS

Command				# of Bit Clocks(1)	Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second)			Comments
Operation	Code		Mode		100 kHz	400 kHz	3.4 MHz(3)	
	C1	C0						
Write Command(4)	0	0	Single	38	2,632	10,526	89,474	
	0	0	Continuous	27n + 11	3,559	14,235	120,996	For ten data words
Read Command	1	1	Random	48	2,083	8,333	70,833	
	1	1	Continuous	18n + 11	4,762	19,048	161,905	For ten data words
	1	1	Last Address	29	3,448	13,793	117,241	
General Call Reset	—	—	Single	20	5,000	20,000	170,000	Note 2
General Call Wake-Up	—	—	Single	20	5,000	20,000	170,000	Note 2

Note 1: "n" indicates the number of times the command operation is to be repeated.

2: Determined by the General Call command byte after the I^2C general call address.

3: There is a minimal overhead to enter the 3.4 MHz mode.

4: This command can be at either normal or high voltage. A high-voltage command requires the HVC pin to be at V_{IHH} for the entire command, until the completion of the MTP cycle.

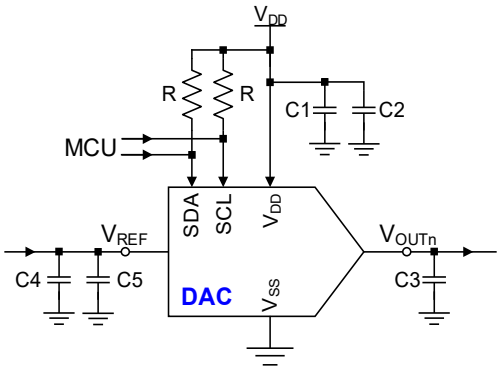
5.2 Power Supply Considerations

The power source must be as clean as possible. Any noise induced on the V_{DD} line can affect the DAC performance.

Typical applications will require a bypass capacitor in order to filter out high-frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity.

If the internal V_{DD} is selected as the resistor ladder's reference voltage (VRnB:VRnA = `00`), the power supply to the device is also used for the DAC voltage reference internally.

Figure 5-3 shows an example of using bypass capacitors to improve performance. The capacitors must be chosen according to the intended application and other external components used in the circuit.



Comp.	Value	Comments
R	5 kΩ - 10 kΩ	f_{SCL} = 100 kHz to 400 kHz
	~700Ω	f_{SCL} = 3.4 MHz
C1	0.1 µF	Ceramic
C2	10 µF	Tantalum or ceramic
C3	0.1 µF	Optional to reduce transition noise on the output (ceramic)
C4	0.1 µF	Ceramic
C5	10 µF	Optional: tantalum or ceramic

FIGURE 5-3: *Example Circuit.*

A ceramic 0.1 µF capacitor must be placed as close to the V_{DD} pin as possible (within 4 mm). If the power supply lacks proper stabilization, another higher value capacitor, tantalum or ceramic, can be added on the application board to reduce supply variations that could have an influence on the output.

When the DAC is in External Reference mode (VRnB:VRnA = `11` or `10`), if using a dedicated voltage reference chip, the capacitors must be chosen according to the external reference specifications. If the reference voltage is derived from a source with significant noise, a similar decoupling scheme as for V_{DD} can be used.

For Internal Band Gap mode (VRnB:VRnA = `01`), the V_{REF} pin must be left floating and surrounded with a ground guard structure to attenuate parasitic noise. A small capacitor can be used to further reduce the possibility of external noise pick-up.

If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the device must reside on the analog plane.

5.3 Output Circuit Design Considerations

The MCP47CXBX4/8 has a buffered output. This means that no filtering is required on the V_{OUT} pin in most cases. There are some applications where a slower rise time or protection against glitches is required, for example in power supplies. In those particular cases, an extra capacitor can be added on the output, that will smooth out any transition noise that may happen during operation.

Refer to the Output Amplifier section in the **DC Characteristics** table for details about the internal precision operational amplifier used on the output.

5.3.1 DRIVING RESISTIVE AND CAPACITIVE LOADS

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications). V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended to use a load with R_L greater than 2 kΩ.

Driving large capacitive loads can cause stability problems for voltage feedback output amplifiers. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the V_{OUT} pin's voltage does not quickly follow the buffer's input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the V_{OUT} pin.

So, when driving large capacitive loads with the output buffer, a small series resistor (R_{ISO}) at the output (see Figure 5-4) improves the output buffer's stability (feedback loop's phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

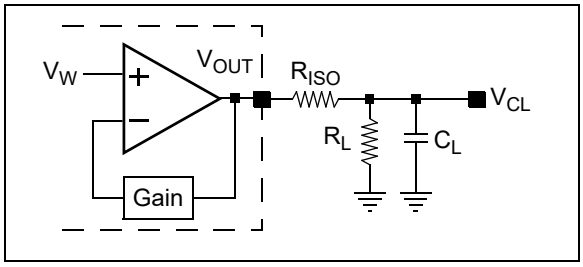


FIGURE 5-4: *Circuit to Stabilize the Output Buffer for Large Capacitive Loads (C_L).*

The R_{ISO} resistor value for the circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this R_{ISO} resistor value must be verified on the bench. Modify the R_{ISO}'s resistance value until the output characteristics meet your requirements.

A method to evaluate the system's performance is to inject a step voltage on the V_{REF} pin and observe the V_{OUT} pin's characteristics.

Note:	Additional insight into circuit design for driving capacitive loads can be found in *AN884, "Driving Capacitive Loads With Op Amps"* (DS00884).

5.4 Layout Considerations

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **PCB Area Requirements**

5.4.1 NOISE

Particularly harsh environments may require shielding of critical signals. Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP47CXBX4/8's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR).

Multilayer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing.

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors must be terminated to the analog ground plane.

Note:	Breadboards and wire-wrapped boards are not recommended.

5.4.2 PCB AREA REQUIREMENTS

In some applications, the PCB area is a criteria for device selection. Table 5-2 shows the typical package dimensions and area for the different package options.

TABLE 5-2: PACKAGE FOOTPRINT(1)

Package			Package Footprint		
Pins	Type	Code	Dimensions (mm)		Area (mm^2)
			Length	Width	
20	TSSOP	ST	6.50	6.40	41.60
20	QFN	ML	4.00	4.00	16.00

Note 1: Does not include recommended land pattern dimensions. Dimensions are typical values.

6.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups:

- **Development Tools**
- **Technical Documentation**

6.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP47CXBX4/8 devices. The currently available tools are shown in Table 6-1.

Figure 6-1 shows how the TSSOP20EV bond-out PCB can be populated to easily evaluate the MCP47CXBX4/8 devices. Device evaluation can use the PICkit™ Serial Analyzer to control the DAC output registers and state of the Configuration, Control and Status register.

The TSSOP20EV boards may be purchased directly from the Microchip website at www.microchip.com.

6.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs and Design Guides. Table 6-2 shows some of these documents.

TABLE 6-1: DEVELOPMENT TOOLS (Note 1)

Board Name	Part #	Comment
20-Pin TSSOP and SSOP Evaluation Board	TSSOP20EV	Most flexible option - recommended bond-out PCB

Note 1: Supports the PICkit™ Serial Analyzer. See the User's Guide for additional information and requirements.

TABLE 6-2: TECHNICAL DOCUMENTATION

Application Note Number	Title	Literature #
AN1326	Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications	DS01326
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

MCP47CXBX4/8

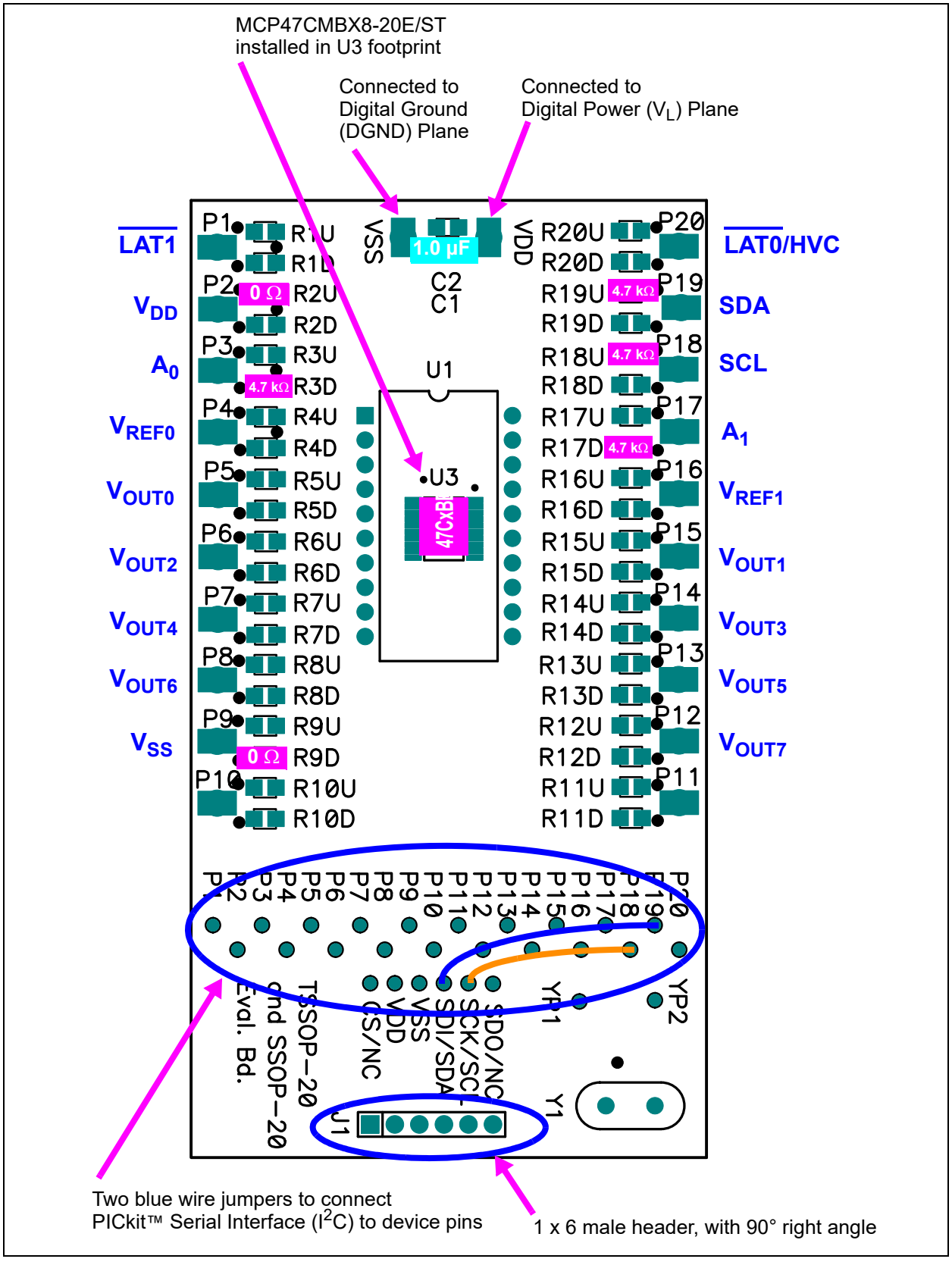
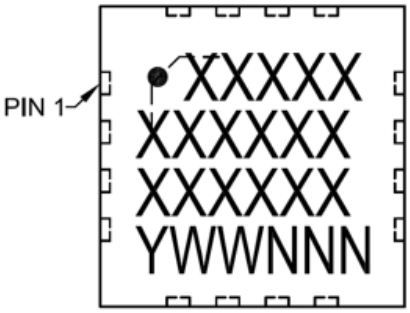


FIGURE 6-1: *MCP47CXBX4/8 Evaluation Board Circuit Using TSSOP20EV.*

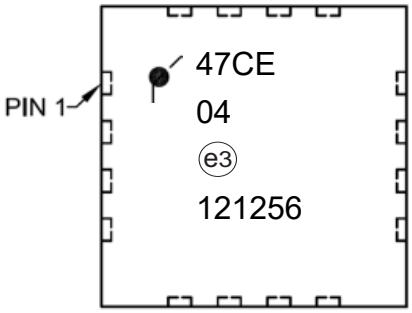
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

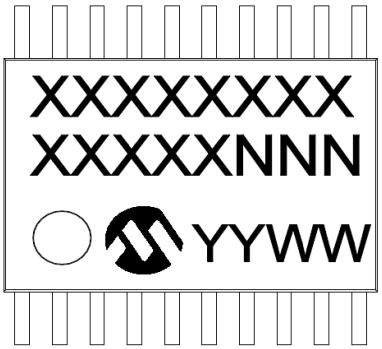
20-Lead 4 mm x 4 mm QFN



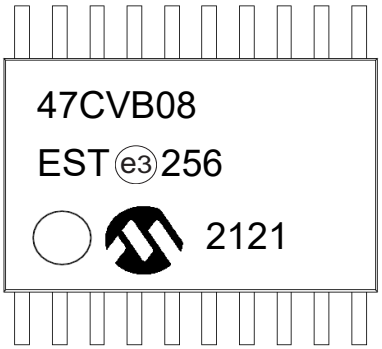
Example



20-Lead TSSOP



Example



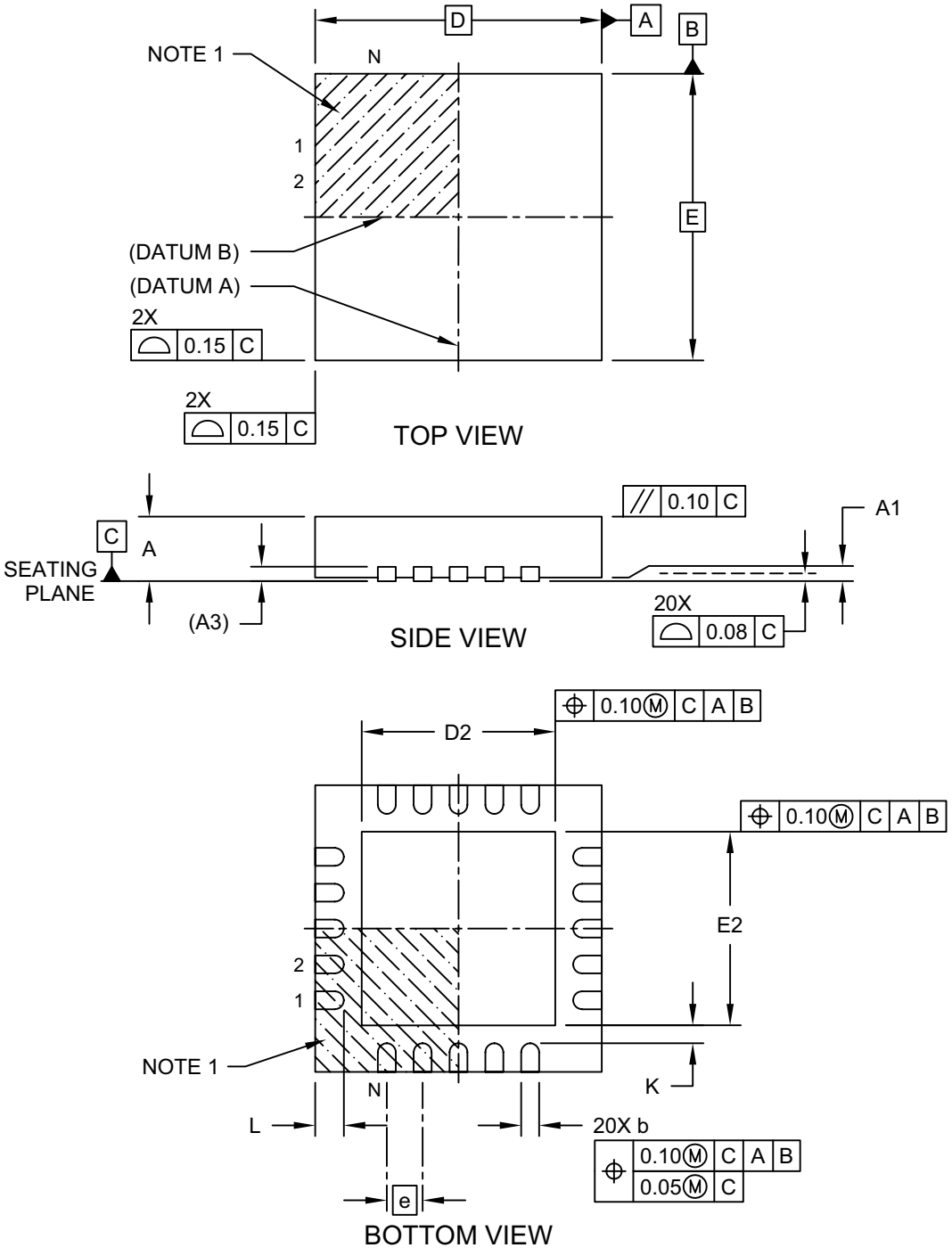
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP47CXBX4/8

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
Also called VQFN

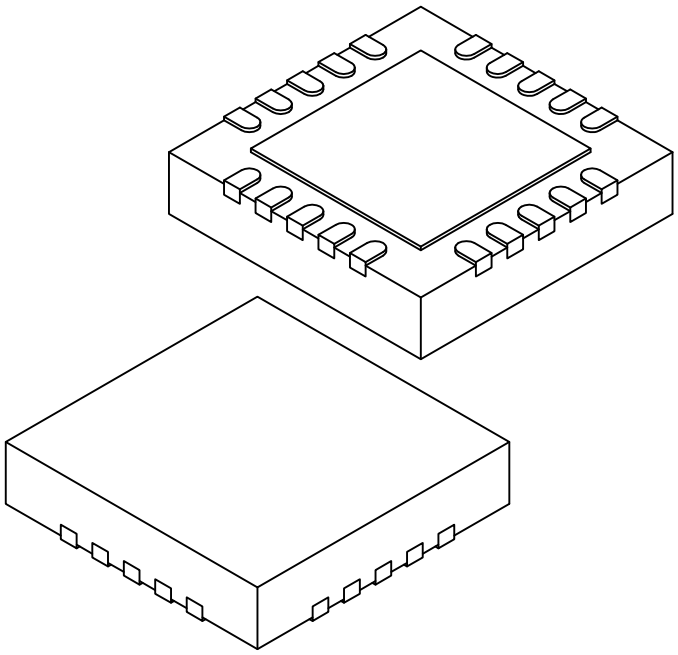
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-126 Rev C Sheet 1 of 2

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
Also called VQFN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

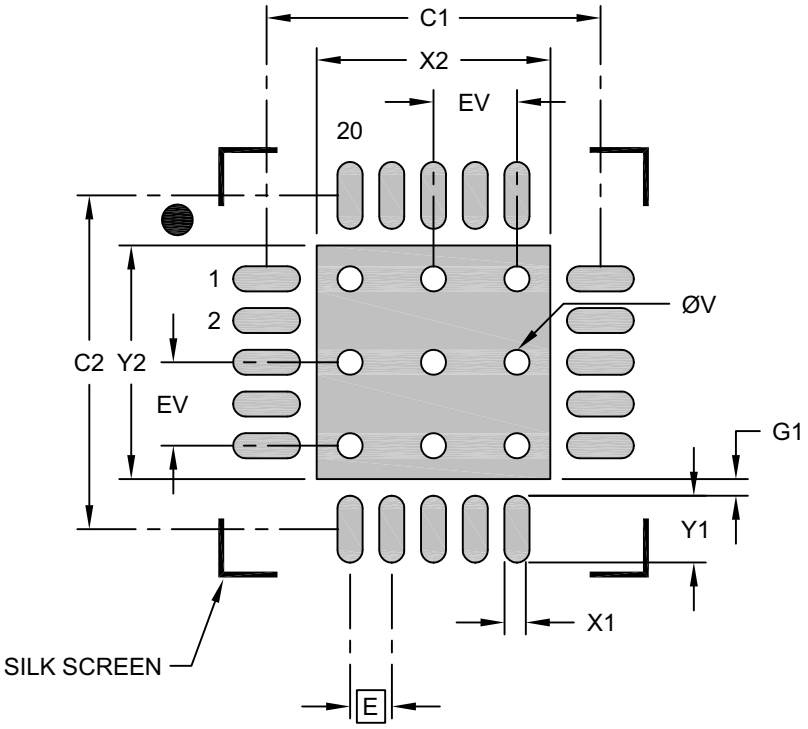
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126 Rev C Sheet 2 of 2

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
Also called VQFN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X16)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

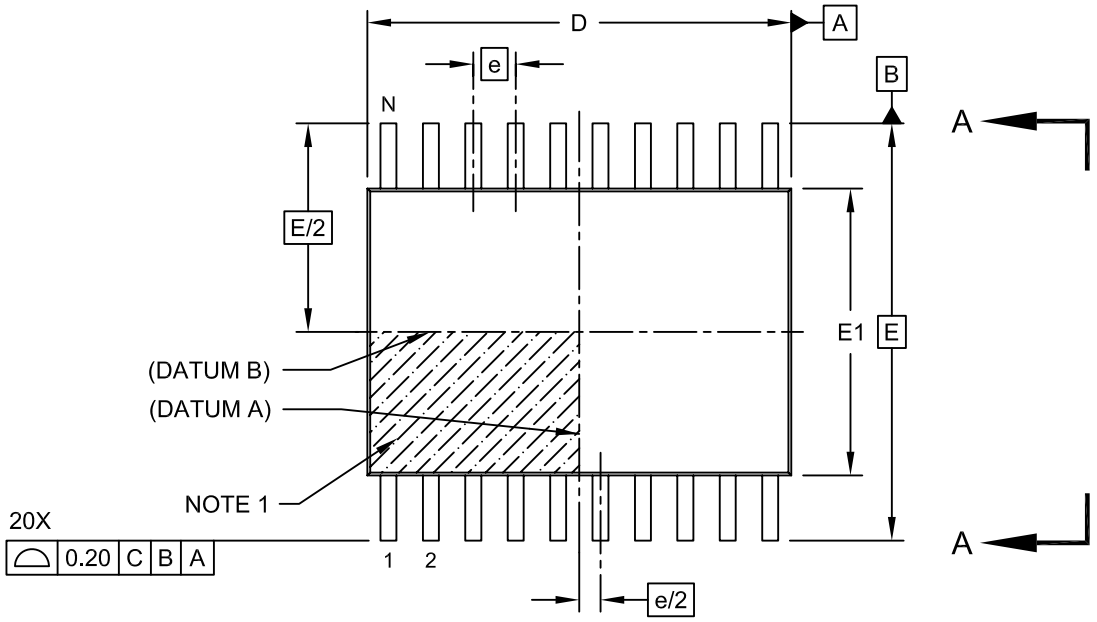
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

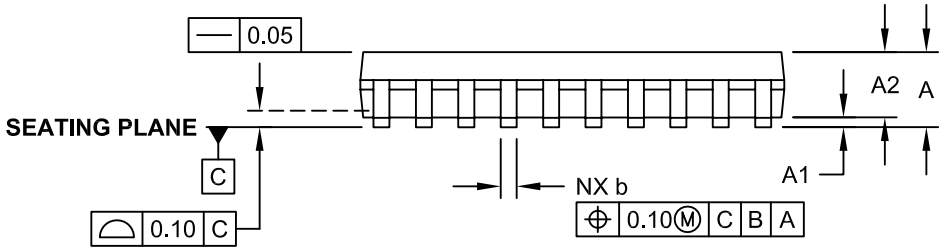
Microchip Technology Drawing C04-2126 Rev B

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

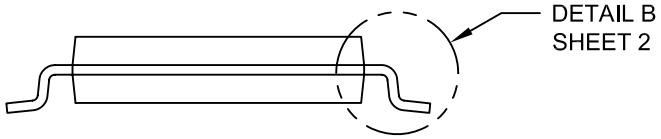
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

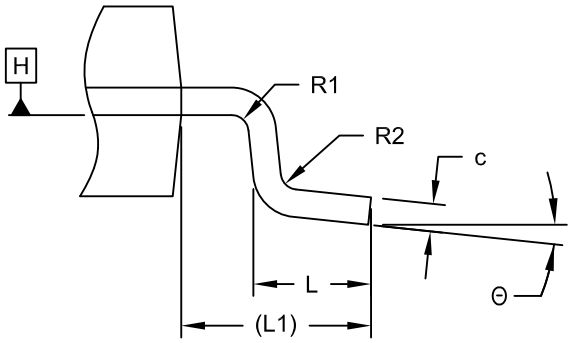


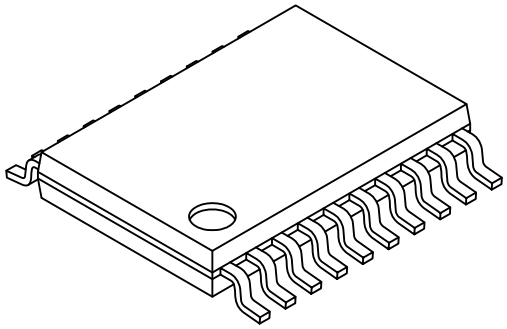
VIEW A—A

Microchip Technology Drawing C04-088C Sheet 1 of 2

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	6.40	6.50	6.60
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	Θ	0°	-	8°
Lead Width	b	0.19	-	0.30
Lead Thickness	c	0.09	-	0.20
Bend Radius	R1	0.09	-	-
Bend Radius	R2	0.09	-	-

Notes:

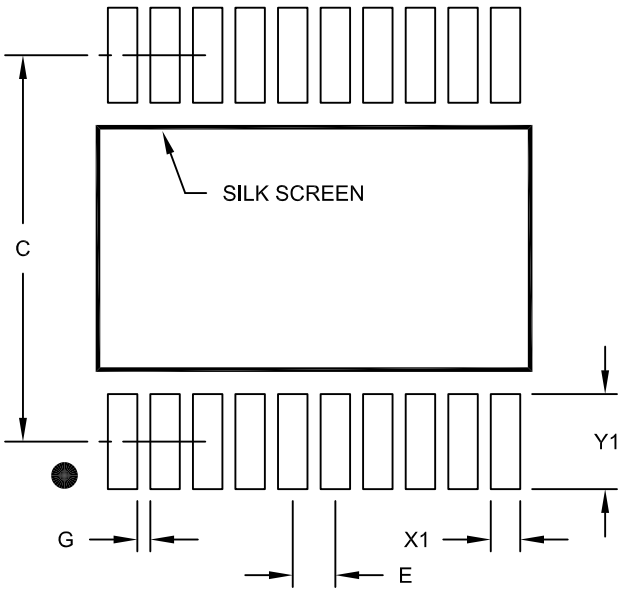
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-088C Sheet 2 of 2

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2088A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (July 2021)

The following is the list of modifications:

- Updated the TSSOP package drawing in **Section 7.1, "Package Marking Information"**.

Revision A (June 2021)

- Original release of this document.

Note: The I^2C standard uses the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client", respectively.

NOTES:

APPENDIX B: I²C SERIAL INTERFACE

This I²C is a two-wire interface that allows multiple devices to be connected to the two-wire bus. Figure B-1 shows a typical I²C interface connection.

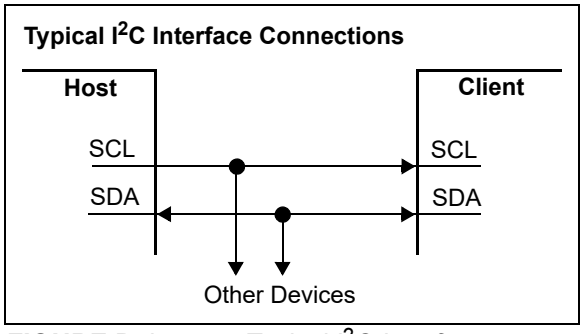


FIGURE B-1: *Typical I²C Interface.*

B.1 Overview

A device that sends data onto the bus is defined as a transmitter and a device receiving data is defined as a receiver. The bus has to be controlled by a host device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions. Devices that do not generate a Serial Clock work as client devices. Both host and client can operate as transmitter or receiver, but the host device determines which mode is activated. Communication is initiated by the host (microcontroller), which sends the Start bit followed by the client address byte. The first byte transmitted is always the client address byte, which contains the device code, the address bits and the R/$\overline{W}$ bit.

The I²C interface specifies different communication bit rates. These are referred to as Standard, Fast or High-Speed modes and the MCP47CXBX4/8 supports these three modes. The clock rates (bit rate) of these modes are:

- Standard mode: up to 100 kHz (Kbit/s)
- Fast mode: up to 400 kHz (Kbit/s)
- High-Speed mode (HS mode): up to 3.4 MHz (Mbit/s)

The I²C protocol supports two addressing modes:

- 7-bit Client Addressing
- 10-bit Client Addressing (allows more devices on the I²C bus)

Only 7-bit Client Addressing will be discussed in this section.

The I²C serial protocol allows multiple host devices on the I²C bus. This is referred to as “multi-host”. For this, all host devices must support the multi-host operation. In this configuration, all host devices monitor their communication. If they detect that they wish to transmit a bit that is a logic high, but is detected as a logic low (some other host device driving), they “get off” the bus. That is, they stop their communication and continue to listen to determine if the communication is directed towards them.

The I²C serial protocol only defines the field types, field lengths, timings, etc., of a frame. The frame content defines the behavior of the device. For details on the frame content (commands/data), see **Section 4.6, “Device Commands”**.

The I²C serial protocol defines some commands, called General Call Addressing, which allow the host device to communicate to all client devices on the I²C bus.

Note:	Refer to the *“NXP Specification #UM10204”*, Rev. 06 document for more details on the I²C specifications.

B.2 Signal Descriptions

The I²C interface uses two pins (signals):

- SDA (Serial Data)
- SCL (Serial Clock)

B.2.1 SERIAL DATA (SDA)

The Serial Data (SDA) signal is the data signal of the device. The value on this pin is latched on the rising edge of the SCL signal when the signal is an input.

With the exception of the Start (Restart) and Stop conditions, the high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. During the high period of the clock, the SDA pin's value (high or low) must be stable. Changes in the SDA pin's value while the SCL pin is high will be interpreted as a Start or Stop condition.

B.2.2 SERIAL CLOCK (SCL)

The Serial Clock (SCL) signal is the clock signal of the device. The rising edge of the SCL signal latches the value on the SDA pin.

Depending on the Clock Rate mode, the interface will display different characteristics.

B.3 I²C Operation

B.3.1 I²C BIT STATES AND SEQUENCE

Figure B-8 shows the I²C transfer sequence, while Figure B-7 shows the bit definitions. The SCL is generated by the host. The following definitions are used for the bit states:

- Start Bit (S)
- Data Bit
- Acknowledge (A) Bit (driven low)/
  No Acknowledge ($\overline{A}$) bit (not driven low)
- Repeated Start Bit (Sr)
- Stop Bit (P)

B.3.1.1 Start Bit

The Start bit (see Figure B-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is high.

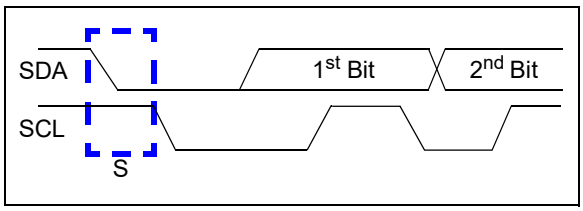


FIGURE B-2: *Start Bit.*

B.3.1.2 Data Bit

The SDA signal may change state while the SCL signal is low. While the SCL signal is high, the SDA signal MUST be stable (see Figure B-3).

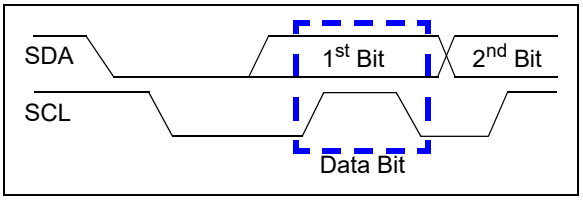


FIGURE B-3: *Data Bit.*

B.3.1.3 Acknowledge (A) Bit

The A bit (see Figure B-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically, the client device will supply an A response after the Start bit and eight data bits are received. An A bit has the SDA signal low, while the $\overline{A}$ bit has the SDA signal high.

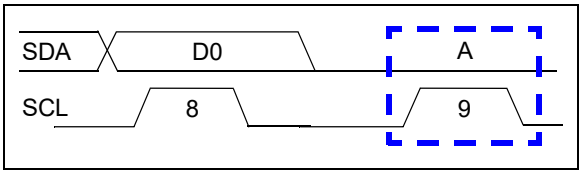


FIGURE B-4: *Acknowledge Waveform.*

Table B-1 shows some of the conditions where the client device issues the A or Not A ($\overline{A}$).

If an error condition occurs (such as an $\overline{A}$ instead of A), a Start bit must be issued to reset the command state machine.

TABLE B-1: MCP47CXBX4/8 A/$\overline{A}$ RESPONSES

Event	Acknowledge Bit Response	Comment
General Call	A	
Client Address Valid	A	
Client Address Not Valid	$\overline{A}$	
Bus Collision	N/A	I²C module resets or is a "Don't Care" if the collision occurs on the host's Start bit

B.3.1.4 Repeated Start Bit

The Repeated Start bit (see Figure B-5) indicates the current host device wishes to continue communicating with the current client device without releasing the I^2C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is high.

Note 1: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another host is attempting to transmit a data '1'.

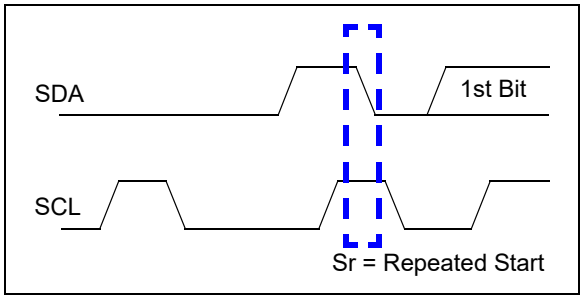


FIGURE B-5: *Repeated Start Condition Waveform.*

B.3.1.5 Stop Bit

The Stop bit (see Figure B-6) Indicates the end of the I^2C data transfer sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is high.

A Stop bit must reset the I^2C interface of the client device.

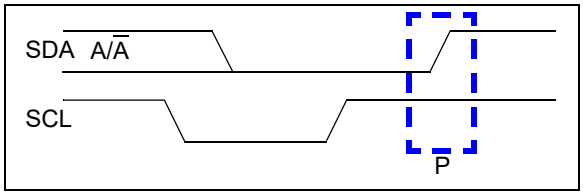


FIGURE B-6: *Stop Condition Receive or Transmit Mode.*

B.3.2 CLOCK STRETCHING

Clock stretching is something the receiving device can do, to allow additional time to respond to the received data.

B.3.3 ABORTING A TRANSMISSION

If any part of the I^2C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a Start or Stop condition. This is done so that noisy transmissions (usually an extra Start or Stop condition) are aborted before they corrupt the device.

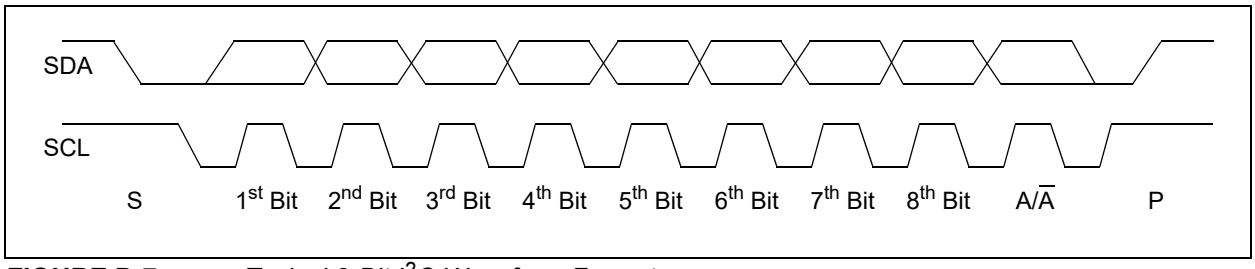


FIGURE B-7: *Typical 8-Bit I^2C Waveform Format.*

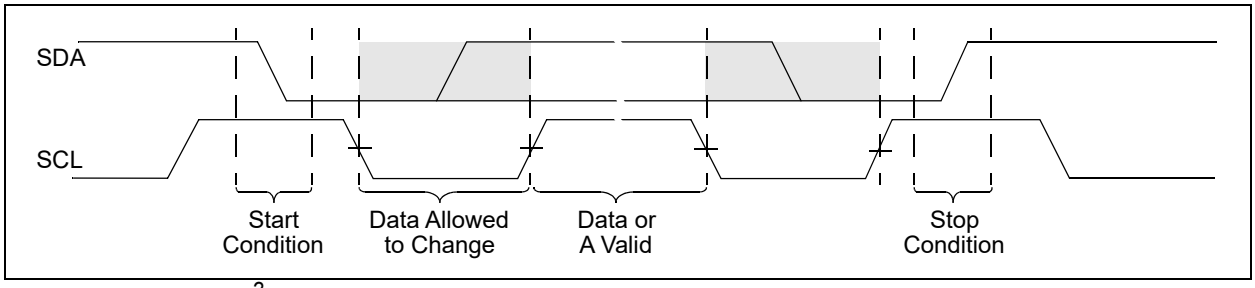


FIGURE B-8: *I^2C Data States and Bit Sequence.*

B.3.4 GENERAL CALL

The host can use the general call method to communicate with all other client devices. In a multi-host application, the other host devices operate in Client mode. The general call address has two documented formats. These are shown in Figure B-9.

The I^2C specification documents three 7-bit command bytes.

The I^2C specification does not allow '00000000' (00h) in the second byte. Also, the '00000100' and '00000110' functionalities are defined by the specification. Lastly, a data byte with a '1' in the LSb indicates a "Hardware General Call".

For details on the operation of the MCP47CXBX4/8 device's General Call commands, see **Section 4.6.1.3, "General Call Commands"**.

Note:	Only one General Call command per issue of the General Call Control byte. Any additional General Call commands are ignored and Not Acknowledged.

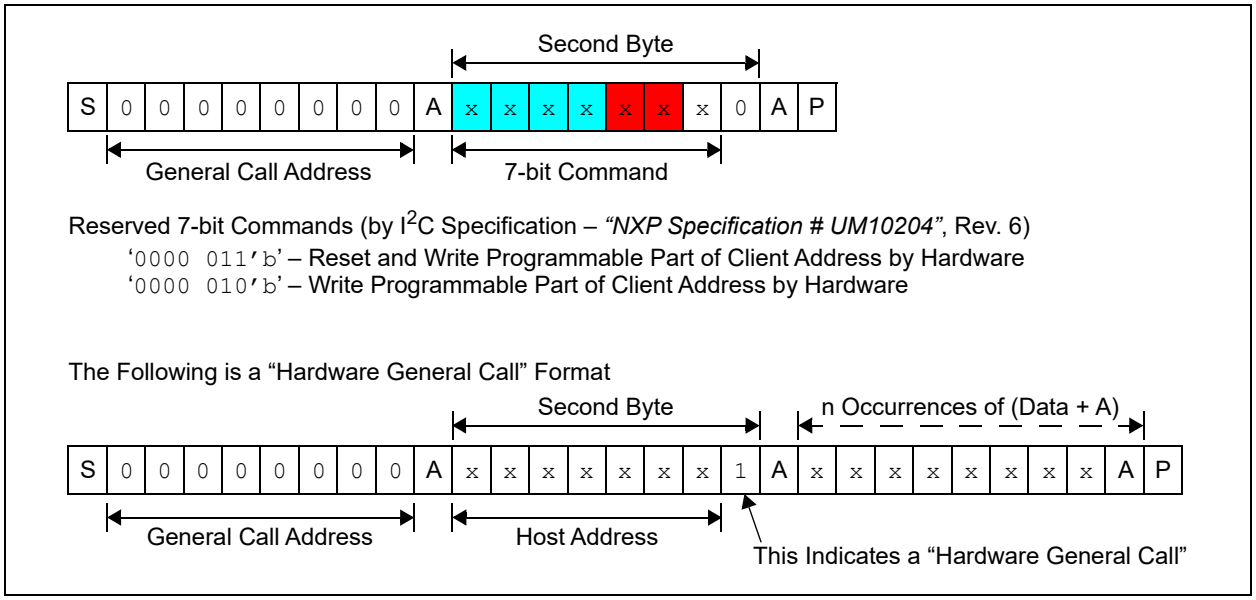


FIGURE B-9: *General Call Formats.*

APPENDIX C: TERMINOLOGY

C.1 Resolution

The resolution is the number of DAC output states that divide the Full-Scale Range (FSR). For the 12-bit DAC, the resolution is 2^{12}, meaning the DAC code ranges from 0 to 4095.

When there are 2^N resistors in the resistor ladder and 2^N tap points, the full-scale DAC register code is the resistor element positioned at 1 LSb from the source reference voltage (V_{DD} or V_{REF}).

C.2 Least Significant Bit (LSb)

This is the voltage difference between two successive codes. For a given output voltage range, it is divided by the resolution of the device (Equation C-1).

EQUATION C-1: LSb VOLTAGE CALCULATION

Ideal

$$V_{LSb(IDEAL)} = \frac{V_{DD}}{2^N} \text{ or } \frac{V_{REF}}{2^N}$$

Measured 1

$$V_{LSb(Measured)} = \frac{V_{OUT(@4032)} - V_{OUT(@64)}}{(4032 - 64)}$$

Measured 2

$$V_{LSb} = \frac{V_{OUT(@FS)} - V_{OUT(@ZS)}}{2^N - 1}$$

2^N = 4096 (MCP47CVB2X)
= 1024 (MCP47CVB1X)
= 256 (MCP47CVB0X)

The range may be V_{DD} (or V_{REF}) to V_{SS} (ideal); the DAC register codes across the linear range of the output driver (Measured 1) or full scale to zero scale (Measured 2).

C.3 Monotonic Operation

The monotonic operation means that the device's output voltage (V_{OUT}) increases with every one code step (LSb) increment (from V_{SS} to the DAC's reference voltage, V_{DD} or V_{REF}).

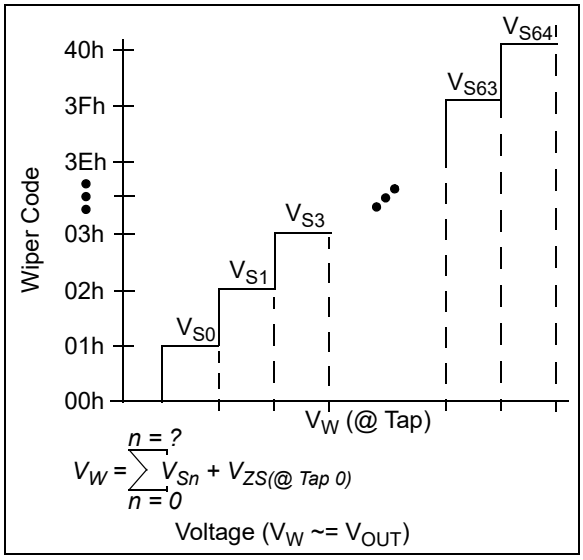


FIGURE C-1: *V_W (V_{OUT}).*

C.4 Zero-Scale Error (E_{ZS})

The zero-scale error, E_{ZS} (see Figure C-2), is the difference between the ideal and the measured V_{OUT} voltage with the DAC register code equal to 000h (Equation C.5).

EQUATION C-2: ZERO-SCALE ERROR

$$E_{ZS} = \frac{V_{OUT(@ZS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{ZS} = expressed in LSb

$V_{OUT(@ZS)}$ = V_{OUT} voltage when the DAC register code is at zero scale

$V_{LSb(IDEAL)}$ = theoretical voltage step-size

The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{DD}) greater than specified, the zero-scale error is greater.

The error in bits is determined by the theoretical voltage step-size to give an error in LSb.

C.5 Full-Scale Error (E_{FS})

The full-scale error, E_{FS} (see Figure C-3), is the error on the V_{OUT} pin relative to the expected V_{OUT} voltage (theoretical) for the maximum device DAC register code (FFFh for 12-bit, 3FFh for 10-bit and FFh for 8-bit); see Equation C-3. The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{SS}) greater than specified, the full-scale error will be greater.

The error in bits is determined by the theoretical voltage step-size to give an error in LSb.

EQUATION C-3: FULL-SCALE ERROR

$$E_{FS} = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS} = expressed in LSb

$V_{OUT(@FS)}$ = V_{OUT} voltage when the DAC register code is at full scale

$V_{IDEAL(@FS)}$ = ideal output voltage when the DAC register code is at full scale

$V_{LSb(IDEAL)}$ = theoretical voltage step-size

C.6 Offset Error (E_{OS})

The offset error (E_{OS}) is the delta voltage of the V_{OUT} voltage from the ideal output voltage at the specified code. This code is specified where the output amplifier is in the linear operating range; for the MCP47CXBX4/8, we specify code 64 (decimal). Offset error does not include gain error, which is illustrated in Figure C-2.

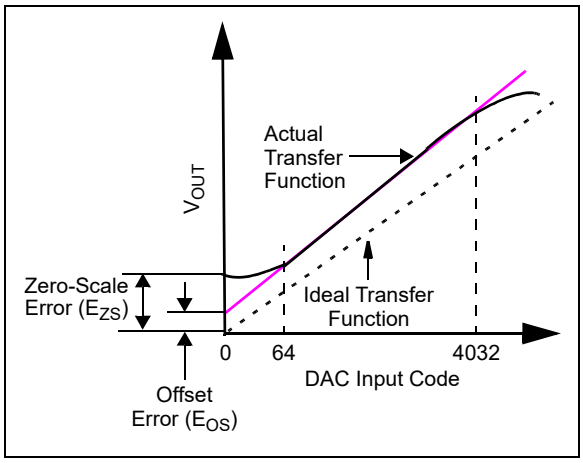


***FIGURE C-2:** Offset Error (Zero Gain Error).*

This error is expressed in mV. Offset error can be negative or positive. The error can be calibrated by software in application circuits.

C.7 Offset Error Drift (E_{OSD})

The offset error drift (E_{OSD}) is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/°C or µV/°C.

C.8 Gain Error (E_G)

Gain error (E_G) is a calculation based on the ideal slope using the voltage boundaries for the linear range of the output driver (e.g., code 64 and code 4032); see Figure C-3. The gain error calculation nullifies the device's offset error.

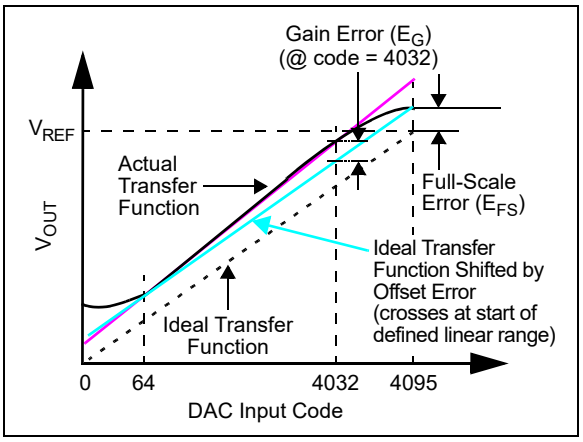


***FIGURE C-3:** Gain Error and Full-Scale Error Example.*

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as a percentage of FSR or in LSb. FSR is the ideal full-scale voltage of the DAC (see Equation C-4).

EQUATION C-4: GAIN ERROR EXAMPLE

$$E_G = \frac{(V_{OUT(@4032)} - V_{OS} - V_{OUT\_Ideal(@4032)})}{V_{Full\text{-}Scale\ Range}} * 100$$

Where:

E_G is expressed in % of FSR

$V_{OUT(@4032)}$ = measured DAC output voltage at the specified code

$V_{OUT\_Ideal(@4032)}$ = calculated DAC output voltage at the specified code (4032 * $V_{LSb(Ideal)}$)

V_{OS} = measured offset voltage

$V_{Full\text{-}Scale\ Range}$ = expected full-scale output value (such as the V_{REF} voltage)

C.9 Gain Error Drift (E_{GD})

The gain error drift (E_{GD}) is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/°C (of FSR).

C.10 Total Unadjusted Error (E_T)

The total unadjusted error (E_T) is the difference between the ideal and the measured V_{OUT} voltage. Typically, calibration of the output voltage is implemented to improve the system's performance.

The error in bits is determined by the theortical voltage step-size to give an error in LSb.

Equation C-5 shows the total unadjusted error calculation.

EQUATION C-5: TOTAL UNADJUSTED ERROR CALCULATION

$$E_T = \frac{(V_{OUT\_Actual(@code)} - V_{OUT\_Ideal(@code)})}{V_{LSb(Ideal)}}$$

Where:

E_T = expressed in LSb

$V_{OUT\_Actual(@code)}$ = measured DAC output voltage at the specified code

$V_{OUT\_Ideal(@code)}$ = calculated DAC output voltage at the specified code (*code* * $V_{LSb(Ideal)}$)

$V_{LSb(Ideal)}$ = V_{REF}/# Steps
12-bit = V_{REF}/4096
10-bit = V_{REF}/1024
8-bit = V_{REF}/256

C.11 Integral Nonlinearity (INL)

The integral nonlinearity error (INL) is the maximum deviation of an actual transfer function, from an ideal transfer function (straight line), passing through the defined end-points of the DAC transfer function (after offset and gain errors are removed).

For the MCP47CXBX4/8, INL is calculated using the defined end-points, DAC code 64 and code 4032. INL can be expressed as a percentage of FSR or in LSb. INL is also called relative accuracy. Equation C-6 shows how to calculate the INL error in LSb and Figure C-4 shows an example of INL accuracy.

Positive INL means a V_{OUT} voltage higher than the ideal one. Negative INL means a V_{OUT} voltage lower than the ideal one.

EQUATION C-6: INL ERROR

$$E_{INL} = \frac{(V_{OUT} - V_{Calc\_Ideal})}{V_{LSb(Measured)}}$$

Where:

INL = expressed in LSb

V_{Calc_Ideal} = Code * $V_{LSb(Measured)}$ + V_{OS}

$V_{OUT(Code = n)}$ = measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = for measured:
($V_{OUT(4032)}$ – $V_{OUT(64)}$)/3968

V_{OS} = measured offset voltage

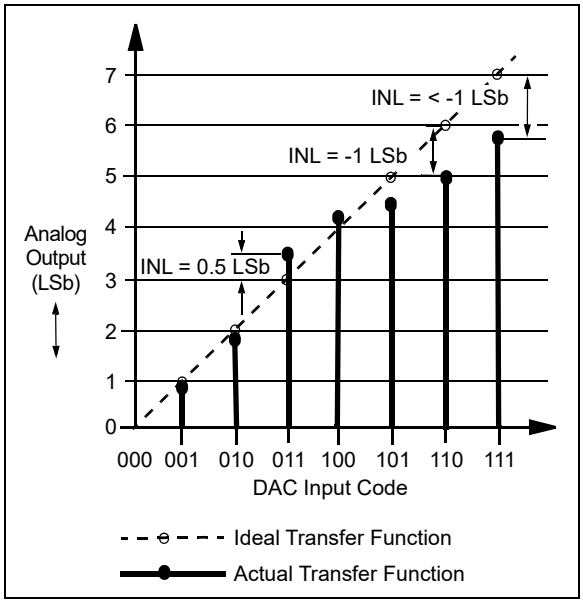


FIGURE C-4: *INL Accuracy.*

MCP47CXBX4/8

C.12 Differential Nonlinearity (DNL)

The differential nonlinearity error (DNL) (see Figure C-5) is the measure of step-size between codes in an actual transfer function. The ideal step-size between codes is 1 LSb. A DNL error of zero implies that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC ensures monotonic output and no missing codes. Equation C-7 shows how to calculate the DNL error between any two adjacent codes in LSb.

EQUATION C-7: DNL ERROR

$$E_{DNL} = \frac{(V_{OUT(code = n+1)} - V_{OUT(code = n)})}{V_{LSb(Measured)}} - 1$$

Where:

DNL = expressed in LSb

$V_{OUT(Code = n)}$ = measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = for measured: $(V_{OUT(4032)} - V_{OUT(64)})/3968$

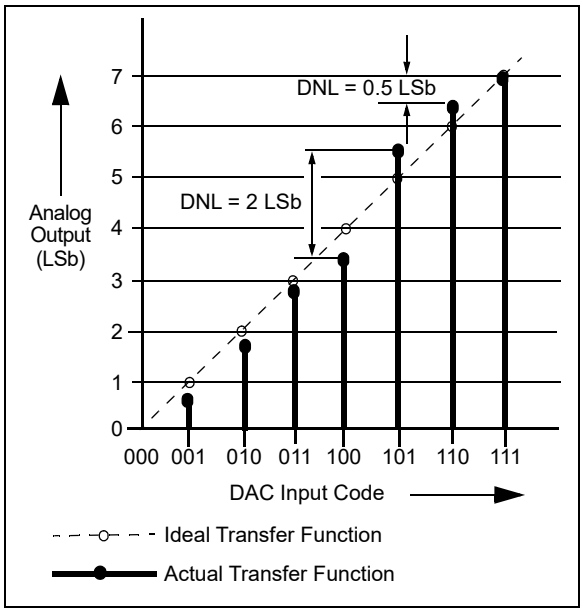


FIGURE C-5: *DNL Accuracy.*

C.13 Settling Time

The settling time is the time delay required for the V_{OUT} voltage to settle into its new output value. This time is measured from the start of code transition to when the V_{OUT} voltage is within the specified accuracy.

For the MCP47CXBX4/8, the settling time is a measure of the time delay until the V_{OUT} voltage reaches within 0.5 LSb of its final value, when the volatile DAC register changes from 1/4 to 3/4 of the FSR (12-bit device: 400h to C00h).

C.14 Major Code Transition Glitch

Major code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes the state. It is normally specified as the area of the glitch in nV-Sec and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: `011...111` to `100...000`, or `100...000` to `011...111`).

C.15 Digital Feedthrough

The digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec and is measured with a full-scale change (example: all '`0`'s to all '`1`'s and vice versa) on the digital input pins. The digital feedthrough is measured when the DAC is not being written to the output register.

C.16 -3 dB Bandwidth

This is the frequency of the signal at the V_{REF} pin that causes the voltage at the V_{OUT} pin to fall to -3 dB from a static value on the V_{REF} pin. The output decreases due to the RC characteristics of the resistor ladder and the characteristics of the output buffer.

C.17 Power Supply Sensitivity (PSS)

PSS indicates how the output of the DAC is affected by changes in the supply voltage. PSS is the ratio of the change in V_{OUT} to a change in V_{DD} for mid-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied from 5.5V to 2.7V as a step (V_{REF} voltage held constant) and expressed in %/%, which is the % change of the DAC output voltage with respect to the % change of the V_{DD} voltage.

EQUATION C-8: PSS CALCULATION

$$PSS = \frac{(V_{OUT(@5.5V)} - V_{OUT(@2.7V)})/V_{OUT(@5.5V)}}{(5.5V - 2.7V)/(5.5V)}$$

Where:

PSS = expressed in %/%

$V_{OUT(@5.5V)}$ = measured DAC output voltage with V_{DD} = 5.5V

$V_{OUT(@2.7V)}$ = measured DAC output voltage with V_{DD} = 2.7V

C.18 Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied ±10% (V_{REF} voltage held constant) and expressed in dB or µV/V.

C.19 V_{OUT} Temperature Coefficient

The V_{OUT} temperature coefficient quantifies the error in the resistor ladder's resistance ratio (DAC register code value) and output buffer due to temperature drift.

C.20 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (nominal output voltage, V_{OUT}) due to temperature drift. For a DAC, this error is typically not an issue due to the ratiometric aspect of the output.

C.21 Noise Spectral Density

The noise spectral density is a measurement of the device's internally generated random noise and is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to the mid-scale value and measuring the noise at the V_{OUT} pin. It is measured in nV/√Hz.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	—	XX	X	/XX
Device	Tape and Reel		Pin Count	Temperature Range	Package

Device:	MCP47CXBX4/8:1 LSb INL Voltage Output, Digital-to-Analog Converters with I^2C Interface, 8/10/12-Bit Resolution, Quad/Octal Outputs and Volatile/MTP Memory	
Tape and Reel:	T	= Tape and Reel
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	ST	= Thin Shrink Small Outline Package (TSSOP), 20-Lead
	ML	= Plastic Quad Flat, No Lead Package (QFN), 4 mm x 4 mm, 20-Lead

Examples:

a) MCP47CVB04-20E/ST: 1 LSb INL Voltage Output Digital-to-Analog Converter, 8-Bit Resolution, Extended Temperature, 20LD TSSOP, with Volatile Memory.

b) MCP47CVB04T-20E/ST: 1 LSb INL Voltage Output Digital-to-Analog Converter, 8-Bit Resolution, Tape and Reel, Extended Temperature, 20LD TSSOP, with Volatile Memory.

c) MCP47CVB18-E/ML: 1 LSb INL Voltage Output Digital-to-Analog Converter, 10-Bit Resolution, Extended Temperature, 20LD QFN, with Volatile Memory.

d) MCP47CVB18T-E/ML: 1 LSb INL Voltage Output Digital-to-Analog Converter, 10-Bit Resolution, Tape and Reel, Extended Temperature, 20LD QFN, with Volatile Memory.

e) MCP47CMB24-E/ML: 1 LSb INL Voltage Output Digital-to-Analog Converter, 12-Bit Resolution, Extended Temperature, 20LD QFN, with MTP Memory.

f) MCP47CMB28T-20E/ST: 1 LSb INL Voltage Output Digital-to-Analog Converter, 12-Bit Resolution, Tape and Reel, Extended Temperature, 20LD TSSOP, with MTP Memory.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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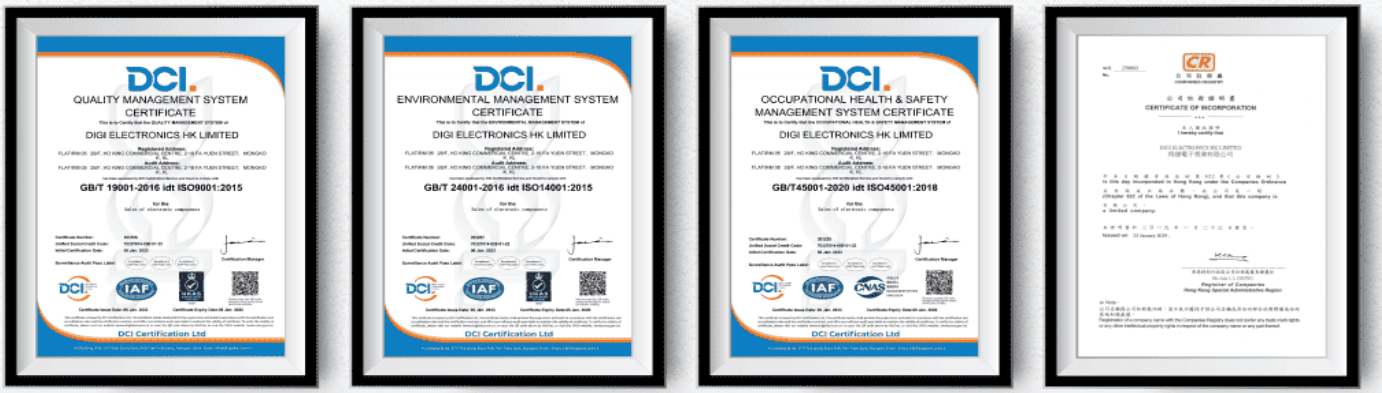

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