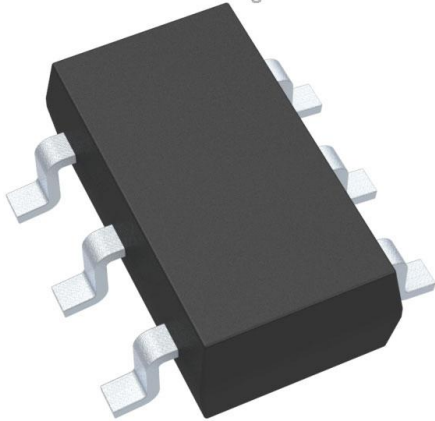


PL102-10TI-R Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|--------------------------------------|
| DiGi Electronics Part Number | PL102-10TI-R-DG |
| Manufacturer | Microchip Technology |
| Manufacturer Product Number | PL102-10TI-R |
| Description | IC CLK BUFFER 1:3 170MHZ 6SOT23 |
| Detailed Description | IC 170MHz 1 SOT-23-6 |



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RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

PL102-10TI-R

Series:

-

DiGi-Electronics Programmable:

Not Verified

Input:

Clock

Number of Circuits:

1

Differential - Input:Output:

No/No

Divider/Multiplier:

No/No

Operating Temperature:

-40°C ~ 85°C

Package / Case:

SOT-23-6

Base Product Number:

PL102

Manufacturer:

Microchip Technology

Product Status:

Discontinued at Digi-Key

PLL:

Yes with Bypass

Output:

Clock

Ratio - Input:Output:

1:3

Frequency - Max:

170MHz

Voltage - Supply:

2.25V ~ 3.63V

Mounting Type:

Surface Mount

Supplier Device Package:

SOT-23-6

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



PL102-10

Low Skew Output Buffer

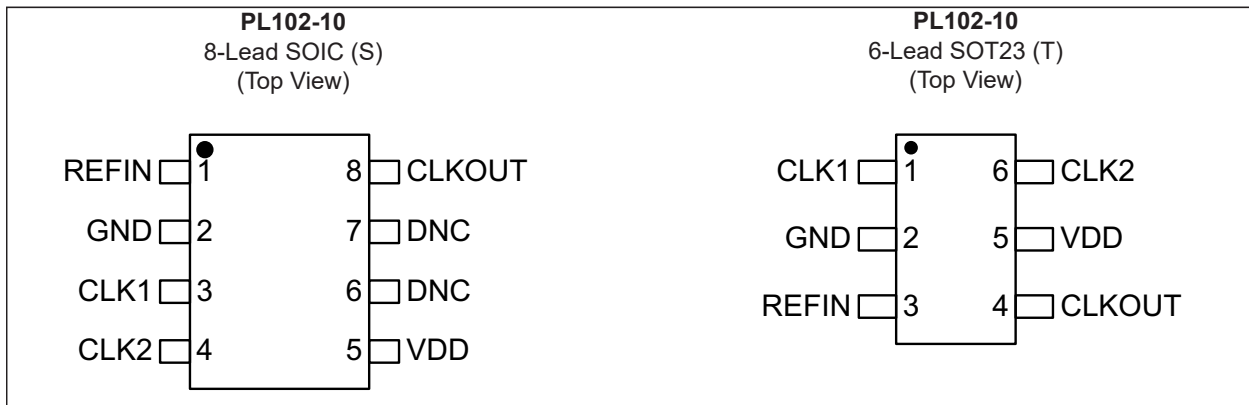
Features

- Frequency Range:
 - 15 MHz to 170 MHz @ 3.3V
 - 15 MHz to 145 MHz @ 2.5V
- Internal Phase Locked Loop Allows Spread Spectrum Modulation on Reference Clock to Pass to Outputs
- Zero Input-to-Output Delay
- Less than 700 ps Device-to-Device Skew
- Less than 200 ps Skew between Outputs
- Less than 100 ps Cycle-to-Cycle Jitter
- 2.5V or 3.3V Power Supply
- Available in 8-Lead SOIC or 6-Lead SOT23 GREEN/RoHS-Compliant Packages

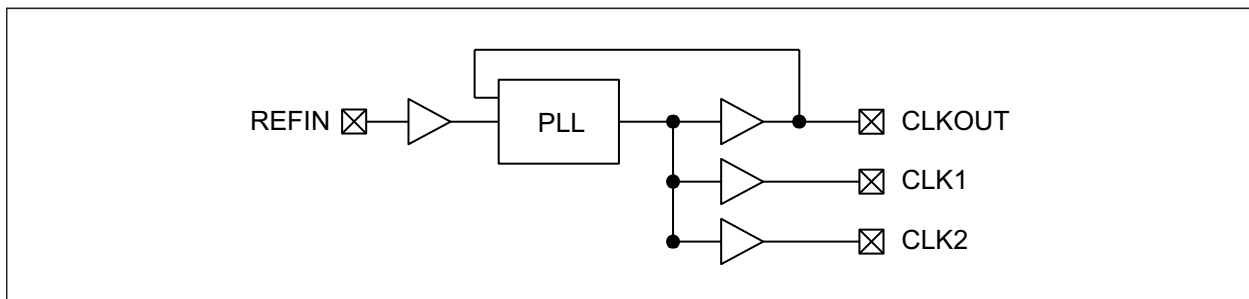
General Description

The PL102-10 is a high performance, low skew, low jitter zero delay buffer designed to distribute high speed clocks and is available in 8-lead SOIC or 6-lead SOT23 package. It has two outputs that are synchronized with the input. The synchronization is established via CLKOUT feed back to the input of the PLL. Because the skew between the input and output is less than ± 350 ps, the device acts as a zero delay buffer.

Package Types



Block Diagram



PL102-10

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| | |
|-----------------------------|--------------------------|
| Supply Voltage (V_{DD}) | +4.6V |
| DC Input Voltage (V_I) | -0.5V to $V_{DD} + 0.5V$ |
| DC Output Voltage (V_O) | -0.5V to $V_{DD} + 0.5V$ |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---------------------|----------|------|------|------|-------|---|
| Supply Voltage | V_{DD} | 2.25 | — | 3.63 | V | — |
| Input Low Voltage | V_{IL} | — | — | 0.8 | V | — |
| Input High Voltage | V_{IH} | 2.0 | — | — | V | — |
| Output Low Voltage | V_{OL} | — | — | 0.4 | V | $I_{OL} = 24\text{ mA}$ |
| Output High Voltage | V_{OH} | 2.4 | — | — | V | $I_{OH} = 24\text{ mA}$ |
| Supply Current | I_{DD} | — | 22 | 30 | mA | Unloaded outputs at 100 MHz, $V_{DD} = 3.3V$ |

SWITCHING CHARACTERISTICS

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|--|----------------------|------|------|------|-------|---|
| Input/Output Frequency | f ₁ | 15 | — | 145 | MHz | 2.5V |
| | | 15 | — | 170 | | 3.3V |
| Duty Cycle | DC | 45 | 50 | 55 | % | Measured at $V_{DD}/2$, $C_L = 15\text{ pF}$, $f_{OUT} = 100\text{ MHz}$ |
| Rise Time | t _r | — | 1.2 | 1.5 | ns | Measured between 10% and 90% of V_{DD} , $C_L = 15\text{ pF}$ |
| Fall Time | t _f | — | 1.2 | 1.5 | ns | Measured between 90% and 10% of V_{DD} , $C_L = 15\text{ pF}$ |
| Output to Output Skew | t _{SKREW} | — | — | 200 | ps | All outputs equally loaded, $C_L = 15\text{ pF}$ |
| Delay, REF Rising Edge to CLKOUT Rising Edge | t _{DELAY} | — | 0 | ±350 | ps | Measured at $V_{DD}/2$ |
| Device to Device Skew | t _{DSK-DSK} | — | 0 | 700 | ps | Measured at $V_{DD}/2$ on the CLKOUT pins of devices |
| Cycle to Cycle Jitter | t _{CYC-CYC} | — | — | 60 | ps | Measured at 100 MHz |
| PLL Lock Time | t _{LOCK} | — | — | 1.0 | ms | Stable power supply, valid clock presented on REF pin |
| Jitter; Absolute Jitter | t _{JABS} | — | 20 | 50 | ps | Measured 10,000 cycles, low jitter input signal |
| Jitter; 1-Sigma | t _{J1-S} | — | 9 | 15 | ps | Measured 10,000 cycles, low jitter input signal |

TEMPERATURE SPECIFICATIONS

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|--------------------------------|-------|------|------|------|-------|----------------|
| Temperature Ranges | | | | | | |
| Ambient Operating Temperature | T_A | -40 | — | +85 | °C | — |
| Junction Operating Temperature | T_J | — | — | +125 | °C | — |
| Storage Temperature Range | T_S | -65 | — | +150 | °C | — |
| Lead Temperature | — | — | +260 | — | °C | Soldering, 10s |

Switching Waveforms

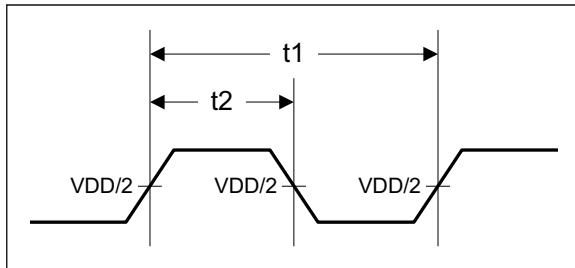


FIGURE 1-1: Duty Cycle Timing.

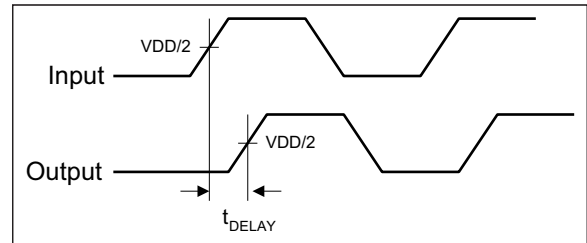


FIGURE 1-4: Input-to-Output Propagation Delay.

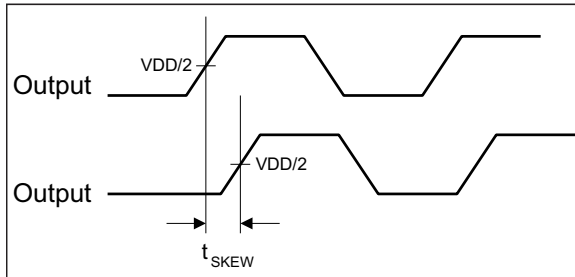


FIGURE 1-2: Output-to-Output Skew.

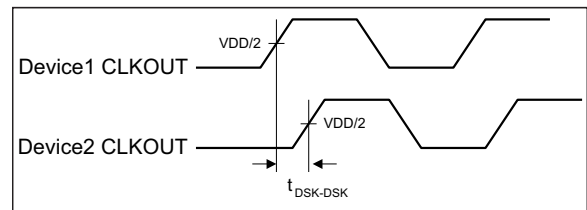


FIGURE 1-5: Device-to-Device Skew.

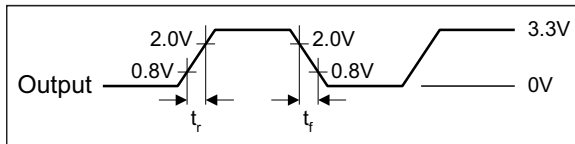


FIGURE 1-3: All Outputs Rise/Fall Time.

PL102-10

2.0 PIN DESCRIPTION

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

| Pin Number SOIC-8 | Pin Number SOT23-6 | Pin Name | Pin Type | Description |
|----------------------|-----------------------|----------|----------|---|
| 1 | 3 | REFIN | I | Input reference frequency. Spread spectrum modulation on this signal will be passed to the output (up to 100 kHz SST modulation). |
| 2 | 2 | GND | P | Ground connection. |
| 3 | 1 | CLK1 | O | Buffered clock output. |
| 4 | 6 | CLK2 | O | Buffered clock output. If CLK2 is pulled high during startup, the device will enter test mode. |
| 5 | 5 | VDD | P | 2.5V or 3.3V power supply connection. |
| 6, 7 | — | NC | — | Do not connect. |
| 8 | 4 | CLKOUT | O | Buffered clock output. Internal feedback on this pin. |

3.0 OUTPUT-TO-OUTPUT SKEW

The skew between CLKOUT and the CLK(1-2) outputs is not dynamically adjusted by the PLL. Because CLKOUT is one of the inputs to the PLL, zero phase difference is maintained from REF to CLKOUT. If all outputs are equally loaded, zero phase difference will be maintained from REF to all outputs.

If applications requiring zero output-output skew, all the outputs must be equally loaded.

If the CLK(1-2) outputs are less loaded than CLKOUT, CLK(1-2) outputs will lead it; if the CLK(1-2) is more loaded than CLKOUT, CLK(1-2) will lag the CLKOUT.

Because the CLKOUT and the CLK(1-2) outputs are identical, they all start at the same time, but difference loads cause them to have different rise times and different times crossing the measurement thresholds.

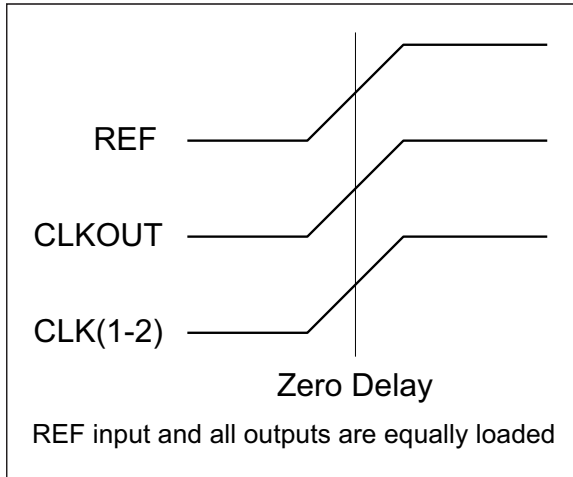


FIGURE 3-1: Zero Delay.

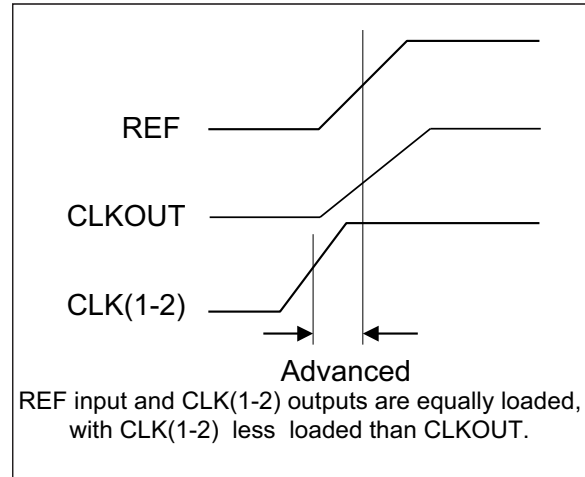


FIGURE 3-3: Advanced.

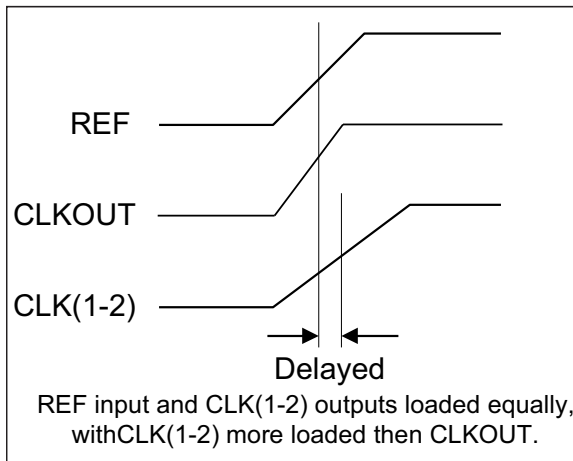


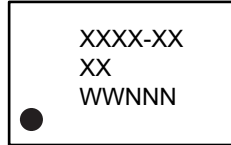
FIGURE 3-2: Delayed.

PL102-10

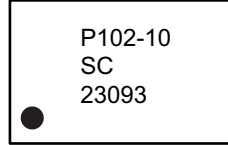
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

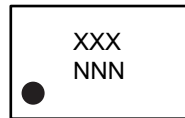
8-Lead SOIC*



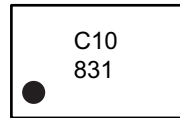
Example



6-Lead SOT23*



Example

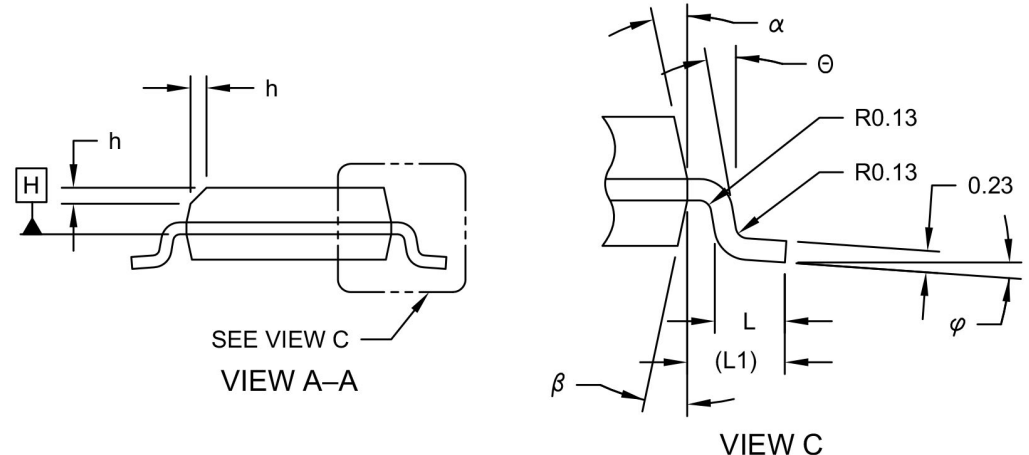
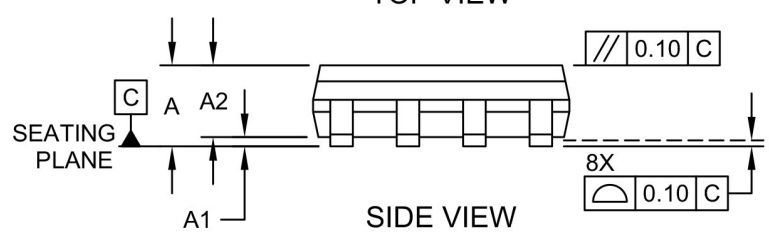
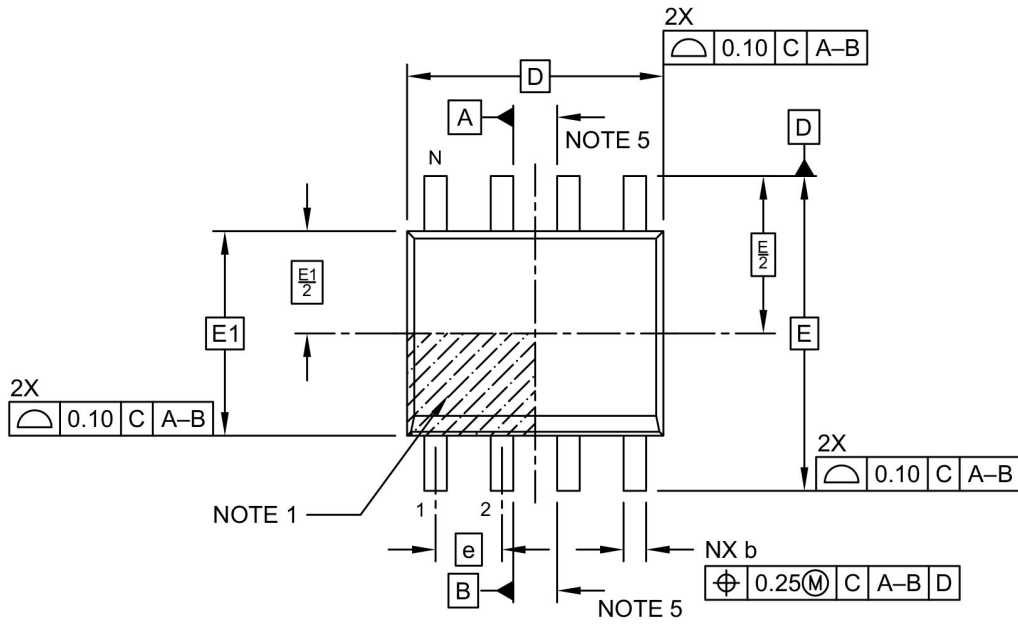


| | | |
|----------------|--|--|
| Legend: | XX...X | Product code |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | (e3) | This package is Pb-free. The Pb-free JEDEC designator () can be found on the outer packaging for this package. (e3) |
| | •, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. | |
| | Underbar () and/or Overbar () symbol may not be to scale. | |

8-Lead SOIC Package Outline and Recommended Land Pattern

8-Lead Plastic Small Outline (ENA) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Micrel Legacy Package FSLOC-08L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

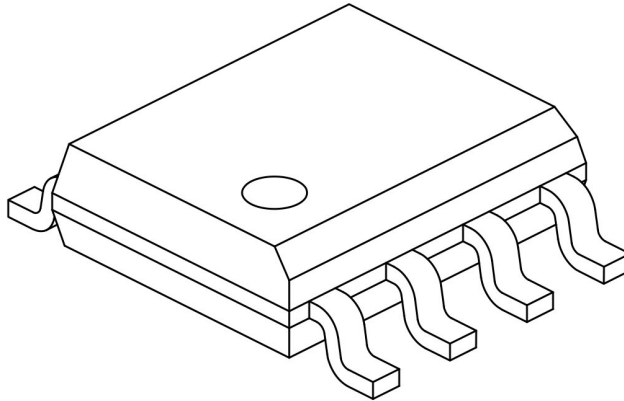


Microchip Technology Drawing No. C04-057-ENA Rev F Sheet 1 of 2

PL102-10

8-Lead Plastic Small Outline (ENA) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Micrel Legacy Package FSLOC-08L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-----------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

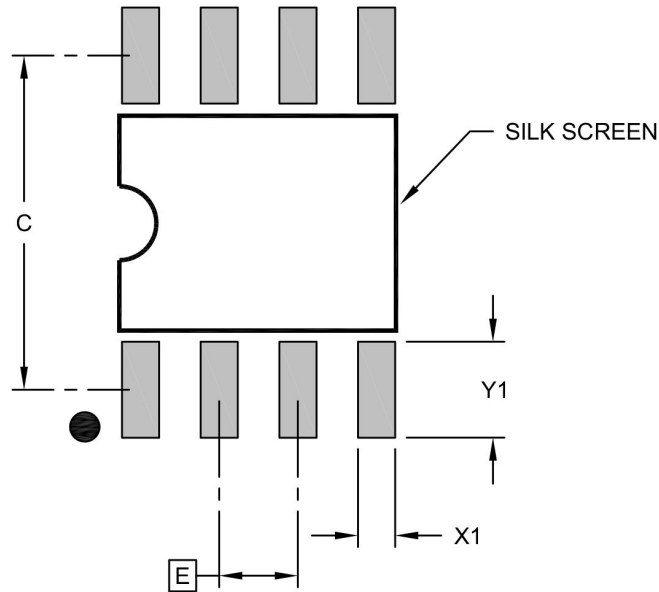
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-ENA Rev F Sheet 1 of 2

8-Lead Plastic Small Outline (ENA) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Micrel Legacy Package FSLOC-08L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|----------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-ENA Rev F

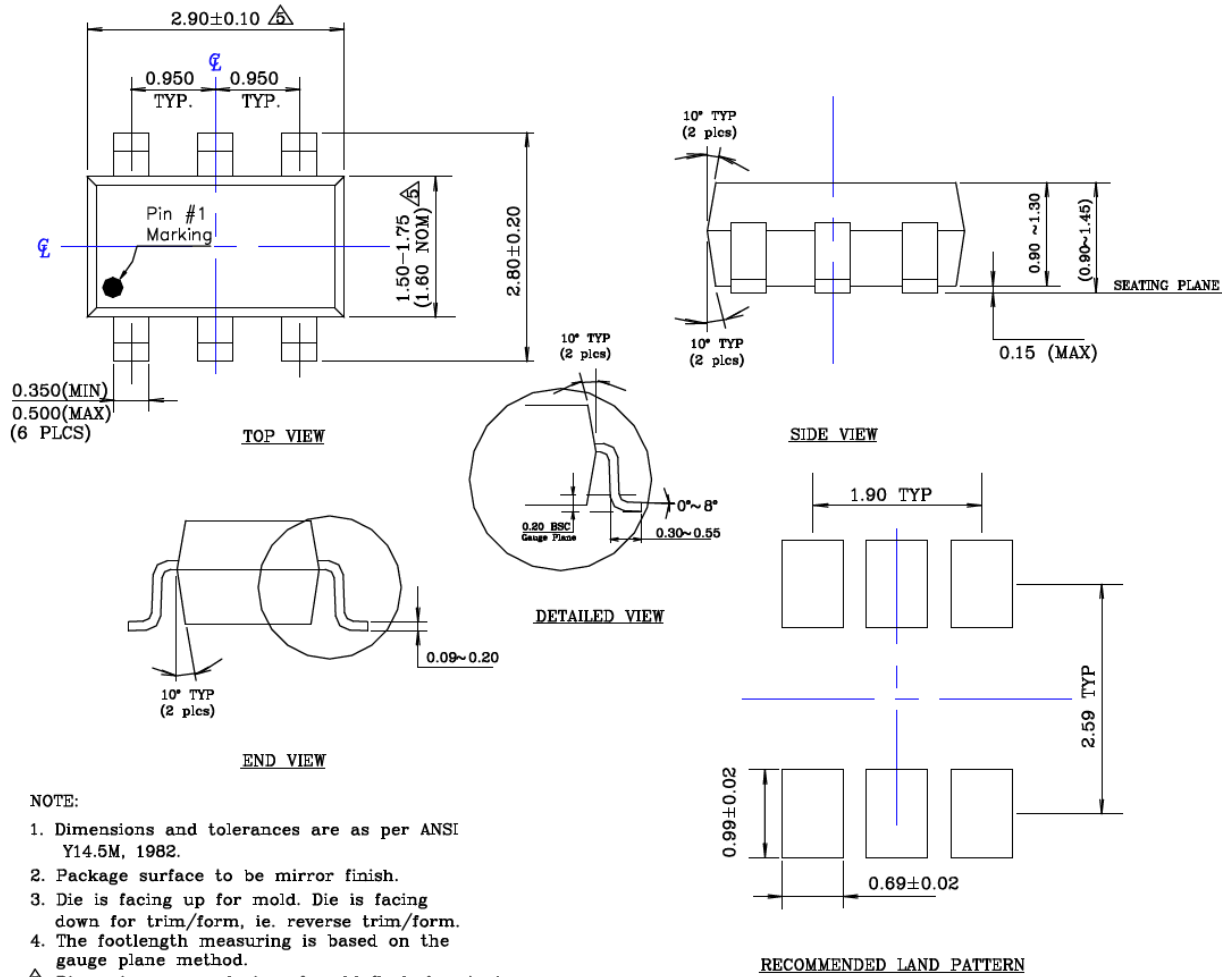
PL102-10

6-Lead SOT23 Package Outline and Recommended Land Pattern

TITLE

6 LEAD SOT23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| | | | |
|------------------|----------------|-------------|----|
| DRAWING # | SOT23-6LD-PL-1 | UNIT | MM |
|------------------|----------------|-------------|----|



NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
 2. Package surface to be mirror finish.
 3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
 4. The footlength measuring is based on the gauge plane method.
- △ Dimension are exclusive of mold flash & gate burr.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY**Revision A (April 2020)**

- Converted Micrel document PL102-10 to Microchip data sheet template DS20006345A.
- Minor text changes throughout.

PL102-10

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART No.</u> | <u>X</u> | <u>X</u> | <u>-X</u> | Examples: |
|---------------------------|-----------|--------------------------------|------------|---|
| Device | Package | Temperature Range | Media Type | |
| Device: | PL102-10: | Low Skew Output Buffer | | a) PL102-10SC-R: Low Skew Output Buffer, 8-Lead SOIC, 0°C to +70°C Temperature Range, 2,500/Reel |
| Package: | S = | 8-Lead SOIC | | b) PL102-10TC: Low Skew Output Buffer, 6-Lead SOT23, 0°C to +70°C Temperature Range, 20/Bag |
| | T = | 6-Lead SOT23 | | c) PL102-10TC-R: Low Skew Output Buffer, 6-Lead SOT23, 0°C to +70°C Temperature Range, 3,000/Reel |
| Temperature Range: | C = | 0°C to +70°C (Commercial) | | Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. |
| Media Type: | <blank>= | 20/Bag (SOT23 Option Only) | | |
| | R = | 3,000/Reel (SOT23 Option Only) | | |
| | R = | 2,500/Reel (SO?? Option Only) | | |

PL102-10

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