

# SY100S321JZ Datasheet

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DiGi Electronics Part Number	SY100S321JZ-DG
Manufacturer	<a href="#">Microchip Technology</a>
Manufacturer Product Number	SY100S321JZ
Description	IC INVERTER 9CH 1-INP 28PLCC
Detailed Description	Inverter IC 9 Channel 28-PLCC (11.48x11.48)



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## Purchase and inquiry

Manufacturer Product Number:

SY100S321JZ

Series:

100S

Logic Type:

Inverter

Number of Inputs:

1

Voltage - Supply:

-4.2V ~ -5.5V

Input Logic Level - Low:

-

Max Propagation Delay @ V, Max CL:

700ps @ -5V, -

Mounting Type:

Surface Mount

Package / Case:

28-LCC (J-Lead)

Manufacturer:

Microchip Technology

Product Status:

Discontinued at Digi-Key

Number of Circuits:

9

Features:

-

Current - Output High, Low:

-

Input Logic Level - High:

-

Operating Temperature:

0°C ~ 85°C

Supplier Device Package:

28-PLCC (11.48x11.48)

Base Product Number:

100S321

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

2 (1 Year)

ECCN:

EAR99





## LOW-POWER 9-BIT INVERTER

SY100S321

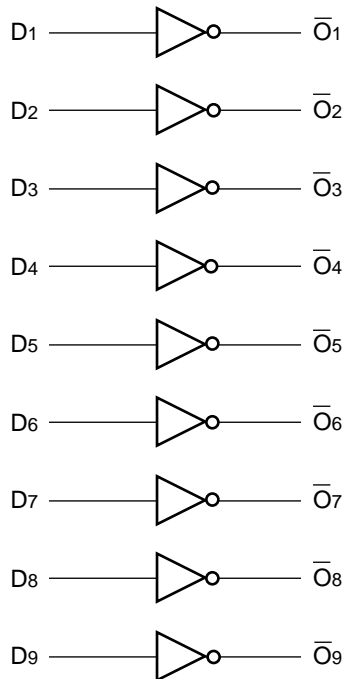
### FEATURES

- Max. propagation delay of 700ps
- IEE min. of -55mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- 70% faster than Fairchild 300K at lower power
- Internal 75kΩ input pull-down resistors
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

### DESCRIPTION

The SY100S321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output.

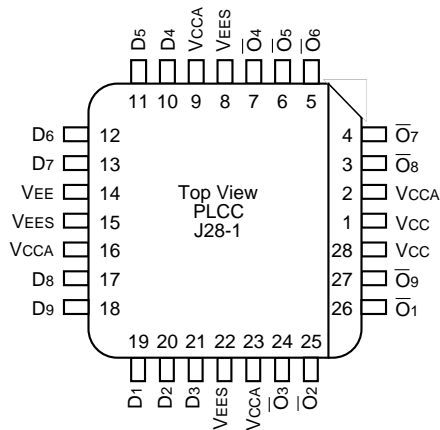
### BLOCK DIAGRAM



### PIN NAMES

Pin	Function
D1 – D9	Data Inputs
$\bar{Q}1 – \bar{Q}9$	Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

## PACKAGE/ORDERING INFORMATION



**28-Pin PLCC (J28-1)**

## Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S321JC	J28-1	Commercial	SY100S321JC	Sn-Pb
SY100S321JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S321JC	Sn-Pb
SY100S321JZ <sup>(2)</sup>	J28-1	Commercial	SY100S321JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S321JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S321JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

**DC ELECTRICAL CHARACTERISTICS**

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>IH</sub>	Input HIGH Current	—	—	200	μA	V <sub>IN</sub> = V <sub>IH</sub> (Max.)
I <sub>EE</sub>	Power Supply Current	-55	-41	-25	mA	Inputs Open

**AC ELECTRICAL CHARACTERISTICS**

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(1)</sup> Data to Output	300	700	300	700	300	700	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time <sup>(1)</sup> 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t <sub>s</sub> , G-G	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	

**NOTE:**

1. Reference Figures 1 and 2

## TEST CIRCUITRY<sup>(1)</sup>

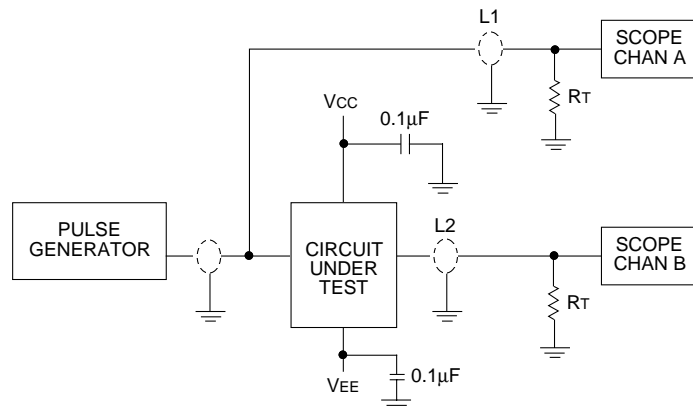


Figure 1. AC Test Circuit

**Note:**

1.  $V_{CC}$ ,  $V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$ .

L1 and L2 = equal length  $50\Omega$  impedance lines.

$R_T = 50\Omega$  terminator internal to scope.

Decoupling  $0.1\mu F$  from GND to  $V_{CC}$  and  $V_{EE}$ .

All unused outputs are loaded with  $50\Omega$  to GND.

$C_L$  = Fixture and stray capacitance  $\leq 3pF$ .

## SWITCHING WAVEFORMS

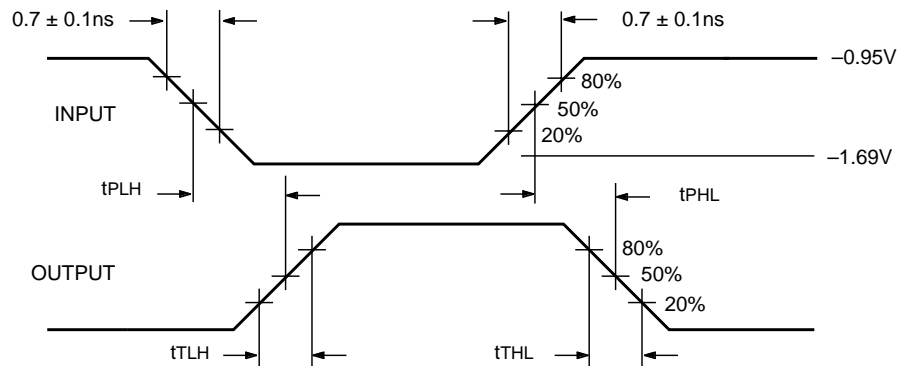
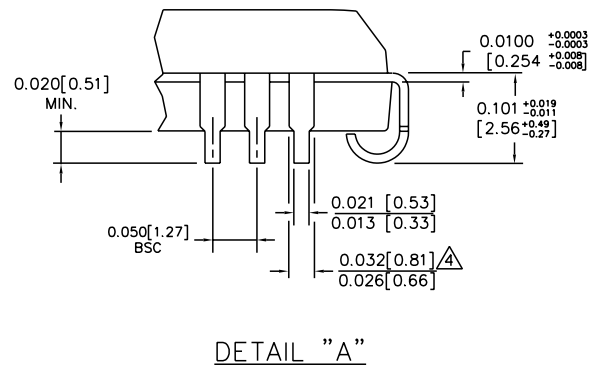
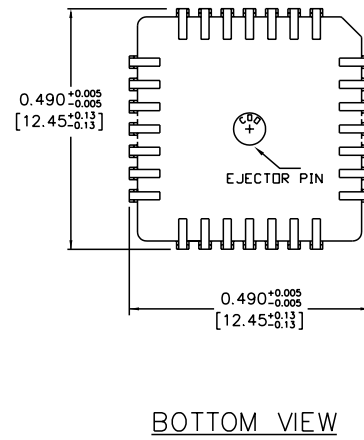
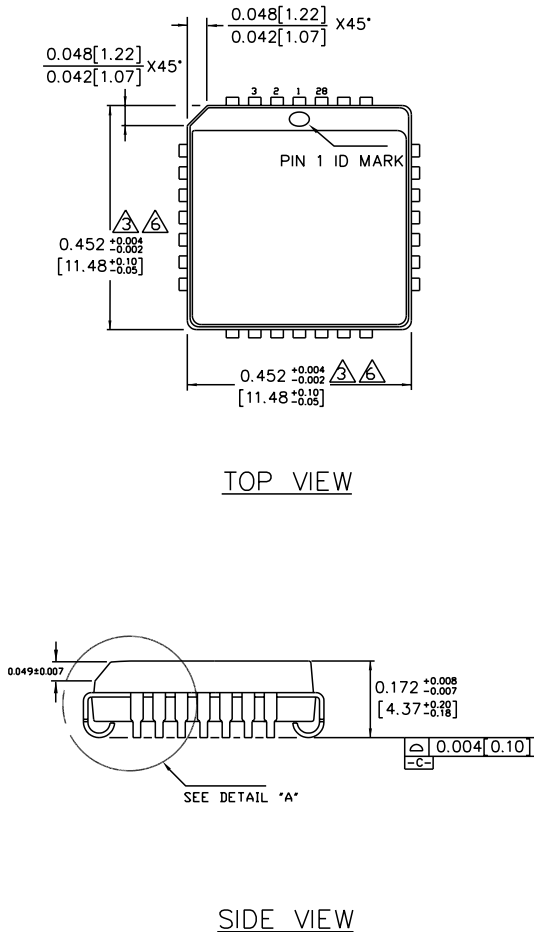


Figure 2. Propagation Delay and Transition Times

**Note:**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

**28-PIN PLCC (J28-1)****NOTES:**

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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