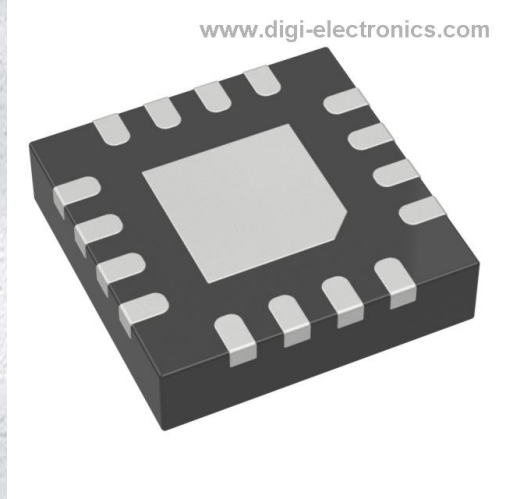
SY54011RMG-TR Datasheet



DiGi Electronics Part Number	SY54011RMG-TR-DG
Manufacturer	Microchip Technology
Manufacturer Product Number	SY54011RMG-TR
Description	IC CLK BUFFER 1:2 3.2GHZ 16MLF
Detailed Description	Clock Fanout Buffer (Distribution) IC 1:2 3.2 GHz 16-VFQFN Exposed Pad, 16-MLF®

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
SY54011RMG-TR	Microchip Technology
Series:	Product Status:
Precision Edge®	Active
Type:	Number of Circuits:
Fanout Buffer (Distribution)	1
Ratio - Input:Output:	Differential - Input:Output:
1:2	Yes/Yes
Input:	Output:
CML, LVDS, LVPECL	CML
Frequency - Max:	Voltage - Supply:
3.2 GHz	2.375V ~ 2.625V
Operating Temperature:	Mounting Type:
-40°C ~ 85°C	Surface Mount
Package / Case:	Supplier Device Package:
16-VFQFN Exposed Pad, 16-MLF®	16-MLF® (3x3)
Base Product Number:	
SY54011	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	2 (1 Year)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

SY54011R

Low-Voltage 1.2V/1.8V CML 1:2 Fanout Buffer, 3.2 Gbps, 3.2 GHz

Features

- 1.2V/1.8V CML 1:2 Fanout Buffer
- Guaranteed AC Performance over Temperature and Voltage:
  - DC-to->3.2 Gbps Throughput
  - <300 ps Propagation Delay (IN-to-Q)
  - <15 ps Within-Device Skew
  - <95 ps Rise/Fall Times
- Ultra-Low Jitter Design
  - 50 fs_{RMS} Typical Additive Phase Jitter
- High Speed CML Outputs
- 2.5V ±5%, 1.2V/1.8V ±5% Power Supply Operation
- Industrial Temperature Range: –40°C to +85°C
- Available in 16-pin (3 mm x 3 mm) QFN Package

Applications

- Data Distribution: OC-48, OC-48+FEC
- SONET Clock and Data Distribution
- Fibre Channel Clock and Data Distribution
- Gigabit Ethernet Clock and Data Distribution

Markets

- Storage
- ATE
- Test and Measurement
- Enterprise Networking Equipment
- High-End Servers
- Access
- Metro Area Network Equipment

General Description

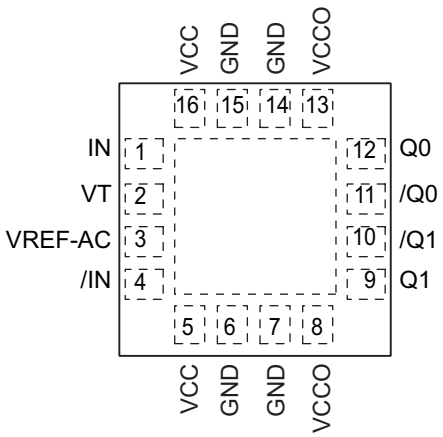
The SY54011R is a fully differential, low-voltage 1.2V/1.8V CML 1:2 fanout buffer. It is optimized to provide two identical output copies with less than 15 ps of skew and 50 fs_{RMS} of typical additive phase jitter. The SY54011R can process clock signals as fast as 3.2 GHz or data patterns up to 3.2 Gbps.

The differential input includes a unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled from a 2.5V driver) as small as 100 mV (200 mV_{PP}) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated voltage reference (V_{REF-AC}) is provided to bias the V_T pin. The outputs are CML, with extremely fast rise/fall times less than 95 ps.

The SY54011R operates from a 2.5V ±5% core supply and a 1.2V or 1.8V ±5% output supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). The SY54011R is part of the high speed, Precision Edge® product line.

Package Type

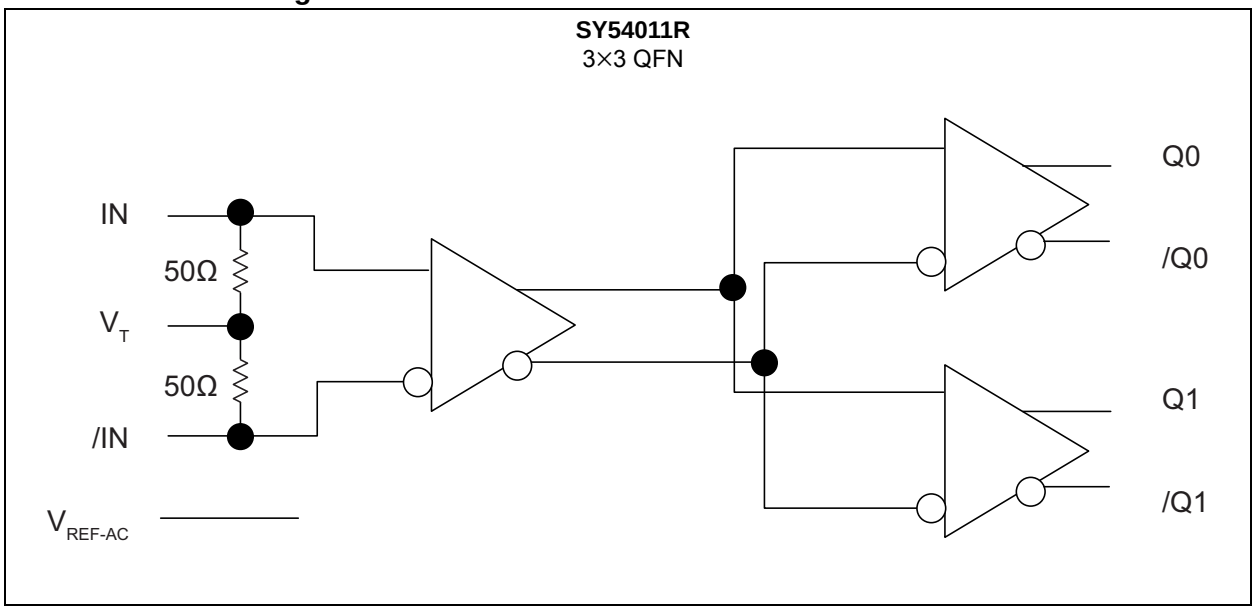
SY54011R
3x3 QFN
(Top View)



United States Patent No. RE44,134

SY54011R

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +3.0V
Supply Voltage (V_{CCO}) ..... –0.5V to +2.7V
V_{CC} - V_{CCO} ..... <1.8V
V_{CCO} - V_{CC} ..... <0.5V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) ..... 0.6V to V_{CCO}+0.5V
Current (V_T)
Source or sink current on V_T pin ..... ±100 mA
Input Current
Source or sink current on (IN, /IN) ..... ±50 mA
Current (V_{REF-AC})
Source or sink current on V_{REF-AC} (Note 1) ..... ±0.5 mA

Operating Ratings ††

Supply Voltage (V_{CC}) ..... 2.375V to 2.625V
(V_{CCO}) ..... 1.14V to 1.9V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: Unless otherwise indicated, T_A = –40°C to +85°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage Range	V_{CC}	2.375	2.500	2.625	V	V_{CC}
		1.140	1.200	1.260	V	V_{CCO}
		1.700	1.800	1.900	V	V_{CCO}
Power Supply Current	I_{CC}	—	15	22	mA	Max. V_{CC}
Power Supply Current	I_{CCO}	—	32	42	mA	No Load. V_{CCO}
Input Resistance (IN-to-V_T, /IN-to-V_T)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (IN-to-/IN)	R_{DIFF_IN}	90	100	110	Ω	—
Input HIGH Voltage (IN, /IN)	V_{IH}	1.2	—	V_{CC}	V	IN, /IN
Input LOW Voltage (IN, /IN)	V_{IL}	0.2	—	V_{IH} – 0.1	V	V_{IL} with V_{IH} of 1.2V
Input HIGH Voltage (IN, /IN)	V_{IH}	1.140	—	V_{CC}	V	IN, /IN
Input LOW Voltage (IN, /IN)	V_{IL}	0.66	—	V_{IH} – 0.10	V	V_{IL} with V_{IH} of 1.140V, (1.2V-5%)

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
2: Due to the limited drive capability, use for input of the same package only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = –40°C to +85°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Voltage Swing (IN, /IN)	V_{IN}	0.1	—	1.0	V	See Figure 6-3
Differential Input Voltage Swing (|IN, /IN|)	V_{DIFF_IN}	0.2	—	2.0	V	See Figure 6-5
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.3	V_{CC} – 1.15	V_{CC} – 1.0	V	Note 2
Voltage from Input to V_T	V_{T_IN}	—	—	1.28	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Due to the limited drive capability, use for input of the same package only.

TABLE 1-2: CML OUTPUTS DC ELECTRICAL CHARACTERISTICS (Note 1)

V_{CCO} = 1.14V to 1.26V, R_L = 50Ω to V_{CCO},
V_{CCO} = 1.7V to 1.9V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs,
V_{CC} = 2.375V to 2.625V. T_A = –40°C to +85°C, unless otherwise stated.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output HIGH Voltage	V_{OH}	V_{CCO} – 0.020	V_{CCO} – 0.010	V_{CCO}	V	R_L = 50Ω to V_{CCO}
Output Voltage Swing	V_{OUT}	300	390	475	mV	See Figure 6-3
Differential Output Voltage Swing	V_{DIFF_OUT}	600	780	950	mV	See Figure 6-5
Output Source Impedance	R_{OUT}	45	50	55	Ω	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-3: AC ELECTRICAL CHARACTERISTICS

V_{CCO} = 1.14V to 1.26V, R_L = 50Ω to V_{CCO},
V_{CCO} = 1.7V to 1.9V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs,
V_{CC} = 2.375V to 2.625V. T_A = –40°C to +85°C, unless otherwise stated.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	f_{MAX}	3.2	—	—	Gbps	NRZ Data
		3.2	—	—	GHz	V_{OUT} > 200 mV
Propagation Delay IN-to-Q	t_{PD}	150	205	300	ps	Figure 6-1
Within Device Skew	t_{SKEW}	—	3	15	ps	Note 1
Part-to-Part Skew		—	—	75	ps	Note 2
Additive Phase Jitter	t_{JITTER}	—	42	—	fs_{RMS}	Carrier = 622 MHz Integration Range: 12 kHz – 20 MHz
		—	250	—		Carrier = 156.25 MHz. Integration Range: 12 kHz – 20 MHz
Output Rise/Fall Times (20% to 80%)	t_R, t_F	30	60	95	ps	At full output swing.
Duty Cycle	—	47	—	53	%	Differential I/O

Note 1: Within device skew is measured between two different outputs under identical input transitions.

2: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	–40	—	+85	°C	—
Junction Operating Temperature	T_J	—	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 20 sec.
Package Thermal Resistance (Note 2)						
Thermal Resistance, 3 x 3 QFN-16LD	θ_{JA}	—	75	—	°C/W	Still-Air
	Ψ_{JB}	—	33	—	°C/W	Junction-to-board

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. θ_{JA} and Ψ_{Jb} values are determined for a 4-layer board in still-air number, unless otherwise stated.

2.0 TYPICAL OPERATING CHARACTERISTICS

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

For Figure 2-1 through Figure 2-3, V_{CC} = 2.5V, V_{CCO} = 1.2V, GND = 0V, V_{IN} = 100 mV; R_L = 50Ω to 1.2V; T_A = +25°C, unless otherwise stated.

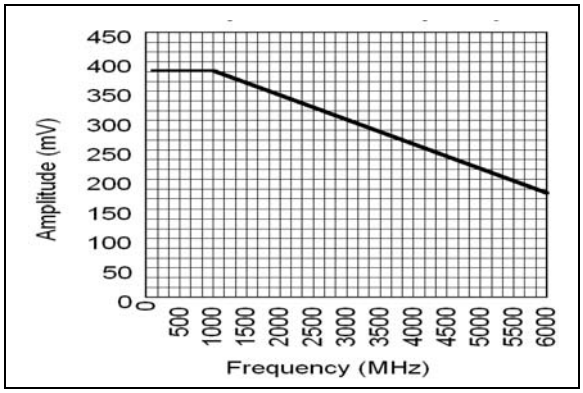


FIGURE 2-1: *Amplitude vs. Frequency.*

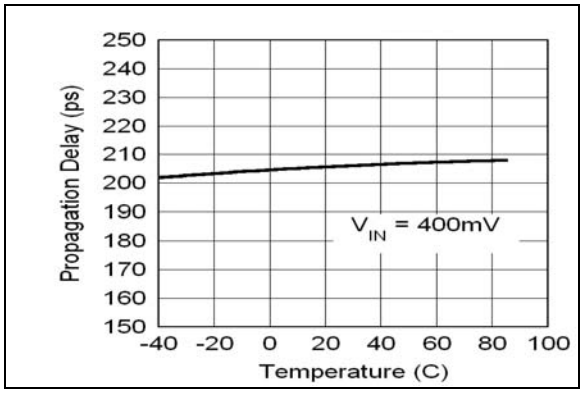


FIGURE 2-2: *Propagation Delay vs. Temperature.*

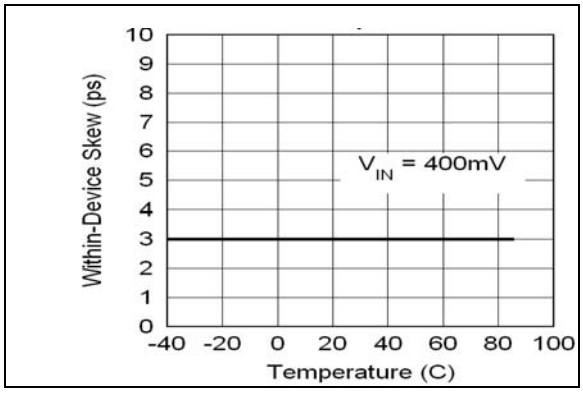


FIGURE 2-3: *Within-Device Skew vs. Temperature.*

For Figure 2-4 through Figure 2-7, V_{CC} = 2.5V, V_{CCO} = 1.2V, GND = 0V, V_{IN} = 100 mV; R_L = 50Ω to 1.2V, Data Pattern: 2^{23}-1; T_A = +25°C, unless otherwise stated.

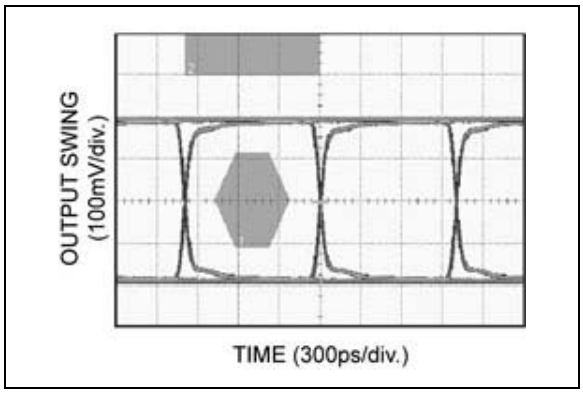


FIGURE 2-4: *1.0 Gbps Data.*

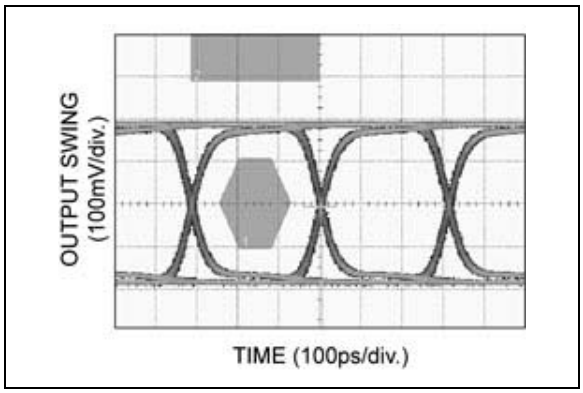


FIGURE 2-6: *3.2 Gbps Data.*

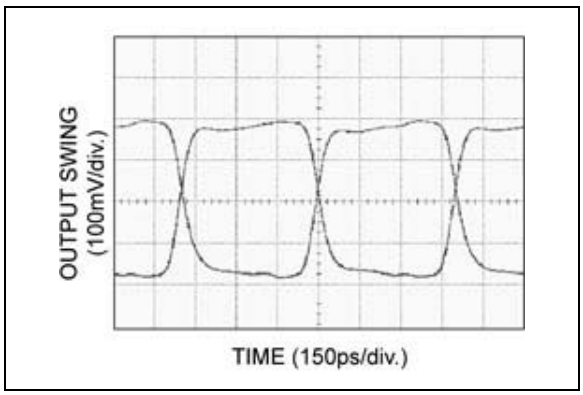


FIGURE 2-5: *1.0 GHz Clock.*

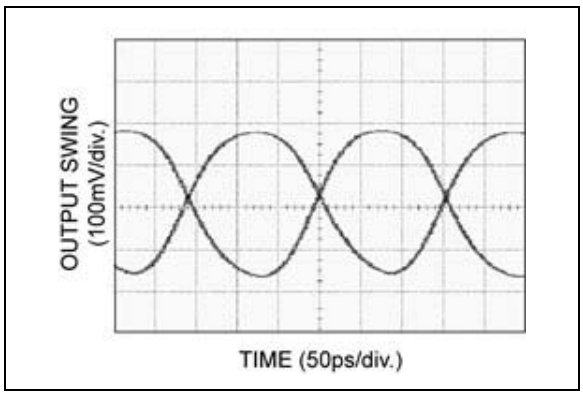


FIGURE 2-7: *3.2 GHz Clock.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1, 4	IN, /IN	Differential Input: This input pair is the differential signal input to the device. Input accepts differential signals as small as 100 mV (200 mV_{PP}). Each input pin internally terminates with 50Ω to the V_T pin.
2	V_T	Input Termination Center-Tap: Each side of the differential input pair terminates to V_T pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See the Input Interface Applications section.
3	V_{REF-AC}	Reference Voltage: This output biases to V_{CC} – 1.150V. It is used for AC-coupling inputs IN and /IN. Connect V_{REF-AC} directly to the V_T pin. Bypass with 0.1 µF low ESR capacitor to V_{CC}. Maximum sink/source current is ±0.5 mA. See the Input Interface Applications section.
5, 16	V_{CC}	Positive Power Supply: Bypass with 0.1 µF/0.01 µF low ESR capacitors as close to the V_{CC} pins as possible. Supplies input and core circuitry.
8, 13	V_{CCO}	Output Supply: Bypass with 0.1 µF//0.01 µF low ESR capacitors as close to the V_{CCO} pins as possible. Supplies the output buffers.
6, 7, 14, 15	GND, EP	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
10, 9 11, 12	/Q1, Q1 /Q0, Q0	CML Differential Output Pairs: Differential buffered copies of the input signal. The output swing is typically 390 mV. See the Input Interface Applications section for termination information.

4.0 INTERFACE APPLICATIONS

For Input Interface Applications see Figure 7-1 through Figure 7-7 and for CML Output Termination see Figure 8-1 through Figure 8-4.

4.1 CML Output Termination with V_{CCO} 1.2V

For V_{CCO} of 1.2V (see Figure 8-1), terminate the output with 50Ω-to-1.2V, DC-coupled, not 100Ω differentially across the outputs.

If AC-coupling is used (see Figure 8-4), terminate into 50Ω-to-1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage.

Do not AC couple with internally terminated receiver. For example, 50Ω ANY-IN input. AC-coupling will offset the output voltage by 200 mV and this offset voltage will be too low for proper driver operation.

Any unused output pair needs to be terminated when V_{CCO} is 1.2V, do not leave floating.

4.2 CML Output Termination with V_{CCO} 1.8V

For V_{CCO} of 1.8V, Figure 8-1 and Figure 8-2, terminate with either 50Ω-to-V_{CCO} or 100Ω differentially across the outputs. AC- or DC-coupling is fine.

4.3 Input AC Coupling

The SY54011R input can accept AC coupling from any driver. Tie V_T to V_{REF-AC} and bypass with a 0.1 µF capacitor as shown in Figure 7-3 and Figure 7-4.

5.0 ADDITIVE PHASE NOISE PLOTS

V_{CC} = +2.5V, GND = 0V, T_A = +25°C.

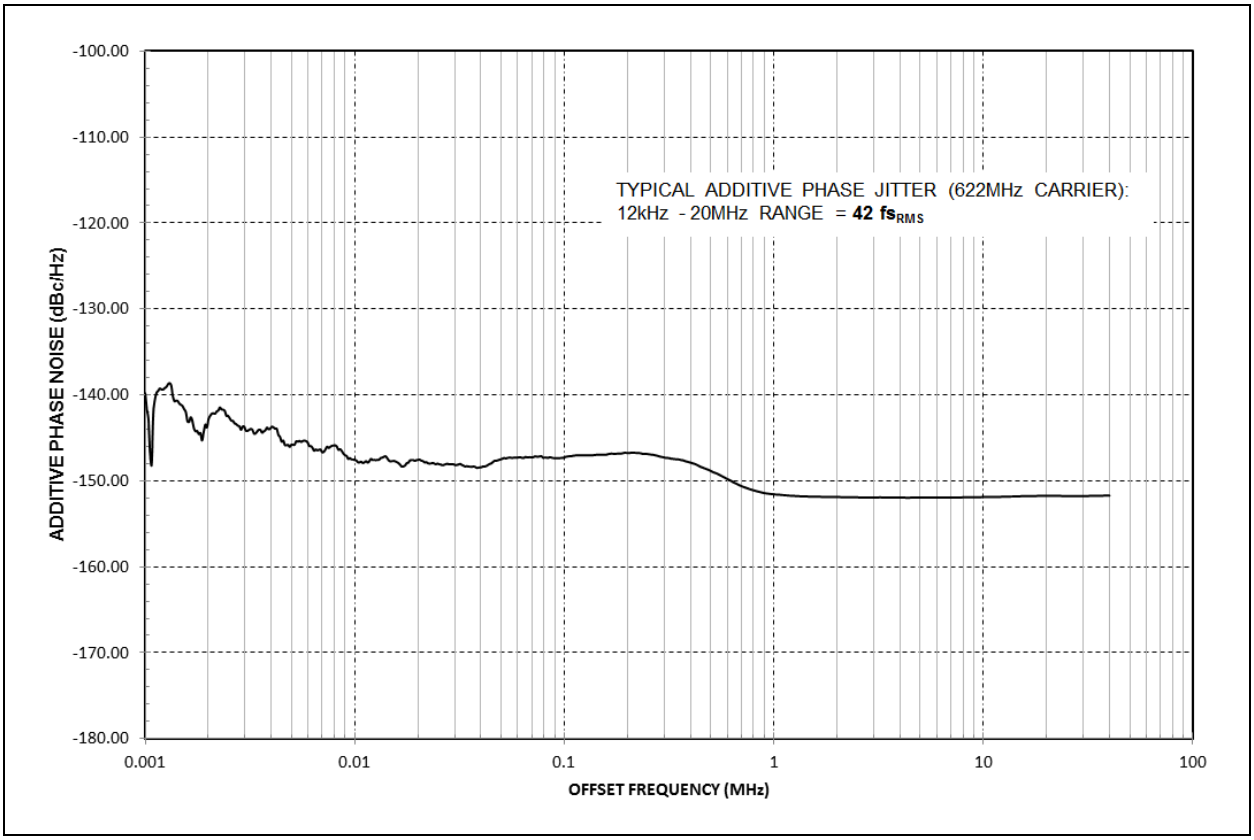


FIGURE 5-1: *Typical Additive Phase Jitter: 622 MHz Carrier, 12 kHz to 20 MHz Range, 42 fs_{RMS}.*

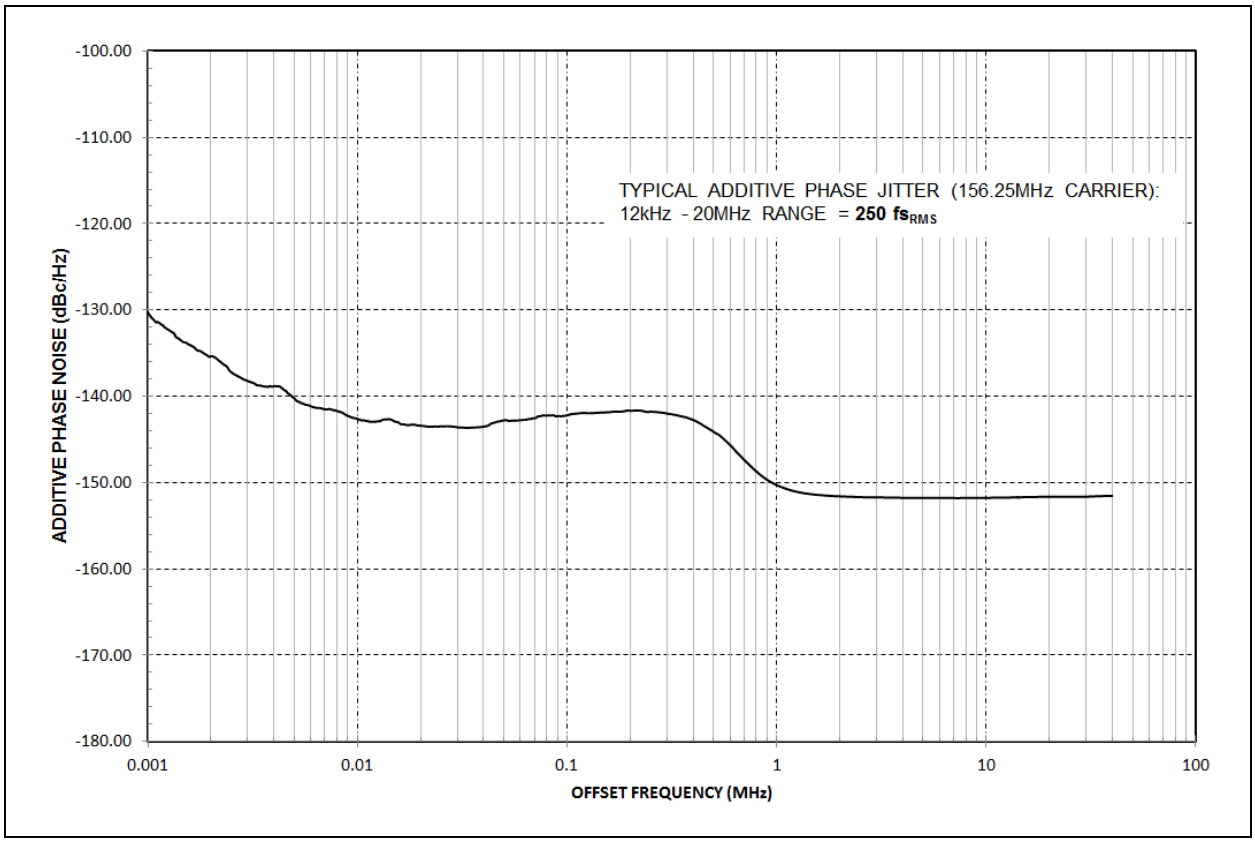


FIGURE 5-2: *Typical Additive Phase Jitter: 156.25 MHz Carrier, 12 kHz to 20 MHz Range, 250 fs_{RMS}.*

SY54011R

6.0 TIMING DIAGRAMS

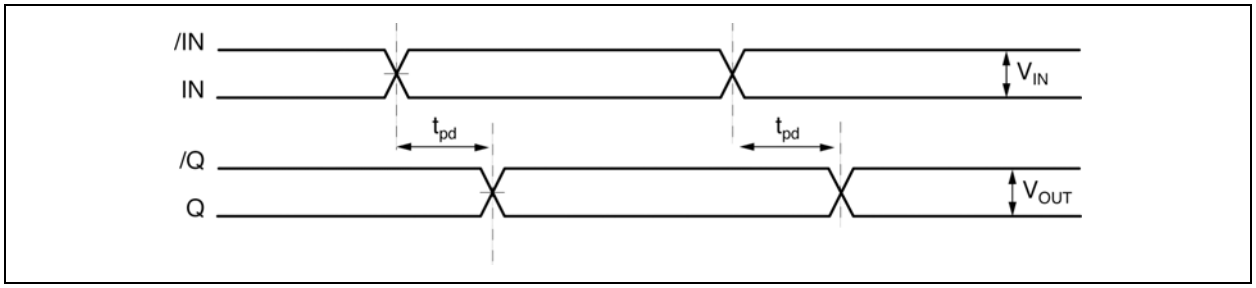


FIGURE 6-1: *Propagation Delay.*

6.1 Input and Output Stage

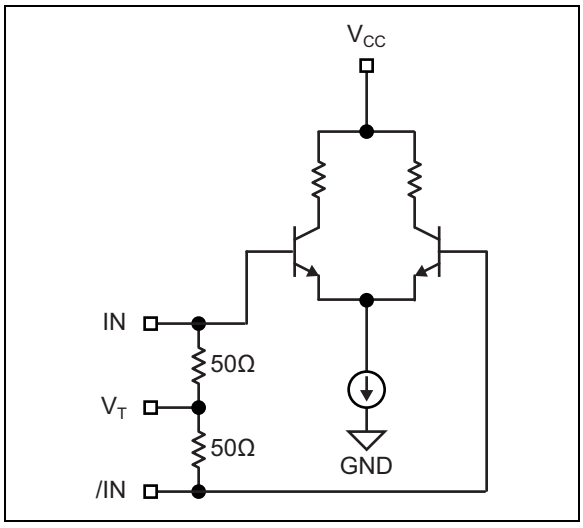


FIGURE 6-2: *Simplified Differential Input Buffer.*

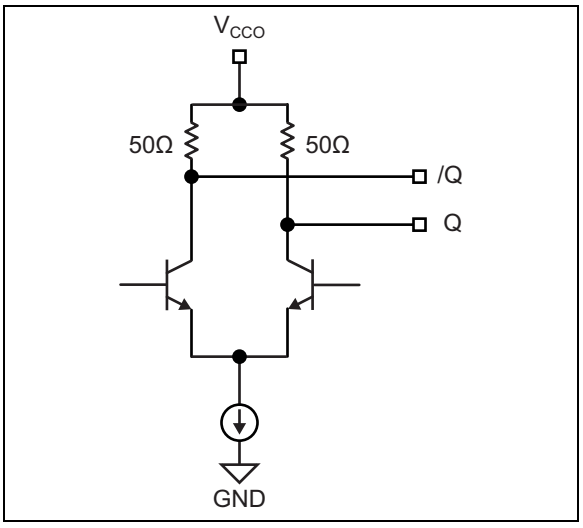


FIGURE 6-4: *Simplified CML Output Buffer.*

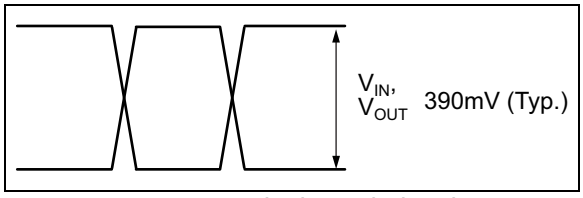


FIGURE 6-3: *Single-Ended Swing.*

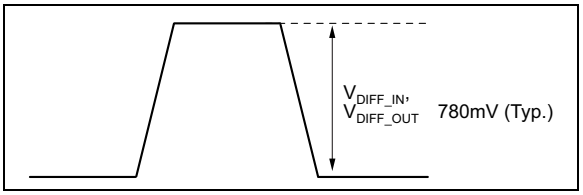


FIGURE 6-5: *Differential Swing.*

7.0 INPUT INTERFACE APPLICATIONS

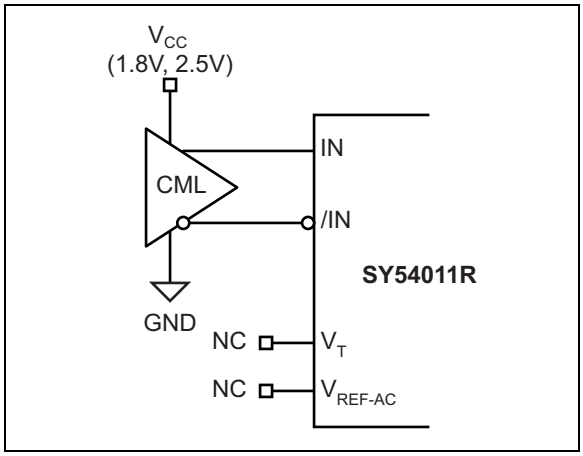


FIGURE 7-1: *CML Interface (DC-Coupled, 1.8V, 2.5V).*

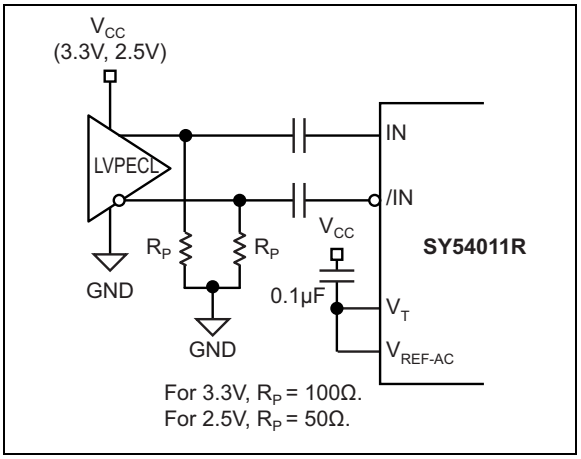


FIGURE 7-4: *LVPECL Interface (AC-Coupled).*

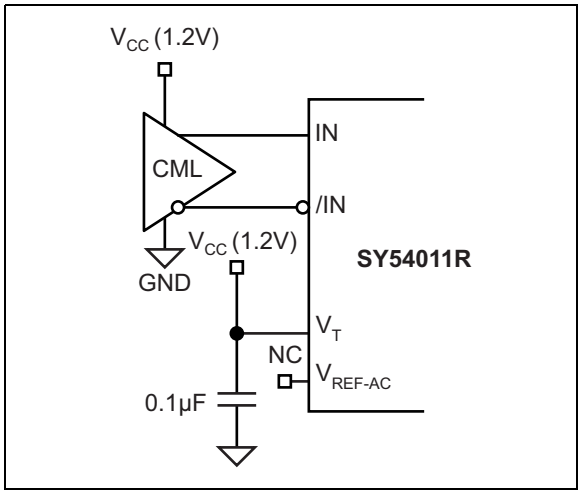


FIGURE 7-2: *CML Interface (DC-Coupled, 1.2V).*

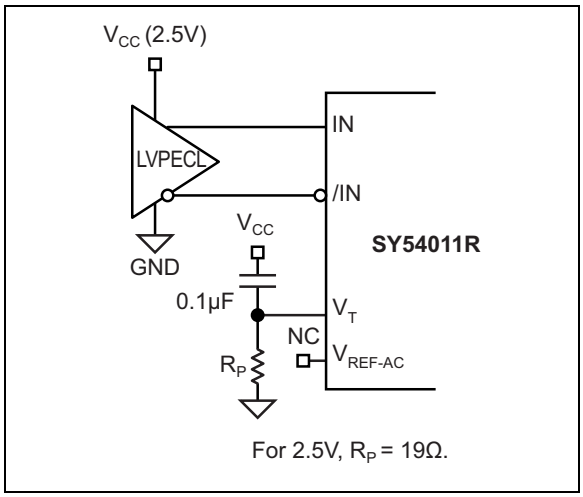


FIGURE 7-5: *LVPECL Interface (DC-Coupled).*

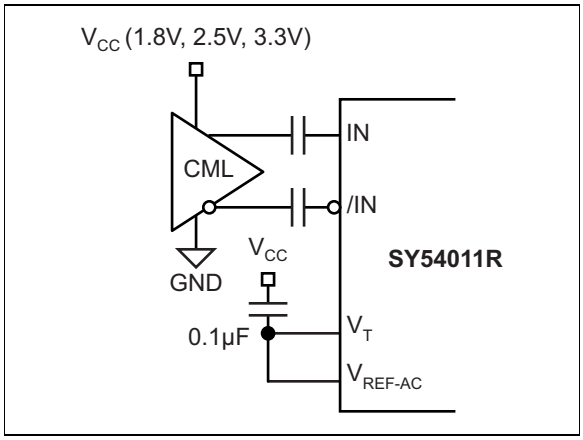


FIGURE 7-3: *CML Interface (AC-Coupled).*

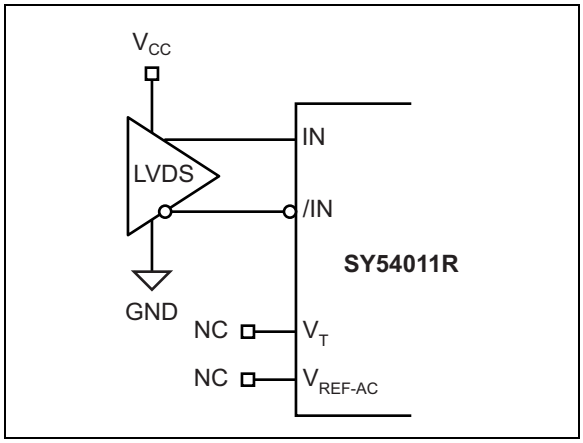


FIGURE 7-6: *LVDS Interface.*

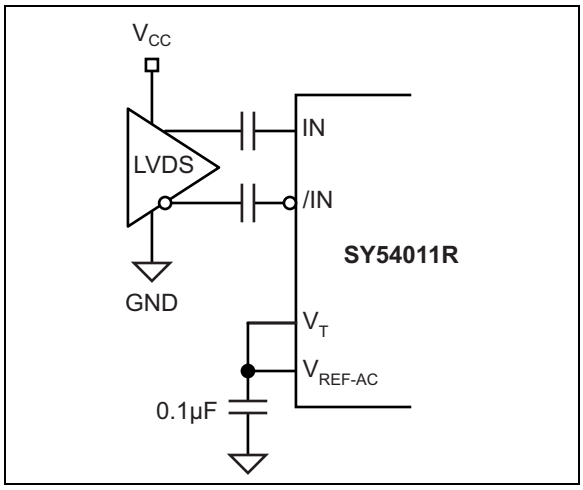


FIGURE 7-7: *LVDS Interface (AC-Coupled).*

8.0 CML OUTPUT TERMINATION

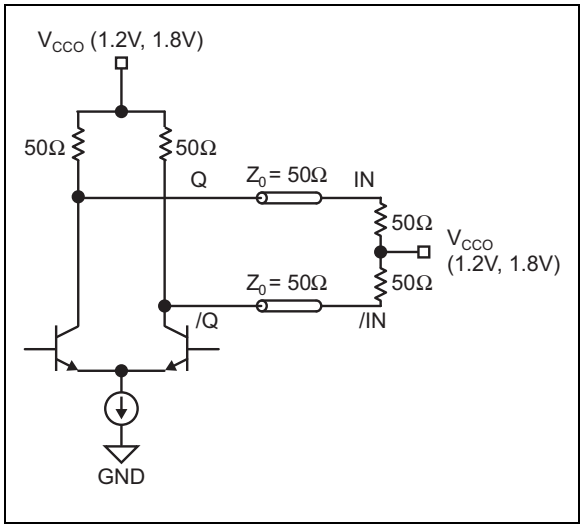


FIGURE 8-1: *1.2V or 1.8V CML DC-Coupled Termination.*

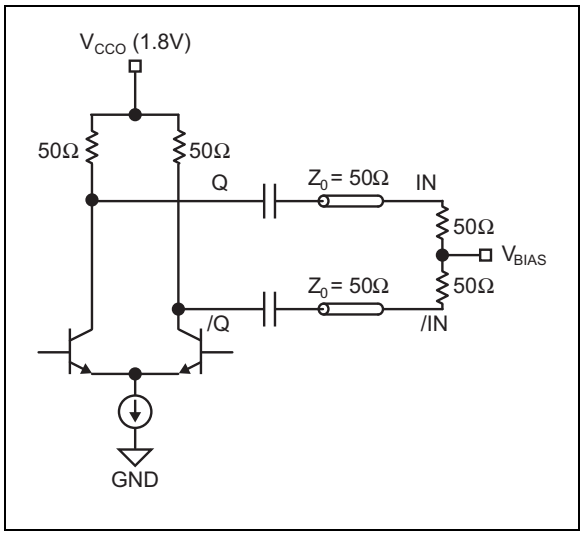


FIGURE 8-3: *CML AC-Coupled Termination (V_{CCO} 1.8V Only).*

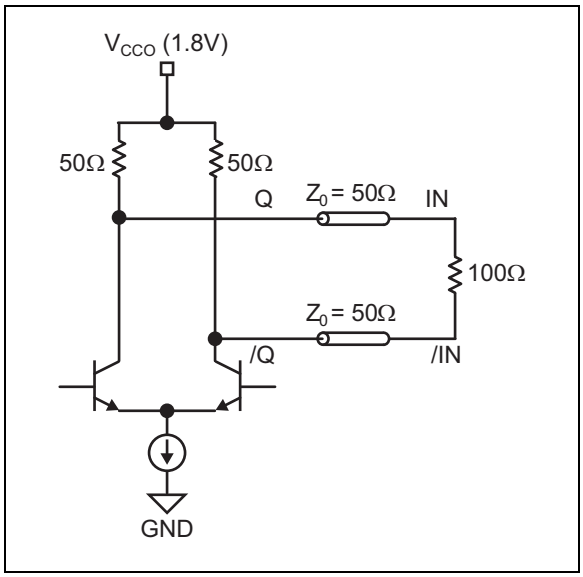


FIGURE 8-2: *1.8V CML DC-Coupled Termination.*

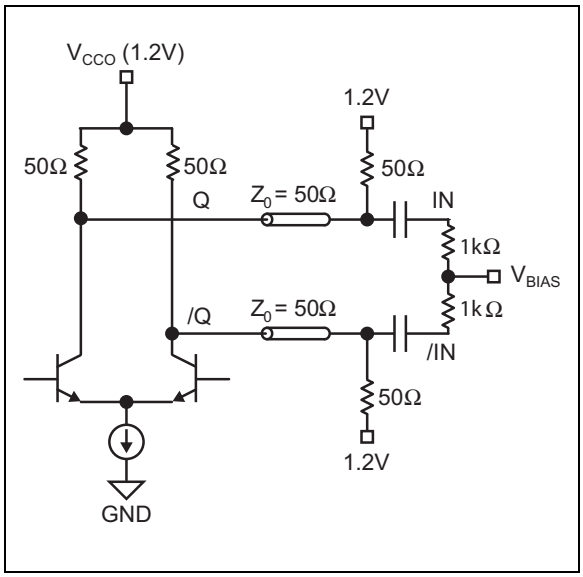
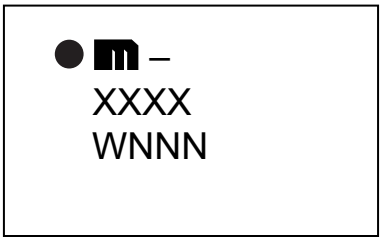


FIGURE 8-4: *CML AC-Coupled Termination (V_{CCO} 1.2V Only).*

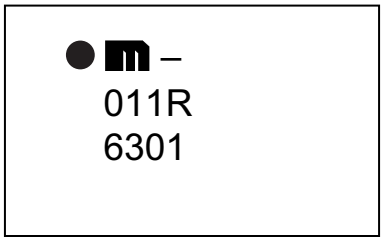
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

16-Pin QFN*



Example

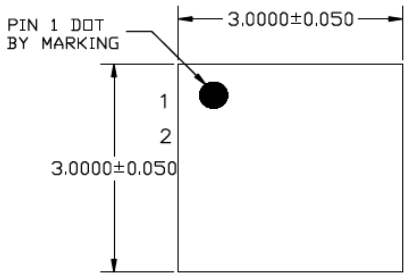


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

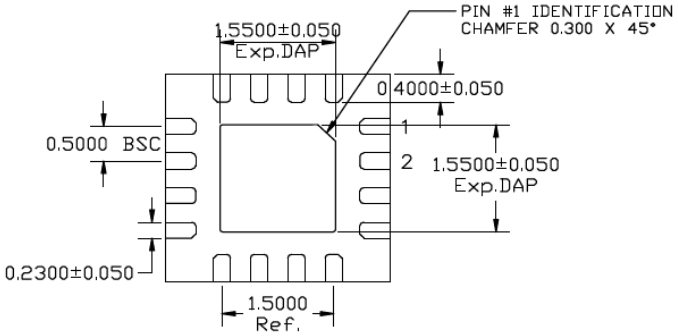
16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

TITLE
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

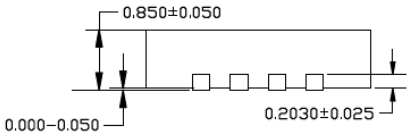
DRAWING #	QFN33-16LD-PL-1	UNIT	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



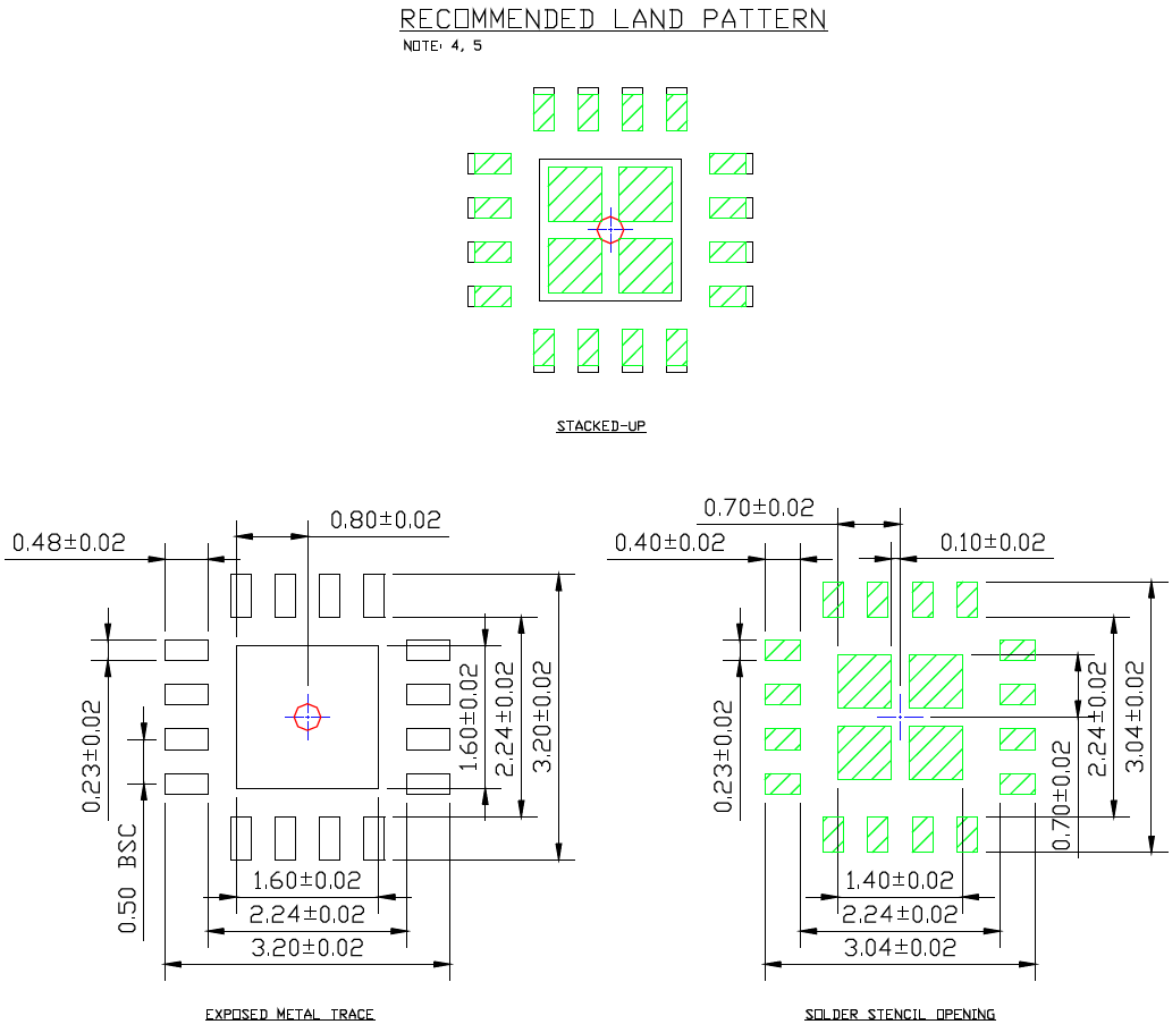
SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

SY54011R

POD-Land Pattern drawing # QFN33-16LD-PL-1



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (January 2018)

- Converted to Micrel data sheet SY54011R to Microchip data sheet template DS20005525A.
- Minor text changes throughout.
- Updated Additive Phase Noise Plots images.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Voltage Option	Package	Temperature Range	Media Type

Device:	SY54011:		Low Voltage 1.2V/1.8V CML 1:2 Fanout Buffer, 3.2 Gbps, 3.2 GHz
Voltage Option:	R	=	1.2V/1.8V/2.5V
Package:	M	=	16-Lead 3 mm x 3 mm QFN
Temperature Range:	G	=	–40°C to +85°C (NiPdAu Lead Free)
Media Type:	<blank>	=	100/Tube
	TR	=	1,000/Reel

Examples:

a) SY54011RMG: 1.2V, 1.8V, and 2.5V Output Voltage, 16-Lead 3 mm x 3 mm QFN, –40°C to +85°C, 100/Tube

b) SY54011RMG-TR: 1.2V, 1.8V, and 2.5V Output Voltage, 16-Lead 3 mm x 3 mm QFN, –40°C to +85°C, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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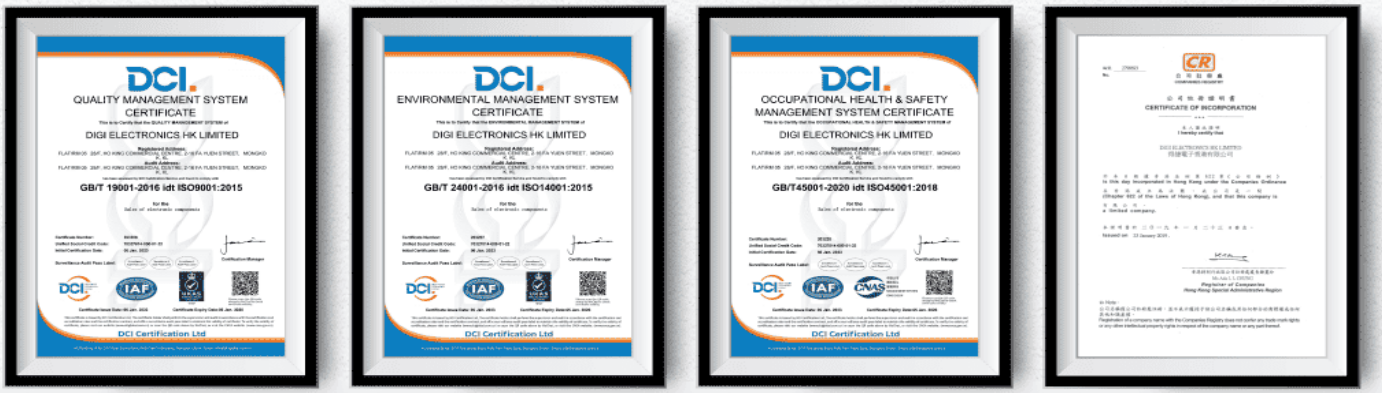

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