SY55853UKC Datasheet

www.digi-electronics.com

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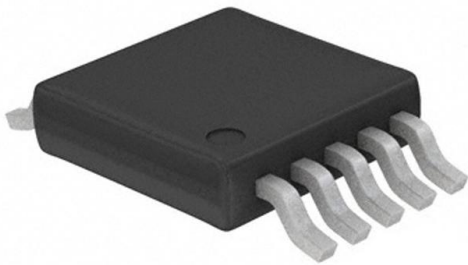
DiGi Electronics Part Number	SY55853UKC-DG
Manufacturer	Microchip Technology
Manufacturer Product Number	SY55853UKC
Description	IC LATCH D 2.5GHZ 10-MSOP
Detailed Description	D-Type Transparent Latch 1 Channel 1:1 IC Differential 10-MSOP

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
SY55853UKC	Microchip Technology
Series:	Product Status:
SY55	Discontinued at Digi-Key
Logic Type:	Circuit:
D-Type Transparent Latch	1:1
Output Type:	Voltage - Supply:
Differential	2.3V ~ 5.7V
Independent Circuits:	Delay Time - Propagation:
1	400ps
Current - Output High, Low:	Operating Temperature:
-	-40°C ~ 85°C
Mounting Type:	Package / Case:
Surface Mount	10-TFSOP, 10-MSOP (0.118", 3.00mm Width)
Supplier Device Package:	Base Product Number:
10-MSOP	SY55853

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
RoHS non-compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

MICREL ®

D LATCH

SuperLite™
SY55853U

FEATURES

- **2.5GHz min f$_{max}$**
- **2.3V to 5.7V power supply**
- **Single bit latch**
- **Stores or flows through 1 bit of data**
- **Optimized to work with SuperLite™ family**
- **Fully differential**
- **Source terminated CML outputs for fast edge rates**
- **Accepts CML, PECL, LVPECL input logic levels**
- **Available in a tiny 10-pin MSOP**

SuperLite™

DESCRIPTION

The SY55853U is a latch. Its differential output will flow through the input while it's enable is high. The output will remain static while the enable is low. In addition, an asynchronous, level sensitive reset is provided.

SY55853U inputs can be terminated with a single resistor between the true and the complement pins of a given input.

The SY55853U is a member of Micrel's SuperLite™ family of high-speed CML logic. This family features very small packaging and 2.3V to 5.7V operation.
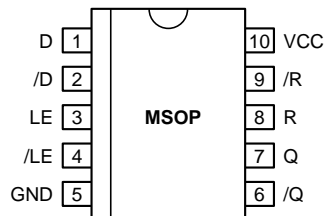
APPLICATIONS

- **High-speed logic**
- **OC-48 communication systems**

FUNCTIONAL BLOCK DIAGRAM

SuperLite is a trademark of Micrel, Inc.
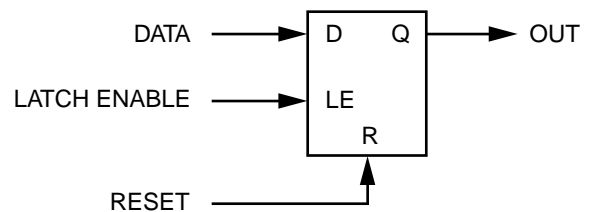
PACKAGE/ORDERING INFORMATION

10-Pin MSOP (K10-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY55853UKC	K10-1	Commercial	55853U	Sn-Pb
SY55853UKCTR[2]	K10-1	Commercial	55853U	Sn-Pb
SY55853UKI	K10-1	Industrial	55853U	Sn-Pb
SY55853UKITR[2]	K10-1	Industrial	55853U	Sn-Pb
SY55853UKG[3]	K10-1	Industrial	55853U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY55853UKGTR[2, 3]	K10-1	Industrial	55853U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25°C$, DC Electricals only.

2. Tape and Reel.

3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 2	D, /D	CML/PECL/LVPECL Input (Differential): This is the single bit of data that gets clocked in and remembered.
3, 4	LE, /LE	CML/PECL/LVPECL Latch Enable Input (Differential): The rising edge of this signal is the clock signal that determines when the Boolean value at the data input gets stored.
5	GND	Ground.
6, 7	Q, /Q	CML Output (Differential): This is the output of the flip-flop.
8, 9	R, /R	CML/PECL/LVPECL Reset Input (Differential): This is an asynchronous active high level reset, that forces the flip-flop into a known state, namely zero.
10	VCC	Power Supply.

TRUTH TABLE

D	LE	R	Q	/Q
X	0	0	Latched[1]	Latched[1]
0	1	0	0	1
1	1	0	1	0
X	X	1	0	1

Note 1. Retains data before LE falling transition.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

The true pin of an input pair is internally biased to ground through a 75kΩ resistor. The complement pin of an input pair is internally biased halfway between V_{CC} and ground by a voltage divider consisting of two 75kΩ resistors. To keep an input at static logic zero at $V_{CC} > 3.0V$, leave both inputs unconnected. For $V_{CC} \le 3.0V$, connect the complement input to V_{CC} and leave the true input unconnected. To make an input static logic one, connect the true input to V_{CC}, leave the complement input unconnected. These are the only ;safe ways to cause inputs to be at a static value. In particular, no input pin should be directly connected to ground. All NC (no connect) pins should be unconnected.
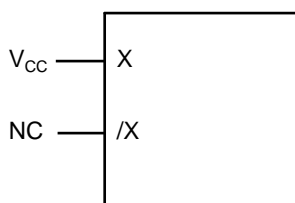

Figure 1. Hard Wiring A Logic "1" [1]

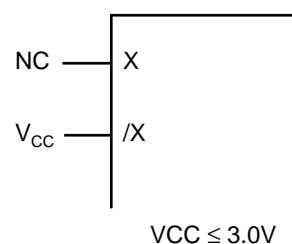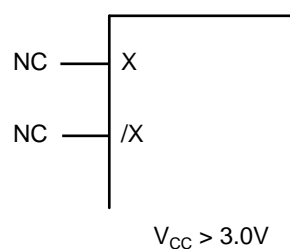**Note 1.**   X is either D, LE, R input. /X is either /D, /LE, /R input.

$V_{CC} > 3.0V$

VCC $\le$ 3.0V

Figure 2. Hard Wiring A Logic "0" [1]

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) .... –0.5V to +6.0V

CML Output Voltage.......................... V_{CC} –1.0 to V_{CC} +0.5

Lead Temperature (soldering, 20 sec.) .... 260°C

Storage Temperature (T_S) .... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage (V_{IN}) .... –0.5 to V_{CC} +0.5

Ambient Temperature (T_A) .... –40°C to +85°C

Package Thermal Resistance
　MSOP (θ_{JA})
　　Still-Air .... 113°C/W
　　500lpfm .... 96°C/W

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

DC ELECTRICAL CHARACTERISTICS(Note 1)

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = –40°C to +85°C; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		2.3		5.7	V
I_{CC}	Power Supply Current				37	mA

Note 1. The device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥500lfpm is maintained.

CML DC ELECTRICAL CHARACTERISTICS(Note 1)

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = –40°C to +85°C; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{ID}	Differential Input Voltage		100			mV
V_{IH}	Input HIGH Voltage	**Note 2**	1.6	—	V_{CC}	V
V_{IL}	Input LOW Voltage	**Note 2**	1.5	—	$V_{CC} - 0.1$	V
V_{OH}	Output HIGH Voltage	No Load	$V_{CC} - 0.020$	$V_{CC} - 0.010$	V_{CC}	V
V_{OL}	Output LOW Voltage	No Load	$V_{CC} - 0.97$	$V_{CC} - 0.825$	$V_{CC} - 0.660$	V
V_{OS}	Output Voltage Swing	No Load, **Note 3** 100Ω Environment, **Note 4** 50Ω Environment, **Note 5**	0.660	0.800 0.400 0.200	0.950	V
R_{DRIVE}	Output Source Impedance		80	100	120	Ω

Note 1. The device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥500lfpm is maintained.

**Note 2.** Inputs must be biased to logic LOW or HIGH when V_{CC} is less than 3.0V.

Note 3. Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in the 100Ω environment and a 200mV swing in the 50Ω environment. Refer to the "CML Termination" diagram for more details.

Note 4. See Figure 4.

Note 5. See Figure 3a and 3b.

AC ELECTRICAL CHARACTERISTICS(Note 1)

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = −40°C to +85°C; unless noted.

| Symbol	Parameter		Condition	Min	Typ	Max	Units
f_{MAX}	Max. Operating Frequency			2.5			GHz
t_{pd}	Propagation Delay	D to Q				400	ps
		LE to Q				400	ps
		R to Q				500	ps
t_S	Set-Up Time	D to LE		70			ps
		D to R					
t_H	Hold Time	LE to D		40			ps
t_{RR}	Reset Recovery			400			ps
t_{PW}	Minimum Pulse Width	LE High		160			ps
		R High		250			
t_r, t_f	CML Output Rise/Fall Times	−40°C to 0°C				175	ps
	(20% to 80%)	0°C to 85°C		35		160	

Note 1. Tested using environment of Figure 3b, 50Ω load CML output.
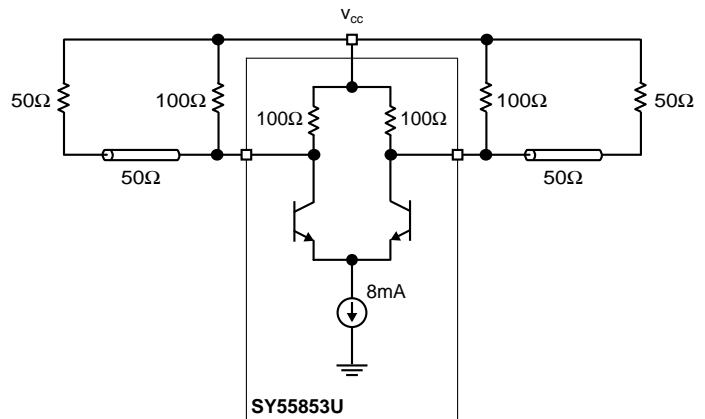
TIMING DIAGRAMS
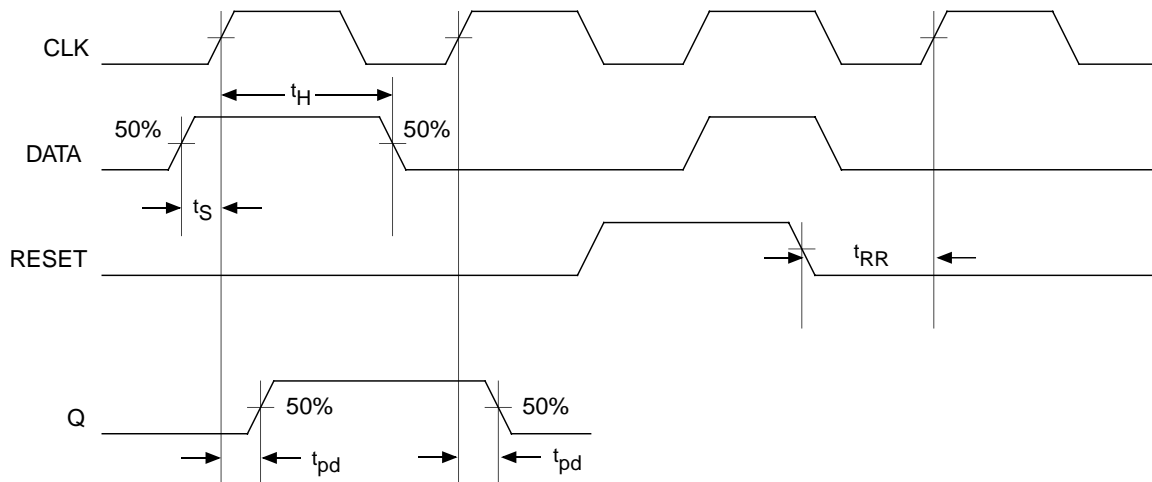
CML TERMINATION

All inputs accept the output from any other member of this family. All outputs are source terminated 100Ω CML differential drivers as shown in Figures 3 and 4. SY55853U expects the inputs to be terminated, and that good high speed design practices be adhered to. SY55853U inputs are designed to accept a termination resistor between the true and complement inputs of a differential pair. 0402 form factor chip resistors will fit with some trace fanout.
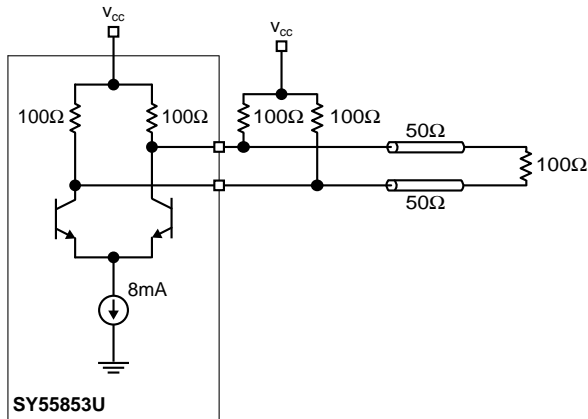
Figure 3a.   Differentially Terminated
(50Ω Load CML Output)

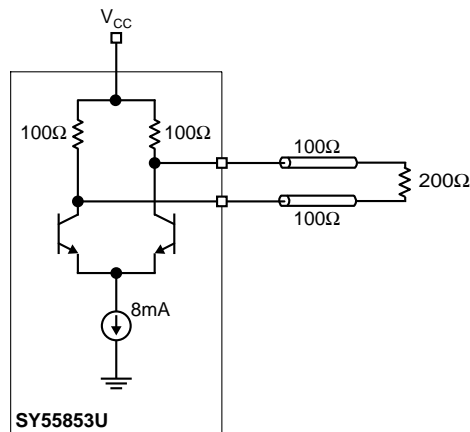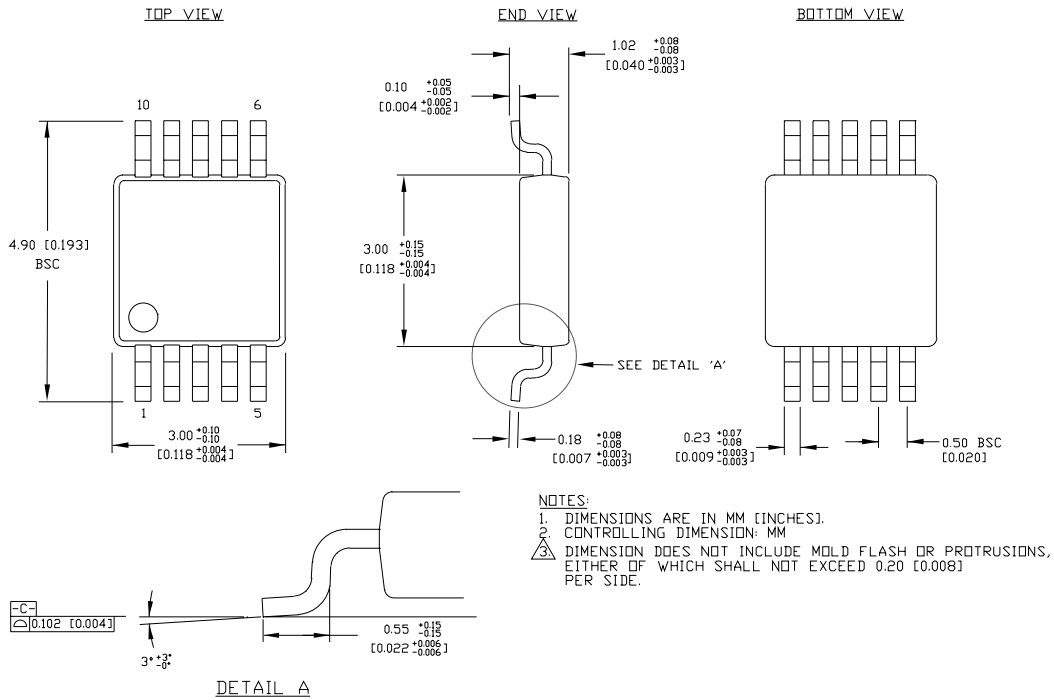**Figure 3b.   Individually Terminated**
(50Ω Load CML Output)

Figure 4.   100Ω Load CML Output

Micrel, Inc.

SuperLite™
SY55853U

10-PIN MSOP (K10-1)

TOP VIEW

END VIEW

BOTTOM VIEW

1.02 $^{+0.08}_{-0.08}$ [0.040 $^{+0.003}_{-0.003}$]

0.10 $^{+0.05}_{-0.05}$ [0.004 $^{+0.002}_{-0.002}$]

3.00 $^{+0.15}_{-0.15}$ [0.118 $^{+0.004}_{-0.004}$]

SEE DETAIL 'A'

0.18 $^{+0.08}_{-0.08}$ [0.007 $^{+0.003}_{-0.003}$]

0.23 $^{+0.07}_{-0.08}$ [0.009 $^{+0.003}_{-0.003}$]

0.50 BSC [0.020]

10   6

4.90 [0.193] BSC

1   5

3.00 $^{+0.10}_{-0.10}$ [0.118 $^{+0.004}_{-0.004}$]

NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

-C-
0.102 [0.004]

3° $^{+3°}_{-0°}$

0.55 $^{+0.15}_{-0.15}$ [0.022 $^{+0.006}_{-0.006}$]

DETAIL A

Rev. 00

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