# VN0550N3-G Datasheet


| | |
|---|---|
| DiGi Electronics Part Number | VN0550N3-G-DG |
| Manufacturer | Microchip Technology |
| Manufacturer Product Number | VN0550N3-G |
| Description | MOSFET N-CH 500V 50MA TO92-3 |
| Detailed Description | N-Channel 500 V 50mA (Tj) 1W (Tc) Through Hole TO-92-3 |

https://www.DiGi-Electronics.com

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## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| VN0550N3-G | Microchip Technology |
| Series: | Product Status: |
| - | Active |
| FET Type: | Technology: |
| N-Channel | MOSFET (Metal Oxide) |
| Drain to Source Voltage (Vdss): | Current - Continuous Drain (Id) @ 25°C: |
| 500 V | 50mA (Tj) |
| Drive Voltage (Max Rds On, Min Rds On): | Rds On (Max) @ Id, Vgs: |
| 5V, 10V | 60Ohm @ 50mA, 10V |
| Vgs(th) (Max) @ Id: | Vgs (Max): |
| 4V @ 1mA | ±20V |
| Input Capacitance (Ciss) (Max) @ Vds: | FET Feature: |
| 55 pF @ 25 V | - |
| Power Dissipation (Max): | Operating Temperature: |
| 1W (Tc) | -55°C ~ 150°C (TJ) |
| Mounting Type: | Supplier Device Package: |
| Through Hole | TO-92-3 |
| Package / Case: | Base Product Number: |
| TO-226-3, TO-92-3 (TO-226AA) | VN0550 |

## Environmental & Export classification

| RoHS Status: | Moisture Sensitivity Level (MSL): |
| --- | --- |
| ROHS3 Compliant | 1 (Unlimited) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8541.29.0095 | |

# VN0550

## N-Channel Enhancement-Mode Vertical DMOS FET

### Features

- Free from Secondary Breakdown
- Low Power Drive Requirement
- Ease of Paralleling
- Low $C_{ISS}$ and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- High Input Impedance and High Gain

### Applications

- Motor Controls
- Converters
- Amplifiers
- Switches
- Power Supply Circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

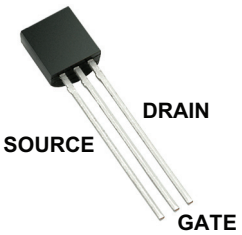
### General Description

The VN0550 Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

### Package Type

**3-lead TO-92**
(Top view)




See Table 3-1 for pin information.

# VN0550

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Drain-to-Source Voltage ..... $BV_{DSS}$
Drain-to-Gate Voltage ..... $BV_{DGS}$
Gate-to-Source Voltage ..... ±20V
Operating Ambient Temperature, $T_A$ ..... –55°C to +150°C
Storage Temperature, $T_S$ ..... –55°C to +150°C

**† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** $T_A$ = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | 500 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 1 mA |
| Gate Threshold Voltage | $V_{GS(th)}$ | 2 | — | 4 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA |
| Change in $V_{GS(th)}$ with Temperature | $\Delta V_{GS(th)}$ | — | –3.8 | –5 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA (**Note 1**) |
| Gate Body Leakage Current | $I_{GSS}$ | — | — | 100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| Zero-Gate Voltage Drain Current | $I_{DSS}$ | — | — | 10 | µA | $V_{GS}$ = 0V, $V_{DS}$ = Maximum rating |
| | | — | — | 1 | mA | $V_{DS}$ = 0.8 Maximum rating, $V_{GS}$ = 0V, $T_A$ = 125°C (**Note 1**) |
| On-State Drain Current | $I_{D(ON)}$ | — | 100 | — | mA | $V_{GS}$ = 5V, $V_{DS}$ = 25V |
| | | 150 | 350 | — | mA | $V_{GS}$ = 10V, $V_{DS}$ = 25V |
| Static Drain-to-Source On-State Resistance | $R_{DS(ON)}$ | — | 45 | — | Ω | $V_{GS}$ = 5V, $I_D$ = 50 mA |
| | | — | 40 | 60 | Ω | $V_{GS}$ = 10V, $I_D$ = 50 mA |
| Change in $R_{DS(ON)}$ with Temperature | $\Delta R_{DS(ON)}$ | — | 1 | 1.7 | %/°C | $V_{GS}$ = 10V, $I_D$ = 50 mA (**Note 1**) |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

## AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** $T_A$ = 25°C unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Forward Transconductance | $G_{FS}$ | 50 | 100 | — | mmho | $V_{DS}$ = 25V, $I_D$ = 50 mA |
| Input Capacitance | $C_{ISS}$ | — | 45 | 55 | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1 MHz |
| Common Source Output Capacitance | $C_{OSS}$ | — | 8 | 10 | pF | |
| Reverse Transfer Capacitance | $C_{RSS}$ | — | 2 | 5 | pF | |
| Turn-On Delay Time | $t_{d(ON)}$ | — | — | 10 | ns | $V_{DD}$ = 25V, $I_D$ = 150 mA, $R_{GEN}$ = 25Ω |
| Rise Time | $t_r$ | — | — | 15 | ns | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | — | — | 10 | ns | |
| Fall Time | $t_f$ | — | — | 10 | ns | |
| **DIODE PARAMETER** | | | | | | |
| Diode Forward Voltage Drop | $V_{SD}$ | — | 0.8 | — | V | $V_{GS}$ = 0V, $I_{SD}$ = 500 mA (**Note 1**) |
| Reverse Recovery Time | $t_{rr}$ | — | 300 | — | ns | $V_{GS}$ = 0V, $I_{SD}$ = 500 mA |

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested at 25°C. Pulse test: 300 µs pulse, 2% duty cycle

## TEMPERATURE SPECIFICATIONS

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **TEMPERATURE RANGE** | | | | | | |
| Operating Ambient Temperature | $T_A$ | –55 | — | +150 | °C | |
| Storage Temperature | $T_S$ | –55 | — | +150 | °C | |
| **PACKAGE THERMAL RESISTANCE** | | | | | | |
| 3-lead TO-92 | $\theta_{JA}$ | — | 132 | — | °C/W | |

## THERMAL CHARACTERISTICS

| Package | $I_D$ (**Note 1**) (Continuous) (mA) | $I_D$ (Pulsed) (mA) | Power Dissipation at $T_A$ = 25°C (W) | $I_{DR}$ (**Note 1**) (mA) | $I_{DRM}$ (mA) |
|---|---|---|---|---|---|
| 3-lead TO-92 | 50 | 250 | 1 | 50 | 250 |

**Note 1:** $I_D$ (continuous) is limited by maximum rated $T_J$.

# VN0550

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

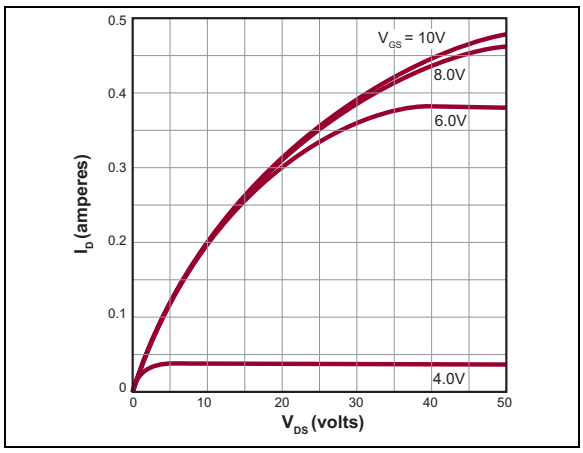



***FIGURE 2-1:*** *Output Characteristics.*

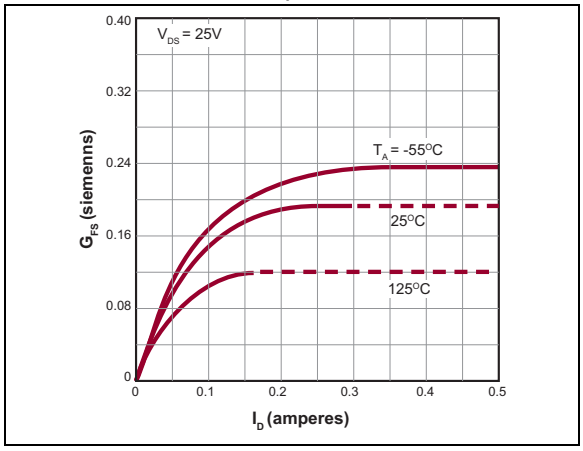



***FIGURE 2-2:*** *Transconductance vs. Drain Current.*

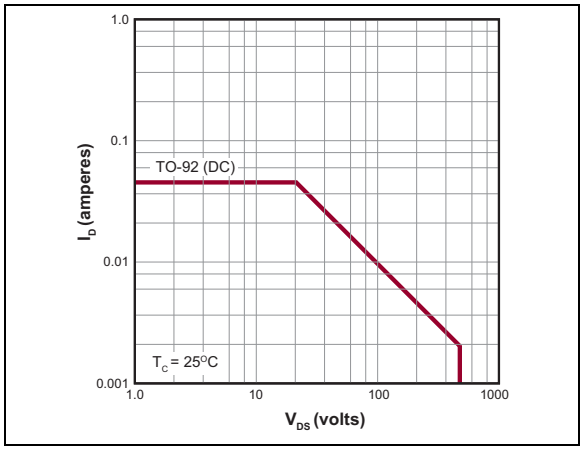



***FIGURE 2-3:*** *Maximum Rated Safe Operating Area.*

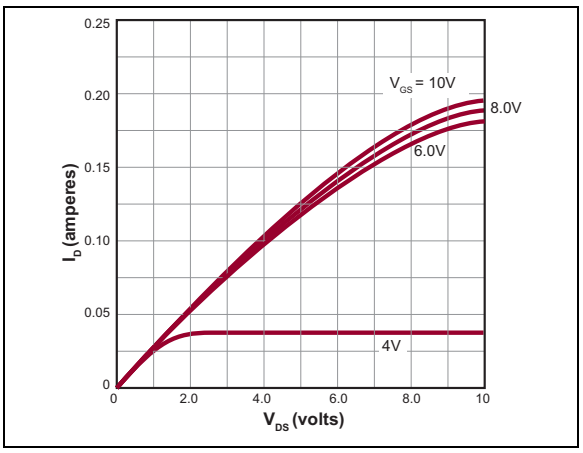



***FIGURE 2-4:*** *Saturation Characteristics.*

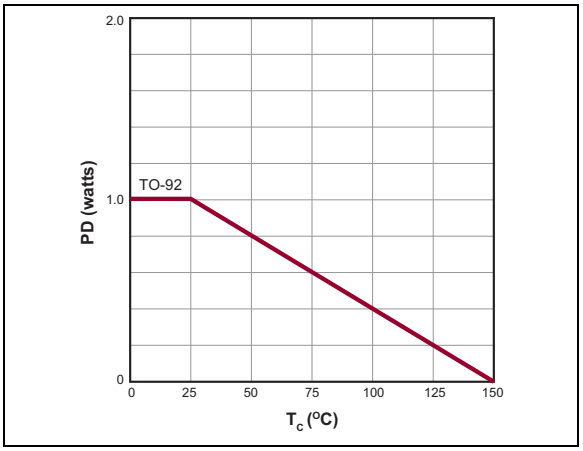



***FIGURE 2-5:*** *Power Dissipation vs. Case Temperature.*

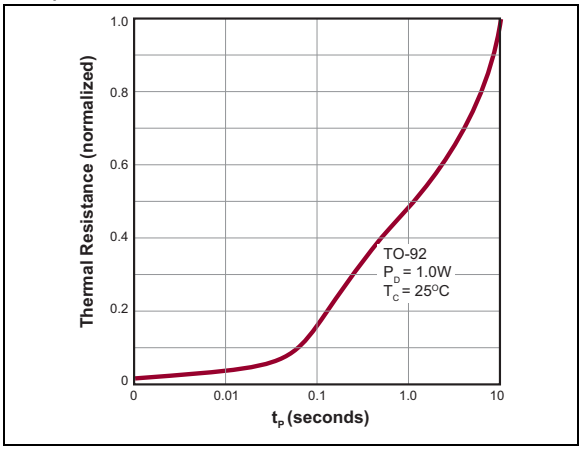



***FIGURE 2-6:*** *Thermal Response Characteristics.*

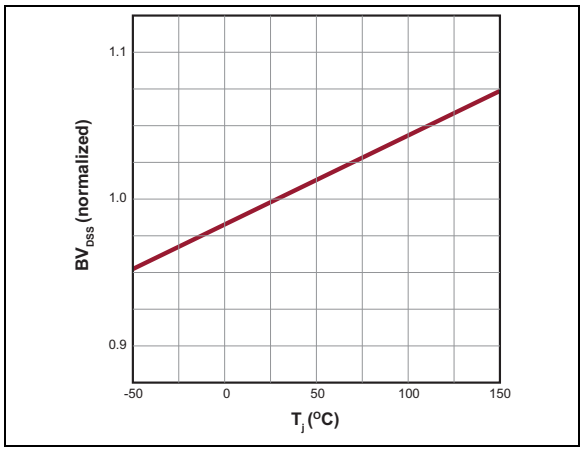



***FIGURE 2-7:*** *$BV_{DSS}$ Variation with Temperature.*

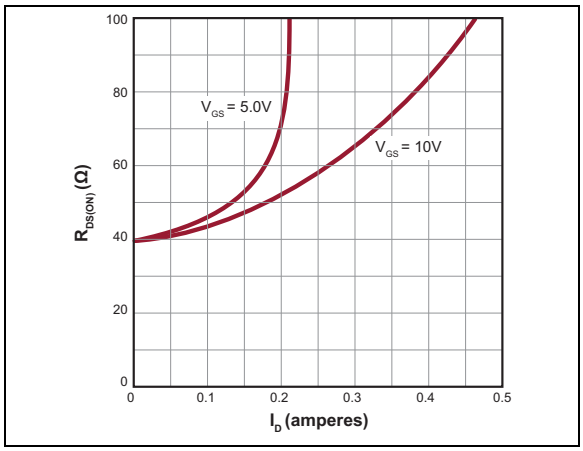



***FIGURE 2-10:*** *On-Resistance vs. Drain Current.*

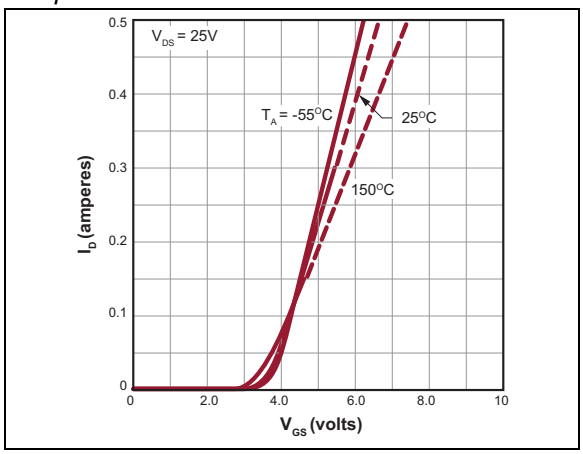



***FIGURE 2-8:*** *Transfer Characteristics.*

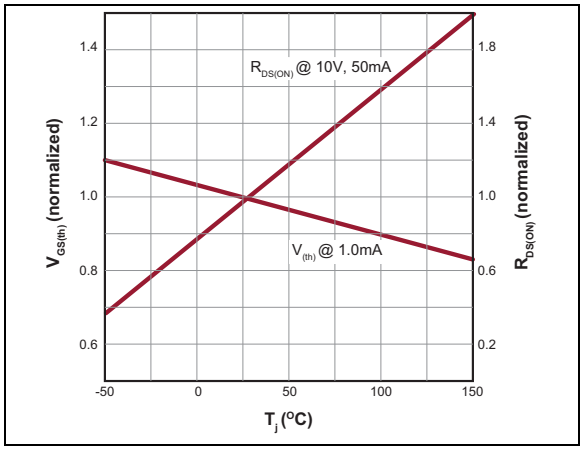



***FIGURE 2-11:*** *$V_{(th)}$ and $R_{DS}$ Variation with Temperature.*

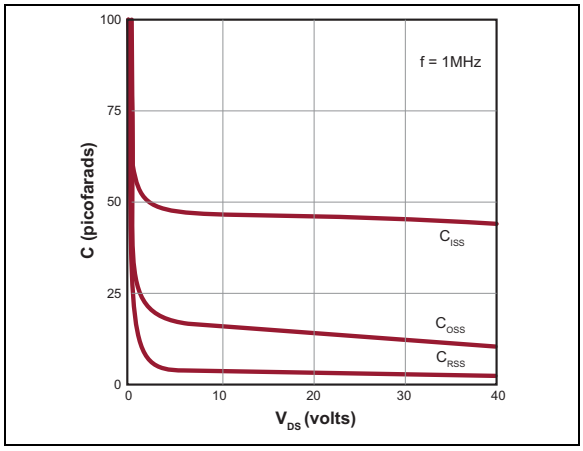



***FIGURE 2-9:*** *Capacitance vs. Drain-to-Source Voltage.*

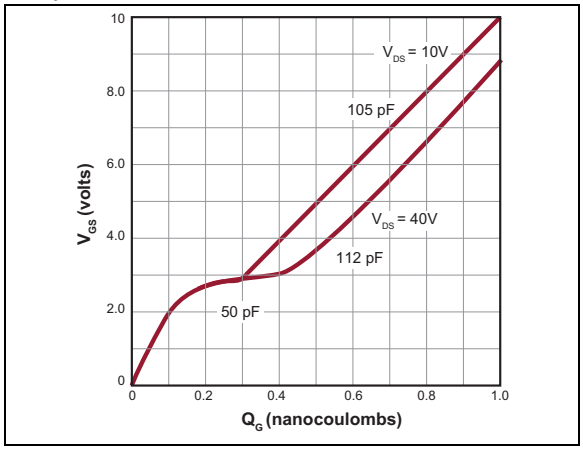



***FIGURE 2-12:*** *Gate Drive Dynamic Characteristics.*

## 3.0 PIN DESCRIPTION

The details on the pins of VN0550 are listed in Table 3-1. Refer to **Package Type** for the location of pins.

**TABLE 3-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | Source | Source |
| 2 | Gate | Gate |
| 3 | Drain | Drain |

## 4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for VN0550.

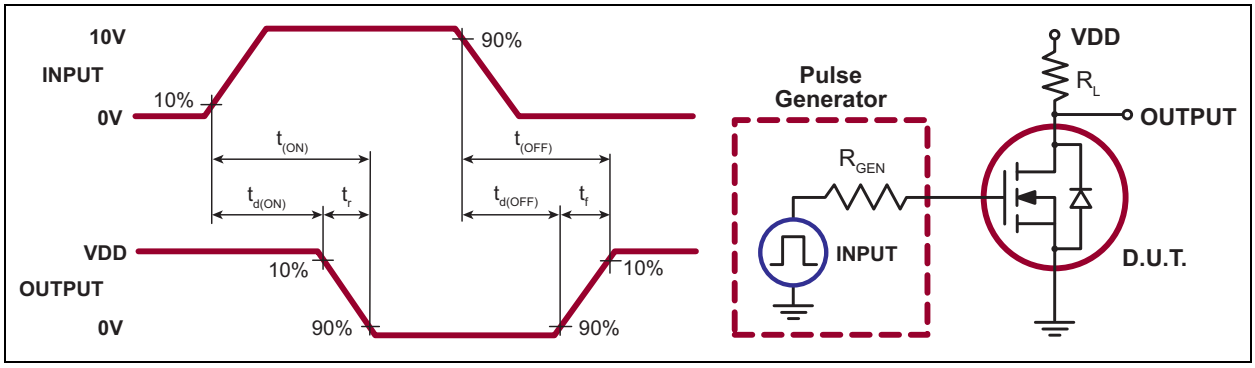



***FIGURE 4-1:*** *Switching Waveforms and Test Circuit.*

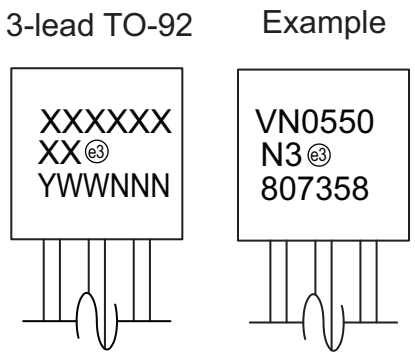
**TABLE 4-1: PRODUCT SUMMARY**

| $BV_{DSS}/BV_{DGS}$ (V) | $R_{DS(ON)}$ (Maximum) (Ω) | $I_{DSS}$ (Minimum) (mA) |
|---|---|---|
| 500 | 60 | 150 |

# VN0550

## 5.0 PACKAGING INFORMATION

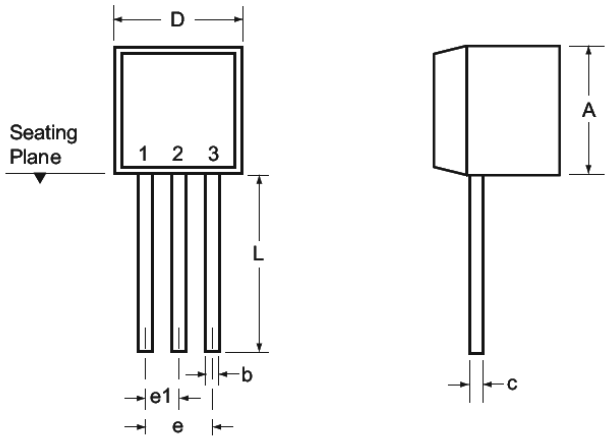
### 5.1 Package Marking Information



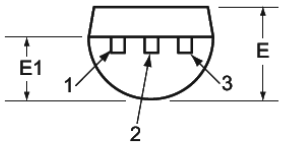

| | | |
|---|---|---|
| **Legend:** | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

## 3-Lead TO-92 Package Outline (L/LL/N3)




**Front View** **Side View**




**Bottom View**

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

| Symbol | | A | b | c | D | E | E1 | e | e1 | L |
|---|---|---|---|---|---|---|---|---|---|---|
| Dimensions (inches) | MIN | .170 | .014† | .014† | .175 | .125 | .080 | .095 | .045 | .500 |
| | NOM | - | - | - | - | - | - | - | - | - |
| | MAX | .210 | .022† | .022† | .205 | .165 | .105 | .105 | .055 | .610* |

*JEDEC Registration TO-92.*
** This dimension is not specified in the JEDEC drawing.*
*† This dimension differs from the JEDEC drawing.*
***Drawings not to scale.***

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision A (October 2018)

- Converted Supertex Doc# DSFP-VN0550 to Microchip DS20005978A
- Added a pin function table
- Changed the package marking format
- Removed the 3-Lead TO-92 N3 P002, P003, P005, and P014 media types
- Made minor text changes throughout the document

# VN0550

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | XX | - | X | - | X |
|---|---|---|---|---|---|
| Device | Package Options | | Environmental | | Media Type |

| | | | |
|---|---|---|---|
| Device: | VN0550 | = | N-Channel Enhancement-Mode Vertical DMOS FET |
| Package: | N3 | = | 3-lead TO-92 |
| Environmental: | G | = | Lead (Pb)-free/RoHS-compliant Package |
| Media Types: | (blank) | = | 1000/Bag for an N3 Package |
| | P013 | = | 2000/Ammo Pack for an N3 Package |

**Examples:**

| | |
|---|---|
| a) VN0550N3-G: | N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 1000/Bag |
| b) VN0550N3-G-P013: | N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 2000/Ammo Pack |

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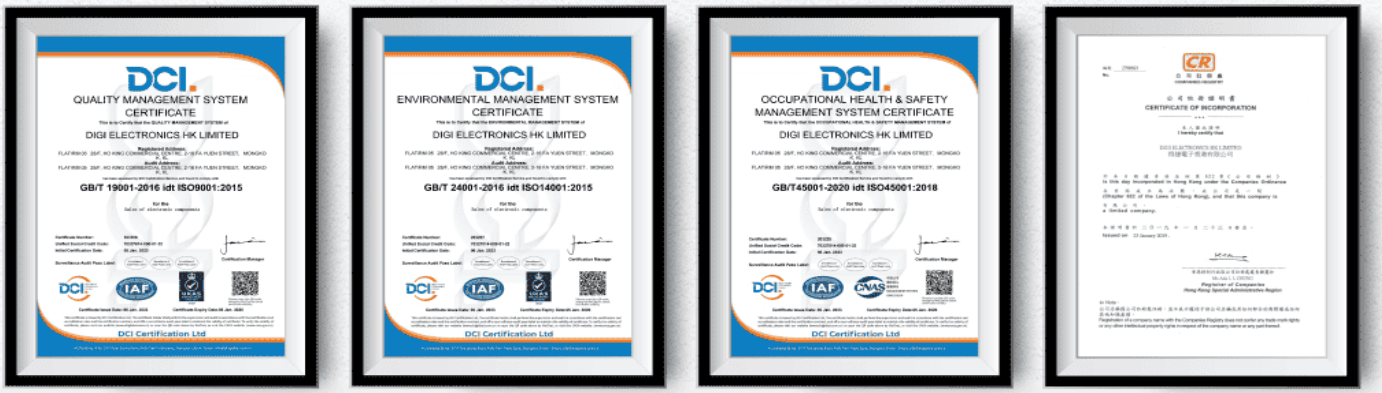



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