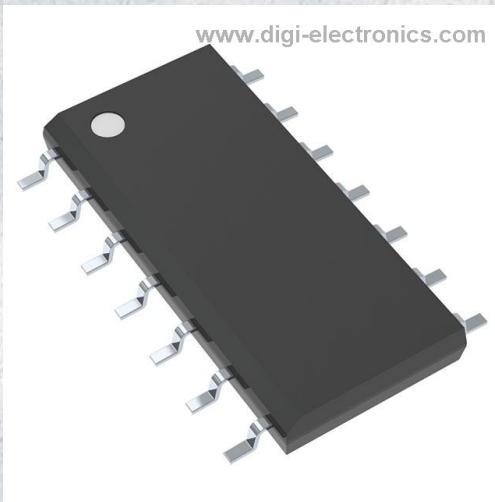


74AC10SCX Datasheet



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	74AC10SCX-DG
Manufacturer	onsemi
Manufacturer Product Number	74AC10SCX
Description	IC GATE NAND 3CH 3-INP 14SOIC
Detailed Description	NAND Gate IC 3 Channel 14-SOIC



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:

74AC10SCX

Series:

74AC

Logic Type:

NAND Gate

Number of Inputs:

3

Voltage - Supply:

2V ~ 6V

Current - Output High, Low:

24mA, 24mA

Input Logic Level - High:

2.1V ~ 3.85V

Operating Temperature:

-40°C ~ 85°C

Supplier Device Package:

14-SOIC

Base Product Number:

74AC10

Manufacturer:

onsemi

Product Status:

Obsolete

Number of Circuits:

3

Features:

-

Current - Quiescent (Max):

2 μ A

Input Logic Level - Low:

0.9V ~ 1.65V

Max Propagation Delay @ V, Max CL:

7ns @ 5V, 50pF

Mounting Type:

Surface Mount

Package / Case:

14-SOIC (0.154", 3.90mm Width)

Environmental & Export classification

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001



January 2008

74AC10, 74ACT10 Triple 3-Input NAND Gate

Features

- I_{CC} reduced by 50% on 74AC only
- Outputs source/sink 24mA


General Description

The AC/ACT10 contains three, 3-input NAND gates.

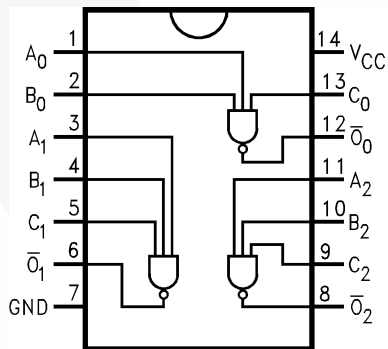
Ordering Information

Order Number	Package Number	Package Description
74AC10SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC10SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC10MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC10PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT10SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT10MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

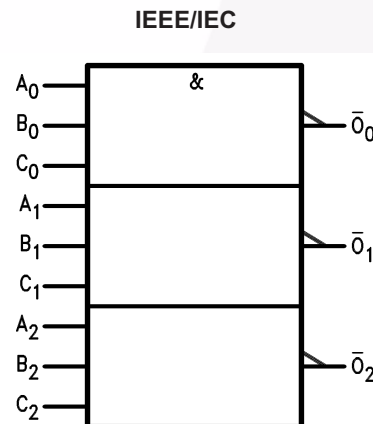
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
A_n, B_n, C_n	Inputs
\bar{O}_n	Outputs

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
V_I	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
V_O	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	$\pm 50mA$
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	$\pm 50mA$
T_{STG}	Storage Temperature	-65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage AC ACT	2.0V to 6.0V 4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C	T _A = -40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V _{IH}	Minimum HIGH Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V _{IL}	Maximum LOW Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V _{OH}	Minimum HIGH Level Output Voltage	3.0	I _{OUT} = -50μA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -12mA		2.56	2.46	
		4.5			3.86	3.76	
		5.5			4.86	4.76	
V _{OL}	Maximum LOW Level Output Voltage	3.0	I _{OUT} = 50μA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA		0.36	0.44	
		4.5			0.36	0.44	
		5.5			0.36	0.44	
I _{IN} ⁽³⁾	Maximum Input Leakage Current	5.5	V _I = V _{CC} or GND		±0.1	±1.0	μA
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	V _{OLD} = 1.65V Max.			75	mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-75	mA
I _{CC} ⁽³⁾	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		2.0	20.0	μA

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.
- I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = -50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA		3.86	3.76		
		5.5		V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ⁽⁴⁾		4.86	4.76	
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA		0.36	0.44		
		5.5		V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽⁴⁾		0.36	0.44	
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V	0.6		1.5		mA
I _{OLD}	Minimum Dynamic Output Current ⁽⁵⁾	5.5	V _{OLD} = 1.65V Max.			75		mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-75		mA
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) ⁽⁶⁾	T _A = +25°C, C _L = 50pF			T _A = -40°C to +85°C, C _L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay	3.3	1.5	6.0	9.5	1.0	10.5	ns
		5.0	1.5	4.5	7.0	1.0	8.0	
t _{PHL}	Propagation Delay	3.3	1.5	5.5	8.5	1.0	10.0	ns
		5.0	1.5	4.0	6.0	1.0	6.5	

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) ⁽⁷⁾	T _A = +25°C, C _L = 50pF			T _A = -40°C to +85°C, C _L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t _{PHL}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	9.5	ns

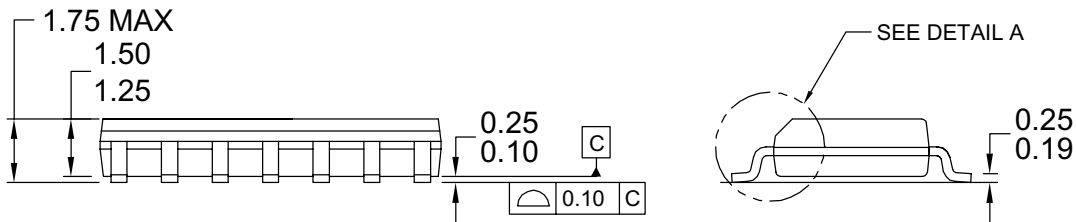
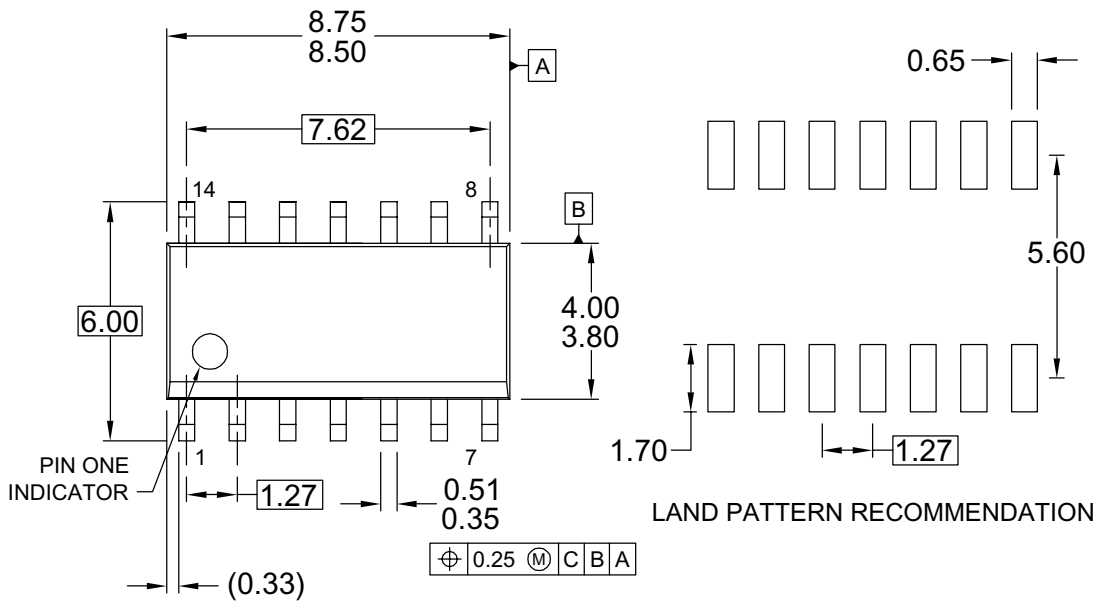
Note:

7. Voltage Range 5.0 is 5.0V ± 0.5V.

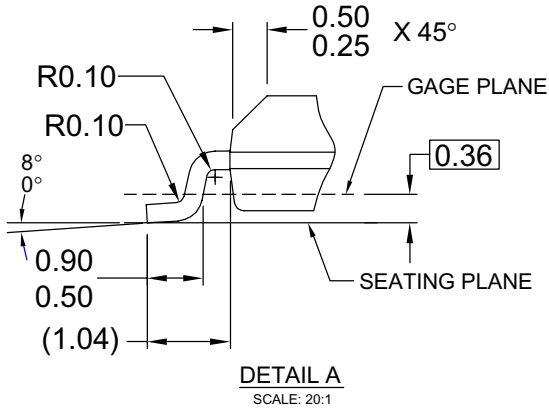
Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C _{IN}	Input Capacitance	V _{CC} = OPEN	4.5	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 5.0V	25.0	pF

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

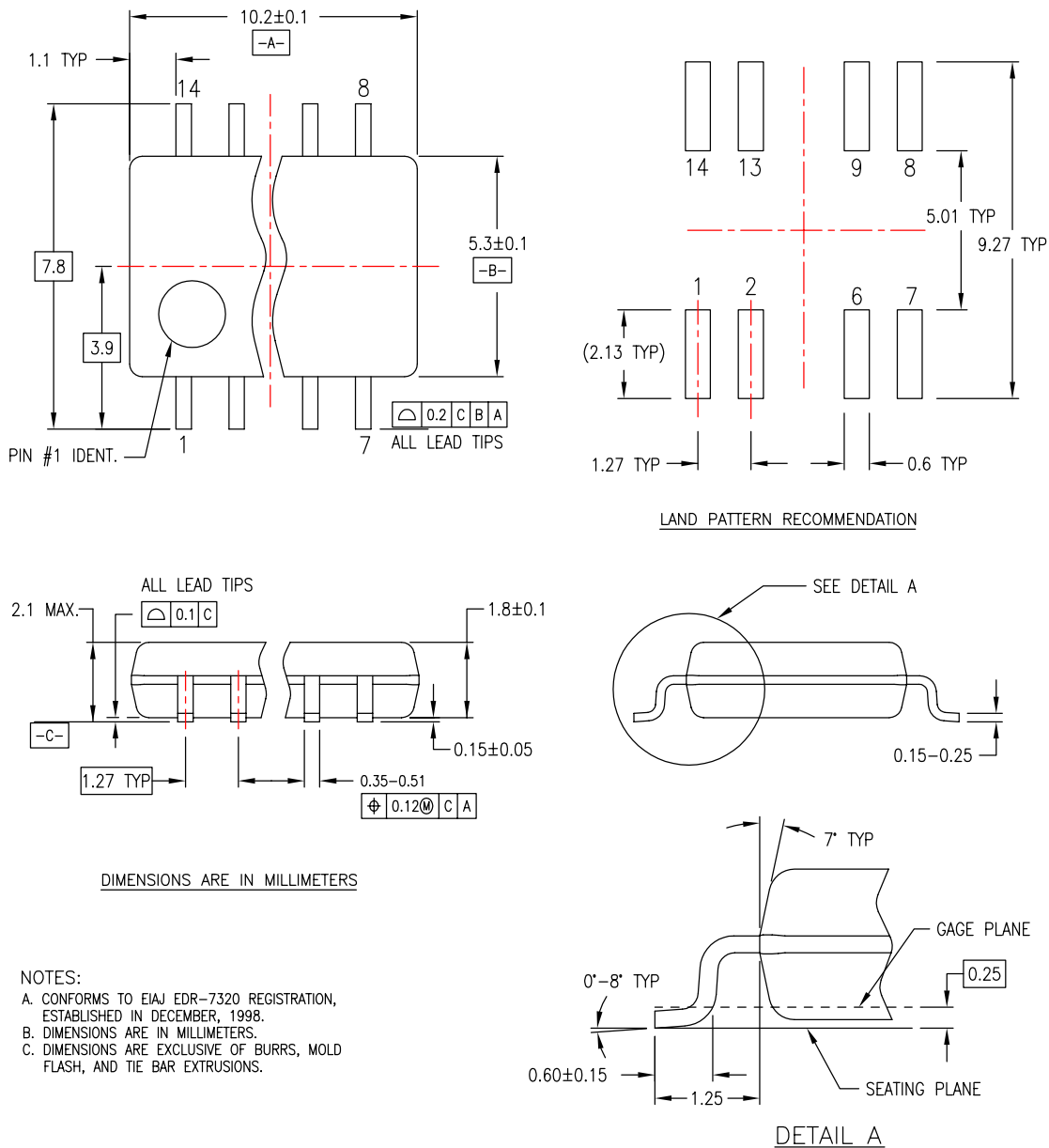
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Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



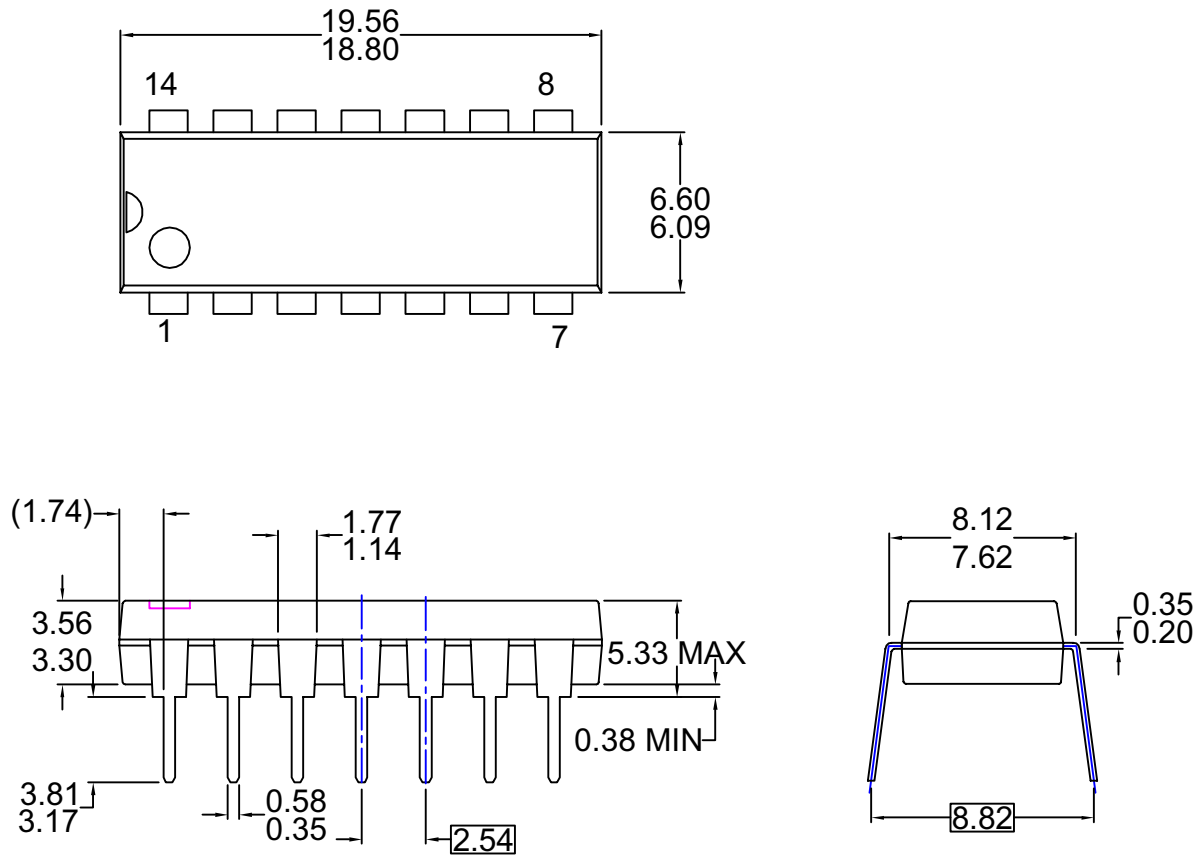
M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)

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 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
 MOLD FLASH, AND TIE BAR EXTRUSIONS.
 D) DIMENSIONS AND TOLERANCES PER
 ASME Y14.5-1994
 E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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

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