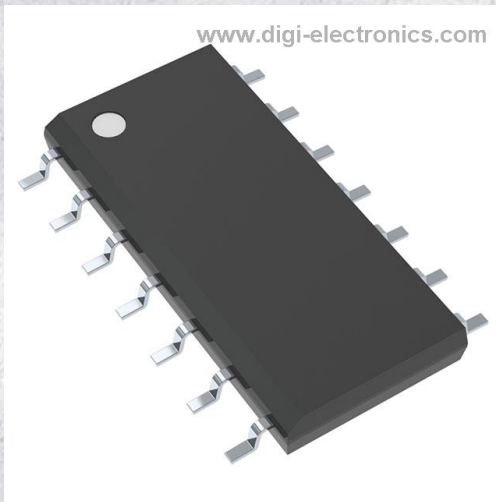


# 74AC74SCX Datasheet



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	74AC74SCX-DG
Manufacturer	<a href="#">onsemi</a>
Manufacturer Product Number	74AC74SCX
Description	IC FF D-TYPE DUAL 1BIT 14SOIC
Detailed Description	Flip Flop 2 Element D-Type 1 Bit Positive Edge 14-SOIC (0.154", 3.90mm Width)



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.

## Purchase and inquiry

Manufacturer Product Number:

74AC74SCX

Series:

74AC

Function:

Set(Preset) and Reset

Output Type:

Complementary

Number of Bits per Element:

1

Max Propagation Delay @ V, Max CL:

10ns @ 5V, 50pF

Current - Output High, Low:

24mA, 24mA

Current - Quiescent (Iq):

20  $\mu$ A

Operating Temperature:

-40°C ~ 85°C (TA)

Supplier Device Package:

14-SOIC

Base Product Number:

74AC74

Manufacturer:

onsemi

Product Status:

Obsolete

Type:

D-Type

Number of Elements:

2

Clock Frequency:

160 MHz

Trigger Type:

Positive Edge

Voltage - Supply:

2V ~ 6V

Input Capacitance:

4.5 pF

Mounting Type:

Surface Mount

Package / Case:

14-SOIC (0.154", 3.90mm Width)

## Environmental & Export classification

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001



January 2008

## 74AC74, 74ACT74

### Dual D-Type Positive Edge-Triggered Flip-Flop

#### Features

- $I_{CC}$  reduced by 50%
- Output source/sink 24mA
- ACT74 has TTL-compatible inputs

#### General Description

The AC/ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  (Set) sets Q to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

#### Ordering Information

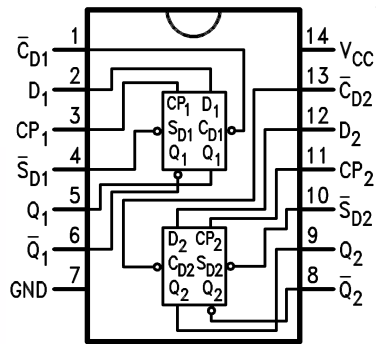
Order Number	Package Number	Package Description
74AC74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

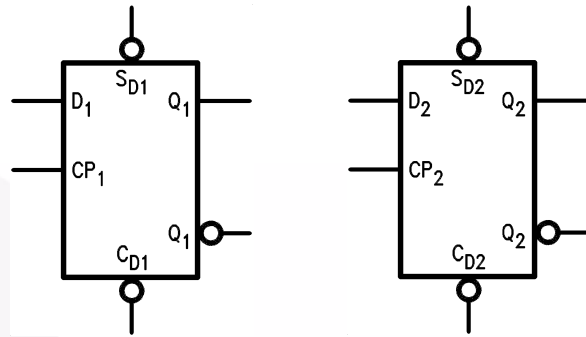


All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagram

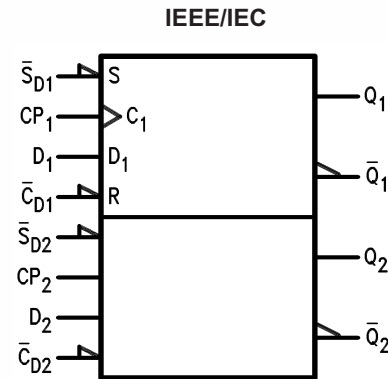


## Logic Symbols



## Pin Descriptions

Pin Names	Description
D <sub>1</sub> , D <sub>2</sub>	Data Inputs
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs
$\bar{C}_{D1}$ , $\bar{C}_{D2}$	Direct Clear Inputs
$\bar{S}_{D1}$ , $\bar{S}_{D2}$	Direct Set Inputs
Q <sub>1</sub> , $\bar{Q}_1$ , Q <sub>2</sub> , $\bar{Q}_2$	Outputs



## Truth Table

(Each Half)

Inputs				Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

H = HIGH Voltage Level

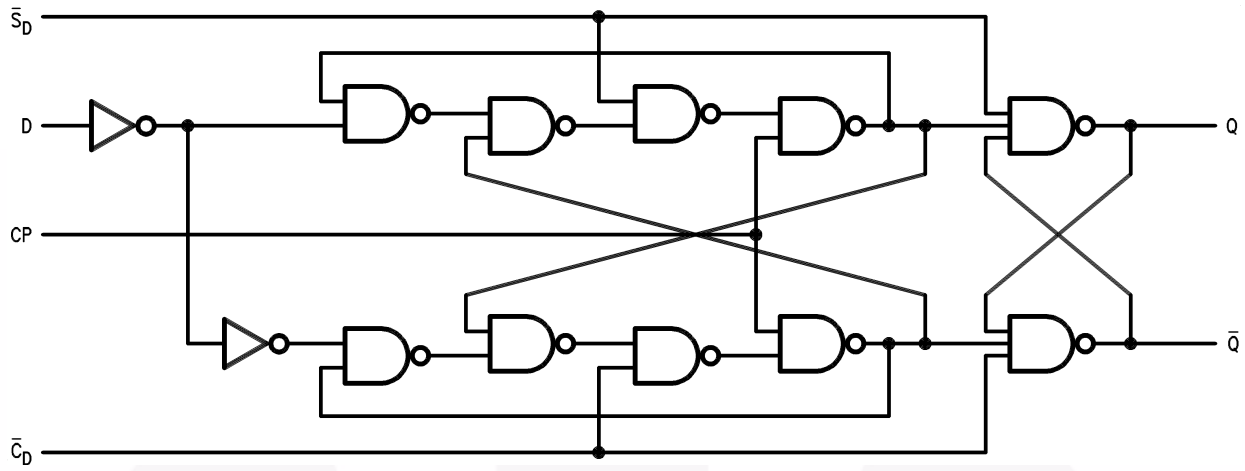
L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

Q<sub>0</sub> ( $\bar{Q}_0$ ) = Previous Q ( $\bar{Q}$ ) before LOW-to-HIGH Transition of Clock

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$	-20mA
	$V_I = V_{CC} + 0.5$	+20mA
$V_I$	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$	-20mA
	$V_O = V_{CC} + 0.5V$	+20mA
$V_O$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	$\pm 50mA$
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: $V_{IN}$ from 30% to 70% of $V_{CC}$ , $V_{CC}$ @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.1	2.1		V	
		4.5		2.25	3.15	3.15			
		5.5		2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.9	0.9		V	
		4.5		2.25	1.35	1.35			
		5.5		2.75	1.65	1.65			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	3.0	I <sub>OUT</sub> = -50μA	2.99	2.9	2.9		V	
		4.5		4.49	4.4	4.4			
		5.5		5.49	5.4	5.4			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -12mA		2.56	2.46			
		4.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>(1)</sup>		4.86		4.76
V <sub>OL</sub>	Maximum LOW Level Output Voltage	3.0	I <sub>OUT</sub> = 50μA	0.002		0.1	0.1		V
		4.5		0.001	0.1	0.1			
		5.5		0.001	0.1	0.1			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 12mA		0.36	0.44			
		4.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>(1)</sup>		0.36	0.44	
I <sub>IN</sub> <sup>(3)</sup>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND			±0.1	±1.0		μA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(2)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA	
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			-75		mA	
I <sub>CC</sub> <sup>(3)</sup>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.0	20.0		μA	

## Notes:

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.
- I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	I <sub>OUT</sub> = -50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>(4)</sup>		4.86	4.76	
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	I <sub>OUT</sub> = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>(4)</sup>		0.36	0.44	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	0.6		1.5		mA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(5)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA
		5.5	V <sub>OHD</sub> = 3.85V Min.			-75		mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.0	20.0		μA

**Notes:**

4. All outputs loaded; thresholds on input associated with output under test.



## AC Electrical Characteristics for AC

Symbol	Parameter	$V_{CC}$ (V) <sup>(6)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
$f_{MAX}$	Maximum Clock Frequency	3.3	100	125		95		MHz
		5.0	140	160		125		
$t_{PLH}$	Propagation Delay, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$	3.3	3.5	8.0	12.0	2.5	13.0	ns
		5.0	2.5	6.0	9.0	2.0	10.0	
$t_{PHL}$	Propagation Delay, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$	3.3	4.0	10.5	12.0	3.5	13.5	ns
		5.0	3.0	8.0	9.5	2.5	10.5	
$t_{PLH}$	Propagation Delay, $CP_n$ to $Q_n$ or $\overline{Q}_n$	3.3	4.5	8.0	13.5	4.0	16.0	ns
		5.0	3.5	6.0	10.0	3.0	10.5	
$t_{PHL}$	Propagation Delay, $CP_n$ to $Q_n$ or $\overline{Q}_n$	3.3	3.5	8.0	14.0	3.5	14.5	ns
		5.0	2.5	6.0	10.0	2.5	10.5	

## Note:

5. Voltage range 3.3 is  $3.3\text{V} \pm 0.3\text{V}$ . Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

## AC Operating Requirements for AC

Symbol	Parameter	$V_{CC}$ (V) <sup>(7)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Typ.	Guaranteed Minimum			
$t_S$	Set-up Time, HIGH or LOW, $D_n$ to $CP_n$	3.3	1.5	4.0	4.5		ns
		5.0	1.0	3.0	3.0		
$t_H$	Hold Time, HIGH or LOW, $D_n$ to $CP_n$	3.3	-2.0	0.5	0.5		ns
		5.0	-1.5	0.5	0.5		
$t_W$	$CP_n$ or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3	3.0	5.5	7.0		ns
		5.0	2.5	4.5	5.0		
$t_{rec}$	Recovery Time, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3	-2.5	0	0		ns
		5.0	-2.0	0	0		

## Note:

6. Voltage range 3.3 is  $3.3\text{V} \pm 0.3\text{V}$ . Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

**AC Electrical Characteristics for ACT**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(8)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF			T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f <sub>MAX</sub>	Maximum Clock Frequency	5.0	145	210		125		MHz
t <sub>PLH</sub>	Propagation Delay, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	5.0	3.0	5.5	9.5	2.5	10.5	ns
t <sub>PHL</sub>	Propagation Delay, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	5.0	3.0	6.0	10.0	3.0	11.5	ns
t <sub>PLH</sub>	Propagation Delay, CP <sub>n</sub> to Q <sub>n</sub> or $\overline{Q}_n$	5.0	4.0	7.5	11.0	4.0	13.0	ns
t <sub>PHL</sub>	Propagation Delay, CP <sub>n</sub> to Q <sub>n</sub> or $\overline{Q}_n$	5.0	3.5	6.0	10.0	3.0	11.5	ns

**Note:**

7. Voltage range 5.0 is 5.0V ± 0.5V.

**AC Operating Requirements for ACT**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(9)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF		T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Typ.	Guaranteed Minimum			
t <sub>S</sub>	Set-up Time, HIGH or LOW, D <sub>n</sub> to CP <sub>n</sub>	5.0	1.0	3.0	3.5		ns
t <sub>H</sub>	Hold Time, HIGH or LOW, D <sub>n</sub> to CP <sub>n</sub>	5.0	-0.5	1.0	1.0		ns
t <sub>W</sub>	CP <sub>n</sub> or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	6.0		ns
t <sub>rec</sub>	Recovery Time, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	-2.5	0	0		ns

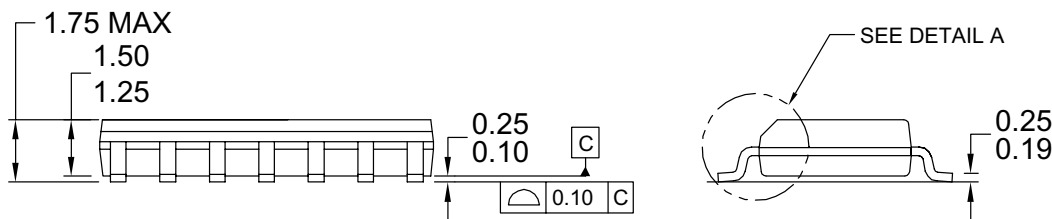
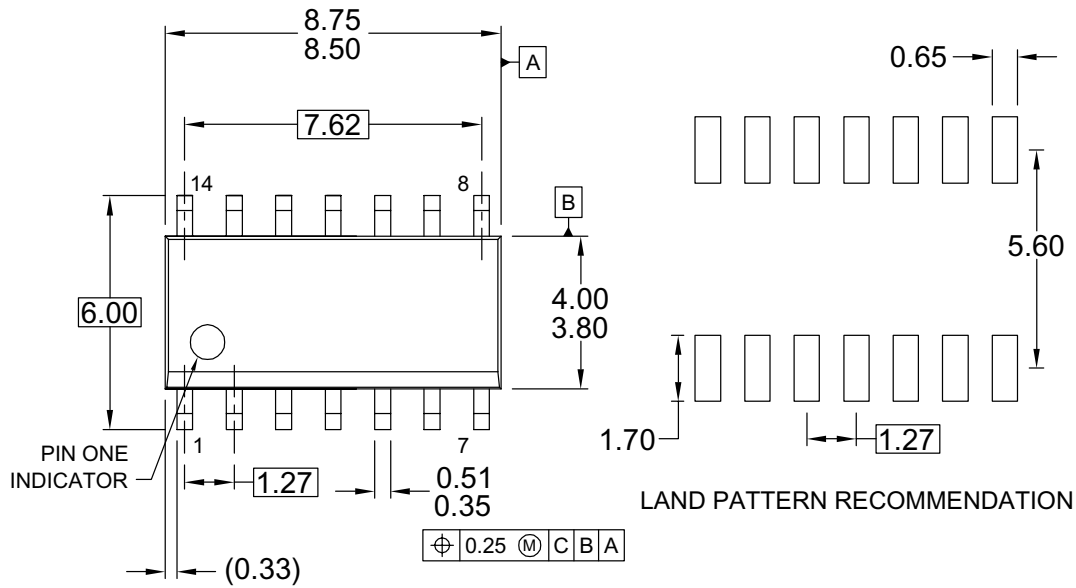
**Note:**

8. Voltage range 5.0 is 5.0V ± 0.5V.

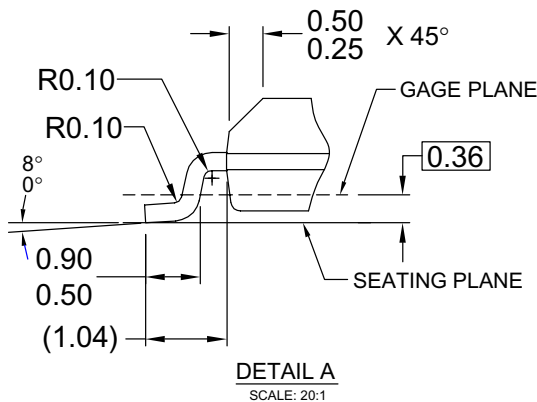
**Capacitance**

Symbol	Parameter	Conditions	Typ.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = OPEN	4.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 5.0V	35.0	pF

**Physical Dimensions**



NOTES: UNLESS OTHERWISE SPECIFIED



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

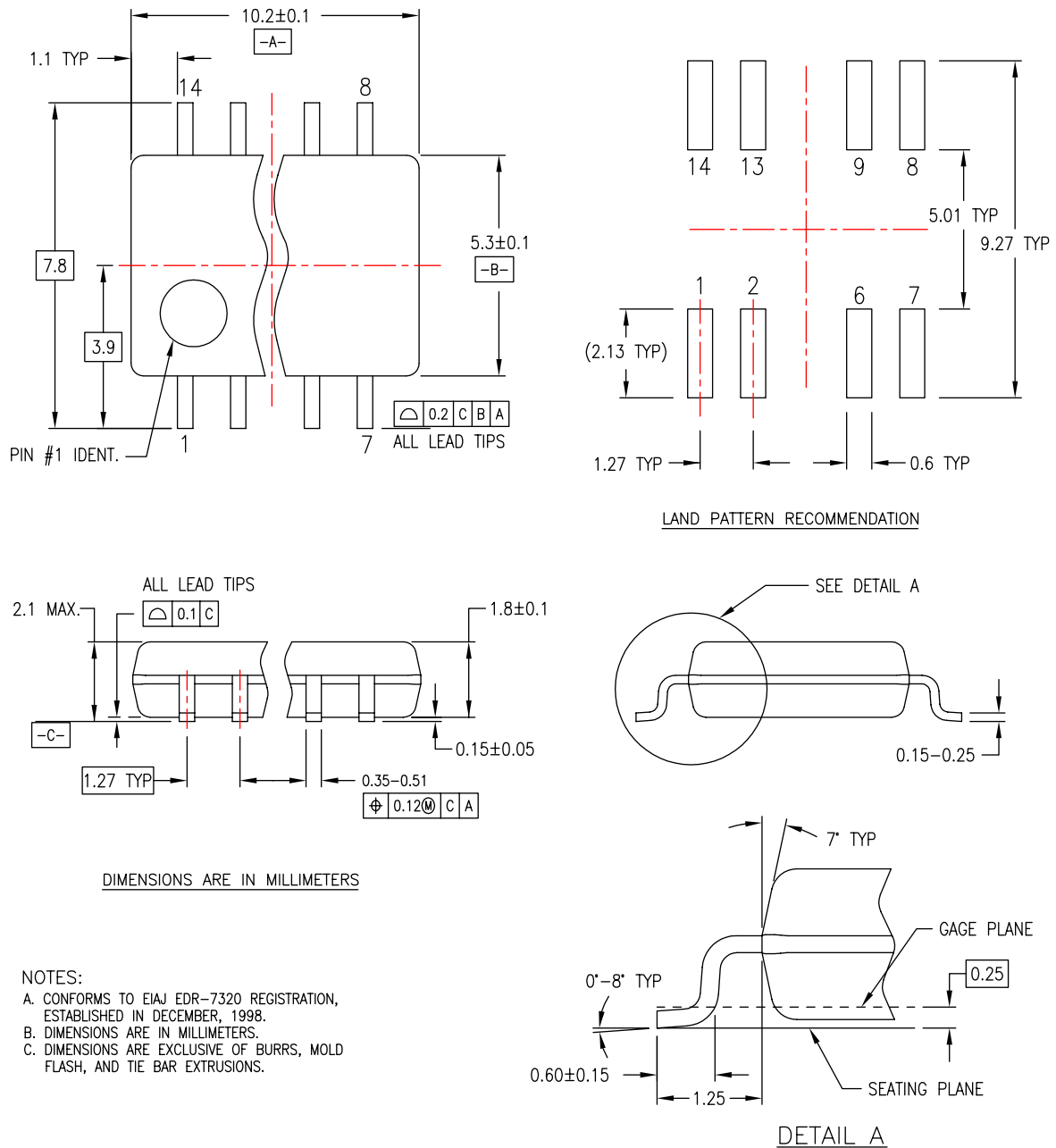
**Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

## Physical Dimensions (Continued)



M14DREVC

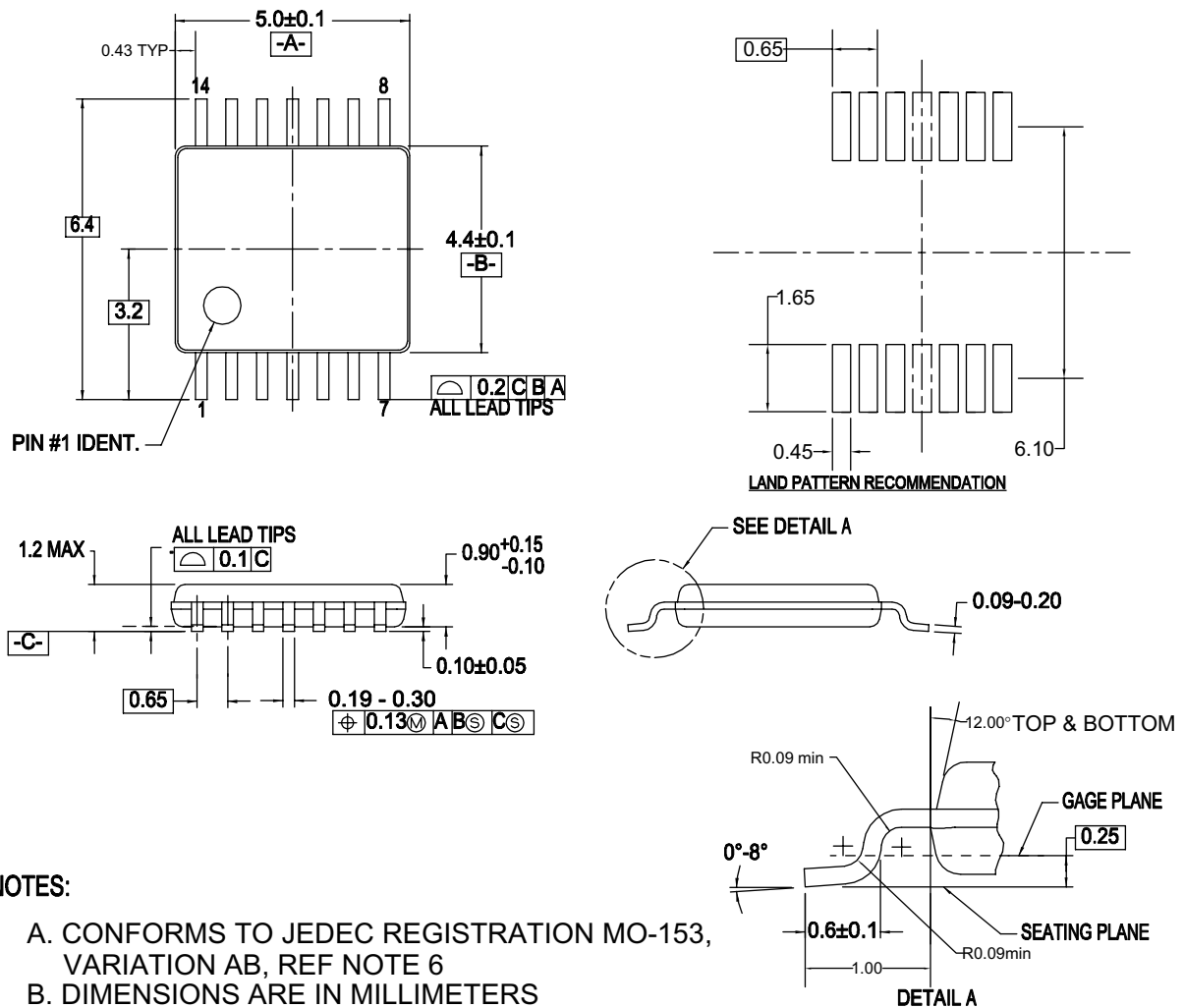
Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

## Physical Dimensions (Continued)



## NOTES:

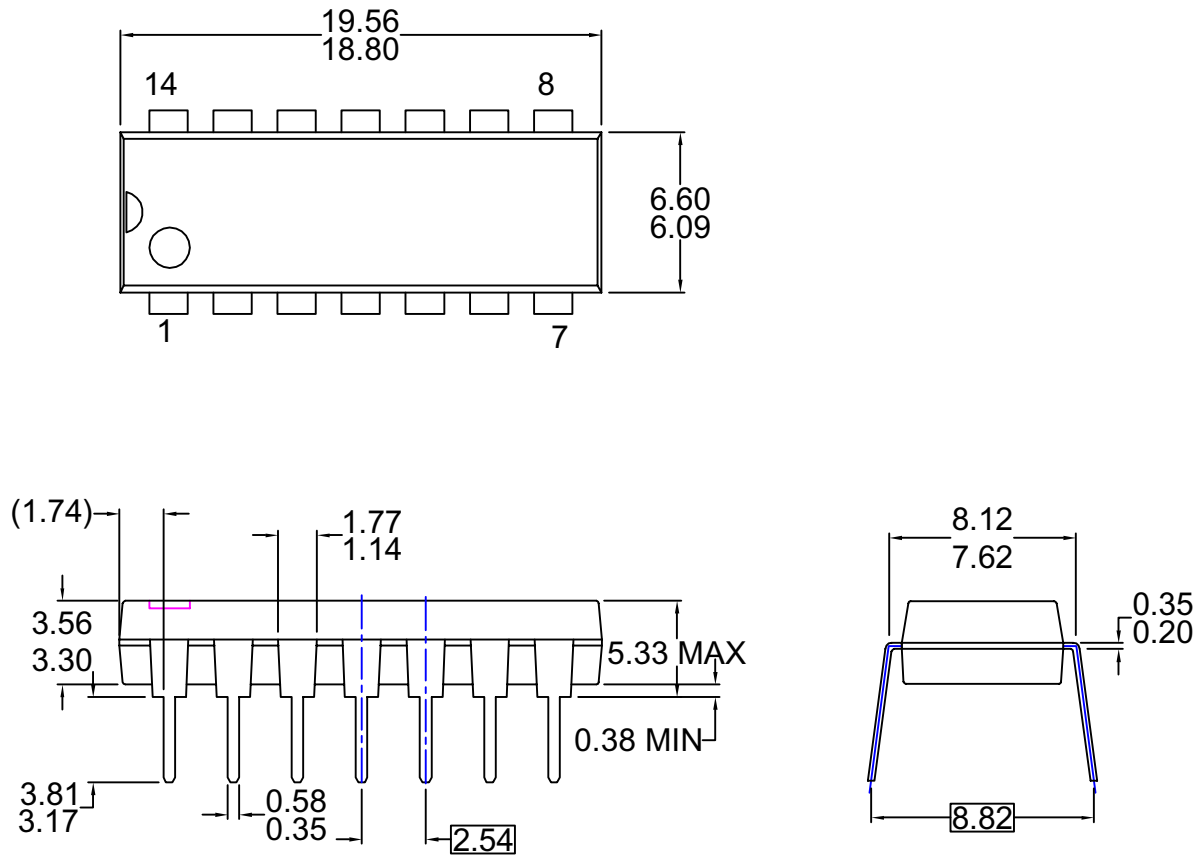
- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- LANDPATTERN STANDARD: SOP65P640X110-14M
- DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

**Physical Dimensions** (Continued)

- NOTES: UNLESS OTHERWISE SPECIFIED**
- THIS PACKAGE CONFORMS TO**
- A) JEDEC MS-001 VARIATION BA
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D) DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994
  - E) DRAWING FILE NAME: MKT-N14AREV7

**Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.



Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx <sup>®</sup>	FPST <sup>™</sup>	PDP-SPM <sup>™</sup>	SyncFET <sup>™</sup>
Build it Now <sup>™</sup>	FRFET <sup>®</sup>	Power220 <sup>®</sup>	SYSTEM <sup>®</sup>
CorePLUS <sup>™</sup>	Global Power Resource <sup>SM</sup>	Power247 <sup>®</sup>	GENERAL <sup>®</sup>
CROSSVOLT <sup>™</sup>	Green FPS <sup>™</sup>	POWEREDGE <sup>®</sup>	The Power Franchise <sup>®</sup>
CTL <sup>™</sup>	Green FPS <sup>™</sup> e-Series <sup>™</sup>	Power-SPM <sup>™</sup>	the power <sup>™</sup>
Current Transfer Logic <sup>™</sup>	GTO <sup>™</sup>	PowerTrench <sup>®</sup>	franchise
EcoSPARK <sup>®</sup>	<i>i-Lo</i> <sup>™</sup>	Programmable Active Droop <sup>™</sup>	TinyBoost <sup>™</sup>
EZSWITCH <sup>™</sup> *	IntelliMAX <sup>™</sup>	QFET <sup>®</sup>	TinyBuck <sup>™</sup>
 ™	ISOPLANAR <sup>™</sup>	QST <sup>™</sup>	TinyLogic <sup>®</sup>
 ™	MegaBuck <sup>™</sup>	QT Optoelectronics <sup>™</sup>	TINYOPTO <sup>™</sup>
Fairchild <sup>®</sup>	MICROCOUPLER <sup>™</sup>	Quiet Series <sup>™</sup>	TinyPower <sup>™</sup>
Fairchild Semiconductor <sup>®</sup>	MicroFET <sup>™</sup>	RapidConfigure <sup>™</sup>	TinyPWM <sup>™</sup>
FACT Quiet Series <sup>™</sup>	MicroPak <sup>™</sup>	SMART START <sup>™</sup>	TinyWire <sup>™</sup>
FACT <sup>®</sup>	MillerDrive <sup>™</sup>	SPM <sup>®</sup>	μSerDes <sup>™</sup>
FAST <sup>®</sup>	Motion-SPM <sup>™</sup>	STEALTH <sup>™</sup>	UHC <sup>®</sup>
FastvCore <sup>™</sup> *	OPTOLOGIC <sup>®</sup>	SuperFET <sup>™</sup>	Ultra FRFET <sup>™</sup>
FlashWriter <sup>®</sup> *	OPTOPLANAR <sup>®</sup>	SuperSOT <sup>™</sup> -3	UniFET <sup>™</sup>
		SuperSOT <sup>™</sup> -6	VCX <sup>™</sup>
		SuperSOT <sup>™</sup> -8	

\* EZSWITCH<sup>™</sup> and FlashWriter<sup>®</sup> are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I32

## OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we strictly control the quality of products and services. Welcome your RFQ to

Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.