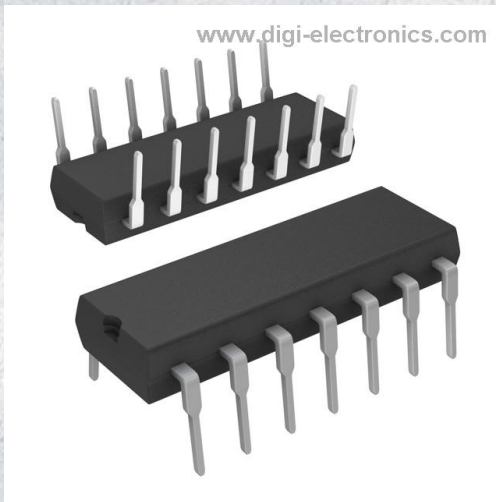


74ACT10PC Datasheet



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	74ACT10PC-DG
Manufacturer	onsemi
Manufacturer Product Number	74ACT10PC
Description	IC GATE NAND 3CH 3-INP 14MDIP
Detailed Description	NAND Gate IC 3 Channel 14-MDIP



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

74ACT10PC

Series:

74ACT

Logic Type:

NAND Gate

Number of Inputs:

3

Voltage - Supply:

4.5V ~ 5.5V

Current - Output High, Low:

24mA, 24mA

Input Logic Level - High:

2V

Operating Temperature:

-40°C ~ 85°C

Supplier Device Package:

14-MDIP

Base Product Number:

74ACT10

Manufacturer:

onsemi

Product Status:

Obsolete

Number of Circuits:

3

Features:

-

Current - Quiescent (Max):

4 μ A

Input Logic Level - Low:

0.8V

Max Propagation Delay @ V, Max CL:

9ns @ 5V, 50pF

Mounting Type:

Through Hole

Package / Case:

14-DIP (0.300", 7.62mm)

Environmental & Export classification

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001



November 1988
Revised January 2000

74AC10 • 74ACT10 Triple 3-Input NAND Gate

General Description

The AC/ACT10 contains three, 3-input NAND gates.

Features

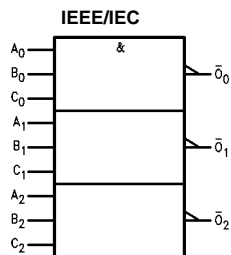
- I_{CC} reduced by 50% on 74AC only
- Outputs source/sink 24 mA

Ordering Code:

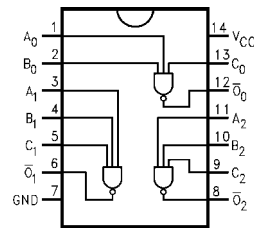
Order Number	Package Number	Package Description
74AC10SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74AC10SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC10MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC10PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT10SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74ACT10PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n, C_n	Inputs
\bar{O}_n	Outputs

74AC10 • 74ACT10 Triple 3-Input NAND Gate

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-out exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
			3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ (Note 2)
			4.5		3.86	3.76		
			5.5		4.86	4.76		
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
			3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ (Note 2)
			4.5		0.36	0.44		
			5.5		0.36	0.44		
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}$ or GND	
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max	
I_{OHD}	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min	
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

DC Electrical Characteristics for ACT								
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA	
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
		5.5	0.6		1.5			
I _{OLD}	Maximum Dynamic Output Current (Note 6)	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V _{IN} = V _{CC} or GND	

Note 5: All outputs loaded; thresholds on input associated with output under test.
Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) (Note 7)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5	6.0 4.5	9.5 7.0	1.0 1.0	10.5 8.0	ns
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	5.5 4.0	8.5 6.0	1.0 1.0	10.0 6.5	ns

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) (Note 8)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t _{PHL}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	9.5	ns

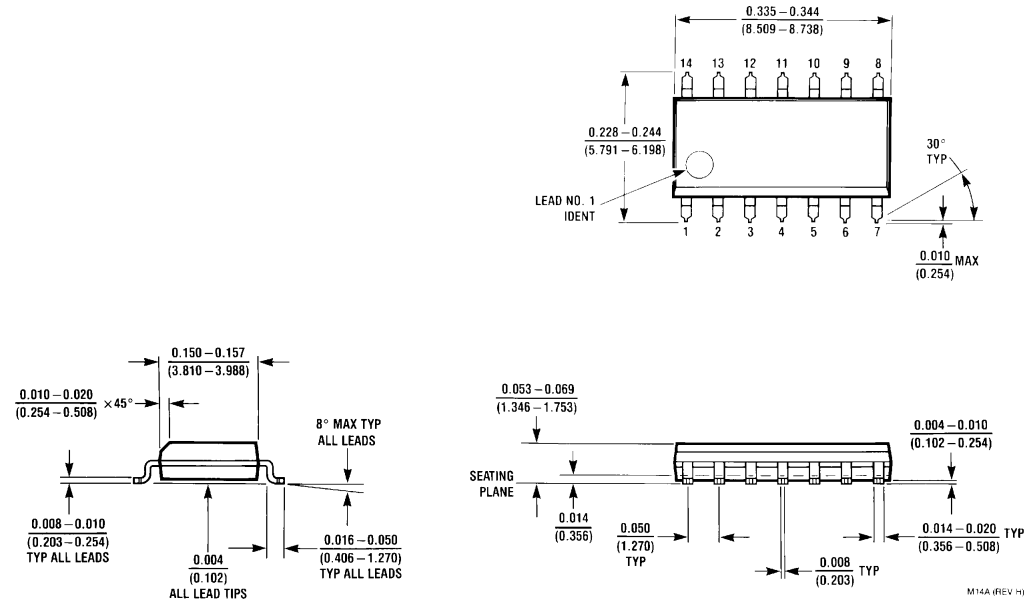
Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	25.0	pF	V _{CC} = 5.0V

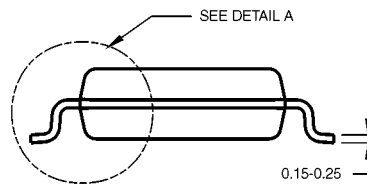
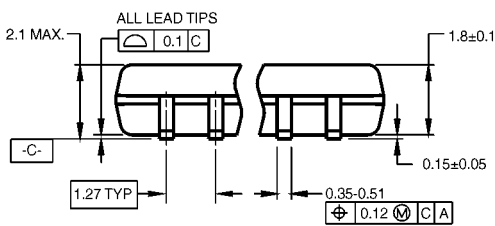
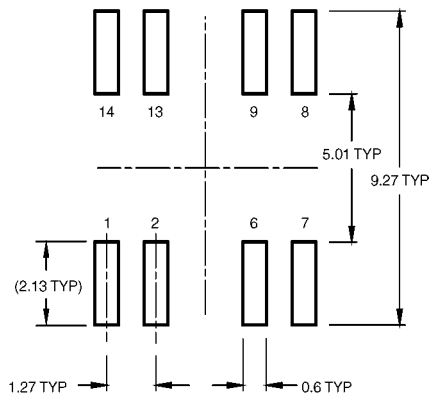
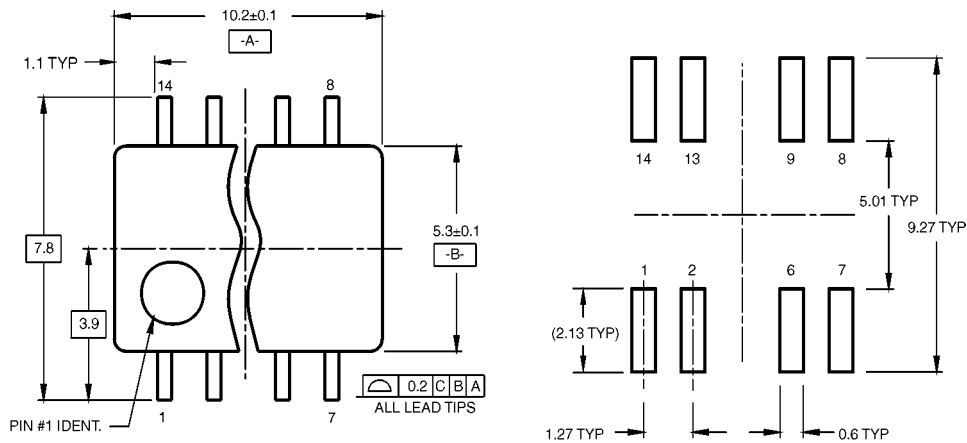
74ACT10 • 74ACT10

Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
Package Number M14A**

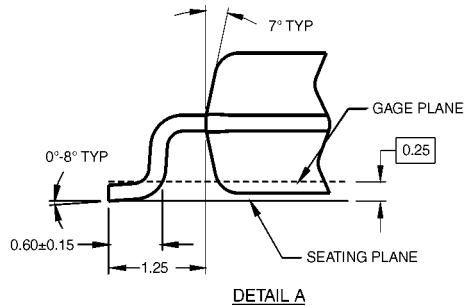
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

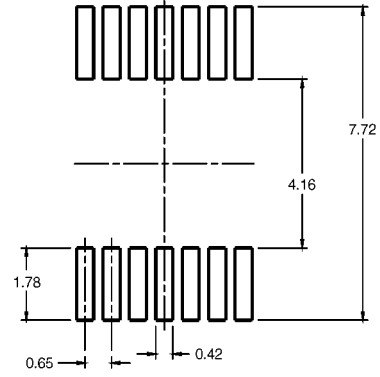
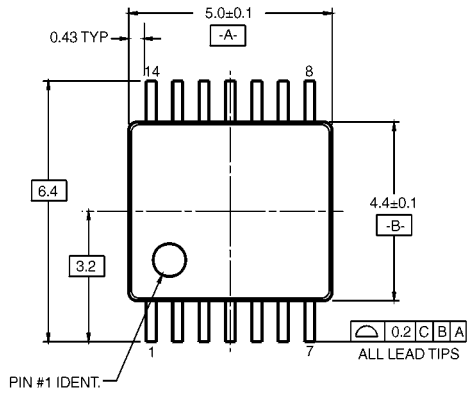
M14DRevB1



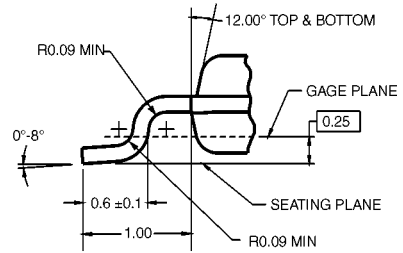
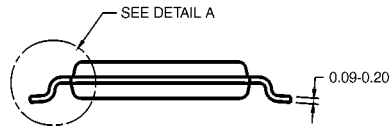
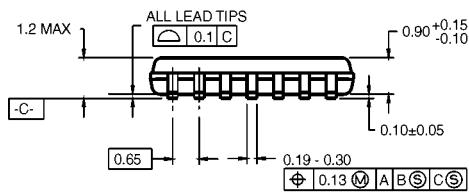
**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M14D**

74ACT10 • 74ACT10

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

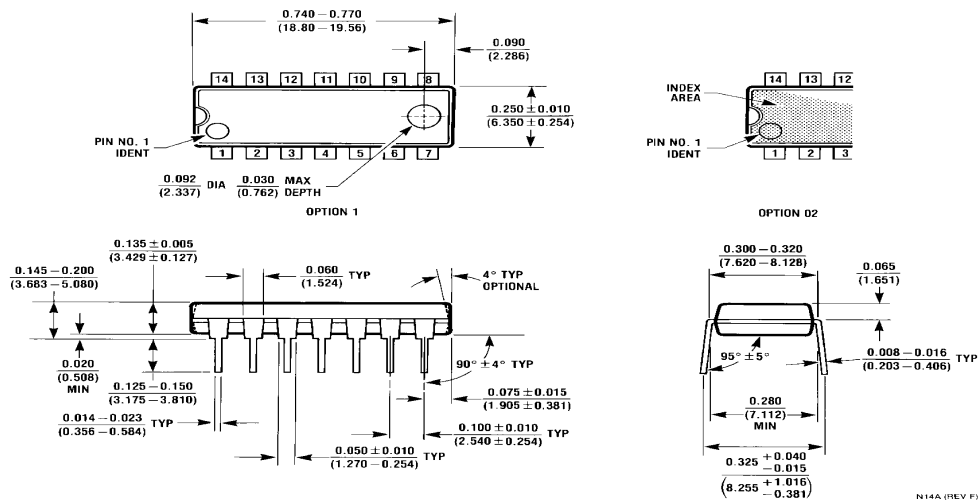


DETAIL A

- NOTES:
 A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
 Package Number MTC14**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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