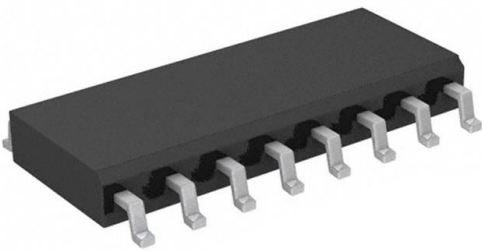


74ACT174SC Datasheet

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DiGi Electronics Part Number	74ACT174SC-DG
Manufacturer	onsemi
Manufacturer Product Number	74ACT174SC
Description	IC FF D-TYPE SNGL 6BIT 16SOIC
Detailed Description	Flip Flop 1 Element D-Type 6 Bit Positive Edge 16-SOIC (0.154", 3.90mm Width)

This model 74ACT174SC is available at DiGi Electronics.

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Purchase and inquiry

Manufacturer Product Number:

74ACT174SC

Series:

74ACT

Function:

Master Reset

Output Type:

Non-Inverted

Number of Bits per Element:

6

Max Propagation Delay @ V, Max CL:

10.5ns @ 5V, 50pF

Current - Output High, Low:

24mA, 24mA

Current - Quiescent (Iq):

40 μ A

Operating Temperature:

-40°C ~ 85°C (TA)

Supplier Device Package:

16-SOIC

Base Product Number:

74ACT174

Manufacturer:

onsemi

Product Status:

Obsolete

Type:

D-Type

Number of Elements:

1

Clock Frequency:

200 MHz

Trigger Type:

Positive Edge

Voltage - Supply:

4.5V ~ 5.5V

Input Capacitance:

4.5 pF

Mounting Type:

Surface Mount

Package / Case:

16-SOIC (0.154", 3.90mm Width)

Environmental & Export classification

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

FAIRCHILD
SEMICONDUCTOR™

November 1988
Revised October 2000

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Hex D-Type Flip-Flop with Master Reset

General Description

The AC/ACT174 is a high-speed hex D-type flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

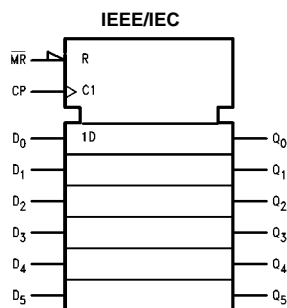
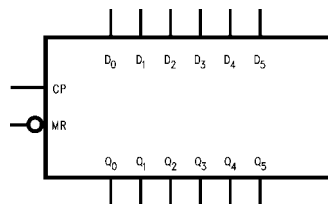
- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- ACT174 has TTL-compatible inputs

Ordering Code:

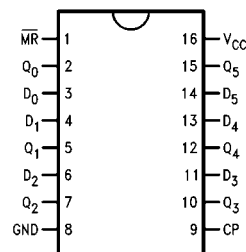
Order Number	Package Number	Package Description
74AC174SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74AC174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC174MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC174PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACT174SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74ACT174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT174MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT174PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ -D ₅	Data Inputs
CP	Clock Pulse Input
\overline{MR}	Master Reset Input
Q ₀ -Q ₅	Outputs

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Functional Description

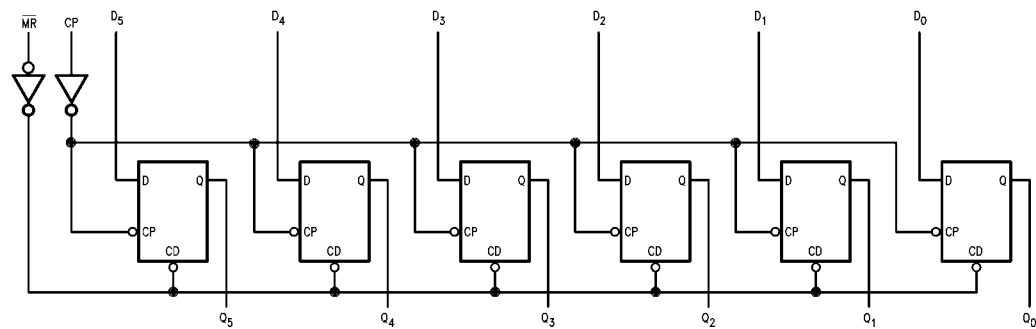
The AC/ACT174 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{\text{MR}}$) will force all outputs LOW independent of Clock or Data inputs. The AC/ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Output
$\overline{\text{MR}}$	CP	D	Q
L	X	X	L
H	↗	H	H
H	↗	L	L
H	L	X	Q

H = HIGH Voltage Level
 L = LOW Voltage Level
 ↗ = LOW-to-HIGH Transition
 X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions	
Supply Voltage (V_{CC})	-0.5V to +7.0V	Supply Voltage (V_{CC})	AC 2.0V to 6.0V
DC Input Diode Current (I_{IK})		ACT 4.5V to 5.5V	
$V_I = -0.5V$	-20 mA	Input Voltage (V_I)	0V to V_{CC}
$V_I = V_{CC} + 0.5V$	+20 mA	Output Voltage (V_O)	0V to V_{CC}
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$	Operating Temperature (T_A)	-40°C to +85°C
DC Output Diode Current (I_{OK})		Minimum Input Edge Rate ($\Delta V/\Delta t$)	
$V_O = -0.5V$	-20 mA	AC Devices	V_{IN} from 30% to 70% of V_{CC}
$V = V_{CC} + 0.5V$	+20 mA	V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate ($\Delta V/\Delta t$)	
DC Output Source		ACT Devices	V_{IN} from 0.8V to 2.0V
or Sink Current (I_O)	± 50 mA	V_{CC} @ 4.5V, 5.5V	125 mV/ns
DC V_{CC} or Ground Current			
per Output Pin (I_{CC} or I_{GND})	± 50 mA		
Storage Temperature (T_{STG})	-65°C to +150°C		
Junction Temperature (T_J)			
PDIP	140°C		

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2)
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2)
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}$ or GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

74ACT174 • 74ACT174

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA (Note 5)	
		5.5		4.86	4.76			
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 5)	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} - 2.1V	
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 6)	5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V _{IN} = V _{CC} or GND	

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

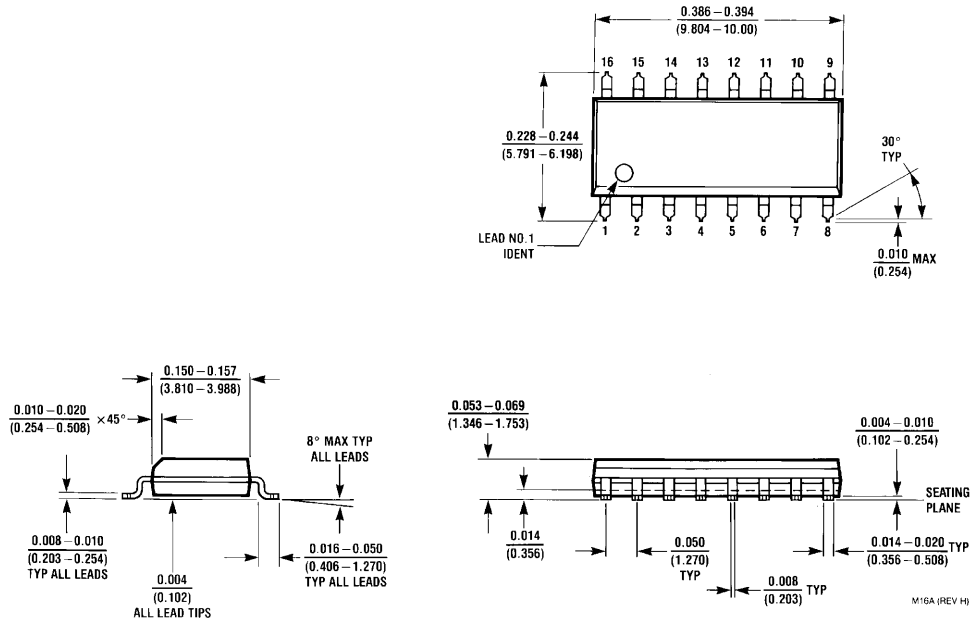
Symbol	Parameter	V _{CC} (V) (Note 7)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	3.3	90	100		70	MHz	
		5.0	100	125		100		
t _{PLH}	Propagation Delay CP to Q _n	3.3	2.0	9.0	11.5	1.5	12.5	ns
		5.0	1.5	6.0	8.5	1.0	9.5	
t _{PHL}	Propagation Delay CP to Q _n	3.3	2.0	8.5	11.0	1.5	12.0	ns
		5.0	1.5	6.0	8.0	1.0	9.0	
t _{PHL}	Propagation Delay MR to Q _n	3.3	2.5	9.0	11.5	2.0	12.5	ns
		5.0	1.5	7.0	9.0	1.5	10.5	

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for AC								
Symbol	Parameter	V _{CC} (V) (Note 8)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units	
			Typ	Guaranteed Minimum				
t _S	Setup Time, HIGH or LOW	3.3	2.5	6.5	7.0		ns	
	D _n to CP	5.0	2.0	5.0	5.5			
t _H	Hold Time, HIGH or LOW	3.3	1.0	3.0	3.0		ns	
	D _n to CP	5.0	0.5	3.0	3.0			
t _W	MR Pulse Width, LOW	3.3	1.0	5.5	7.0		ns	
		5.0	1.0	5.0	5.0			
t _W	CP Pulse Width	3.3	1.0	5.5	7.0		ns	
		5.0	1.0	5.0	5.0			
t _{REC}	Recovery Time	3.3	0	2.5	2.5		ns	
	MR to CP	5.0	0	2.0	2.0			
Note 8: Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V ± 0.5V								
AC Electrical Characteristics for ACT								
Symbol	Parameter	V _{CC} (V) (Note 9)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	5.0	165	200		140	MHz	
t _{PLH}	Propagation Delay CP to Q _n	5.0	1.5	7.0	10.5	1.5	11.5	ns
t _{PHL}	Propagation Delay CP to Q _n	5.0	1.5	7.0	10.5	1.5	11.5	ns
t _{PHL}	Propagation Delay MR to Q _n	5.0	1.5	6.5	9.5	1.5	11.0	ns
Note 9: Voltage Range 5.0 is 5.0V ± 0.5V								
AC Operating Requirements for ACT								
Symbol	Parameter	V _{CC} (V) (Note 10)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units	
			Typ	Guaranteed Minimum				
t _S	Setup Time, HIGH or LOW D _n to CP	5.0	0.5	1.5	1.5		ns	
t _H	Hold Time, HIGH or LOW D _n to CP	5.0	1.0	2.0	2.0		ns	
t _W	MR Pulse Width, LOW	5.0	1.5	3.0	3.5		ns	
t _W	CP Pulse Width, HIGH or LOW	5.0	1.5	3.0	3.5		ns	
t _{rec}	Recovery Time MR to CP	5.0	-1.0	0.5	0.5		ns	
Note 10: Voltage Range 5.0 is 5.0V ± 0.5V								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions				
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN				
C _{PD}	Power Dissipation Capacitance	85.0	pF	V _{CC} = 5.0V				

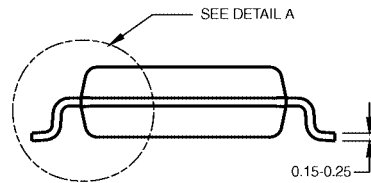
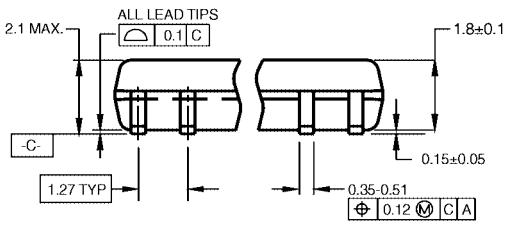
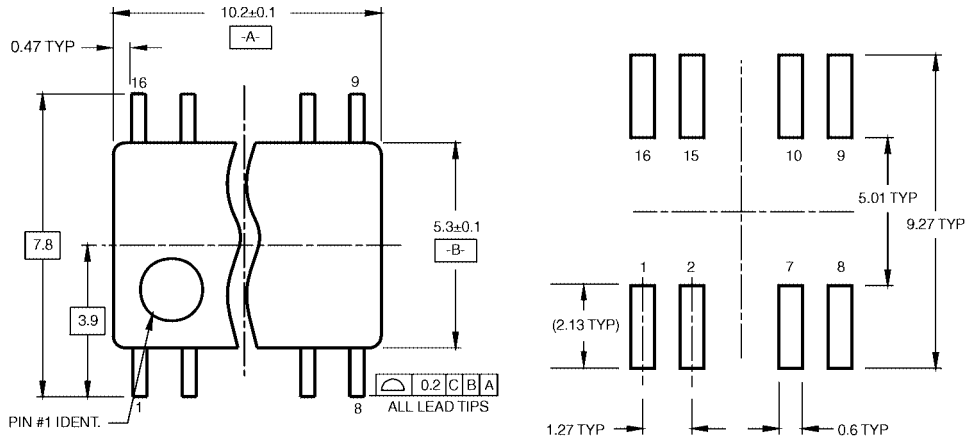
74ACT174 • 74ACT174

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A

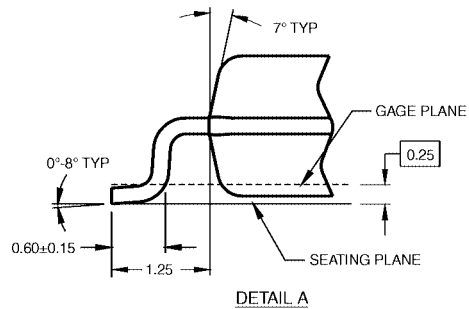
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

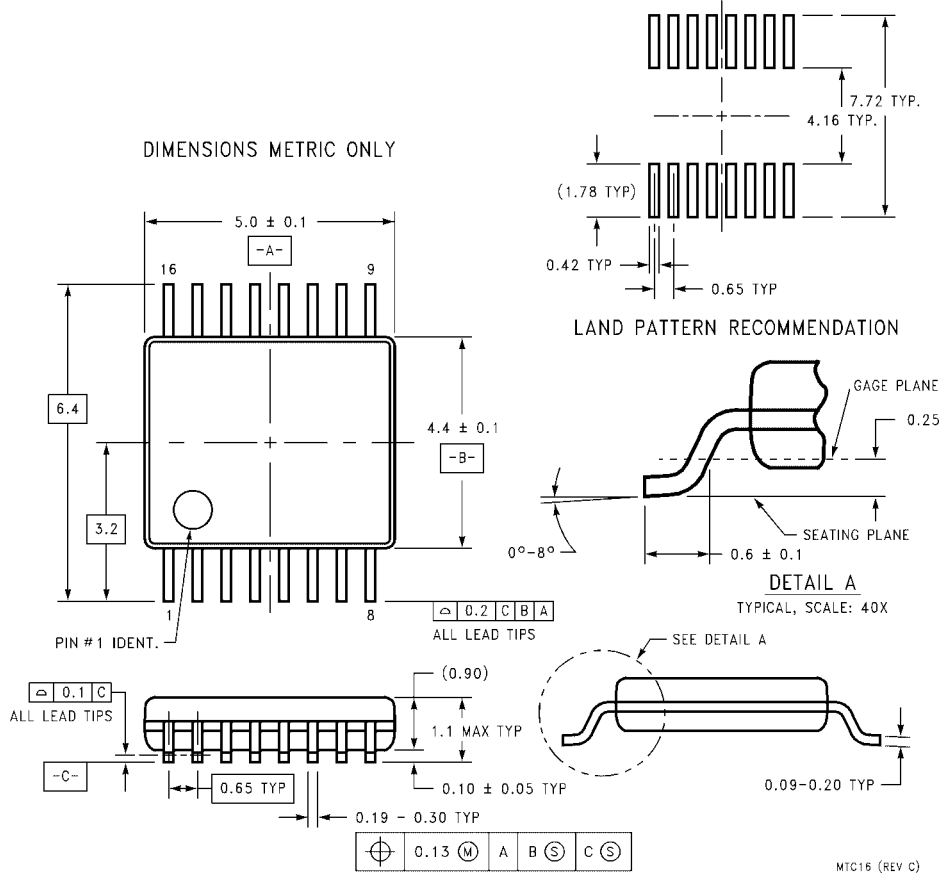
M16DRevB1



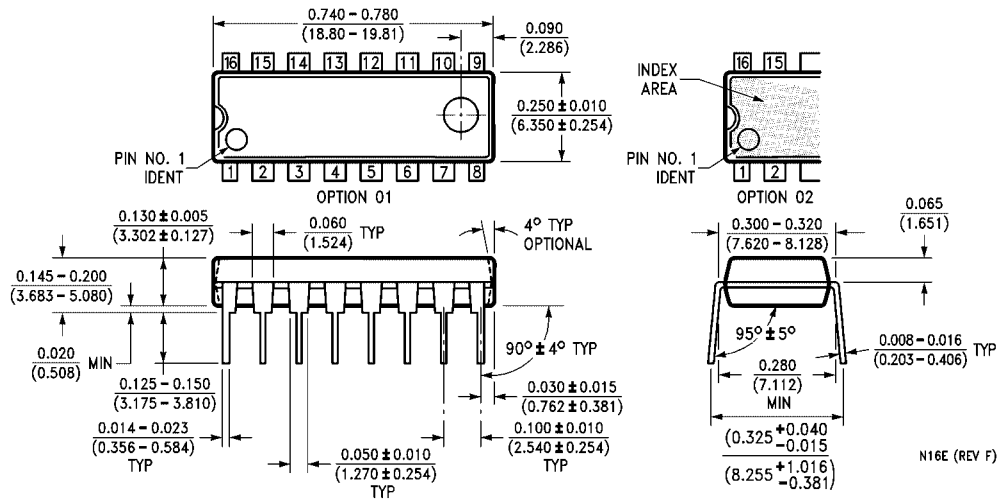
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M16D**

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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