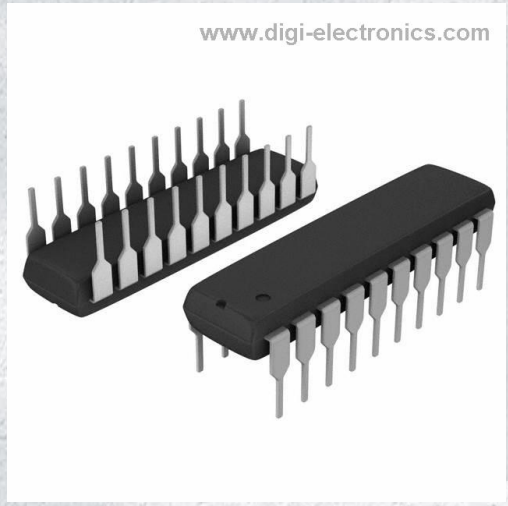
74ACT541PC Datasheet



DiGi Electronics Part Number	74ACT541PC-DG
Manufacturer	onsemi
Manufacturer Product Number	74ACT541PC
Description	IC BUFF NON-INVERT 5.5V 20DIP
Detailed Description	Buffer, Non-Inverting 1 Element 8 Bit per Element 3 -State Output 20-PDIP

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74ACT541PC	onsemi
Series:	Product Status:
74ACT	Obsolete
Logic Type:	Number of Elements:
Buffer, Non-Inverting	1
Number of Bits per Element:	Input Type:
8	-
Output Type:	Current - Output High, Low:
3-State	24mA, 24mA
Voltage - Supply:	Operating Temperature:
4.5V ~ 5.5V	-40°C ~ 85°C (TA)
Mounting Type:	Package / Case:
Through Hole	20-DIP (0.300", 7.62mm)
Supplier Device Package:	Base Product Number:
20-PDIP	74ACT541

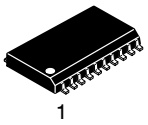
Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8542.39.0001

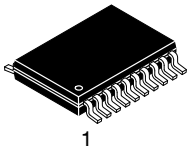
DATA SHEET
www.onsemi.com

Octal Buffer/Line Driver with 3-State Outputs

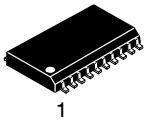
74AC541, 74ACT541



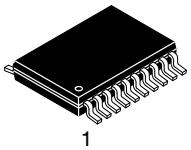
SOIC−20W
CASE 751D



TSSOP−20
CASE 948E



SOIC−20W
CASE 751BJ



TSSOP−20
CASE 948AQ

General Description

The 74AC541 and 74ACT541 are octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

These devices are similar in function to the 74AC244 and 74ACTC244 while providing flow−through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

Features

- I_{CC} and I_{OZ} Reduced by 50%
- 3−State Outputs
- Inputs and Outputs Opposite Side of Package, allowing easier Interface to Microprocessors
- Outputs Source/Sink 24 mA
- 74AC541 is a Non−inverting Option of the 74AC540
- 74ACT541 has TTL−compatible Inputs
- These are Pb−Free Devices

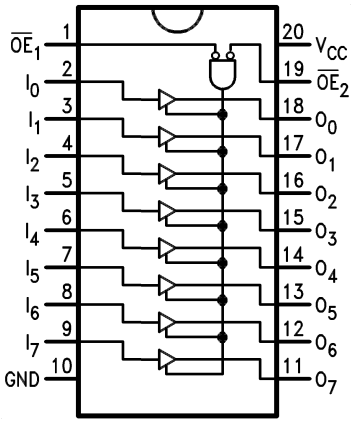


Figure 1. Connection Diagram

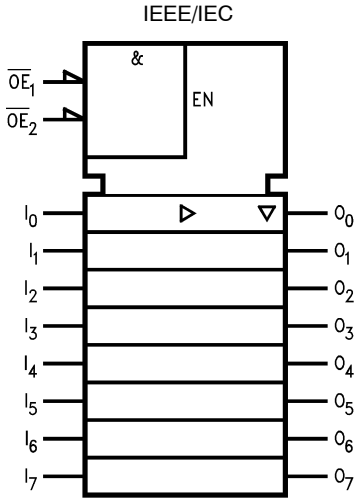


Figure 2. Logic Symbol

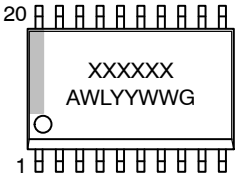
TRUTH TABLE

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

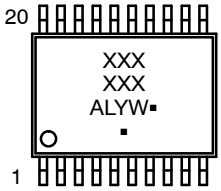
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

MARKING DIAGRAMS

SOIC−20W



TSSOP−20



XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	−0.5 to +6.5	V
I_{IK}	DC Input Diode Current V_I = −0.5 V V_I = V_{CC} + 0.5 V	 −20 +20	mA
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
I_{OK}	DC Output Diode Current V_O = −0.5 V V_O = V_{CC} + 0.5 V	 −20 +20	mA
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_O	DC Output Source or Sink Current	±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50	mA
T_{STG}	Storage Temperature	−65 to +150	°C
T_J	Junction Temperature	140	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage AC ACT	 2.0 4.5	 6.0 5.5	V
V_I	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	−40	85	°C
$\Delta V/\Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% V_{CC}, V_{CC} @ 3.3 V, 4.5 V, 5.5 V	125		mV/ns
$\Delta V/\Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8 V to 2.0 V, V_{CC} @ 4.5 V, 5.5 V	125		mV/ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS FOR AC

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = −40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	3.0	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	I_{OUT} = −50 μA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −12 mA		2.56	2.46	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24 mA		3.86	3.76	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24 mA (1)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	I_{OUT} = 50 μA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 12 mA		0.36	0.44	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24 mA		0.36	0.44	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24 mA (1)		0.36	0.44	
I_{IN} (Note 2)	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	μA
I_{OZ}	Maximum 3−STATE Leakage Current	5.5	V_I (OE) = V_{IL}, V_{IH}; V_I = V_{CC}, GND; V_O = V_{CC}, GND		±0.25	±2.5	μA
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5	V_{OLD} = 1.65 V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85 V Min.			−75	mA
I_{CC} (Note 2)	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	μA

1. All outputs loaded; thresholds on input associated with output under test.
2. I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.
3. Maximum test duration 2.0 ms, one output loaded at a time.

DC ELECTRICAL CHARACTERISTICS FOR ACT

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = −40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	I_{OUT} = −50 μA	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24 mA		3.86	3.76	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24 mA (4)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	I_{OUT} = 50 μA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24 mA		0.36	0.44	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24 mA (4)		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	μA
I_{OZ}	Maximum 3−STATE Leakage Current	5.5	V_I = V_{IL}, V_{IH}; V_O = V_{CC}, GND		±0.25	±2.5	μA
I_{CCT}	Maximum I_{CC}/Input	5.5	V_I = V_{CC} − 2.1 V	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current (Note 5)	5.5	V_{OLD} = 1.65 V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85 V Min.			−75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	μA

4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0 ms, one output loaded at a time.

AC ELECTRICAL CHARACTERISTICS FOR AC

Symbol	Parameter	V_{CC} (V) (Note 6)	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Data to Output	3.3	2.0	5.5	8.0	1.5	9.0	ns
		5.0	1.5	4.0	6.0	1.0	6.5	
t_{PHL}	Propagation Delay, Data to Output	3.3	2.0	5.5	8.0	1.5	8.5	ns
		5.0	1.5	4.0	6.0	1.0	6.5	
t_{PZH}	Output Enable Time	3.3	3.0	8.0	11.5	3.0	12.5	ns
		5.0	2.0	6.0	8.5	1.5	9.5	
t_{PZL}	Output Enable Time	3.3	2.5	7.0	10.0	2.5	11.5	ns
		5.0	1.5	5.5	7.5	1.0	8.5	
t_{PHZ}	Output Disable Time	3.3	3.5	9.0	12.5	2.5	14.0	ns
		5.0	2.0	7.0	9.5	1.0	10.5	
t_{PLZ}	Output Disable Time	3.3	2.5	6.5	9.5	2.0	10.5	ns
		5.0	2.0	5.5	7.5	1.0	8.5	

6. Voltage range 3.3 is 3.3 V ± 0.3 V. Voltage range 5.0 is 5.0 V ± 0.5 V.

AC ELECTRICAL CHARACTERISTICS FOR ACT

Symbol	Parameter	V_{CC} (V) (Note 7)	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Data to Output	5.0	2.0	4.5	7.0	2.0	7.5	ns
t_{PHL}		5.0	2.0	5.5	7.0	2.0	7.5	
t_{PZH}	Output Enable Time	5.0	2.0	5.0	9.0	2.0	9.5	ns
t_{PZL}		5.0	2.0	6.5	9.0	2.0	9.5	
t_{PHZ}	Output Disable Time	5.0	1.5	5.5	7.5	1.5	8.0	ns
t_{PLZ}		5.0	1.5	5.5	7.5	1.5	8.0	

7. Voltage range 5.0 is 5.0 V ± 0.5 V.

CAPACITANCE

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance for AC	V_{CC} = 5.0 V	30.0	pF
	Power Dissipation Capacitance for ACT		70.0	

ORDERING INFORMATION

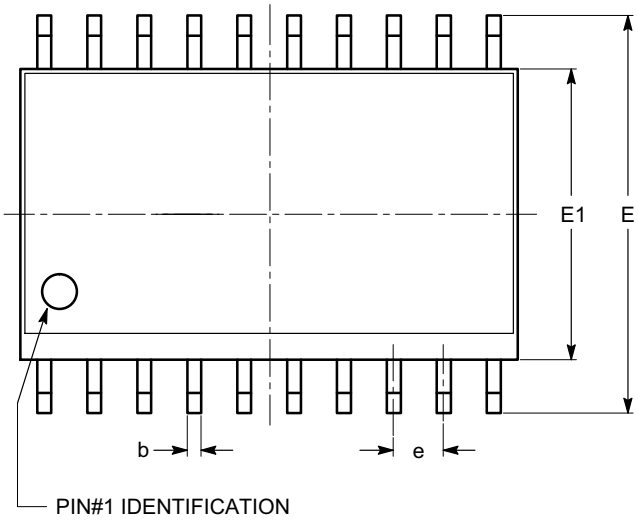
Device	Marking	Package	Shipping†
74AC541MTC	AC 541	TSSOP−20	75 Units / Tube
74AC541MTCX	AC 541	TSSOP−20	2500 Units / Tape & Reel
74AC541SC	AC541	SOIC−20	38 Units / Tube
74AC541SCX	AC541	SOIC−20	1000 Units / Tape & Reel
74ACT541MTCX	ACT 541	TSSOP−20	2500 Units / Tape & Reel
74ACT541SC	ACT541	SOIC−20	38 Units / Tube
74ACT541SCX	ACT541	SOIC−20	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

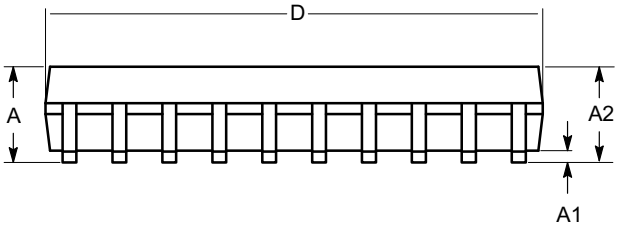
SOIC−20, 300 mils
CASE 751BJ
ISSUE O

DATE 19 DEC 2008

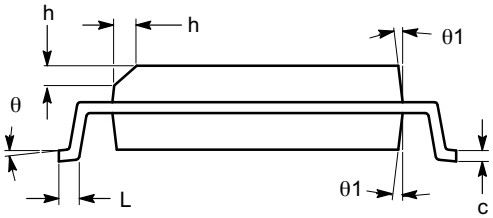


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
A2	2.05		2.55
b	0.31	0.41	0.51
c	0.20	0.27	0.33
D	12.60	12.80	13.00
E	10.01	10.30	10.64
E1	7.40	7.50	7.60
e		1.27 BSC	
h	0.25		0.75
L	0.40	0.81	1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW



END VIEW

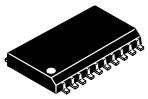
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

DOCUMENT NUMBER:	**98AON34287E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−20, 300 MILS**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



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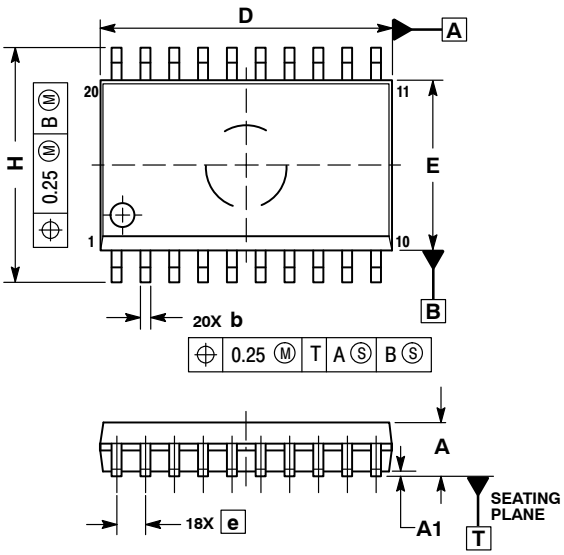
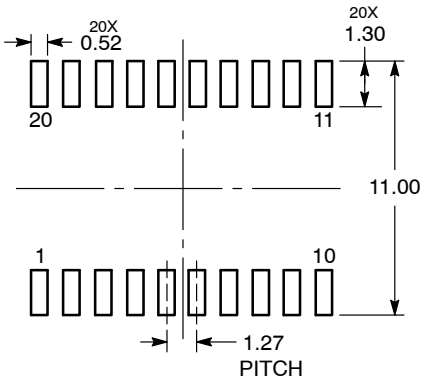


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

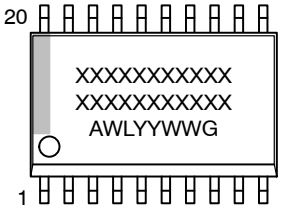
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

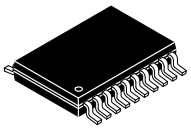
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42343B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−20 WB**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP–20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016



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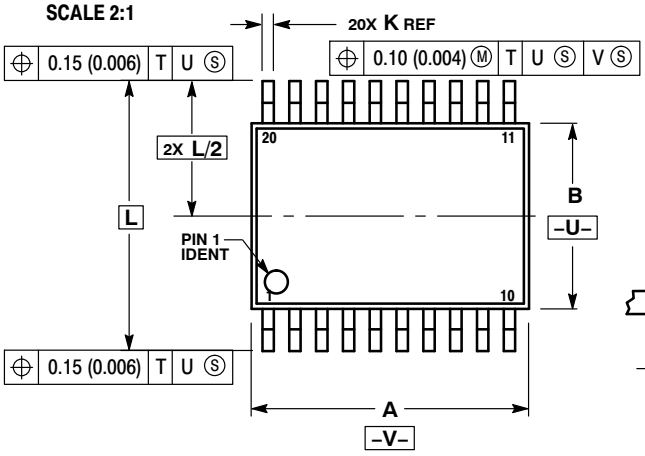
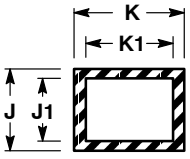
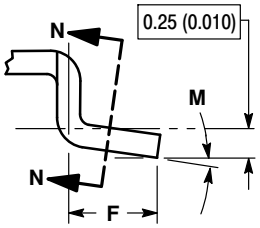
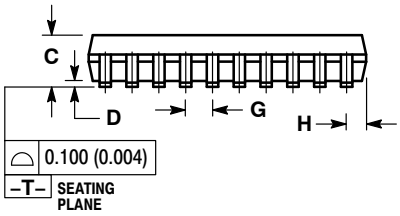


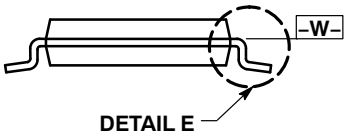


SECTION N–N



DETAIL E



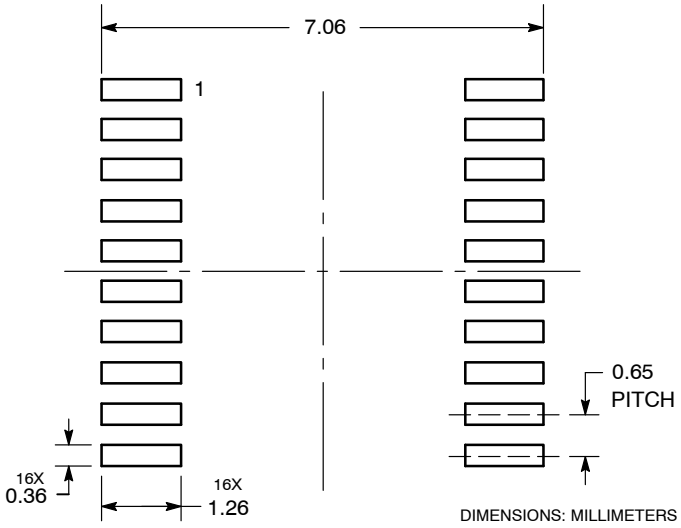


DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

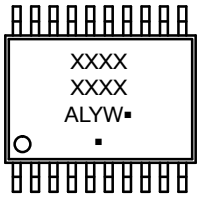
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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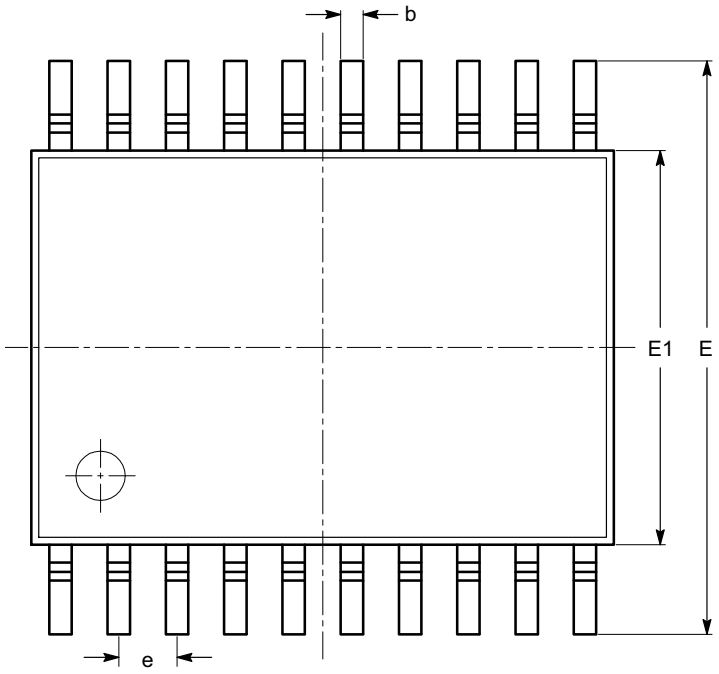
DESCRIPTION:	**TSSOP–20 WB**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

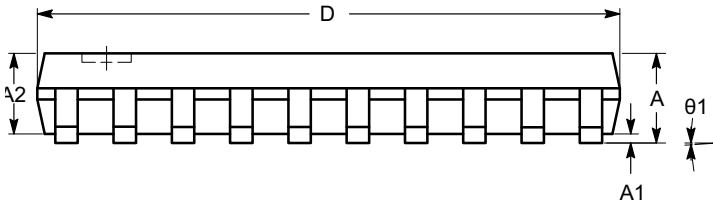
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

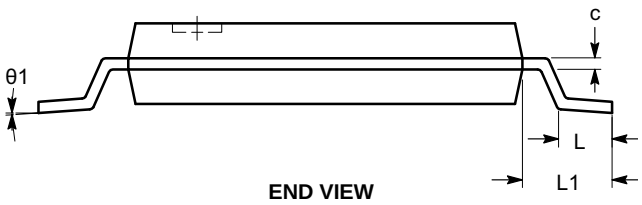


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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DESCRIPTION:	**TSSOP20, 4.4X6.5**	**PAGE 1 OF 1**

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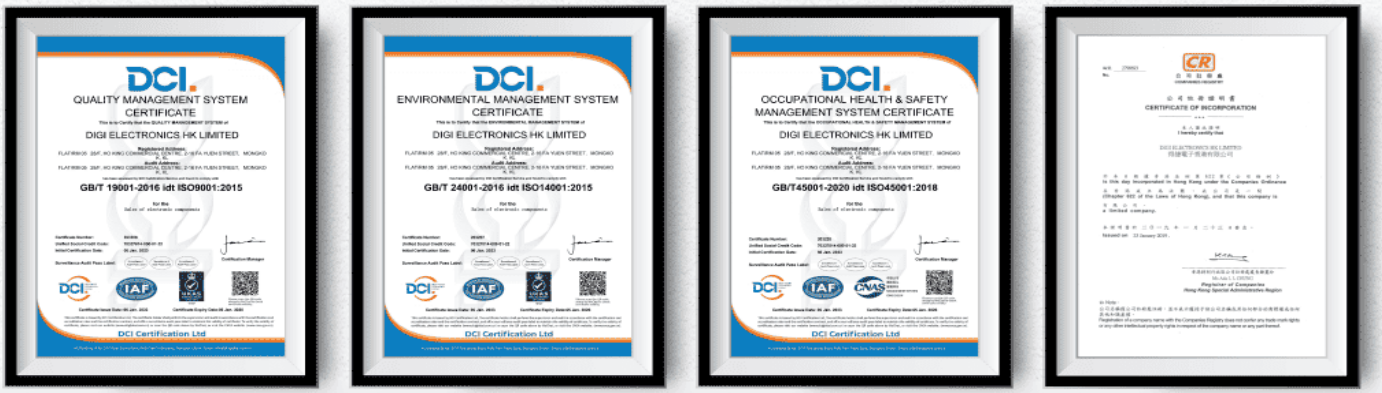

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