74ACTQ563PC Datasheet

DiGi Electronics Part Number	74ACTQ563PC-DG
Manufacturer	onsemi
Manufacturer Product Number	74ACTQ563PC
Description	IC D-TYPE TRANSP SGL 8:8 20DIP
Detailed Description	D-Type Transparent Latch 1 Channel 8:8 IC Tri-State 20-PDIP

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74ACTQ563PC	onsemi
Series:	Product Status:
74ACTQ	Obsolete
Logic Type:	Circuit:
D-Type Transparent Latch	8:8
Output Type:	Voltage - Supply:
Tri-State	4.5V ~ 5.5V
Independent Circuits:	Delay Time - Propagation:
1	1ns
Current - Output High, Low:	Operating Temperature:
24mA, 24mA	-40°C ~ 85°C
Mounting Type:	Package / Case:
Through Hole	20-DIP (0.300", 7.62mm)
Supplier Device Package:	Base Product Number:
20-PDIP	74ACTQ563

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8542.39.0001

FAIRCHILD SEMICONDUCTOR™

January 1990
Revised December 1998

74ACTQ563
Quiet Series™ Octal Latch with 3-STATE Outputs

General Description

The ACTQ563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The ACTQ563 is functionally identical to the ACTQ573, but with inverted outputs. The ACTQ563 utilizes Fairchild FACT Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

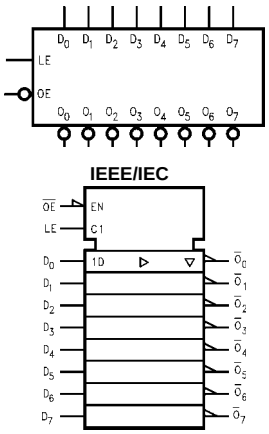
- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Outputs source/sink 24 mA
- Faster prop delays than standard ACT563
- Functionally identical to the ACTQ573 but with inverted outputs

Ordering Code:

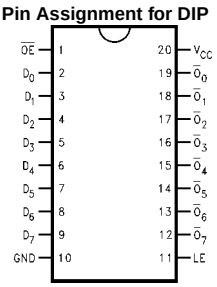
Order Number	Package Number	Package Description
74ACTQ563PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	3-STATE Latch Outputs

FACT™, Quiet Series™, FACT Quiet Series™ and GTO™ are trademarks of Fairchild Semiconductor Corporation.

Functional Description

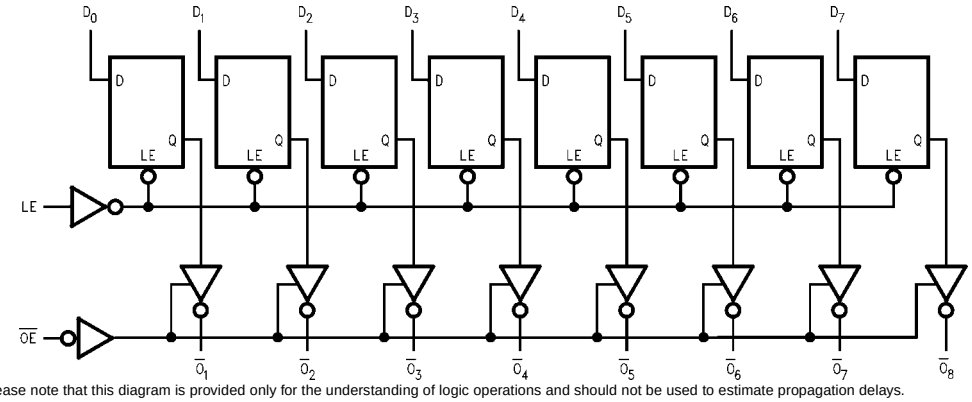
The ACTQ563 contains eight D-type latches with 3-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D	Q	$\overline{O}$	
H	X	X	X	Z	High-Z
H	H	L	H	Z	High-Z
H	H	H	L	Z	High-Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latchup Source or Sink Current	± 300 mA
Junction Temperature (T_J) PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = − 50 µA
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = − 24 mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1		I_{OUT} = 50 µA
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	µA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		± 0.25	± 2.5	µA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 3)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	µA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	Figure 1, Figure 2 (Note 4)(Note 5)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	Figure 1, Figure 2 (Note 4)(Note 5)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Note 4)(Note 6)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Note 4)(Note 6)

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: DIP package.

Note 5: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

DC Electrical Characteristics (Continued)

Note 6: Max number of data inputs (n) switching. (n–1) inputs switching 0V to 3V. Input-under-test switching; 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (Note 7)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL}	Propagation Delay	3.3	2.5	8.5	11.5	2.5	12.0	ns
t_{PLH}	D_n to O_n	5.0	1.5	5.5	7.5	1.5	8.0	
t_{PLH}	Propagation Delay	3.3	2.5	8.5	13.0	2.5	13.5	ns
t_{PHL}	LE to O_n	5.0	2.0	6.0	8.5	2.0	9.0	
t_{PZL}	Output Enable Time	3.3	2.5	8.5	13.0	2.5	13.5	ns
t_{PZH}		5.0	1.5	6.0	8.5	1.5	9.0	
t_{PHZ}	Output Disable Time	3.3	1.0	9.0	14.5	1.0	15.0	ns
t_{PLZ}		5.0	1.0	6.5	9.5	1.0	10.0	
t_{OSHL}	Output to Output Skew (Note 8)	3.3		1.0	1.5		1.5	ns
t_{OSLH}	D_n to O_n	5.0		0.5	1.0		1.0	

Note 7: Voltage Range 5.0 is 5.0V ±0.5V and 3.3 is 3.3V ± 0.3V.

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW	3.3	0	3.0	3.0	ns
	D_n to LE	5.0	0	3.0	3.0	
t_H	Hold Time, HIGH or LOW	3.3	0	1.5	1.5	ns
	D_n to LE	5.0	0	1.5	1.5	
t_W	LE Pulse Width, HIGH	3.3	2.0	4.0	4.0	ns
		5.0	2.0	4.0	4.0	

Note 9: Voltage Range 5.0 is 5.0V ±0.5V and 3.3V is 3.3 ± 0.3V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	42	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

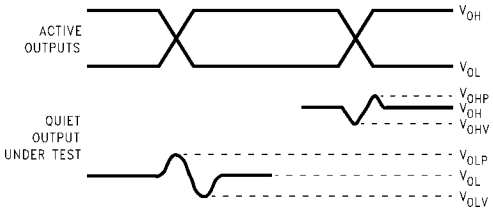
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.



V_{OHV} and V_{OLP} are measured with respect to ground reference.

Input pulses have the following characteristics:

f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

FIGURE 1. Quiet Output Noise Voltage Waveforms

5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a n oscilloscope.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

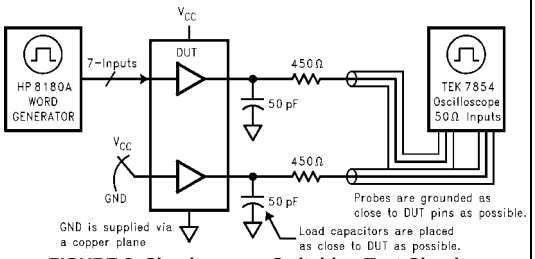
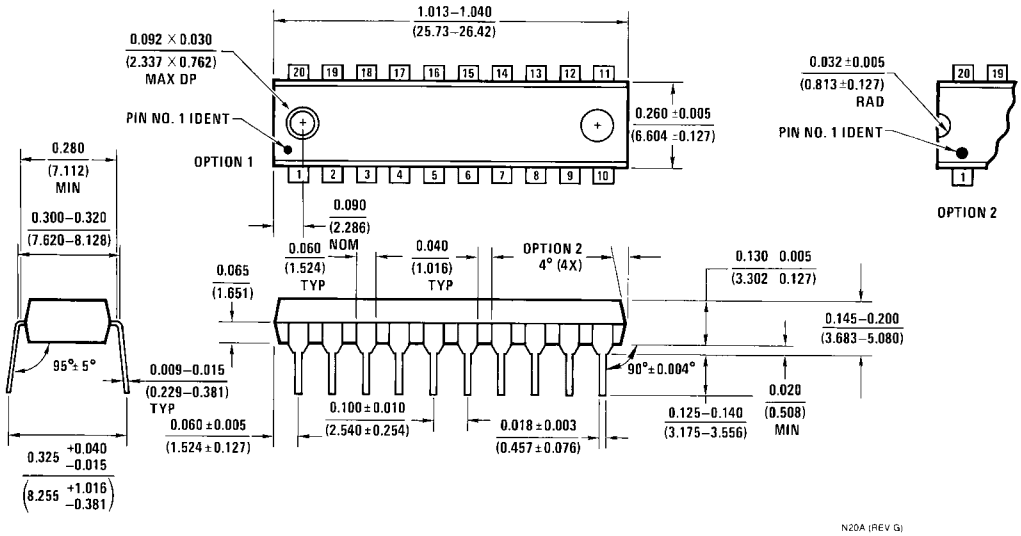


FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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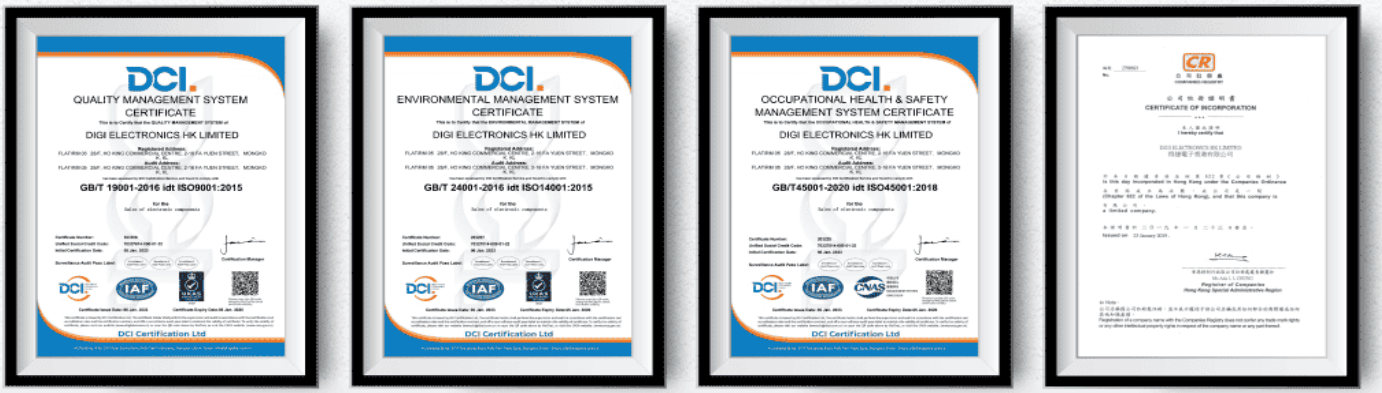

Tel: +00 852-30501935

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