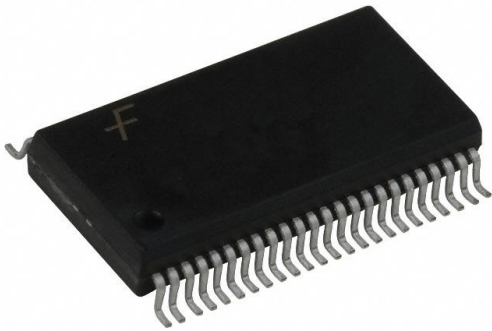


74LVT162244MEA Datasheet

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DiGi Electronics Part Number	74LVT162244MEA-DG
Manufacturer	onsemi
Manufacturer Product Number	74LVT162244MEA
Description	IC BUF NON-INVERT 3.6V 48SSOP
Detailed Description	Buffer, Non-Inverting 4 Element 4 Bit per Element 3-State Output 48-SSOP



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Purchase and inquiry

Manufacturer Product Number:

74LVT162244MEA

Series:

74LVT

Logic Type:

Buffer, Non-Inverting

Number of Bits per Element:

4

Output Type:

3-State

Voltage - Supply:

2.7V ~ 3.6V

Mounting Type:

Surface Mount

Supplier Device Package:

48-SSOP

Manufacturer:

onsemi

Product Status:

Obsolete

Number of Elements:

4

Input Type:

-

Current - Output High, Low:

12mA, 12mA

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

48-BSSOP (0.295", 7.50mm Width)

Base Product Number:

74LVT162244

Environmental & Export classification

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001



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March 1999
Revised June 2005

74LVT162244 • 74LVTH162244

Low Voltage 16-Bit Buffer/Line Driver with 3-STATE Outputs and 25Ω Series Resistors in the Outputs

General Description

The LVT162244 and LVTH162244 contain sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The LVT162244 and LVTH162244 are designed with equivalent 25Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162244 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These buffers and line drivers are designed for low (3.3V) V_{CC} applications, but with the capability to provide TTL interface to a 5V environment. The LVT162244 and LVTH162244 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power consumption.

Features

- Input and output interface capability to systems with 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (LVTH162244), also available without bushold feature (LVT162244).
- Live insertion/contact non-permitting
- Power-on power-down impedance provides glitch-free bus operation
- Outputs include equivalent series resistance of 25.2 to make external termination resistors unnecessary and reduce overshoot and undershoot
- Functionally compatible with the 74 Series 162244
- Switch-up performance exceeds 500 mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device > 1000V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Ordering Code:

Order Number	Package Number	Package Description
74LVT162244G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVT162244MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT162244MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH162244G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVTH162244MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [Tube]
74LVTH162244MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [Tape and Reel]
74LVTH162244MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [Tube]
74LVTH162244MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [Tape and Reel]

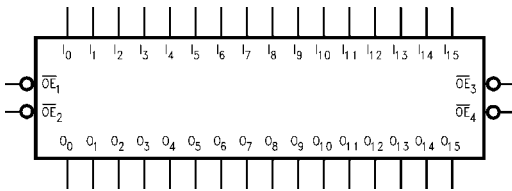
Note 1: Ordering code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

74LVT162244 • 74LVTH162244 Low Voltage 16-Bit Buffer/Line Driver with 3-STATE Outputs and 25Ω Series Resistors in the Outputs

74LV162244 • 74LVTH162244

Logic Symbol

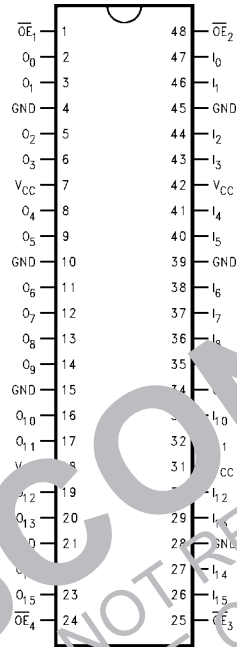


Pin Descriptions

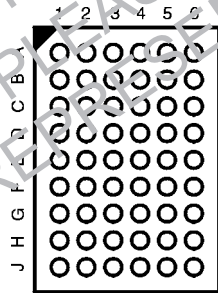
Pin Names	Description
\overline{OE}_n	Output Enable Inputs (Active LOW)
I_0-I_{15}	Inputs
O_0-O_{15}	Outputs
NC	No Connect

Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	\overline{OE}_1	\overline{OE}_2	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	NC	NC	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	D	GND	I_9	I_{10}
G	O_{12}	O_{11}	CC	V _{CC}	I_{11}	I_{12}
H	O_{14}	O_{13}	NC	NC	I_{13}	I_{14}
J	O_{15}	NC	\overline{OE}_4	\overline{OE}_3	NC	I_{15}

Truth Table

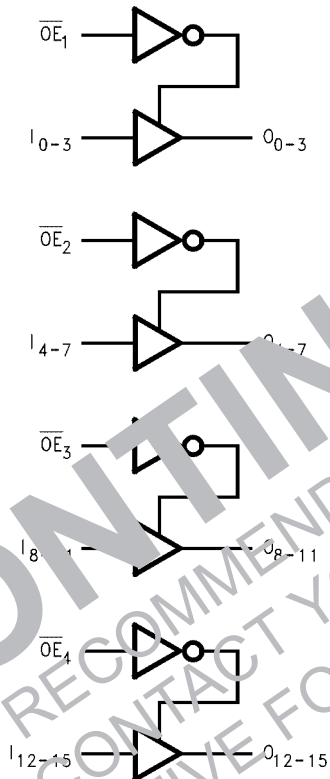
Inputs		Outputs
\overline{OE}_1	I_0-I_3	O_0-O_3
L	L	L
L	H	H
H	X	Z
\overline{OE}_2	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z
\overline{OE}_3	I_8-I_{11}	O_8-O_{11}
L	L	L
L	H	H
H	X	Z
\overline{OE}_4	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level
Z = High Impedance X = Immaterial

Functional Description

The LVT162244 and LVTH162244 contain sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Logic Diagram



74LVT162244 • 74LVTH162244

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74LVT162244 • 74LVTH162244

Absolute Maximum Ratings (Note 3)				
Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	-0.5 to +4.6		V
V_I	DC Input Voltage	-0.5 to +7.0		V
V_O	Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	± 64		mA
I_{GND}	DC Ground Current per Ground Pin	± 128		mA
T_{STG}	Storage Temperature	-65 to +150		$^{\circ}C$

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage		5.5	V
I_{OH}	HIGH-Level Output Current		-12	mA
I_{OL}	LOW-Level Output Current		12	mA
T_A	Free Air Operating Temperature	-40	+85	$^{\circ}C$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$		10	ns/V

Note 3: Absolute Maximum continuous ratings are the values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device performance. Normal operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Rating is per device.

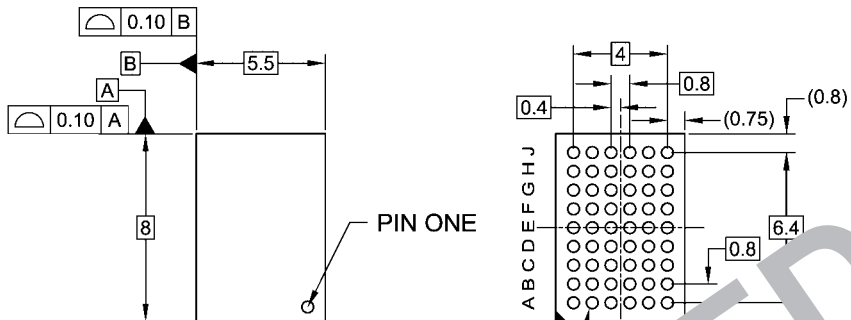
DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40^{\circ}C$ to $+35^{\circ}C$		Units	Conditions	
			Min	Max			
V_{IK}	Input Clamp Diode Voltage	2.7		-1.2	V	$I_I = -18$ mA	
V_{IH}	Input HIGH Voltage	2.7-3.6	2.0		V	$V_O \leq 0.1V$ or $V_O \geq V_{CC} - 0.1V$	
V_{IL}	Input LOW Voltage	2.7-3.6		0.8	V		
V_{OH}	Output HIGH Voltage	2.7-3.6	$V_{CC}-0.2$		V	$I_{OH} = -100$ μA	
		3.0	2.0			$I_{OH} = -12$ mA	
V_{OL}	Output LOW Voltage	2.7		0.2	V	$I_{OL} = 100$ μA	
		3.0		0.8		$I_{OL} = 12$ mA	
$I_{I(HOLD)}$ (Note 5)	Bushold Input Minimum Drive	3.0	75		μA	$V_I = 0.8V$	
			-75			$V_I = 2.0V$	
$I_{I(O)}$ (Note 5)	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 6)	
			-500			(Note 7)	
I_I	Input Current	3.6		10	μA	$V_I = 5.5V$	
		Control Pins	3.6			± 1	$V_I = 0V$ or V_{CC}
		Data Pins	3.6			-5	$V_I = 0V$
				1		$V_I = V_{CC}$	
I_{OFF}	Power Off Leakage Current	0		± 100	μA	$0V \leq V_I$ or $V_O \leq 5.5V$	
$I_{PU/PD}$	Power Up/Down				μA	$V_O = 0.5V$ to $3.0V$	
	3-STATE Current	0-1.5V		± 100	μA	$V_I = GND$ or V_{CC}	
I_{OZL}	3-STATE Output Leakage Current	3.6		-5	μA	$V_O = 0.5V$	
I_{OZH}	3-STATE Output Leakage Current	3.6		5	μA	$V_O = 3.0V$	
I_{OZH+}	3-STATE Output Leakage Current	3.6		10	μA	$V_{CC} < V_O \leq 5.5V$	
I_{CCH}	Power Supply Current	3.6		0.19	mA	Outputs HIGH	
I_{CCL}	Power Supply Current	3.6		5	mA	Outputs LOW	
I_{CCZ}	Power Supply Current	3.6		0.19	mA	Outputs Disabled	

DC Electrical Characteristics (Continued)							
Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions	
			Min	Max			
I _{CCZ} ⁺	Power Supply Current	3.6		0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled	
ΔI _{CC}	Increase in Power Supply Current (Note 8)	3.6		0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND	
<p>Note 5: Applies to bushold versions only (74LVTH162244).</p> <p>Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.</p> <p>Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.</p> <p>Note 8: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.</p>							
Dynamic Switching Characteristics (Note 9)							
Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8	V	V _I = 0V, R _L = 50 Ω (Note 10)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8	V	(Note 10)	
<p>Note 9: Characterized in SSOP package. Guaranteed parameter, but not tested.</p> <p>Note 10: Max number of outputs defined as (n), n-1 data inputs are driven 0V to 3V, Output current is 10 mA LOW.</p>							
AC Electrical Characteristics							
Symbol	Parameter	T _A = -40°C to +85°C, C _L = 50 pF, R _L = 500 Ω				Units	
		V _I = 3.3V ± 0.3V		V _{CC} = 2.7V			
		Min	Max	Min	Max		
t _{PLH}	Propagation Delay Data to output	1.4	4.0	1.4	4.8	ns	
t _{PHL}		1.2	3.7	1.2	4.1	ns	
t _{PZH}	Output Enable	1.2	5.1	1.2	6.5	ns	
t _{PZL}		1.4	5.4	1.4	6.9	ns	
t _{PHZ}	Output Disable Time	2.0	5.0	2.0	5.4	ns	
t _{PLZ}		1.5	5.0	1.5	5.4	ns	
t _{OSHL}	Output Skew (Low)		1.0		1.0	ns	
t _{OSLH}	Output Skew (High) (Note 11)					ns	
<p>Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).</p>							
Capacitance (Note 12)							
Symbol	Parameter	Conditions			Typical	Units	
C _{IN}	Input Capacitance	V _{CC} = 0V, V _I = 0V or V _{CC}			4	pF	
C _{OUT}	Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}			8	pF	
<p>Note 12: Capacitance is measured at a frequency f = 1 MHz, per MIL-STD-883, Method 3012.</p>							

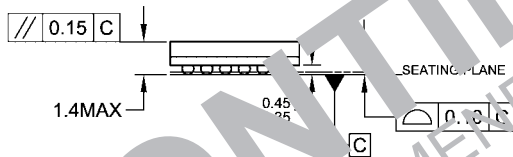
74LVT162244 • 74LVTH162244

Physical Dimensions inches (millimeters) unless otherwise noted



Top View

Bottom View



NOTES:

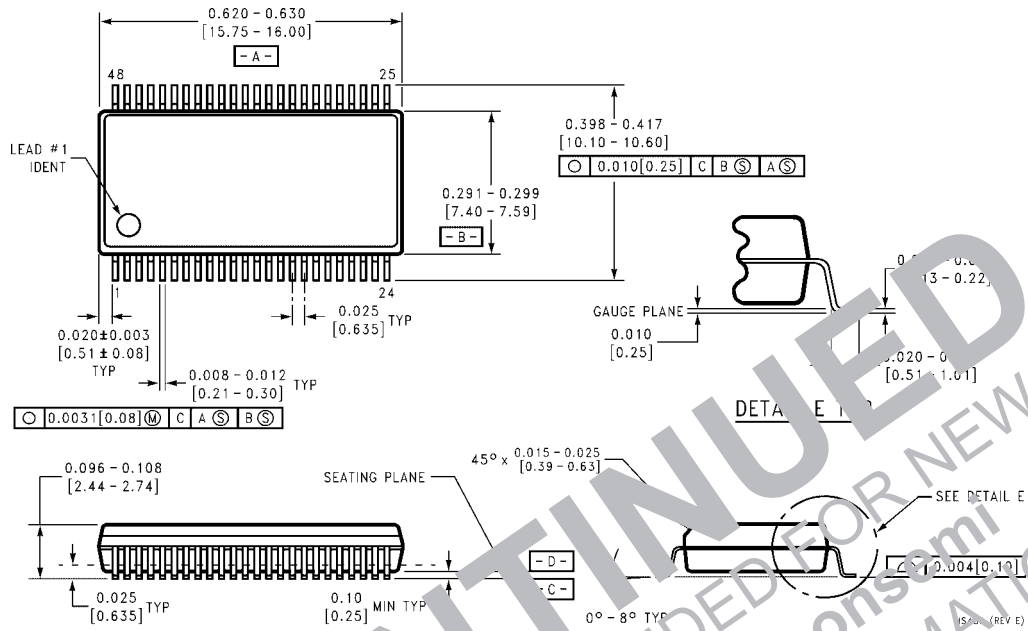
- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LUMINA CORPORATION RECOMMENDATION, NSMD (Non Solder Mask Defined)
- D. 0.35mm DIA PADS WITH A SOLDER MASK OPENING OF .45MM CONCENTRIC TO PADS
- E. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54A revD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

74LVT162244 • 74LVTH162244

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



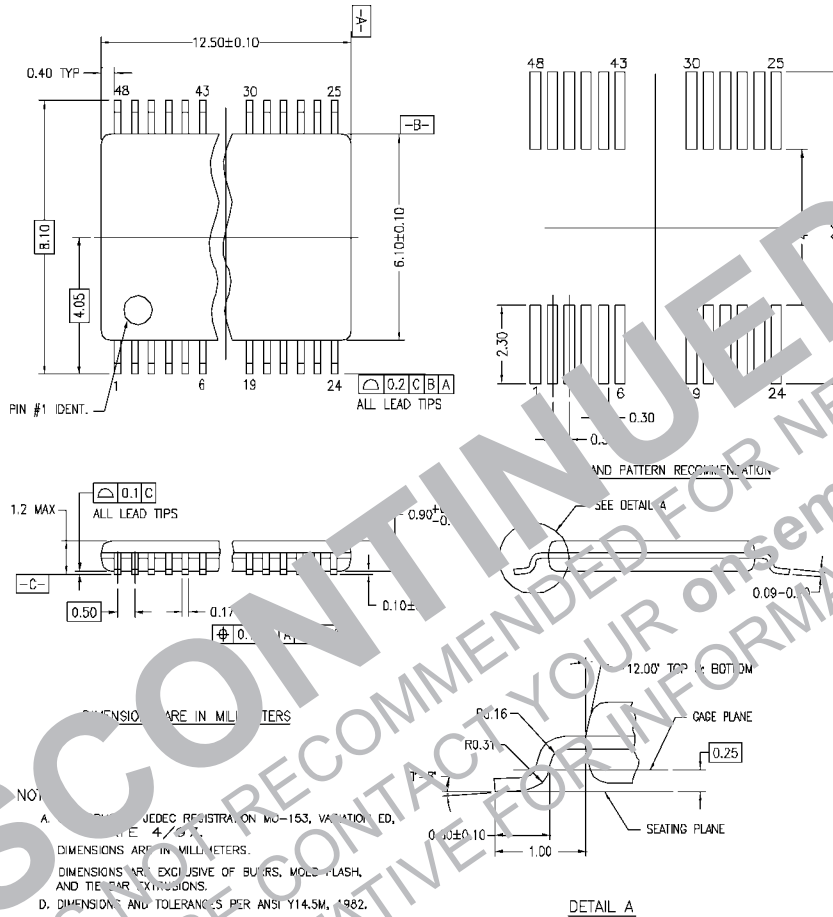
48-Lead Small Shrink Package (SSOP), JEDEC MO-118, 0.400" Wide
 Package Number MS-8A

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74LVT162244 • 74LVT162244 Low Voltage 16-Bit Buffer/Line Driver with 3-STATE Outputs and 25Ω Series Resistors in the Outputs

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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 NOT TO SCALE
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 DIMENSIONS ARE IN MILLIMETERS.
 DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH, AND TIE BAR EXTENSIONS.
 D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
 MTD48REV C

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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